



# PSMN3R0-60ES

N-channel 60 V 3.0 m $\Omega$  standard level MOSFET in I2PAK.

3 June 2014

Product data sheet

## 1. General description

Standard level N-channel MOSFET in a I2PAK package qualified to 175 °C. This product is designed and qualified for use in a wide range of industrial, communications and domestic equipment.

## 2. Features and benefits

- High efficiency due to low switching and conduction losses
- Suitable for standard level gate drive sources

## 3. Applications

- DC-to-DC converters
- Load switching
- Motor control
- Server power supplies

## 4. Quick reference data

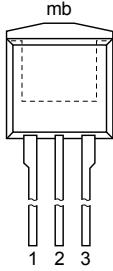
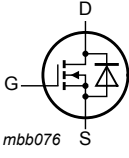
Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 175 °C		-	-	60	V
I <sub>D</sub>	drain current	T <sub>mb</sub> = 25 °C; V <sub>GS</sub> = 10 V; <a href="#">Fig. 2</a>	[1]	-	-	100	A
P <sub>tot</sub>	total power dissipation	T <sub>mb</sub> = 25 °C; <a href="#">Fig. 1</a>		-	-	306	W
<b>Static characteristics</b>							
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>		-	2.4	3	m $\Omega$
<b>Dynamic characteristics</b>							
Q <sub>GD</sub>	gate-drain charge	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 80 A; V <sub>DS</sub> = 12 V; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>		-	28	-	nC

[1] Continuous current is limited by package.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>I2PAK (SOT226)</p>	
2	D	drain		
3	S	source		
mb	D	mounting base; connected to drain		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PSMN3R0-60ES	I2PAK	plastic single-ended package (I2PAK); TO-262	SOT226

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PSMN3R0-60ES	PSMN3R0-60ES

## 8. Limiting values

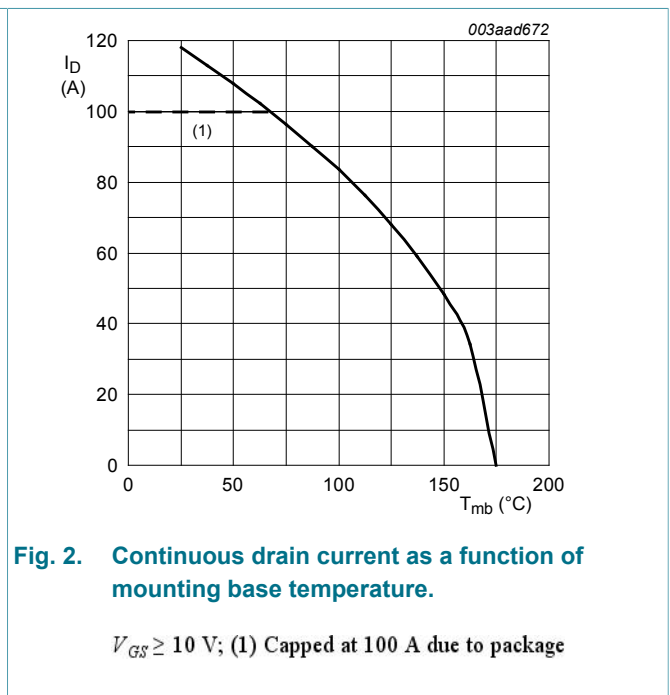
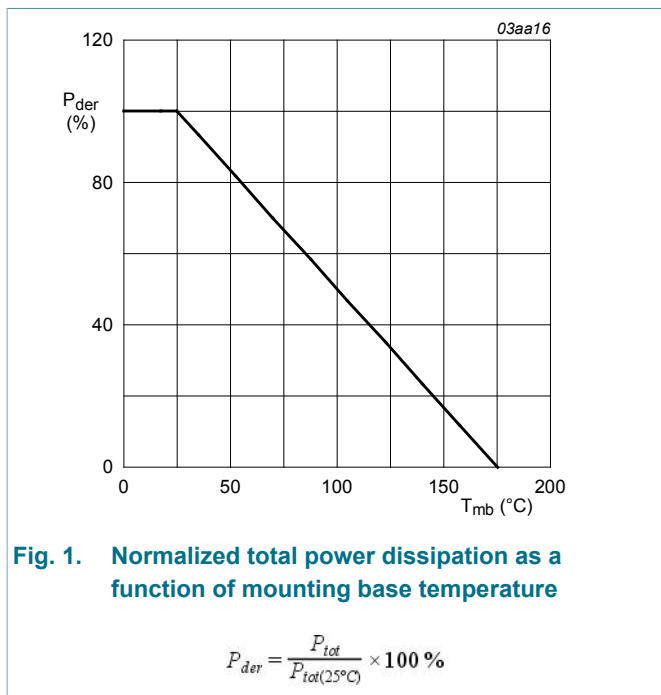
Table 5. Limiting values

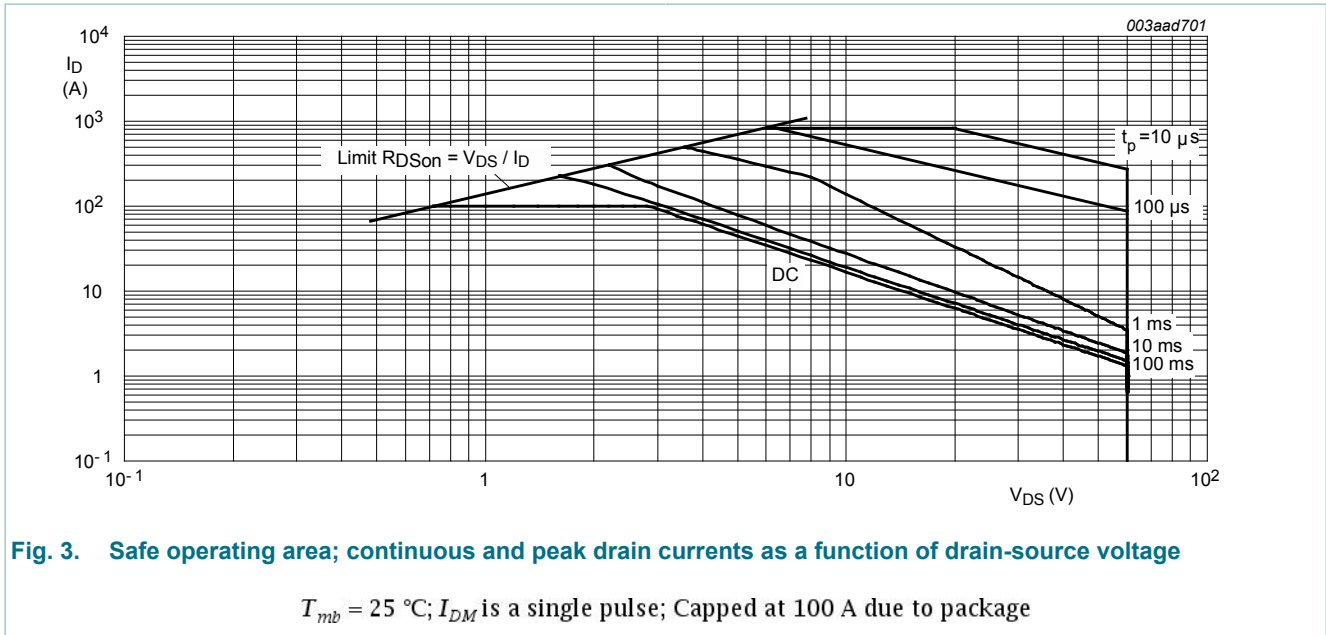
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$	-	60	V
$V_{DGR}$	drain-gate voltage	$T_j \geq 25\text{ °C}$ ; $T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	60	V
$V_{GS}$	gate-source voltage		-20	20	V
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; Fig. 1	-	306	W
$I_D$	drain current	$V_{GS} = 10\text{ V}$ ; $T_{mb} = 100\text{ °C}$ ; Fig. 2	-	83.4	A
		$V_{GS} = 10\text{ V}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 2 [1]	-	100	A
$I_{DM}$	peak drain current	pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; $T_{mb} = 25\text{ °C}$ ; Fig. 3	-	824	A
$T_{stg}$	storage temperature		-55	175	°C

Symbol	Parameter	Conditions		Min	Max	Unit
T <sub>j</sub>	junction temperature			-55	175	°C
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>mb</sub> = 25 °C	[1]	-	100	A
I <sub>SM</sub>	peak source current	pulsed; t <sub>p</sub> ≤ 10 μs; T <sub>mb</sub> = 25 °C		-	824	A
<b>Avalanche ruggedness</b>						
E <sub>DS(AL)S</sub>	non-repetitive drain-source avalanche energy	V <sub>GS</sub> = 10 V; T <sub>j(initial)</sub> = 25 °C; I <sub>D</sub> = 100 A; V <sub>sup</sub> ≤ 60 V; R <sub>GS</sub> = 50 Ω; unclamped		-	800	mJ

[1] Continuous current is limited by package.

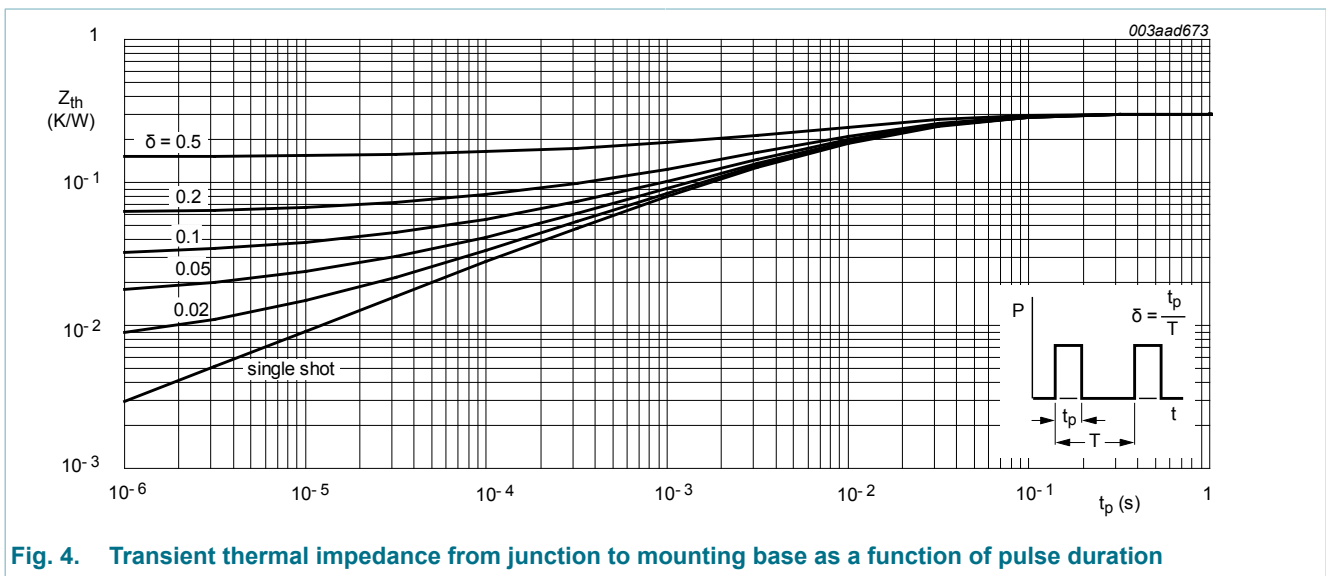




## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 4	-	0.3	0.49	K/W



## 10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = -55 \text{ }^\circ C$	54	-	-	V
		$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	60	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 8</a> ; <a href="#">Fig. 9</a>	2	3	4	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 9</a>	1	-	-	V
		$I_D = 1 \text{ mA}; V_{DS} = V_{GS}; T_j = -55 \text{ }^\circ C$ ; <a href="#">Fig. 9</a>	-	-	4.6	V
$I_{DSS}$	drain leakage current	$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	0.05	10	$\mu A$
		$V_{DS} = 60 V; V_{GS} = 0 V; T_j = 175 \text{ }^\circ C$	-	-	500	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = -20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
		$V_{GS} = 20 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	2	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 V; I_D = 25 \text{ A}; T_j = 175 \text{ }^\circ C$ ; <a href="#">Fig. 10</a>	-	-	7.2	mΩ
		$V_{GS} = 10 V; I_D = 25 \text{ A}; T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 11</a> ; <a href="#">Fig. 12</a>	-	2.4	3	mΩ
$R_G$	gate resistance	$f = 1 \text{ MHz}$	0.55	1.1	2.2	Ω
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$I_D = 80 \text{ A}; V_{DS} = 12 V; V_{GS} = 10 V$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	130	-	nC
$Q_{GS}$	gate-source charge	$I_D = 80 \text{ A}; V_{DS} = 12 V; V_{GS} = 10 V$ ; <a href="#">Fig. 14</a> ; <a href="#">Fig. 13</a>	-	43	-	nC
$Q_{GD}$	gate-drain charge	$I_D = 80 \text{ A}; V_{DS} = 12 V; V_{GS} = 10 V$ ; <a href="#">Fig. 13</a> ; <a href="#">Fig. 14</a>	-	28	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 30 V; V_{GS} = 0 V; f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 15</a> ; <a href="#">Fig. 16</a>	-	8079	-	pF
$C_{oss}$	output capacitance	$V_{DS} = 30 V; V_{GS} = 0 V; f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 15</a>	-	971	-	pF
$C_{riss}$	reverse transfer capacitance	$V_{DS} = 30 V; V_{GS} = 0 V; f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ C$ ; <a href="#">Fig. 15</a> ; <a href="#">Fig. 16</a>	-	492	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 30 V; R_L = 0.5 \text{ } \Omega; V_{GS} = 10 V$ ; $R_{G(ext)} = 1.5 \text{ } \Omega$	-	31	-	ns
$t_r$	rise time		-	26	-	ns
$t_{d(off)}$	turn-off delay time		-	77	-	ns
$t_f$	fall time		-	22	-	ns

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; $T_j = 25\text{ °C}$ ; Fig. 17	-	0.88	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ; $V_{GS} = 0\text{ V}$ ;	-	54	-	ns
$Q_r$	recovered charge	$V_{DS} = 30\text{ V}$	-	97	-	nC

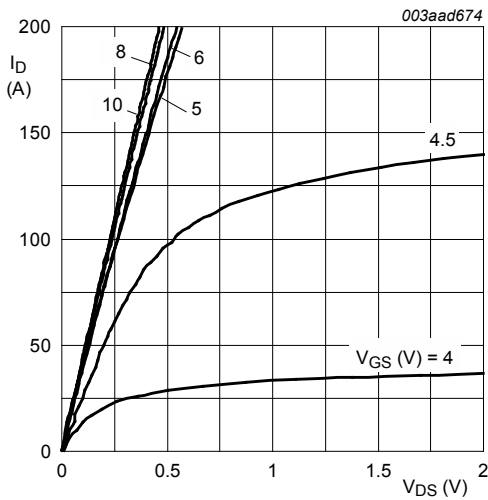


Fig. 5. Output characteristics: drain current as a function of drain-source voltage; typical values

$T_j = 25\text{ °C}$

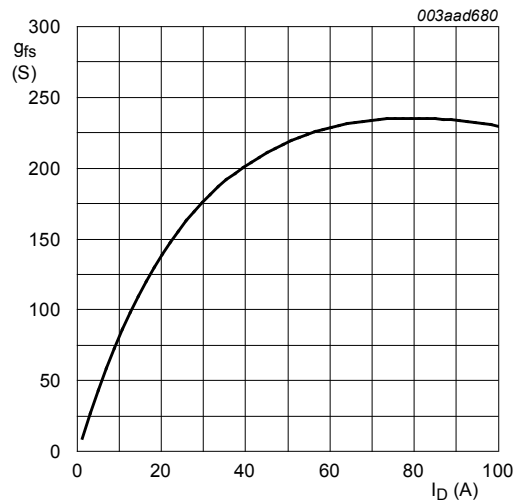


Fig. 6. Forward transconductance as a function of drain current; typical values

$T_j = 25\text{ °C}$ ;  $V_{DS} = 30\text{ V}$

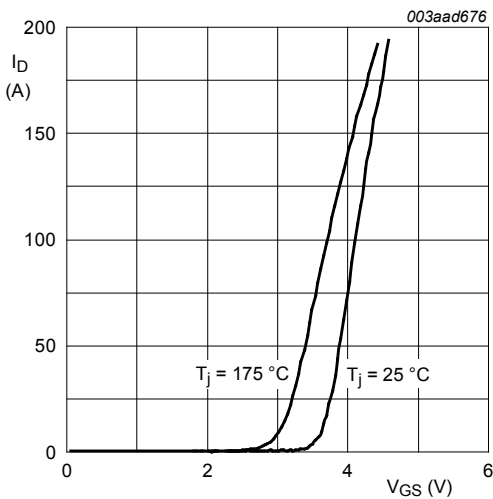


Fig. 7. Transfer characteristics: drain current as a function of gate-source voltage; typical values

$V_{DS} > I_D \times R_{DS(on)}$

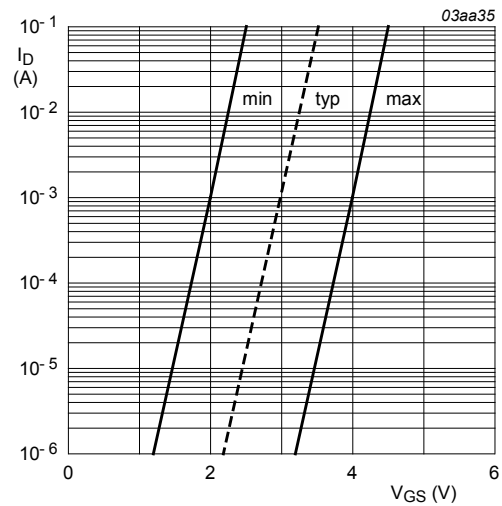
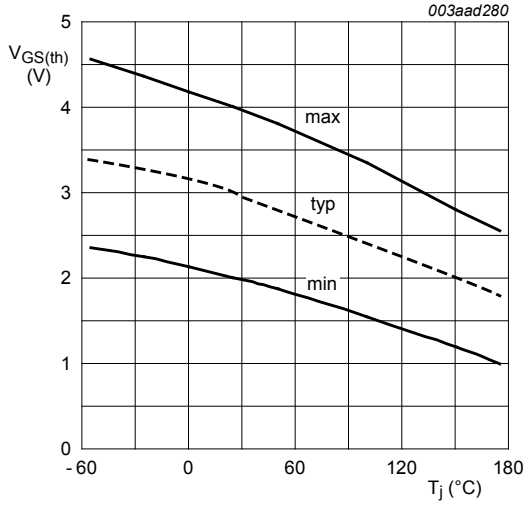


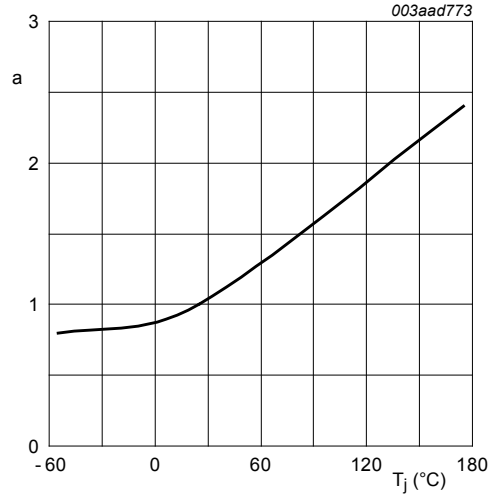
Fig. 8. Sub-threshold drain current as a function of gate-source voltage

$T_j = 25\text{ °C}$ ;  $V_{DS} = 5\text{ V}$



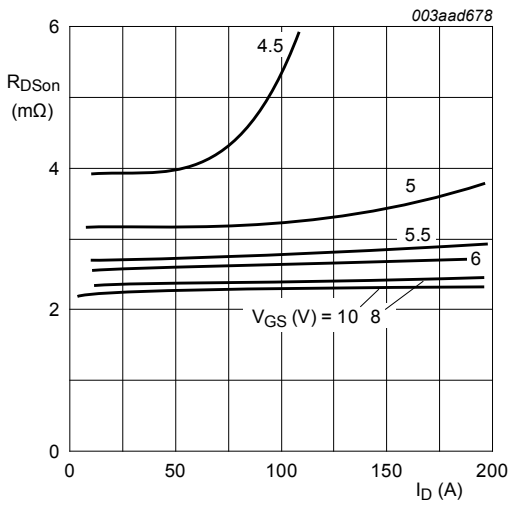
**Fig. 9. Gate-source threshold voltage as a function of junction temperature**

$$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$$



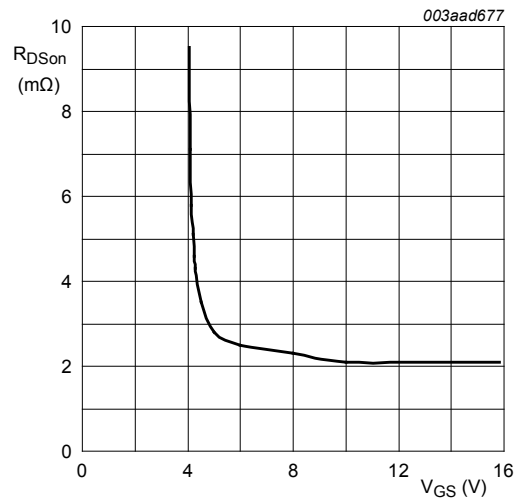
**Fig. 10. Normalized drain-source on-state resistance factor as a function of junction temperature**

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$



**Fig. 11. Drain-source on-state resistance as a function of drain current; typical values**

$$T_j = 25^\circ\text{C}$$



**Fig. 12. Drain-source on-state resistance as a function of gate-source voltage; typical values**

$$T_j = 25^\circ\text{C}; I_D = 25 \text{ A}$$

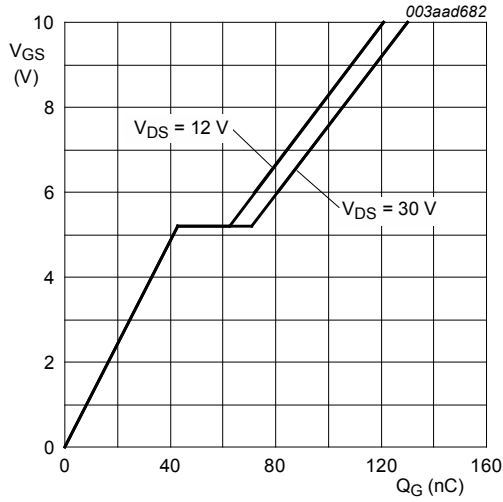


Fig. 13. Gate-source voltage as a function of gate charge; typical values

$T_j = 25\text{ }^\circ\text{C}; I_D = 25\text{ A}$



Fig. 14. Gate charge waveform definitions

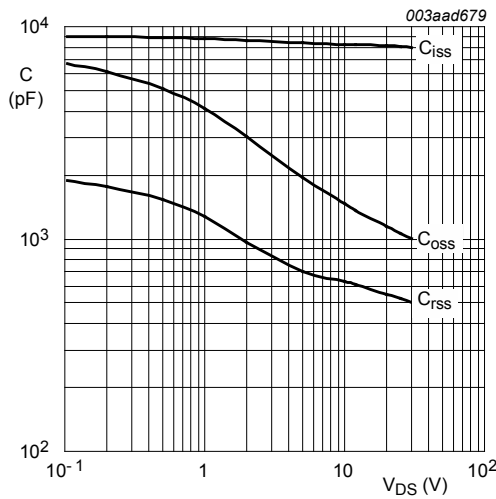


Fig. 15. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

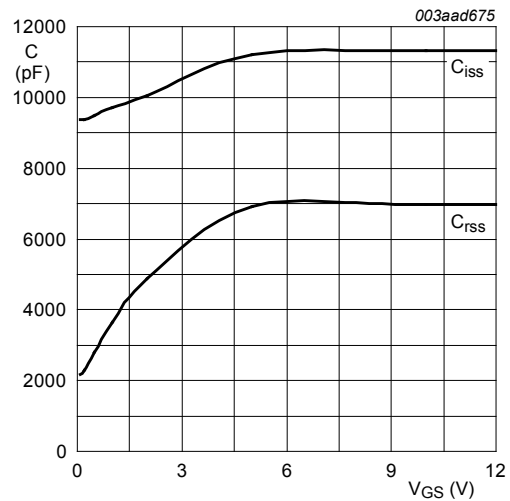


Fig. 16. Input and reverse transfer capacitances as a function of gate-source voltage, typical values

$V_{DS} = 0\text{ V}; f = 1\text{ MHz}$



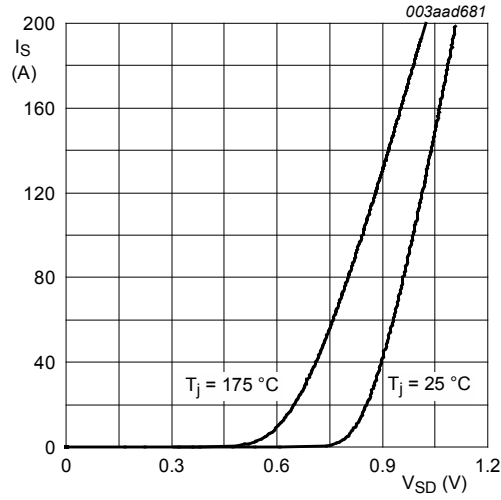


Fig. 17. Source current as a function of source-drain voltage; typical values

$$V_{GS} = 0 \text{ V}$$

### 11. Package outline

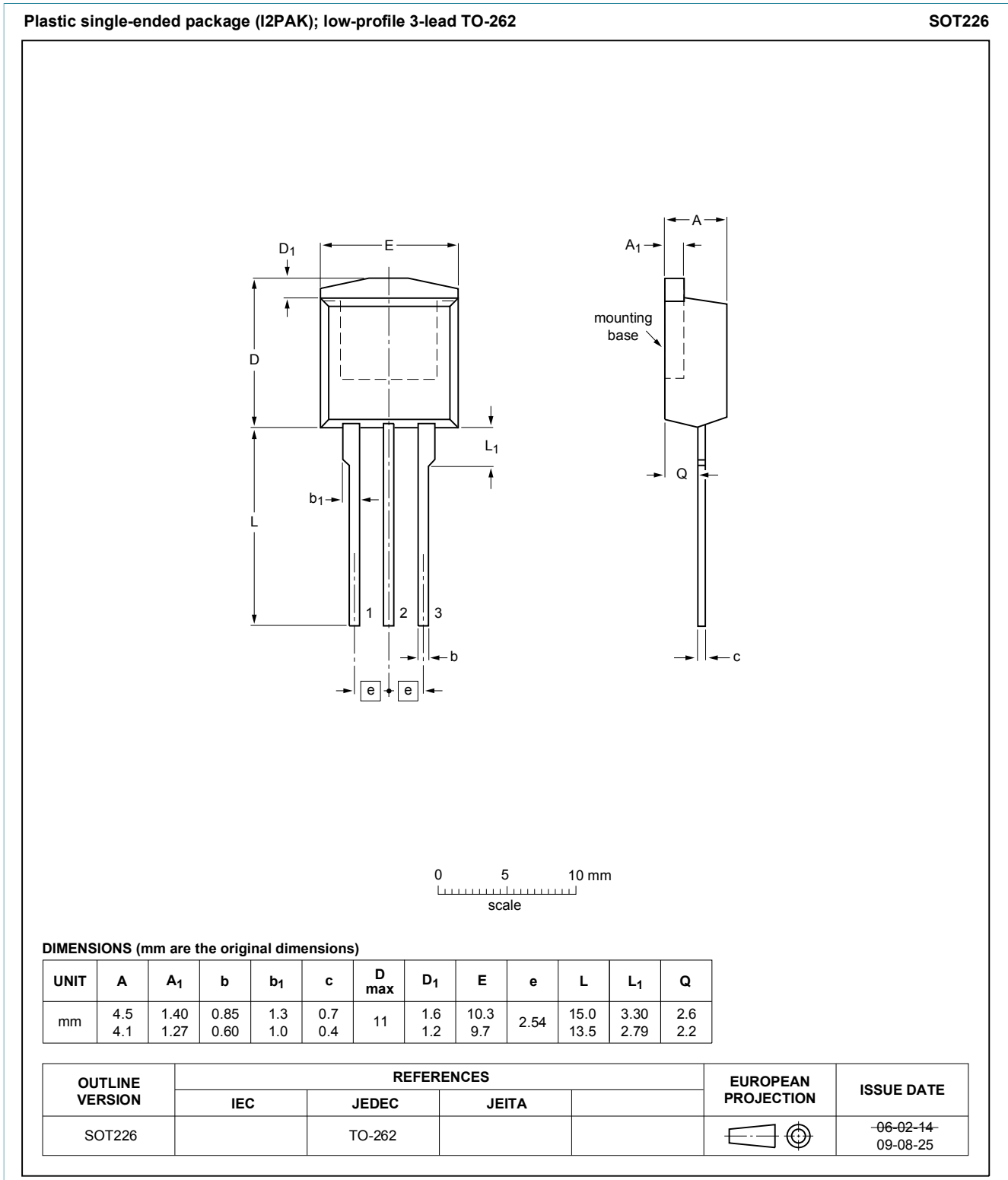


Fig. 18. Package outline I2PAK (SOT226)

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### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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