



# PMPB10UP

12 V, P-channel Trench MOSFET

5 October 2020

Product data sheet

## 1. General description

P-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020MD-6 (SOT1220) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

## 2. Features and benefits

- Low threshold voltage
- Trench MOSFET technology
- Side wettable flanks for optical solder inspection
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction

## 3. Applications

- Charging switch for portable devices
- DC-to-DC converters
- Power management in battery-driven portable devices
- Hard disk and computing power management

## 4. Quick reference data

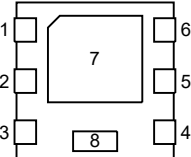
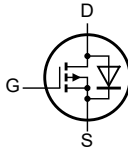
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-12	V
$V_{GS}$	gate-source voltage		-8	-	8	V
$I_D$	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-15	A
<b>Static characteristics</b>						
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -10\text{ A}; T_j = 25\text{ °C}$	-	10	11.5	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>Transparent top view DFN2020MD-6 (SOT1220)</p>	 <p>017aaa257</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		
7	D	drain		
8	S	source		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMPB10UP	DFN2020MD-6	plastic, leadless thermal enhanced ultra thin small outline package with side-wettable flanks (SWF); 6 terminals; 0.65 mm pitch; 2 mm x 2 mm x 0.65 mm body	SOT1220

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PMPB10UP	6G

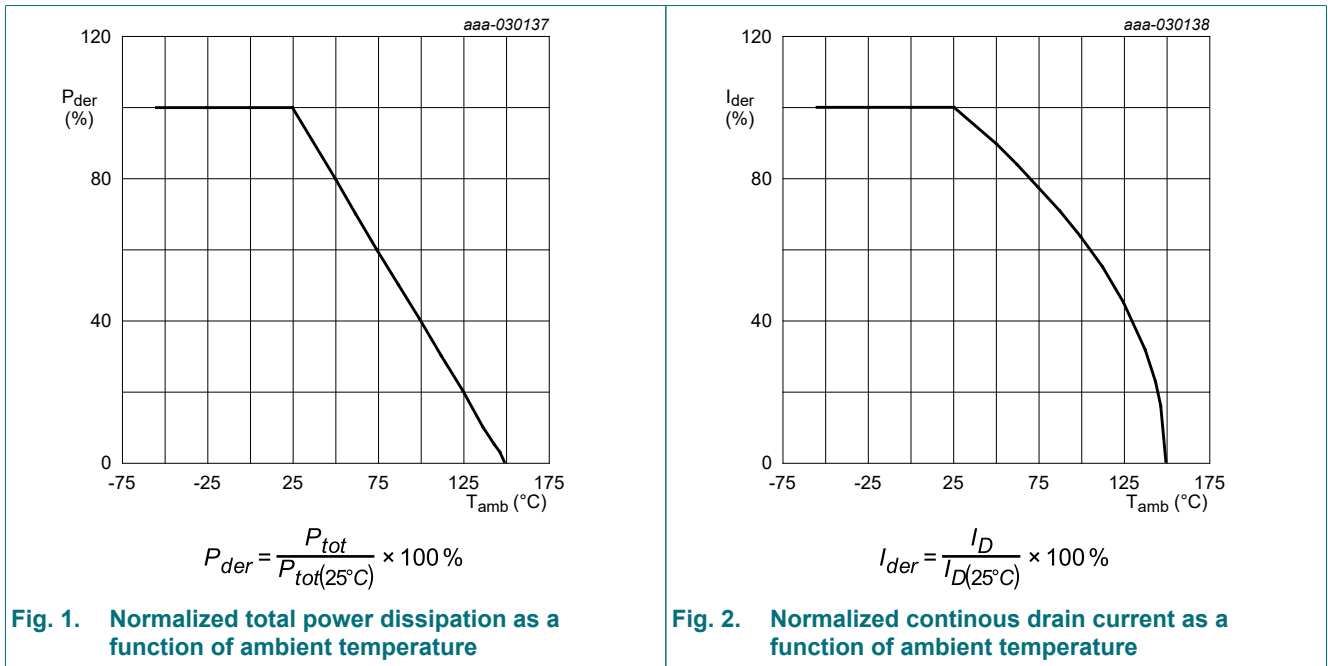
## 8. Limiting values

**Table 5. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C	-	-12	V	
V <sub>GS</sub>	gate-source voltage		-8	8	V	
I <sub>D</sub>	drain current	V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	-15	A
		V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 25 °C	[1]	-	-10	A
		V <sub>GS</sub> = -4.5 V; T <sub>amb</sub> = 100 °C	[1]	-	-6.3	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; pulsed; t <sub>p</sub> ≤ 10 μs	-	-40	A	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[1]	-	1.7	W
		T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	3.5	W
		T <sub>sp</sub> = 25 °C		-	13	W
T <sub>j</sub>	junction temperature		-55	150	°C	
T <sub>amb</sub>	ambient temperature		-55	150	°C	
T <sub>stg</sub>	storage temperature		-65	150	°C	
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	-1.6	A

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.



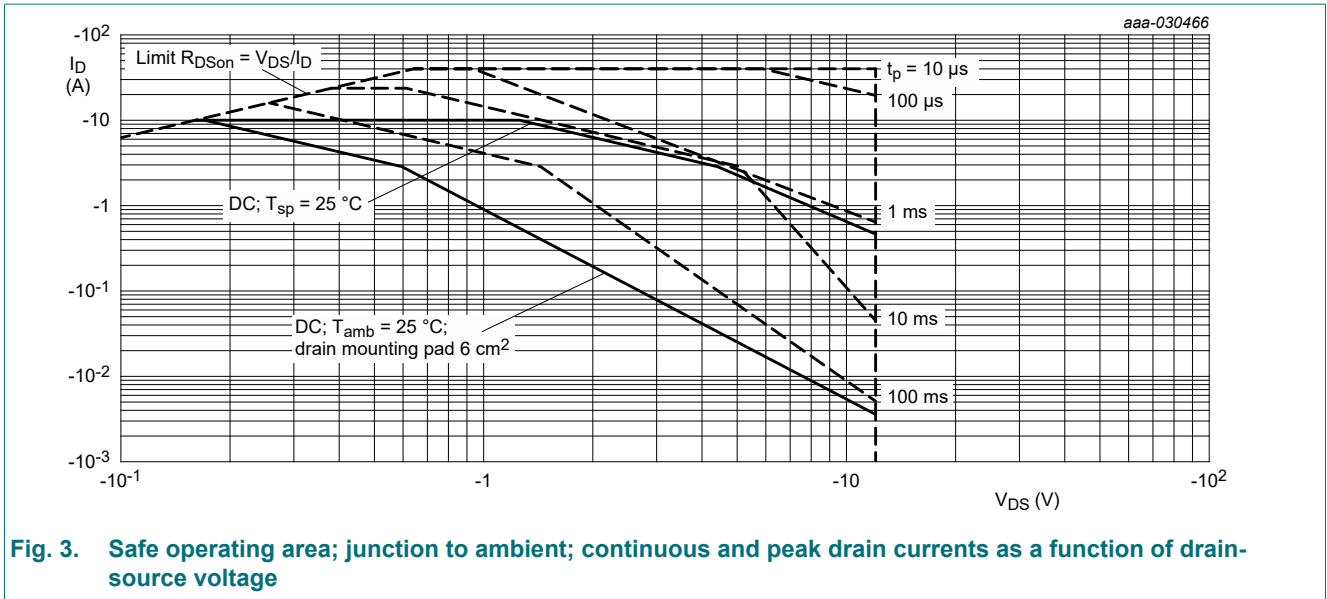


Fig. 3. Safe operating area; junction to ambient; continuous and peak drain currents as a function of drain-source voltage

## 9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	235	270	K/W
			[2]	-	67	74	K/W
		in free air, $t \leq 5$ s	[2]	-	33	36	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	5	10	K/W

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and mounting pad for drain 6 cm<sup>2</sup>.

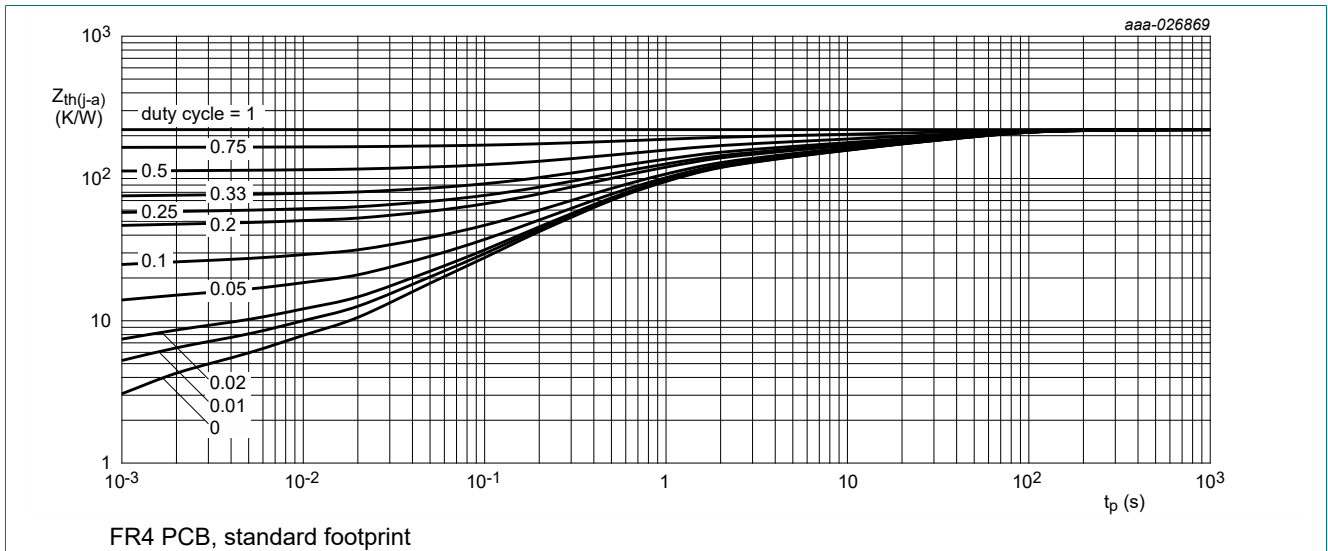


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

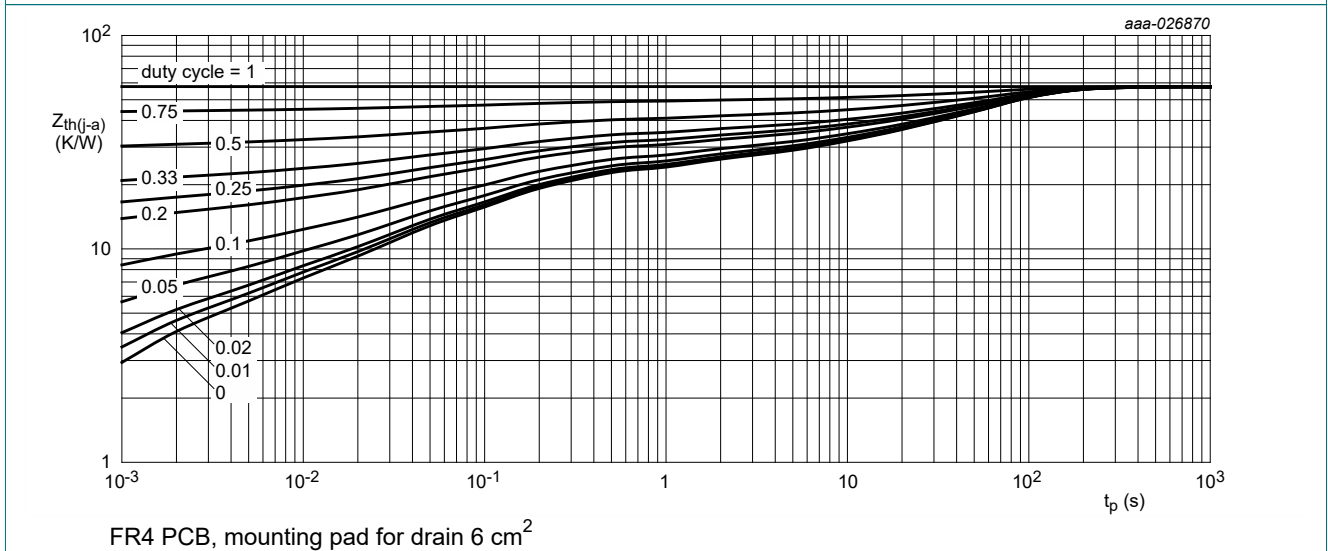
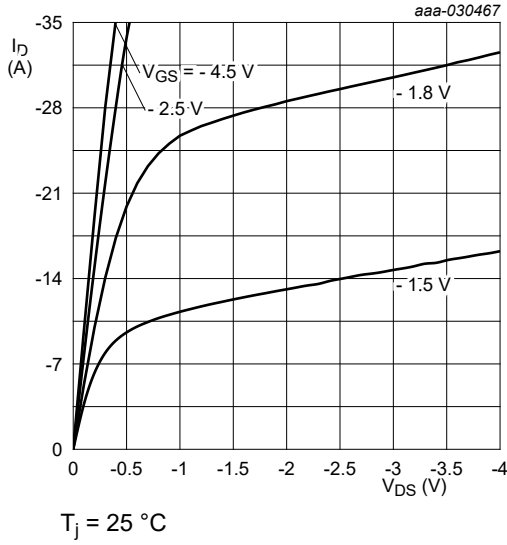


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

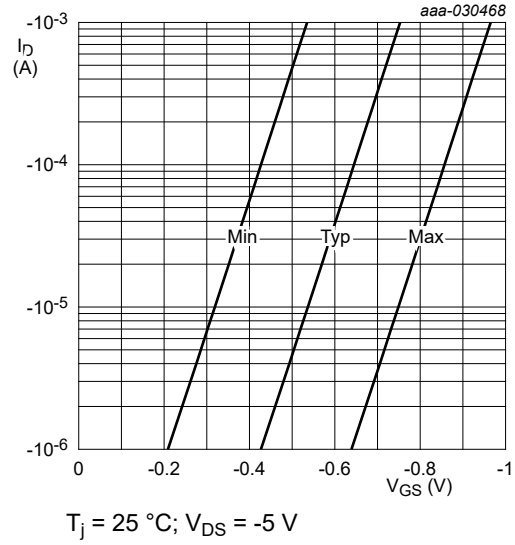
## 10. Characteristics

Table 7. Characteristics

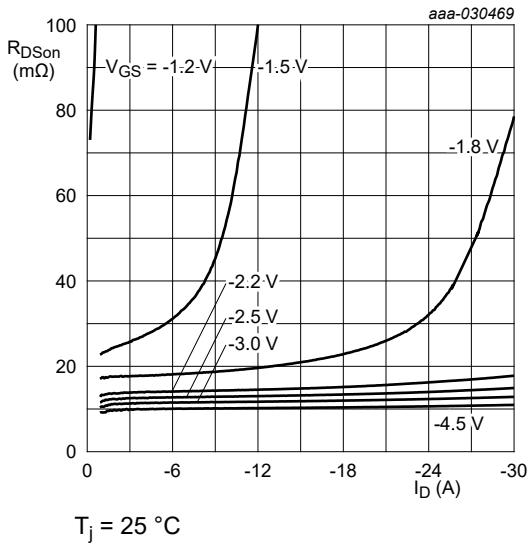
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-12	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = -250 \mu\text{A}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$	0.47	0.7	0.9	V
$I_{DSS}$	drain leakage current	$V_{DS} = -12 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-1	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 8 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -8 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	-100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = -4.5 \text{ V}$ ; $I_D = -10 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	10	11.5	m $\Omega$
		$V_{GS} = -4.5 \text{ V}$ ; $I_D = -10 \text{ A}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	14	16	m $\Omega$
		$V_{GS} = -2.5 \text{ V}$ ; $I_D = -6 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	12	15.5	m $\Omega$
		$V_{GS} = -1.8 \text{ V}$ ; $I_D = -4 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	17	22	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = -10 \text{ V}$ ; $I_D = -10 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	42	-	S
$R_G$	gate resistance	$f = 1 \text{ MHz}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	13.2	-	$\Omega$
<b>Dynamic characteristics</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = -6 \text{ V}$ ; $I_D = -10 \text{ A}$ ; $V_{GS} = -4.5 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	27	40	nC
$Q_{GS}$	gate-source charge		-	3.4	-	nC
$Q_{GD}$	gate-drain charge		-	7.6	-	nC
$C_{iss}$	input capacitance	$V_{DS} = -6 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	2200	-	pF
$C_{oss}$	output capacitance		-	509	-	pF
$C_{rss}$	reverse transfer capacitance		-	454	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = -6 \text{ V}$ ; $I_D = -10 \text{ A}$ ; $V_{GS} = -4.5 \text{ V}$ ; $R_{G(ext)} = 6 \text{ } \Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	4	-	ns
$t_r$	rise time		-	15	-	ns
$t_{d(off)}$	turn-off delay time		-	149	-	ns
$t_f$	fall time		-	100	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain voltage	$I_S = -1.6 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-0.6	-1.2	V



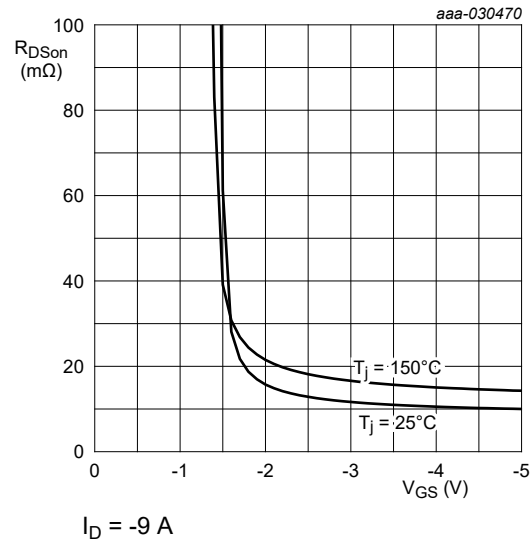
**Fig. 6. Output characteristics; drain current as a function of drain-source voltage; typical values**



**Fig. 7. Sub-threshold drain current as a function of gate-source voltage**



**Fig. 8. Drain-source on-state resistance as a function of drain current; typical values**



**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**

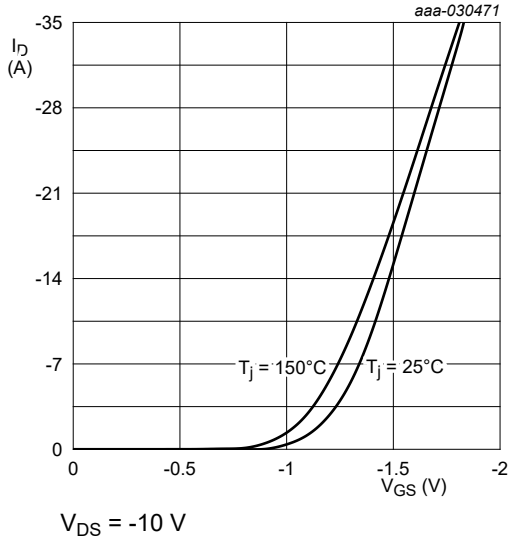
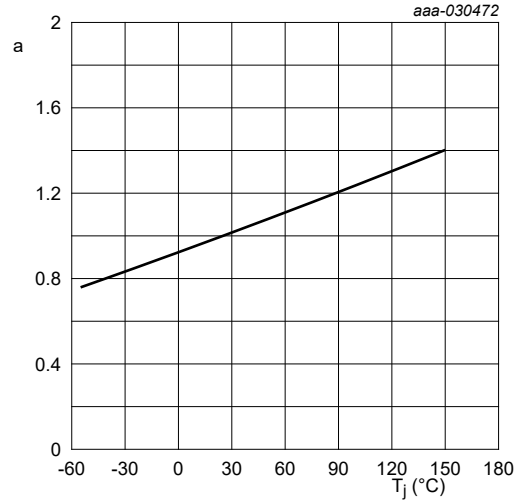
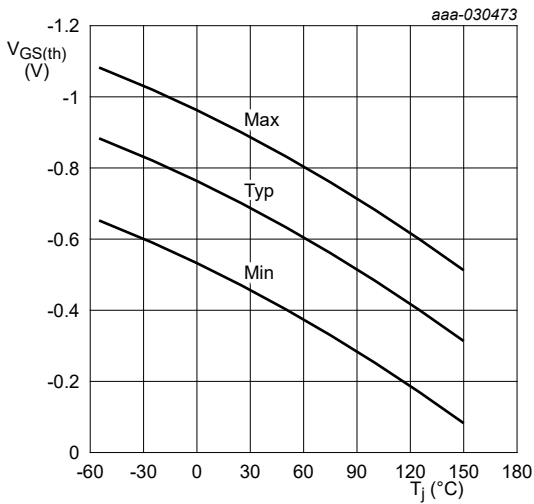


Fig. 10. Transfer characteristics; drain current as a function of gate-source voltage; typical values



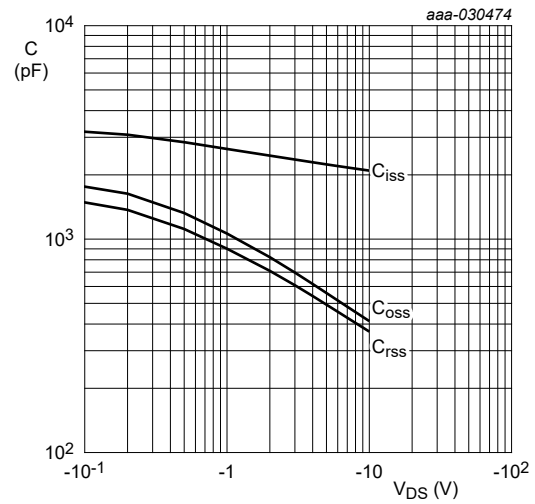
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig. 11. Normalized drain-source on-state resistance factor as a function of junction temperature; typical values



$I_D = -250\ \mu\text{A}$  ;  $V_{DS} = V_{GS}$

Fig. 12. Gate-source threshold voltage as a function of junction temperature



$V_{GS} = 0\text{ V}$  ;  $f = 1\text{ MHz}$

Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



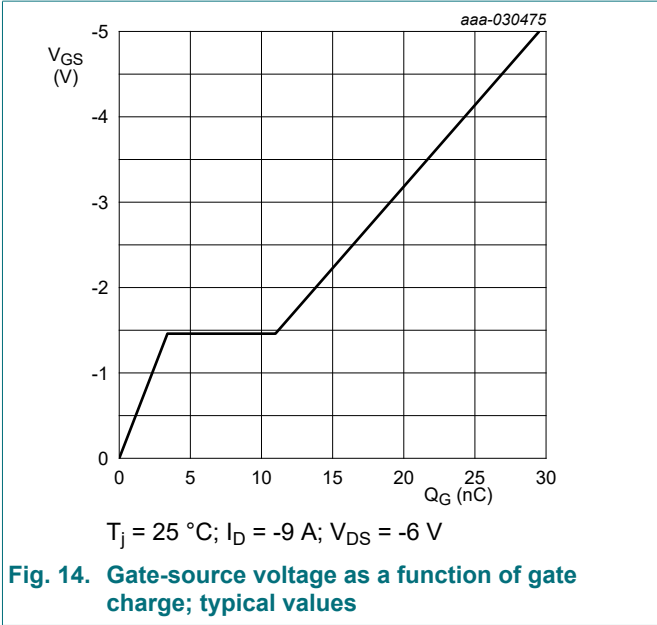


Fig. 14. Gate-source voltage as a function of gate charge; typical values

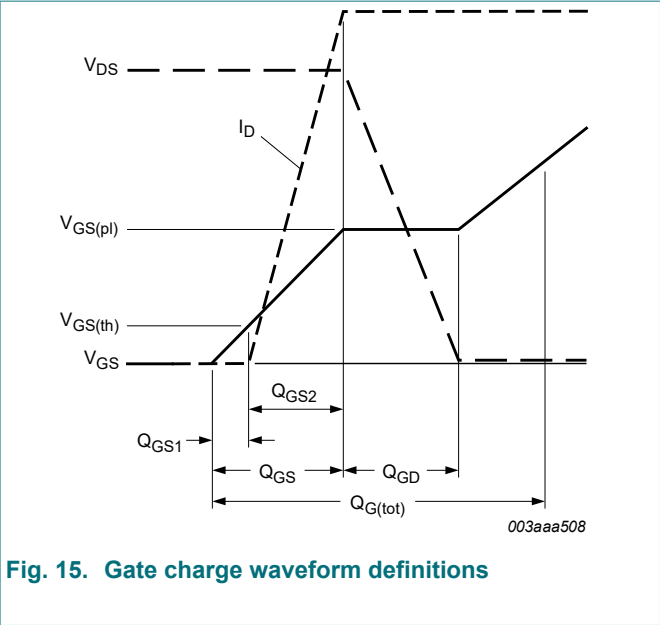


Fig. 15. Gate charge waveform definitions

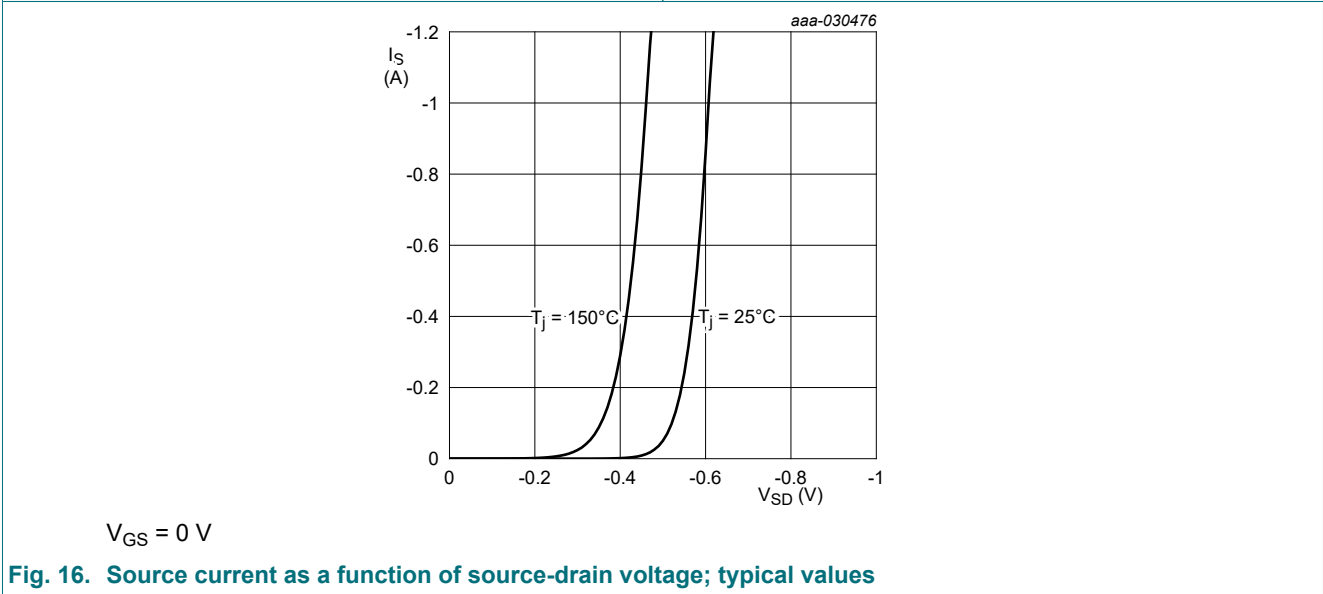


Fig. 16. Source current as a function of source-drain voltage; typical values

## 11. Test information

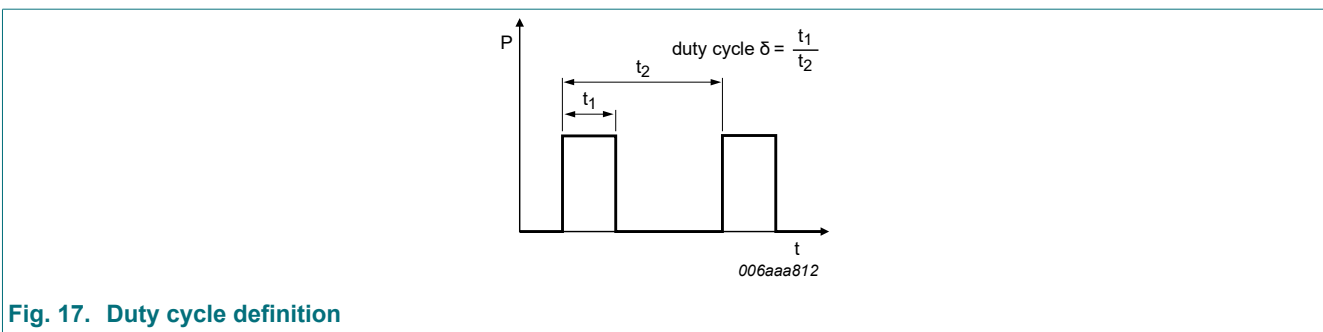


Fig. 17. Duty cycle definition

## 12. Package outline

DFN2020MD-6: plastic thermal enhanced ultra thin small outline package; no leads;  
6 terminals; body 2 x 2 x 0.65 mm

SOT1220

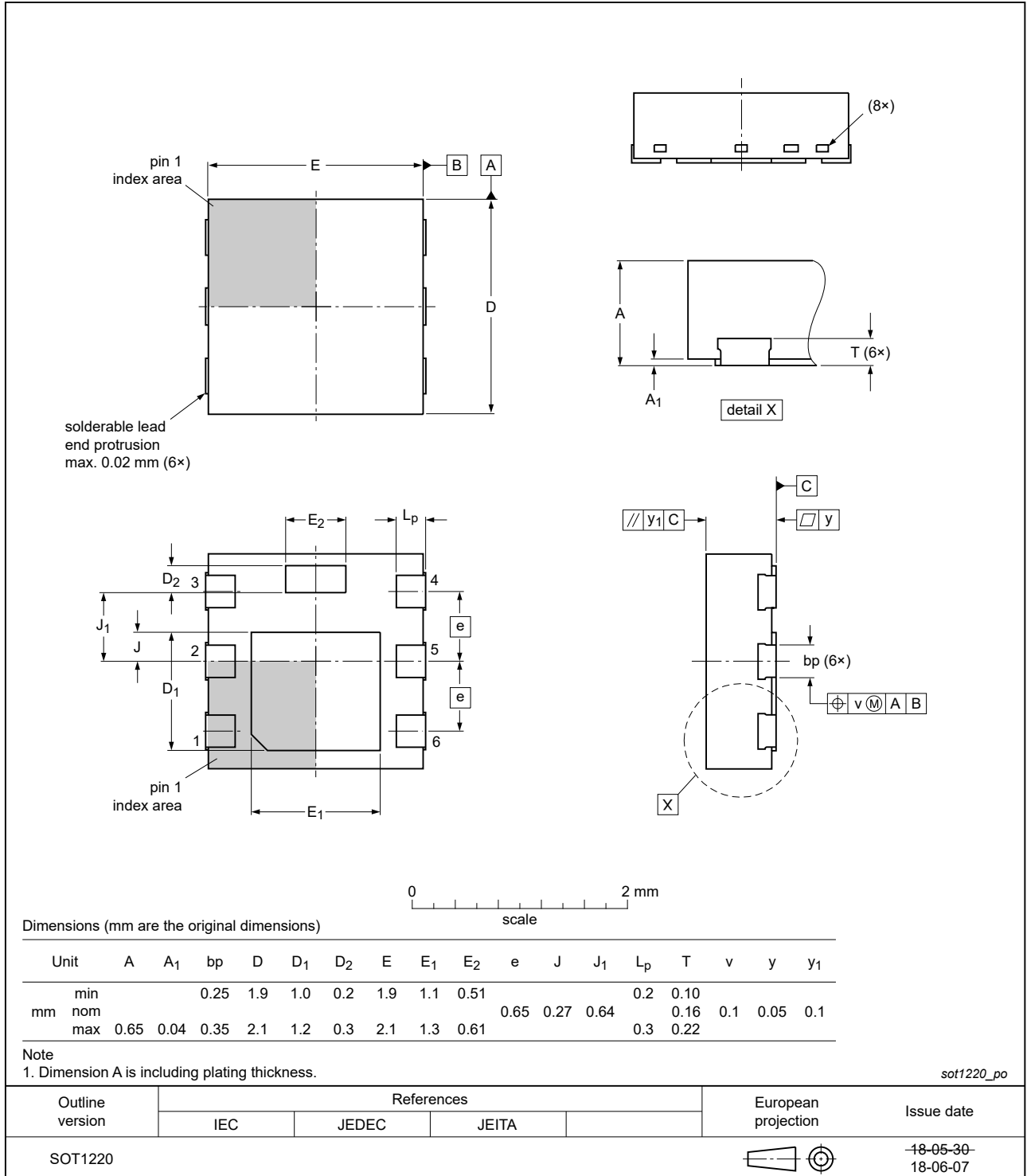


Fig. 18. Package outline DFN2020MD-6 (SOT1220)

### 13. Soldering

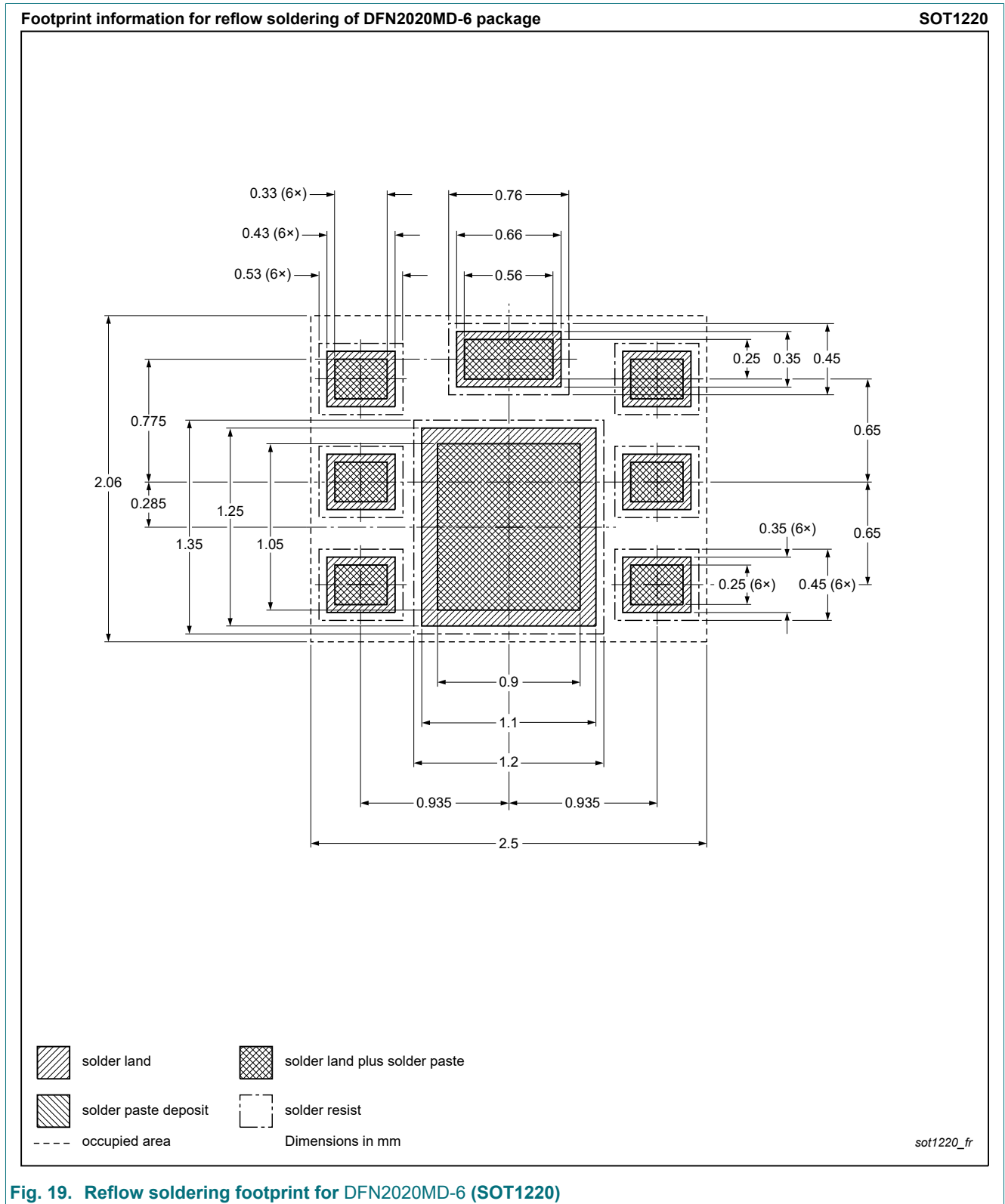


Fig. 19. Reflow soldering footprint for DFN2020MD-6 (SOT1220)

## 14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMPB10UP v.3	20201005	Product data sheet	-	PMPB10UP v.2
Modifications:	• Limiting values: Fig. 3. Safe operating area; curves revised.			
PMPB10UP v.2	20200124	Product data sheet	-	PMPB10UP v.1
PMPB10UP v.1	20191216	Product data sheet	-	-

## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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- [2] The term 'short data sheet' is explained in section "Definitions".
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