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Kind regards,

Team Nexperia

# PMDPB95XNE

30 V dual N-channel Trench MOSFET

26 September 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a leadless medium power DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- Very fast switching
- Trench MOSFET technology
- Leadless medium power SMD plastic package: 2 × 2 × 0.6 mm
- Exposed drain pad for excellent thermal conduction
- ESD protection up to 1.8 kV

### 1.3 Applications

- Charging switch for portable devices
- DC-to-DC converters
- Small brushless DC motor drive
- Power management in battery-driven portables
- Hard disk and computing power management

### 1.4 Quick reference data

Table 1. Quick reference data

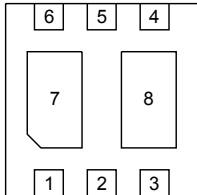
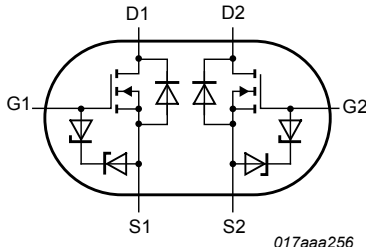
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
V <sub>DS</sub>	drain-source voltage	T <sub>J</sub> = 25 °C	-	-	30	V
V <sub>GS</sub>	gate-source voltage		-12	-	12	V
I <sub>D</sub>	drain current	V <sub>GS</sub> = 4.5 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	3.1	A
<b>Static characteristics (per transistor)</b>						
R <sub>DSon</sub>	drain-source on-state resistance	V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 2 A; T <sub>J</sub> = 25 °C	-	95	120	mΩ

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.



## 2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view <b>DFN2020-6 (SOT1118)</b></p>	 <p>017aaa256</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMDPB95XNE	DFN2020-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals; body 2 x 2 x 0.65 mm	SOT1118

## 4. Marking

Table 4. Marking codes

Type number	Marking code
PMDPB95XNE	2U

## 5. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	30	V	
$V_{GS}$	gate-source voltage		-12	12	V	
$I_D$	drain current	$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	3.1	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	2.4	A
		$V_{GS} = 4.5\text{ V}; T_{amb} = 100\text{ °C}$	[1]	-	1.5	A
$I_{DM}$	peak drain current	$T_{amb} = 25\text{ °C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$	-	9.6	A	

Symbol	Parameter	Conditions		Min	Max	Unit
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	475	mW
			[1]	-	1.1	W
		T <sub>sp</sub> = 25 °C		-	6.25	W
<b>Source-drain diode</b>						
I <sub>s</sub>	source current	T <sub>amb</sub> = 25 °C		-	1.1	A
<b>Per device</b>						
T <sub>j</sub>	junction temperature			-55	150	°C
T <sub>amb</sub>	ambient temperature			-55	150	°C
T <sub>stg</sub>	storage temperature			-65	150	°C
<b>ESD maximum rating</b>						
V <sub>ESD</sub>	electrostatic discharge voltage	HBM	[3]	-	1800	V

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.

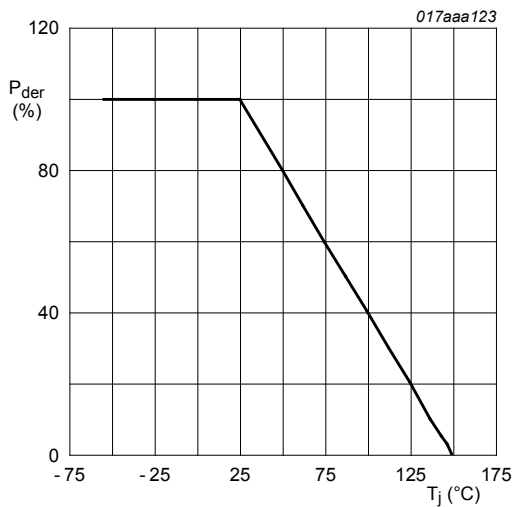


Fig. 1. Normalized total power dissipation as a function of junction temperature

$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100 \%$$

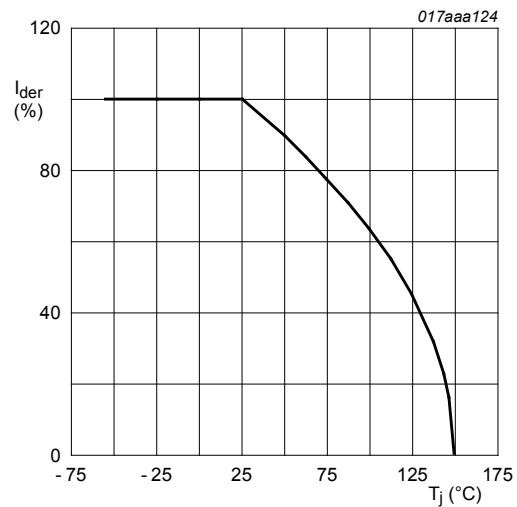
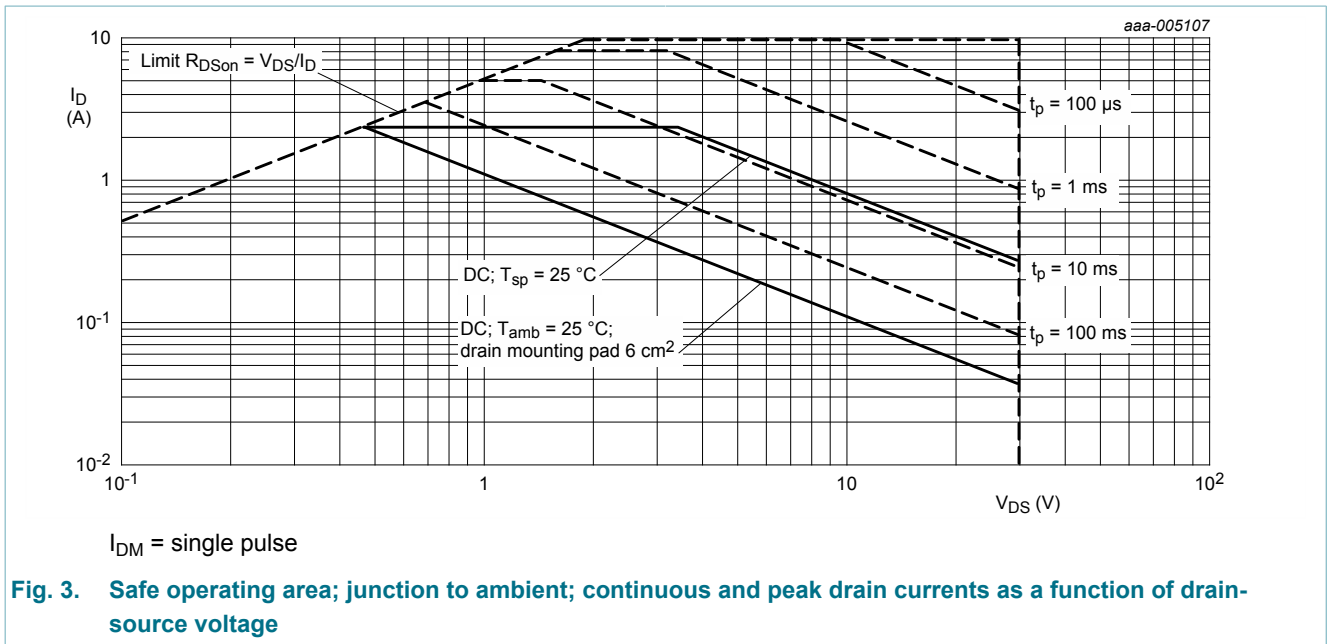


Fig. 2. Normalized continuous drain current as a function of junction temperature

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100 \%$$



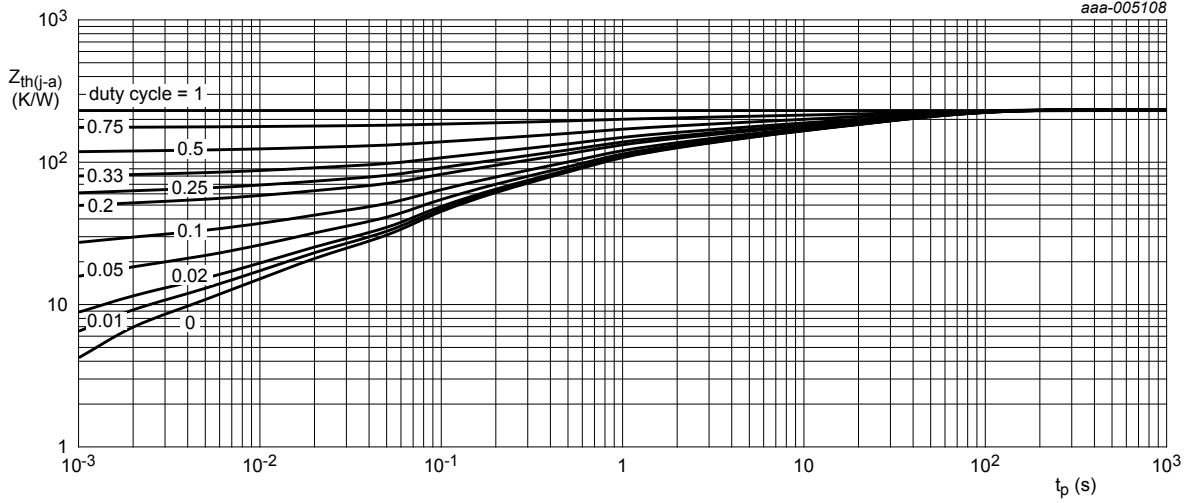
## 6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	230	260	K/W
			[2]	-	94	110	K/W
		in free air; $t \leq 5\text{ s}$	[2]	-	61	78	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	13	20	K/W

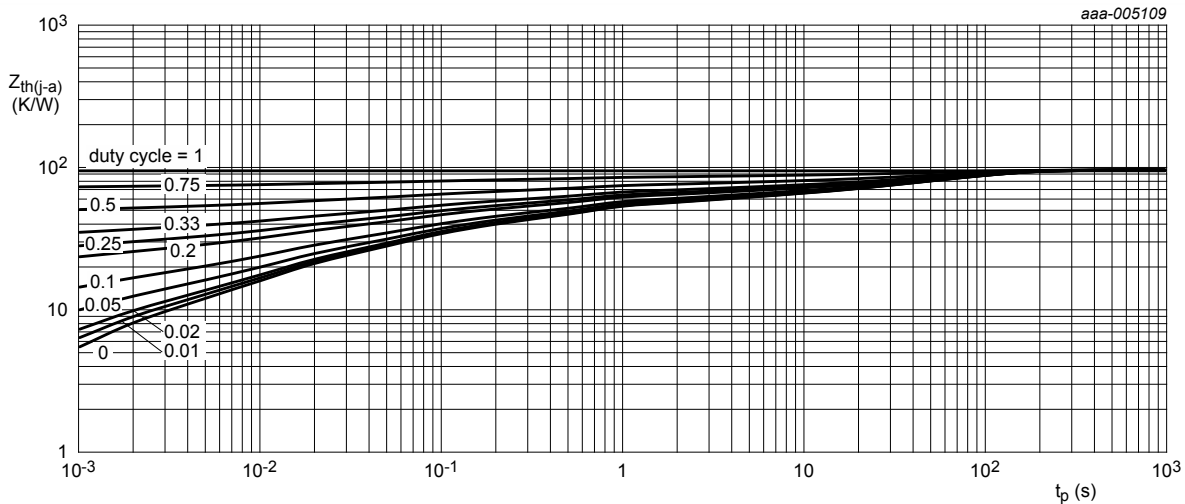
[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $6\text{ cm}^2$ .



FR4 PCB, standard footprint

Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



FR4 PCB, mounting pad for drain 6 cm<sup>2</sup>

Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

## 7. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics (per transistor)</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	30	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	0.5	1	1.5	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	1	$\mu A$
$I_{GSS}$	gate leakage current	$V_{GS} = 12 V; V_{DS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	10	$\mu A$

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_{GS} = -12\text{ V}; V_{DS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	-	-10	$\mu\text{A}$
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 4.5\text{ V}; I_D = 2\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	95	120	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}; I_D = 2\text{ A}; T_j = 150\text{ }^\circ\text{C}$	-	155	200	$\text{m}\Omega$
		$V_{GS} = 2.5\text{ V}; I_D = 0.5\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	130	165	$\text{m}\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 2\text{ A}; T_j = 25\text{ }^\circ\text{C}$	-	11	-	S
<b>Dynamic characteristics (per transistor)</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 15\text{ V}; I_D = 2\text{ A}; V_{GS} = 4.5\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	1.65	2.5	nC
$Q_{GS}$	gate-source charge		-	0.22	-	nC
$Q_{GD}$	gate-drain charge		-	0.45	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 15\text{ V}; f = 1\text{ MHz}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	143	-	pF
$C_{oss}$	output capacitance		-	43	-	pF
$C_{rss}$	reverse transfer capacitance		-	30	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15\text{ V}; I_D = 2\text{ A}; V_{GS} = 4.5\text{ V}; R_{G(ext)} = 6\text{ }\Omega; T_j = 25\text{ }^\circ\text{C}$	-	6	-	ns
$t_r$	rise time		-	11	-	ns
$t_{d(off)}$	turn-off delay time		-	18	-	ns
$t_f$	fall time		-	6	-	ns
<b>Source-drain diode (per transistor)</b>						
$V_{SD}$	source-drain voltage	$I_S = 0.7\text{ A}; V_{GS} = 0\text{ V}; T_j = 25\text{ }^\circ\text{C}$	-	0.75	1.2	V

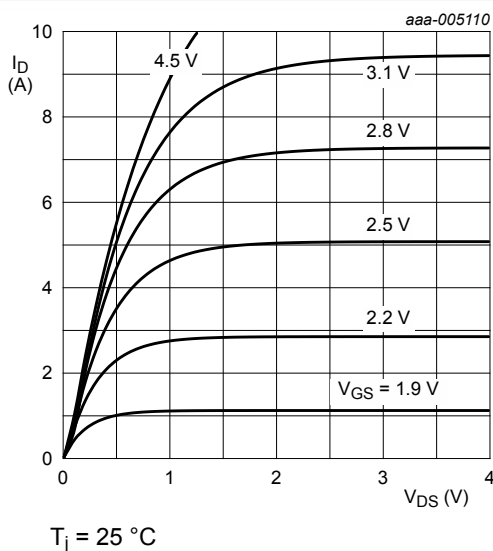


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

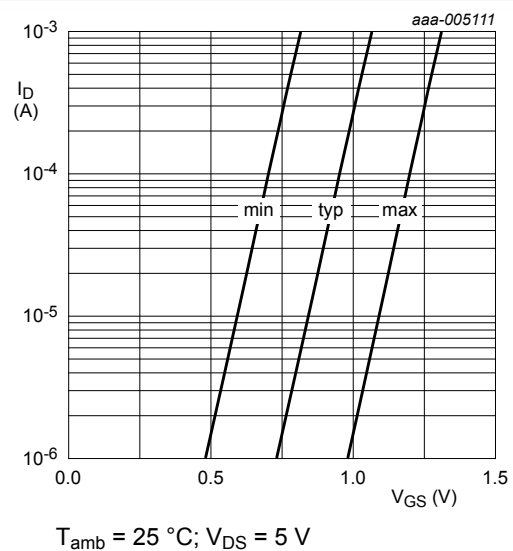
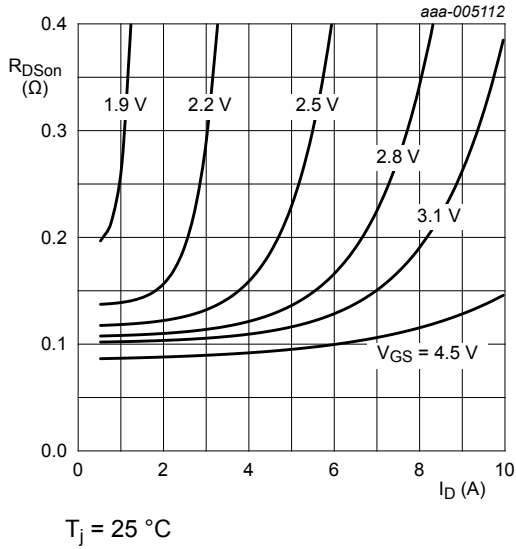
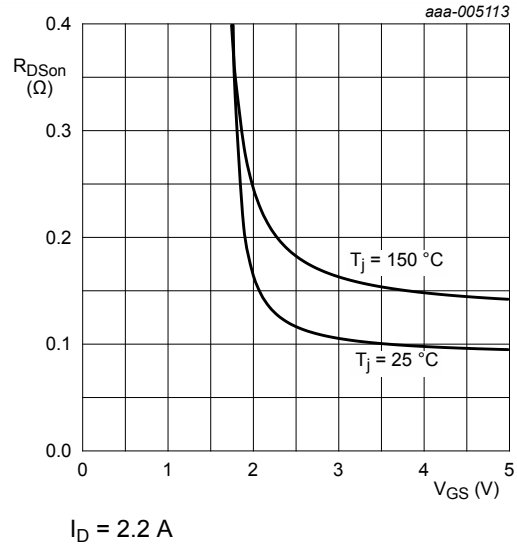


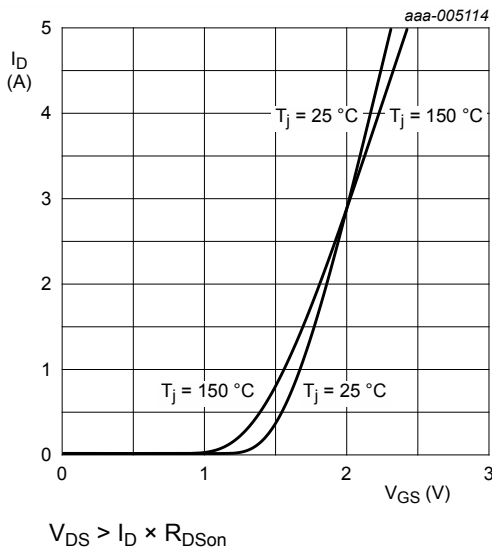
Fig. 7. Subthreshold drain current as a function of gate-source voltage



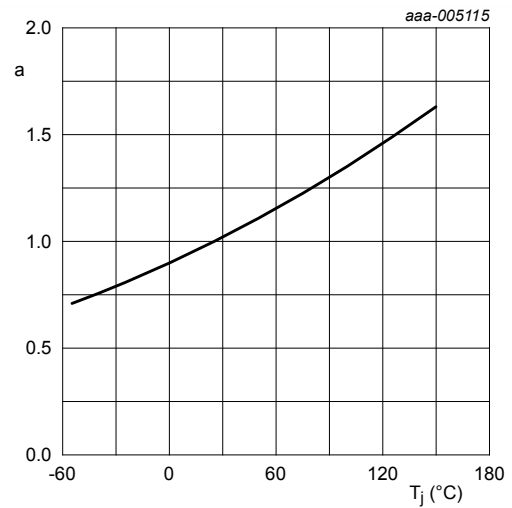
**Fig. 8. Drain-source on-state resistance as a function of drain current; typical values**



**Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



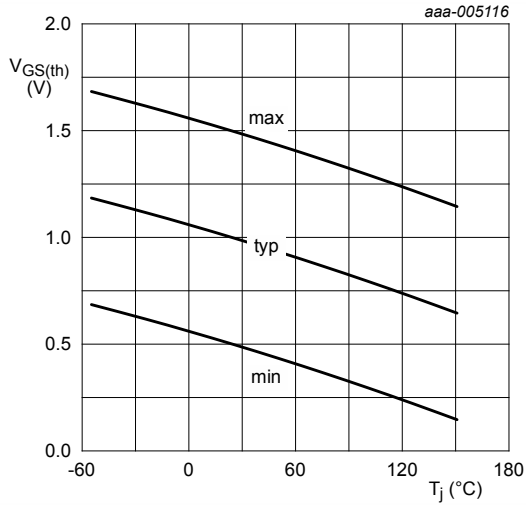
**Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



**Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**

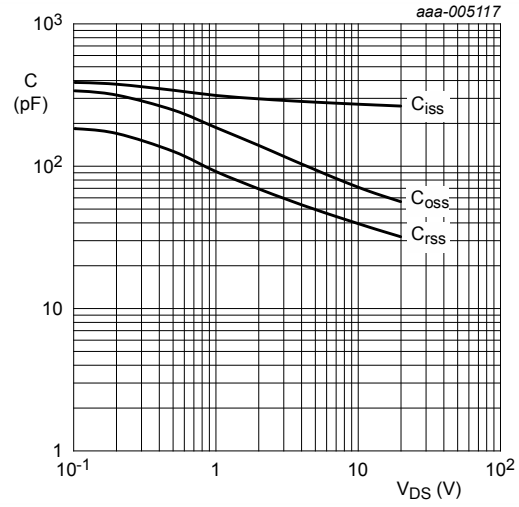
$$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$$





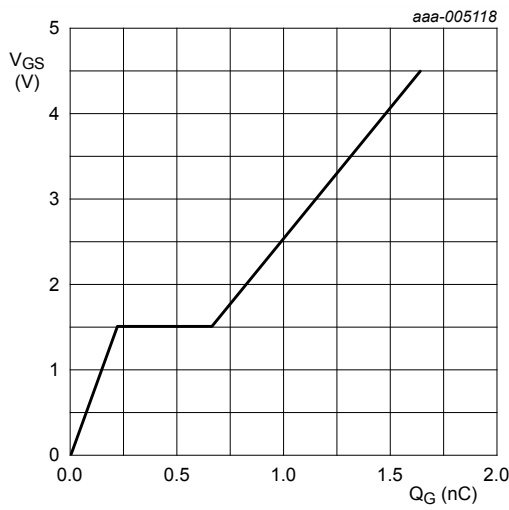
$I_D = 0.25 \text{ mA}; V_{DS} = V_{GS}$

**Fig. 12. Gate-source threshold voltage as a function of junction temperature**



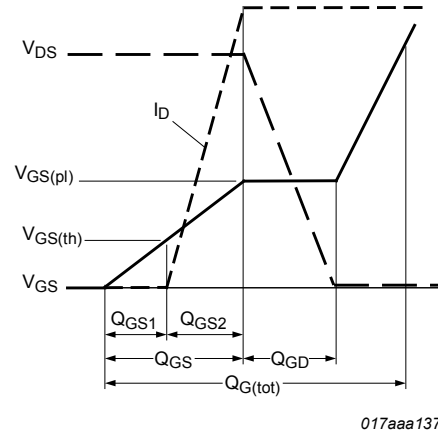
$f = 1 \text{ MHz}; V_{GS} = 0 \text{ V}$

**Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



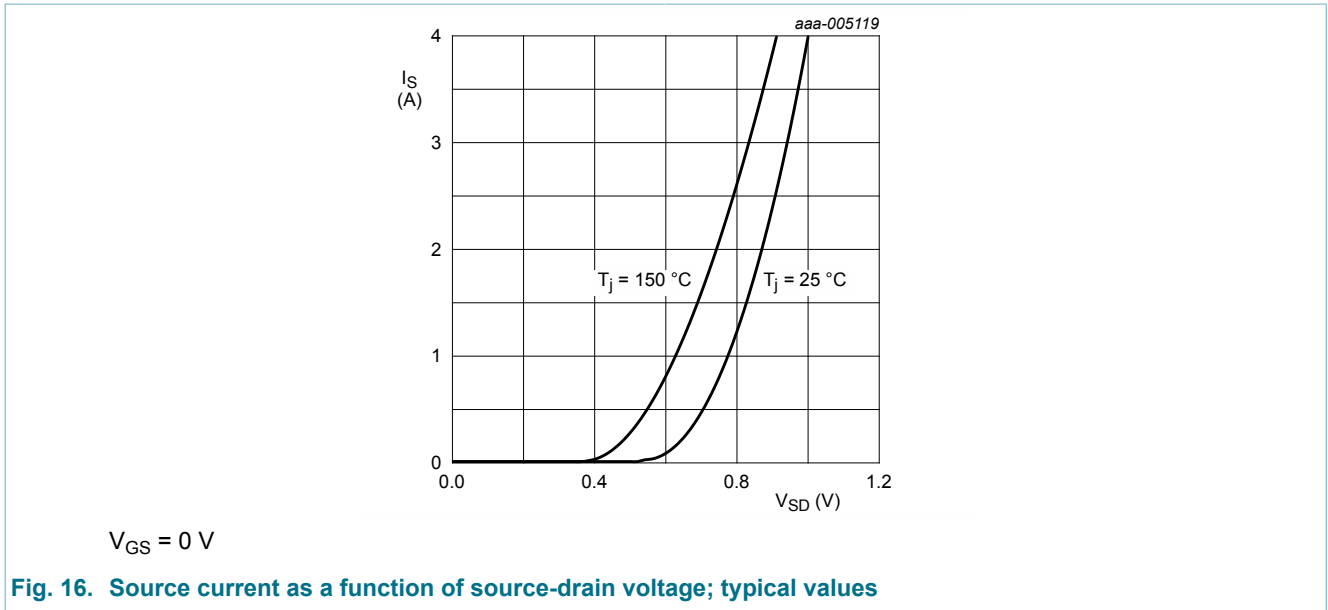
$I_D = 2 \text{ A}; V_{DS} = 15 \text{ V}; T_{amb} = 25 \text{ °C}$

**Fig. 14. Gate-source voltage as a function of gate charge; typical values**

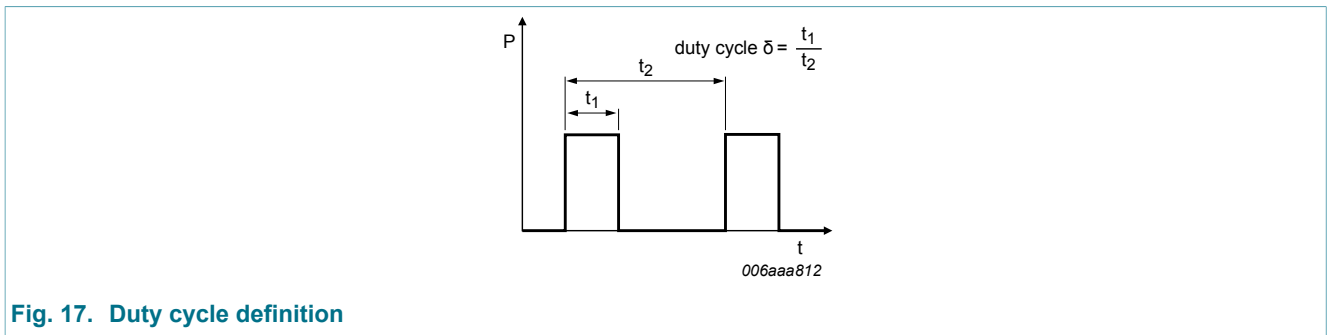


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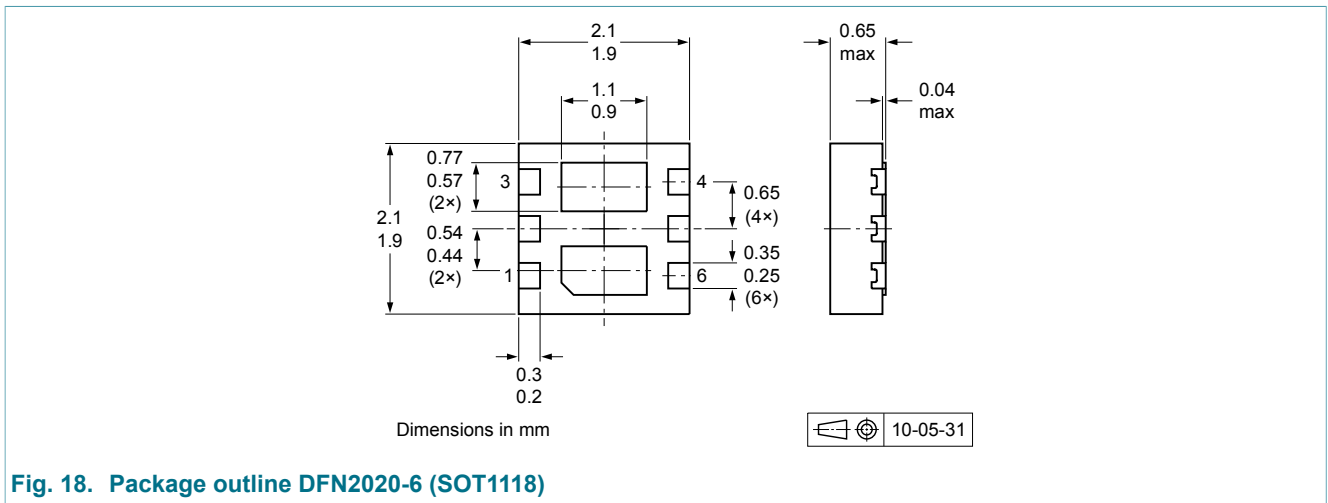
**Fig. 15. Gate charge waveform definitions**



### 8. Test information



### 9. Package outline



### 10. Soldering

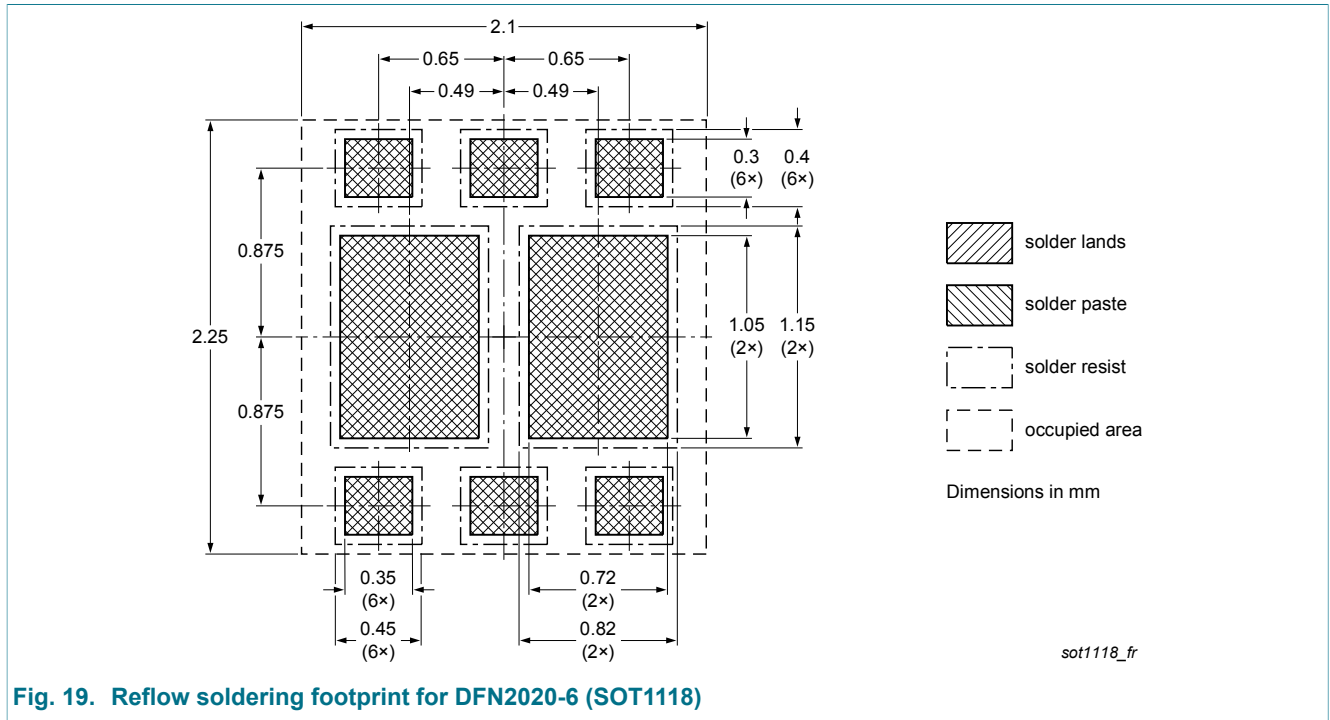


Fig. 19. Reflow soldering footprint for DFN2020-6 (SOT1118)

### 11. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB95XNE v.1	20120926	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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Date of release: 26 September 2012

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