3.2Gbps, 2-Port, SATA/SAS, Serial Re-Driver

Features

- Supports data rates up to 3.2Gbps on each lane
- Adjustable Transmiter De-Emphasis & Amplitude
- Adjustable Receiver Equalization
- Spectrum Reference Clock Buffer Output
- Optimized for SATAx/SAS applications
- Input signal level detection & output squelch on all channels
- 100-Ohm Differential CML I/O's
- Low Power (100mW per Channel)
- Standby Mode – Power Down State
- V_{DD} Operating Range: 1.8V +/-0.1V
- Packaging (Pb-free & Green):48-contact TQFN

Description

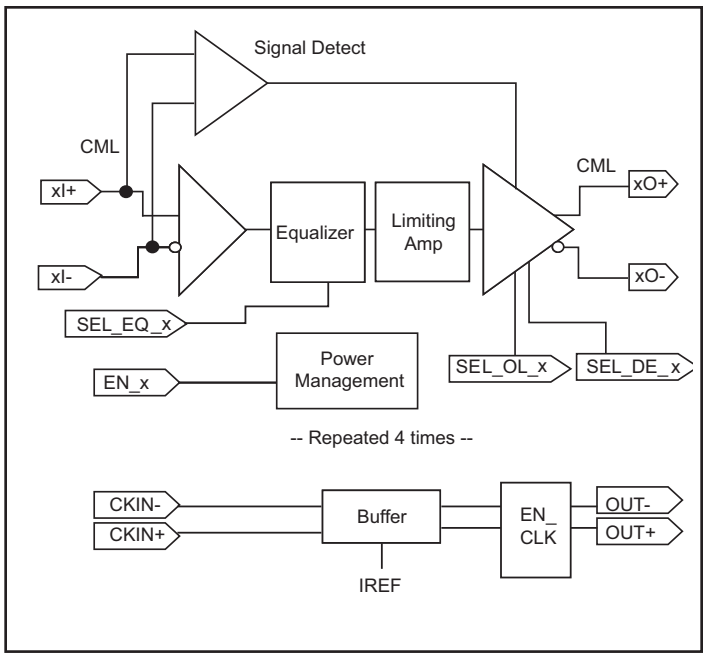
Pericom Semiconductor's PI2EQX3232A is a low power, signal Re-Driver. The device provides programmable equalization, amplification, and de-emphasis, to optimize performance over a variety of physical mediums by reducing Inter-Symbol Interference (ISI). PI2EQX3232A supports four 100-Ohm Differential CML data I/O's between the Protocol ASIC to a switch fabric, across a backplane, or to extend the signals across other distant data pathways on the user's platform.

The integrated equalization circuitry provides flexibility with signal integrity of the signal before the Re-Driver. Whereas the integrated de-emphasis circuitry provides flexibility with signal integrity of the signal after the Re-Driver.

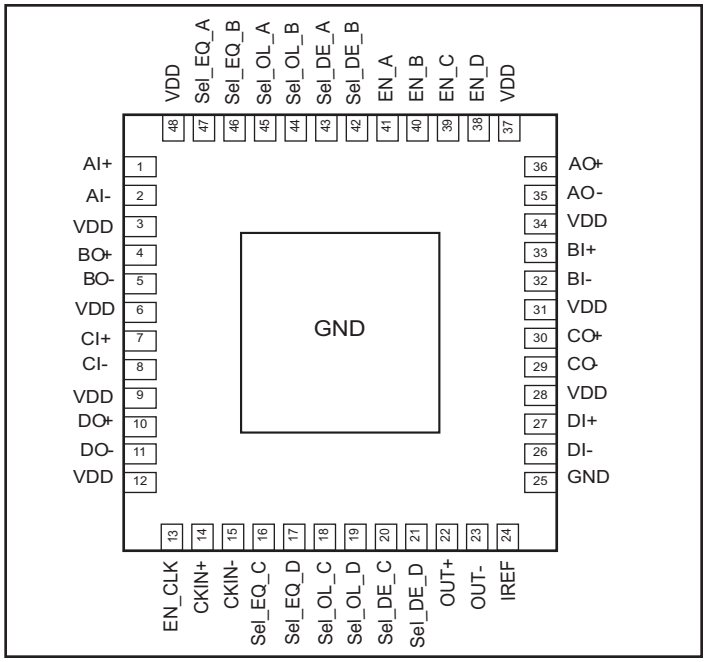
A low-level input signal detection and output squelch function is provided for all four channels. Each channel operates fully independantly. When a channel is enabled (EN_x=1) and operating, that channels input signal level (on xI+/-) determines whether the output is enabled. If the input level of the channel falls below the active threshold level (Vth-) then the output driver switches off, and the pin is pulled to VDD via a high impedance resistor. If the input level of the channel falls below the active threshold level (Vth-) then the outputs are driven to the common mode voltage.

In addition to providing signal re-conditioning, Pericom's PI2EQX3232A also provides power management Stand-by mode operated by an Enable pin.

Block Diagram



Pin Description



Pin Description

Pin #	Pin Name	I/O	Description
1	AI+	I	Positive CML Input Channel A with internal 50Ω pull down
2	AI-	I	Negative CML Input Channel A with internal 50Ω pull down
36	AO+	O	Positive CML Output Channel A internal 50Ω pull up to VDD during normal operation and 2kΩ when EN_A=0. Drives to output common mode voltage when input is $<V_{TH-}$.
35	AO-	O	Negative CML Output Channel A with internal 50Ω pull up to VDD during normal operation and 2kΩ when EN_A=0. Drives to output common mode voltage when input is $<V_{TH-}$.
33	BI+	I	Positive CML Input Channel B with internal 50Ω pull down
32	BI-	I	Negative CML Input Channel B with internal 50Ω pull down
4	BO+	O	Positive CML Output Channel B with internal 50Ω pull up to VDD during normal operation and 2kΩ when EN_B=0. Drives to output common mode voltage when input is $<V_{TH-}$.
5	BO-	O	Negative CMLOutput Channel B with internal 50Ω pull up to VDD during normal operation and 2kΩ when EN_B=0. Drives to output common mode voltage when input is $<V_{TH-}$.
7	CI+	I	Positive CML Input Channel C with internal 50Ω pull down
8	CI-	I	Negative CML Input Channel C with internal 50Ω pull down
14 15	CKIN+ CKIN-	I I	Differential Input Reference Clock The clock buffer is provided for general use, and is not needed for data channel operation.
30	CO+	O	Positive CMLOutput Channel C with internal 50Ω pull up to VDD during normal operation and 2kΩ when EN_C=0. Drives to output common mode voltage when input is $<V_{TH-}$.
29	CO-	O	Negative CMLOutput Channel C with internal 50Ω pull up to VDD during normal operation and 2kΩ when EN_C=0. Drives to output common mode voltage when input is $<V_{TH-}$.
27	DI+	I	Positive CML Input Channel D with internal 50Ω pull down
26	DI-	I	Negative CML Input Channel D with internal 50Ω pull down
10	DO+	O	Positive CMLOutput Channel D with internal 50Ω pull up during normal operation and 2kΩ pull up when EN_C=0. Drives to output common mode voltage when input is $<V_{TH-}$..
11	DO-	O	Negative CMLOutput Channel D with internal 50Ω pull up during normal operation and 2kΩ pull up when EN_C=0. Drives to output common mode voltage when input is $<V_{TH-}$..
41, 40, 39, 38	EN_ [A,B,C,D]	I	Active HIGH LVCMOS signal input pins, when HIGH, it enables the CML output. When LOW, it disables the CML output (x0+, x0-) to HI-z state. Both x0+ & x0- outputs will be pulled up to V_{DD} by internal 2kΩ resistor.
13	EN_CLK	I	Active HIGH LVCMOS signal input pin. When HIGH, it enables the OUTx+/OUTx- outputs. When LOW, it disables these outputs, with 50Ω to ground termination.
25, Center Pad	GND	PWR	Supply Ground
24	IREF	O	External 475Ω resistor connection to set the differential output current
22 23	OUT+ OUT-	O O	Differential Reference Clock Output
47	SEL_EQ_A	I	Selection pins for equalizer (see Equalizer Selection Table) w/ 50kΩ internal pull up
46	SEL_EQ_B	I	
16	SEL_EQ_C	I	
17	SEL_EQ_D	I	

Pin Description (Continued)

Pin #	Pin Name	I/O	Description
45	SEL_OL_A	I	Selection pins for amplifier (see Output Swing Control Table) w/ 50kΩ internal pull up
44	SEL_OL_B	I	
18	SEL_OL_C	I	
19	SEL_OL_D	I	
43	SEL_DE_A	I	Selection pins for De-Emphasis (See De-Emphasis Configuration Table) w/ 50kΩ internal pull up
42	SEL_DE_B	I	
20	SEL_DE_C	I	
21	SEL_DE_D	I	
3,6,9,12,28, 31,34,37,38	V_{DD}	PWR	1.8V Supply Voltage

Output Swing Control

SEL3_[A:D]	Swing
0	1x
1	1.2x

Output De-emphasis Adjustment

SEL5_[A:D]	De-emphasis
0	0dB
1	-3.5dB

Equalizer Selection

SEL0_[A:D]	Compliance Channel
0	[0:3.5dB] @ 1.6 GHz
1	[0:7.5dB] @ 1.6 GHz

Maximum Ratings

(Above which useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Supply Voltage to Ground Potential	–0.5V to +2.5V
DC SIG Voltage	–0.5V to V_{DD} +0.5V
Current Output	-25mA to +25mA
Power Dissipation Continous	800mW
Operating Temperature	0 to +70°C

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

AC/DC Electrical Characteristics (V_{DD} = 1.8 ±0.1V)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Ps	Supply Power	EN = LVCMOS Low			0.1	W
		EN = LVCMOS High			0.6	
	Latency	From input to output		2.0		ns
CML Receiver Input						
RL_{RX}	Return Loss	50 MHz to 1.25 GHz		12		dB
$V_{RX-DIFFP-P}$	Differential Input Peak-to-peak Voltage		0.200			V
$V_{RX-CM-ACP}$	AC Peak Common Mode Input Voltage				150	mV
V_{TH}-(3)	Signal Detect Threshold	E_{N_X} = High	50		200	mVp-p
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance		80	100	120	Ω
Z_{RX-DC}	DC Input Impedance		40	50	60	
Equalization						
J_{RS}	Residual Jitter(1,2)	Total Jitter			0.3	Ulp-p
		Deterministic jitter			0.2	
J_{RM}	Random Jitter(1,2)			1.5		psrms

Notes

1. K28.7 pattern is applied differentially at point A as shown in Figure 1.
2. Total jitter does not include the signal source jitter. Total jitter (TJ) = (14.1 × RJ + DJ) where RJ is random RMS jitter and DJ is maximum deterministic jitter. Signal source is a K28.5 ± pattern (00 1111 1010 11 0000 0101) for the deterministic jitter test and K28.7 (0011111000) or equivalent for random jitter test. Residual jitter is that which remains after equalizing media-induced losses of the environment of Figure 1 or its equivalent. The deterministic jitter at point B must be from media-induced loss, and not from clock source modulation. Jitter is measured at 0V at point C of Figure 1.
3. This parameter refers to OOB detection, and does not reflect data eye sensitivity. Pericom ReDriver can recover data from a closed eye.

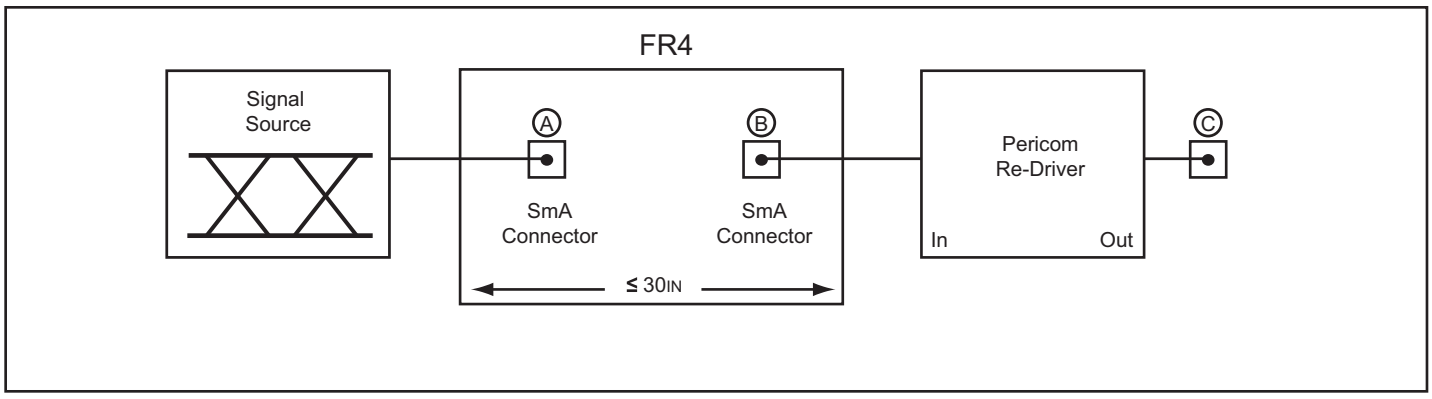


Figure 1. Test Condition Referenced in the Electrical Characteristic Table

AC/DC Electrical Characteristics (TA = 0 to 70˚C)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
CML Transmitter Output (100Ω differential)						
V_{DIFFP}	Output Voltage Swing $\lvert V_{TX-D+} - V_{TX-D-} \rvert$	Swing = 1.0x	400		650	mVp-p
		Swing = 1.2x	500		800	
V_{DIFFP}	Output Voltage Swing $\lvert V_{TX-D+} - V_{TX-D-} \rvert$	Swing = 1.0x	800		1300	mV
		Swing = 1.2x	1000		1600	
V_{TX-C}	Common-Mode Voltage	$\lvert V_{TX-D+} + V_{TX-D-} \rvert$ / 2		V_{DD}-0.3		
t_F, t_R	Transition Time	20% to 80% (1)			150	ps
Z_{OUT}	Output resistance	Single ended	40	50	60	Ω
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance		80	100	120	Ω
C_{TX}	AC Coupling Capacitor		75		200	nF
LVCMOS Control Pins						
V_{IH}	Input High Voltage		0.65 × V_{DD}		V_{DD}	V
V_{IL}	Input Low Voltage				0.35 × V_{DD}	
I_{IH}	Input High Current				250	µA
I_{IL}	Input Low Current				500	

Note:
1. Using K28.7 (0011111000) pattern)
2. When 1.0x swing selected
3. When 1.2x swing selected

AC Switching Characteristics for Clock Buffer (V_{DD} = 1.8 ±0.1V) [3]

Symbol	Parameters	Min	Max.	Units	Notes
T_{rise} / T_{fall}	Rise and Fall Time (measured between 0.175V to 0.525V) [1]	125	525	ps	1
ΔT_{rise} / ΔT_{fall}	Rise and Fall Time Variation		75		1
V_{HIGH}	Voltage High including overshoot	660	900	mV	1
V_{LOW}	Voltage Low including undershoot	-150			1
V_{CROSS}	Absolute crossing point voltages	-200	550		1
ΔV_{CROSS}	Total Variation of Vcross over all edges	200	250		1
T_{DC}	Duty Cycle (input duty cycle = 50%) [2]	45	55	%	2

Notes:
1. Measurement taken from Single Ended waveform.
2. Measurement taken from Differential waveform.
3. Test configuration is R_S = 33.2Ω, Rp = 49.9Ω, and 2pF.

Configuration Test Load Board Termination

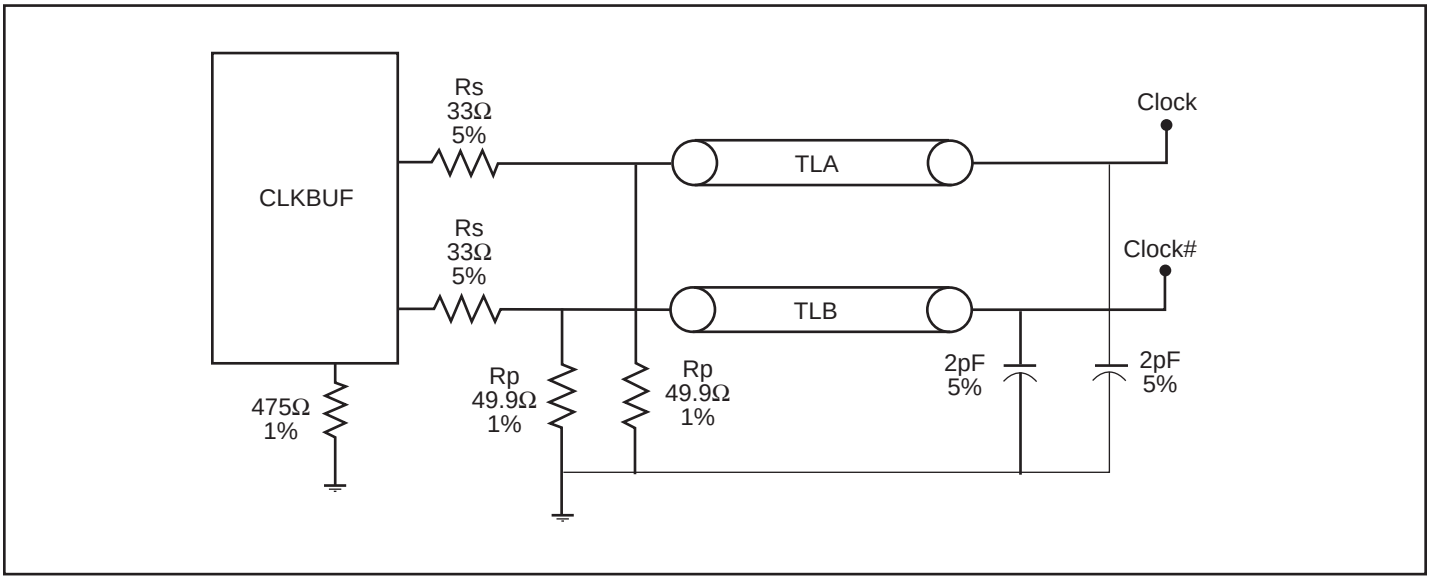
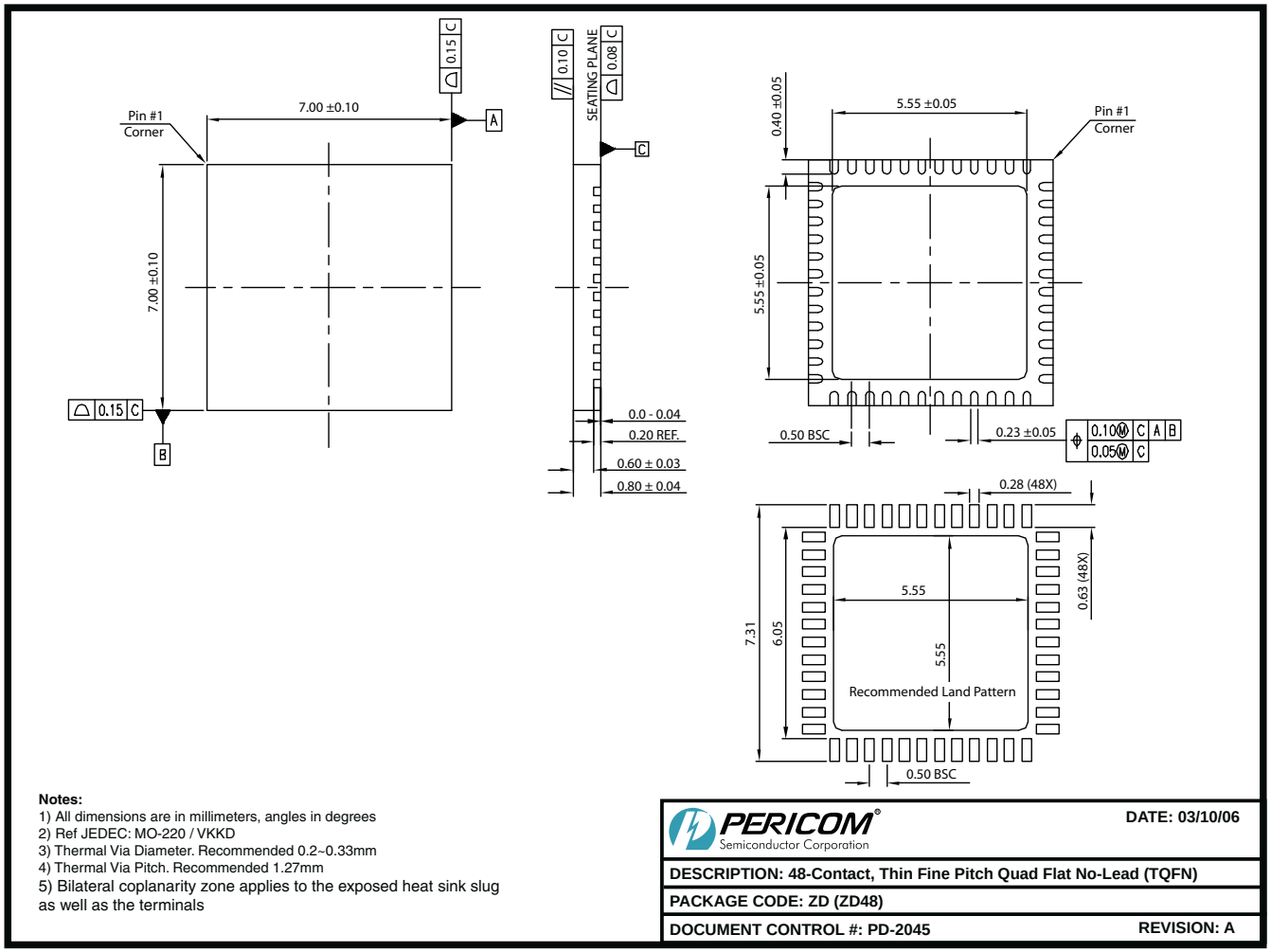


Figure 2. Configuration test load board termination

Note:
• TLA and TLB are 3” transmission lines.

Packaging Mechanical: 48-Contact TQFN (ZD48)



06-0252

Ordering Information

Ordering Number	Package Code	Package Description
PI2EQX3232AZDE	ZD	Pb-free & Green 48-Contact TQFN

Notes:

- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- E = Pb-free and Green
- X suffix = Tape/Reel