



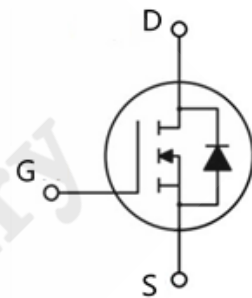
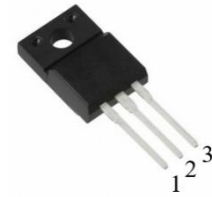
P3M171K0F3 SiC MOS N-Channel Enhancement Mode

V_{RRM}	= 1700	V
I_D	= 6	A
$I_D (100^\circ\text{C})$	= 5.4	A
$R_{DS(on)}$	= 1	Ω

SiC MOS P3M171K0F3 N-Channel Enhancement Mode

Features

- Qualified to AEC-Q101
- High Blocking Voltage with Low On-Resistance
- High-Frequency Operation
- Ultra-Small Q_{gd}
- 100% UIS tested



Standards Benefits

- Improve System Efficiency
- Increase Power Density
- Reduce Heat Sink Requirements
- Reduction of System Cost

TO-220F-3

Gate	1
Drain	2
Source	3

Application

- Solar Inverters
- EV Battery Chargers
- High Voltage DC/DC Converters
- Switch Mode Power Supplies



Order Information

Part number	Package	Marking
P3M171K0F3	TO-220F-3	P3M171K0F3



Contents

Features.....	1
Standards Benefits	1
Application.....	1
Order Information	1
Contents.....	2
1. Maximum Ratings.....	3
2. Electrical Characteristics	4
3. Reverse Diode Characteristics	5
4. Thermal Characteristics.....	5
5. Typical Performance	6
6. Package Outlines.....	10

PNJ Preliminary



1. Maximum Ratings

At $T_J = 25^\circ\text{C}$, unless specified otherwise

Parameter	Symbol	Value	Unit	Test Conditions
Drain - Source Voltage	V_{DSmax}	1700	V	$V_{GS} = 0V$ $I_D = 100\mu A$
Gate - Source Voltage (Dynamic)	V_{GSmax}	-8 / +19	V	AC ($f > 1\text{Hz}$)
Gate - Source Voltage (Static)	V_{GSop}	-3 / +15	V	Static
Continuous Drain Current	I_D	5.5	A	$V_{GS} = 15V$ $T_C = 25^\circ\text{C}$
		3.9		$V_{GS} = 15V$ $T_C = 100^\circ\text{C}$
Power Dissipation	P_D	51	W	
Operating Junction Temperature	T_J	-55 To +175	$^\circ\text{C}$	
Storage Temperature	T_{stg}	-55 To +175	$^\circ\text{C}$	
Solder Temperature	T_L	260	$^\circ\text{C}$	
Mounting Torque	M_d	1 8.8	Nm lbf-in	M3 or 6-32 screw



2. Electrical Characteristics

At $T_J = 25^\circ\text{C}$, unless specified otherwise

Parameter	Symbol	Value			Unit	Test Conditions
		Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	1700	/	/	V	$V_{GS} = 0V$ $I_D = 100\mu A$
Gate Threshold Voltage	$V_{GS(th)}$	1.8	2.2	/	V	$V_{DS} = V_{GS}$ $I_D = 2mA$
		/	1.45	/	V	$V_{DS} = V_{GS}$ $I_D = 2mA$ $T_J = 175^\circ\text{C}$
Gate Voltage Drain Current	I_{DSS}	/	/	200	μA	$V_{GS} = 0V$ $V_{DS} = 1700V$
Gate-Source Leakage Current	I_{GSS}	/	2	125	nA	$V_{GS} = 15V$ $V_{DS} = 0V$
Drain-Source On-State Resistance	$R_{DS(on)}$	/	1	1.4	Ω	$V_{GS} = 15V$ $I_D = 2A$
Transconductance	g_{fs}	/	1.32	/	S	$V_{DS} = 20V$ $I_{DS} = 2A$
		/	1.2	/	S	$V_{DS} = 20V$ $I_{DS} = 2A$ $T_J = 175^\circ\text{C}$
Input Capacitance	C_{iss}	/	459	/	pF	$V_{GS} = 0V$ $V_{DS} = 1000V$ $F = 1MHz$ $V_{AC} = 25mV$
Output Capacitance	C_{oss}	/	47.4	/	pF	
Reverse Transfer Capacitance	C_{rss}	/	5.61	/	pF	
Coss Stored Energy	E_{oss}	/	25.2	/	μJ	
Turn-on Energy	E_{on}	/	151.8	/	μJ	
Turn-off Energy	E_{off}	/	44.7	/		$V_{DS} = 1200V$ $V_{GS} = -3/15V$ $I_{DS} = 0.5A$ $R_G = 1\Omega$



P3M171K0F3 SiC MOS N-Channel Enhancement Mode

Parameter	Symbol	Value			Unit	Test Conditions
		Min.	Typ.	Max.		
Gate to Source Charge	Q_{gs}	/	6.15	/	nC	$V_{DS} = 800V$ $I_{DS} = 2A$ $V_{GS} = 15V$ $I_G = 1mA$
Gate to Drain Charge	Q_{gd}	/	10.1	/		
Total Gate Charge	Q_g	/	24.4	/		

3. Reverse Diode Characteristics

At $T_J = 25^\circ C$, unless specified otherwise

Parameter	Symbol	Value		Unit	Test Conditions
		Typ.	Max.		
Diode Forward Voltage	V_{SD}	4.1	/	V	$V_{GS} = -3V$ $I_{SD} = 1A$
		3.0	/	V	$V_{GS} = -3V$ $I_{SD} = 1A$ $T_J = 175^\circ C$
Continuous Diode Forward Current	I_S	7.7	/	A	$V_{GS} = -3V$ $T_J = 25^\circ C$
Reverse Recovery Charge	Q_{rr}	180	/	nC	$V_{GS} = -3V$ $I_{SD} = 2A$ $V_R = 1200V$ $d_{if}/d_t = 500A/\mu s$ $T_J = 25^\circ C$

4. Thermal Characteristics

Parameter	Symbol	Value	Unit
Thermal Resistance from Junction to Case	$R_{\theta JC}$	2.97	$^\circ C/W$

5. Typical Performance

At $T_J = 25^\circ\text{C}$, unless specified otherwise

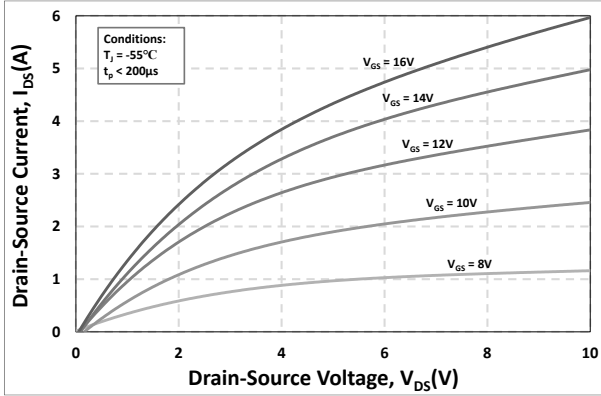


Figure 1. Output Characteristics $T_J = -55^\circ\text{C}$

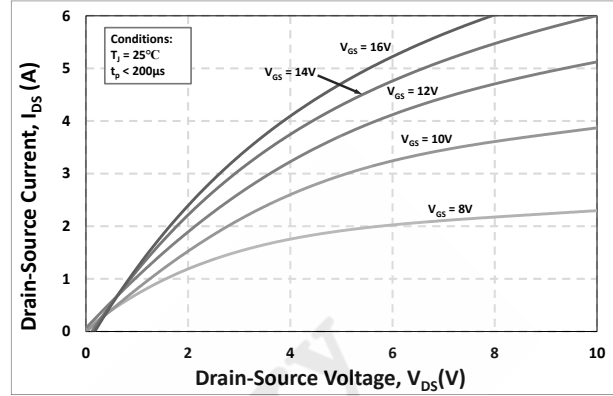


Figure 2. Output Characteristics $T_J = 25^\circ\text{C}$

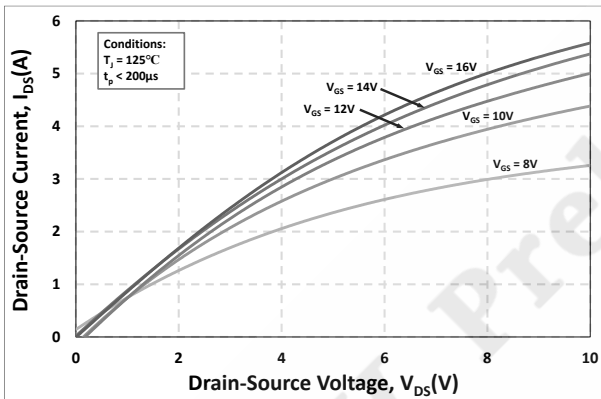


Figure 3. Output Characteristics $T_J = 125^\circ\text{C}$

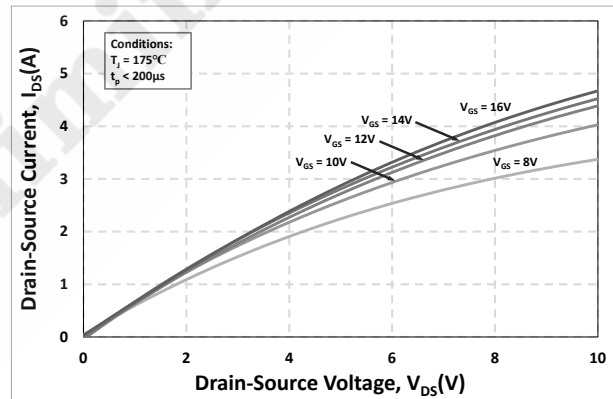


Figure 4. Output Characteristics $T_J = 175^\circ\text{C}$

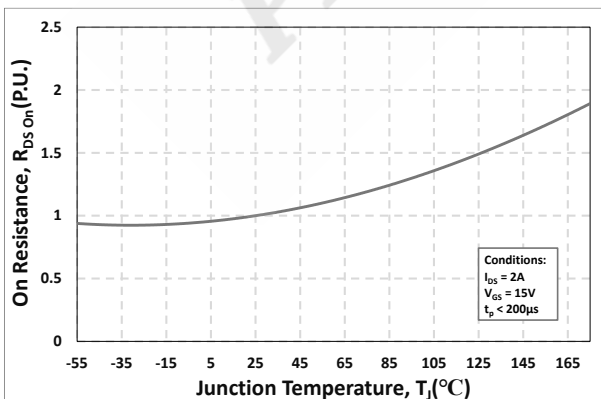


Figure 5. Normalized On-Resistance vs. Temperature

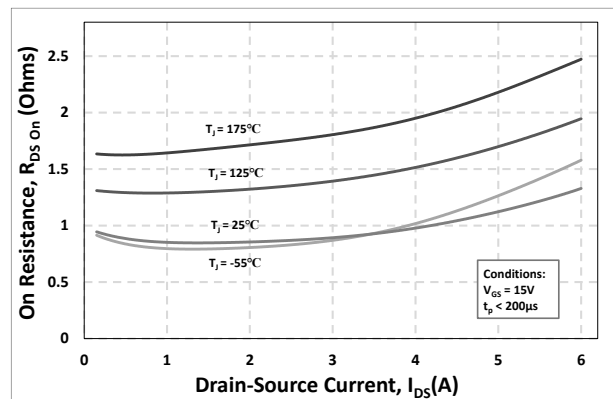


Figure 6. On-Resistance vs. Drain Current Various Temperatures

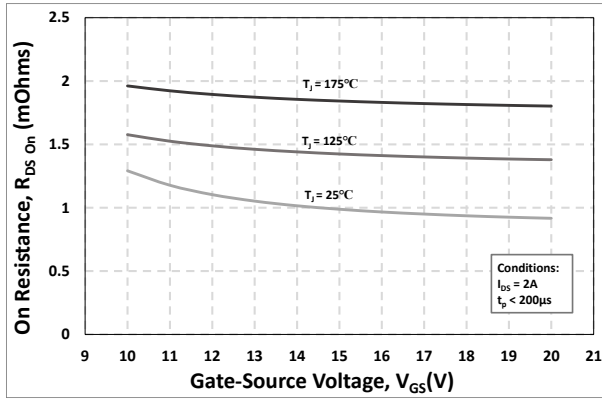


Figure 7. On-Resistance vs. Gate-Source Voltage

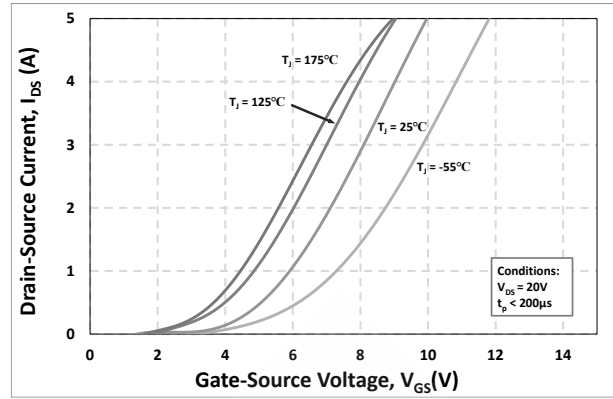


Figure 8. Transfer Characteristic for Various Junction Temperatures

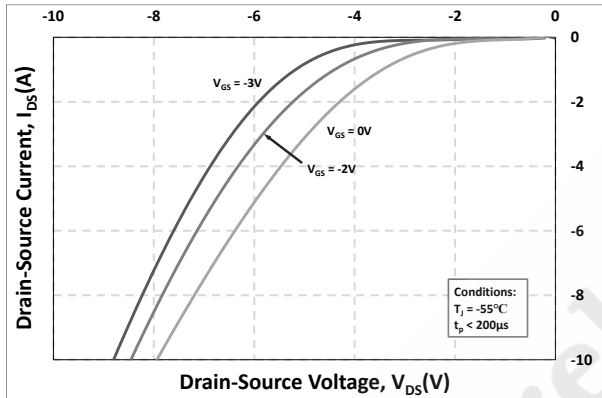


Figure 9. Body Diode Characteristic at -55°C

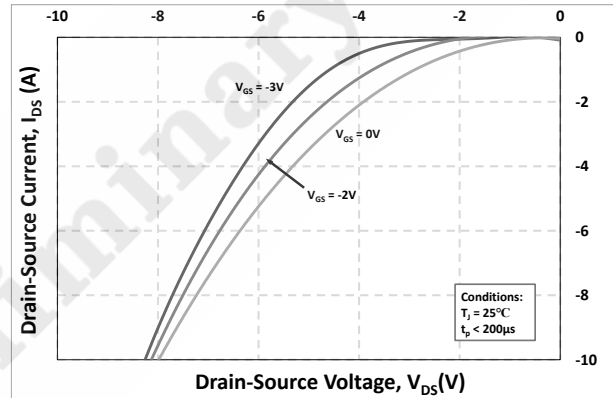


Figure 10. Body Diode Characteristic at 25°C

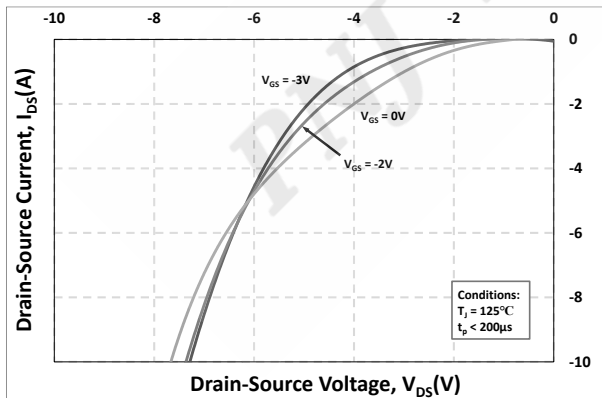


Figure 11. Body Diode Characteristic at 125°C

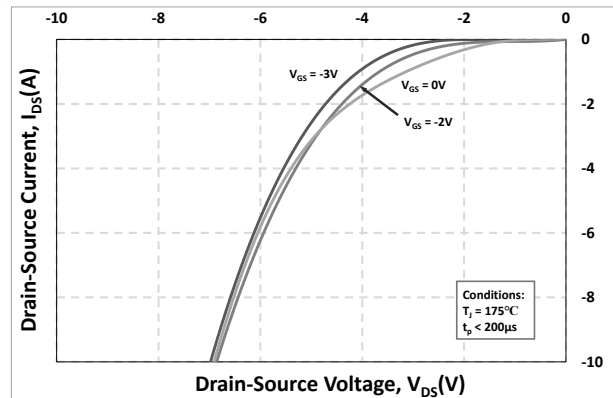


Figure 12. Body Diode Characteristic at 175°C



P3M171K0F3 SiC MOS N-Channel Enhancement Mode

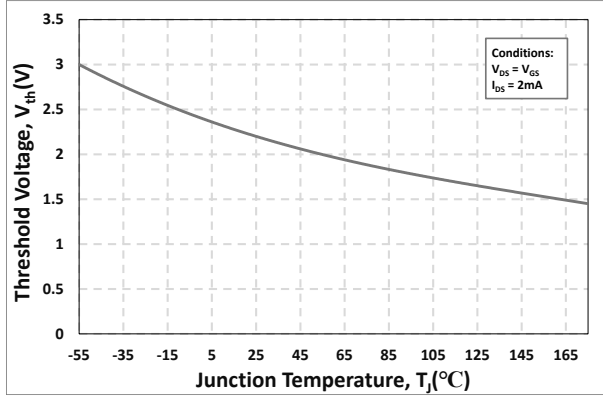


Figure 13. Threshold Voltage vs. Temperatures

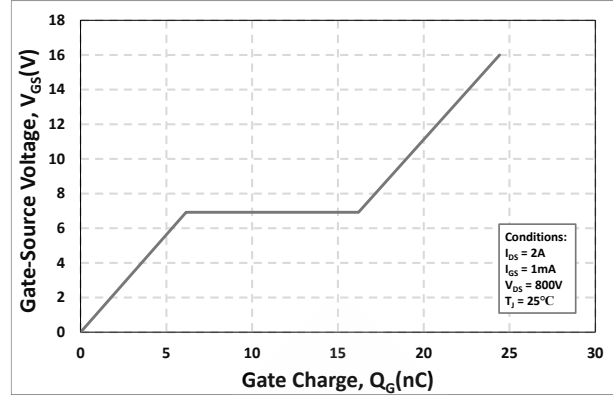


Figure 14. Gate Charge Characteristics

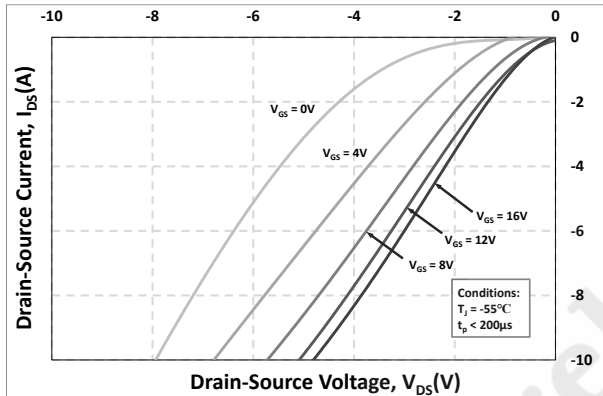


Figure 15. 3rd Quadrant Characteristic at -55°C

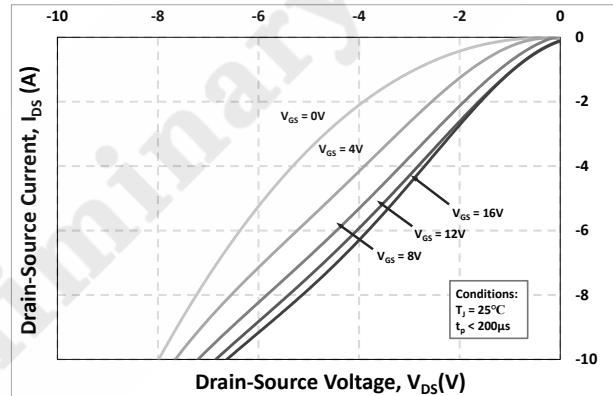


Figure 16. 3rd Quadrant Characteristic at 25°C

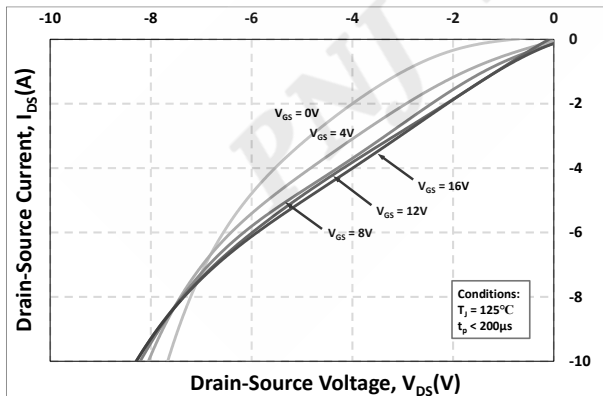


Figure 17. 3rd Quadrant Characteristic at 125°C

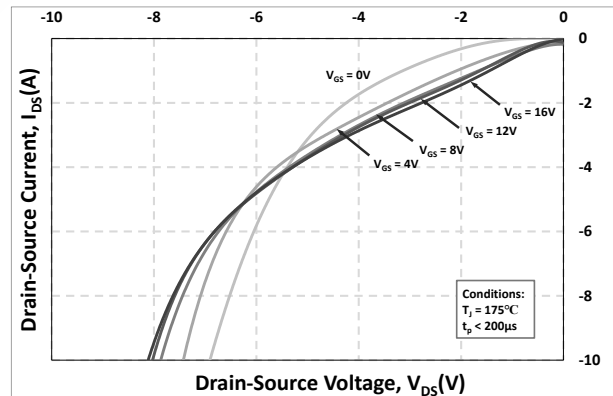


Figure 18. 3rd Quadrant Characteristic at 175°C



P3M171K0F3 SiC MOS N-Channel Enhancement Mode

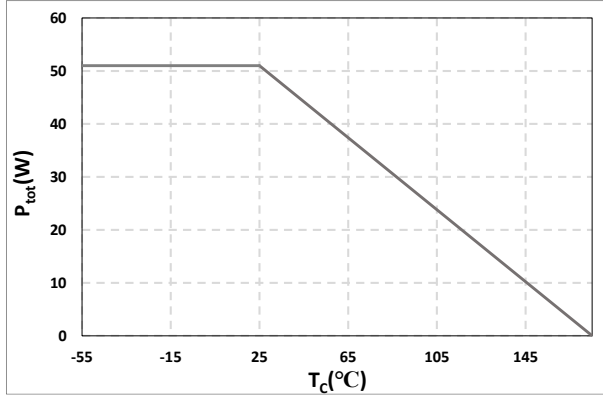


Figure 19. Maximum Power Dissipation Derating vs. Case Temperature

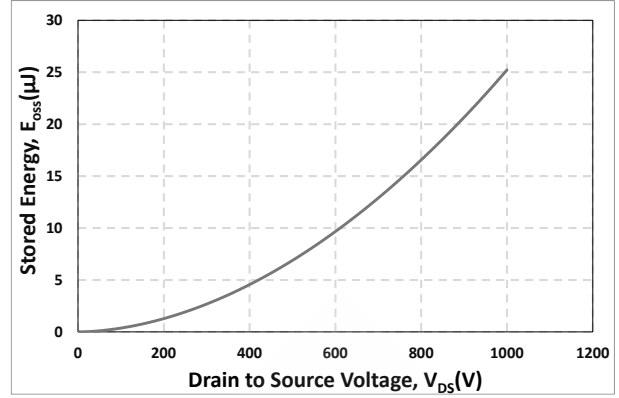


Figure 20. Output Capacitor Stored Energy

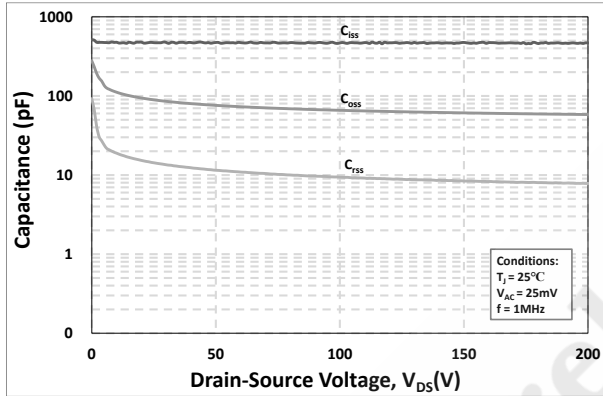


Figure 21. Capacitances vs. Drain-Source Voltage (0-200V)

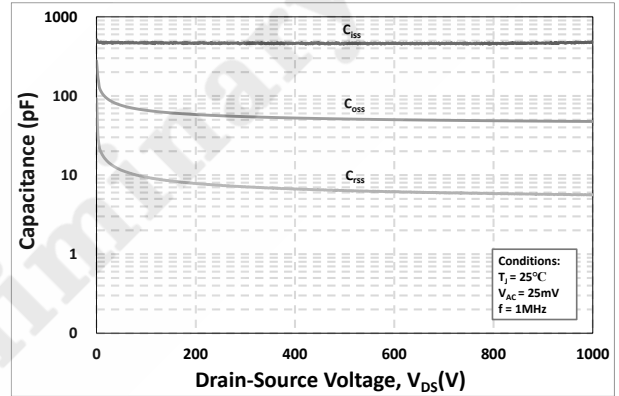
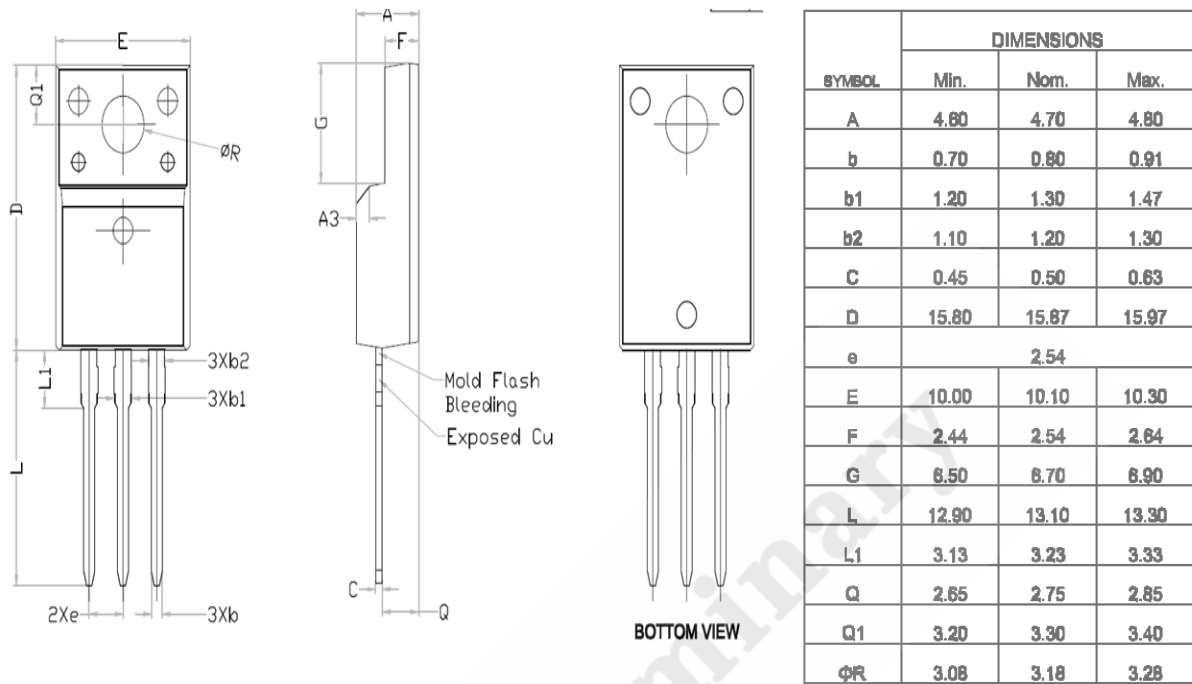


Figure 22. Capacitances vs. Drain-Source Voltage (0-1000V)

6. Package Outlines



Drawing and dimensions

PNJ Preliminary