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## 11.3 Gbps Linear Transimpedance Amplifier With AGC and RSSI

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### FEATURES

- 8 GHz Bandwidth
- 5.5 k $\Omega$  Differential Small Signal Transimpedance
- Automatic Gain Control (AGC)
- 5% THD Typical with 100 MHz Input
- 10 pA/ $\sqrt{\text{Hz}}$  Typical Input Referred Noise
- 2 mA<sub>p-p</sub> Input Current Linear Operation
- Received Signal Strength Indication (RSSI)
- CML Data Outputs With On-Chip 50  $\Omega$  Back-Termination
- On Chip Supply Filter Capacitor
- Single 3.3 V Supply

- Die Size: 945  $\times$  1200  $\mu\text{m}$
- Case temperature operation:  $-25^{\circ}\text{C}$  to  $100^{\circ}\text{C}$

### APPLICATIONS

- 10 Gigabit Ethernet LRM Optical Receivers
- SFP+ Optical Receivers
- 8 $\times$  and 10 $\times$  Fibre Channel Optical Receivers
- SONET OC-192
- PIN Preamplifier-Receivers

### DESCRIPTION

The ONET8511T is a high-speed, high linearity transimpedance amplifier used in optical receivers with data rates up to 11.3 Gbps. It features low input referred noise, 8 GHz bandwidth, 5.5 k $\Omega$  small signal transimpedance, automatic gain control (AGC) which provides highly linear operation and a received signal strength indicator (RSSI).

The ONET8511T is available in die form, includes an on-chip VCC bypass capacitor and is optimized for packaging in a TO can and for the use together with electronic dispersion compensation (EDC) ICs.

The ONET8511T requires a single +3.3 V supply and its power efficient design typically dissipates less than 160 mW. The device is characterized for operation from  $-25^{\circ}\text{C}$  to  $100^{\circ}\text{C}$  (IC back side) temperature..



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**BLOCK DIAGRAM**

Figure 1 shows an ONET8511T block diagram. The ONET8511T consists of the signal path, supply filters, a control block for DC input bias, automatic gain control (AGC), and received signal strength indicator (RSSI). The RSSI provides the bias for the TIA stage and the control for the AGC.

The signal path consists of a transimpedance amplifier stage, an AGC voltage amplifier, and a CML output buffer. The on-chip filter circuit provides a filtered VCC for the photodiode and for the transimpedance amplifier.

The DC input bias circuit and automatic gain control use internal low pass filters to cancel the DC current on the input and to adjust the transimpedance amplifier gain. Additionally, the chip provides circuitry to monitor the received signal strength.

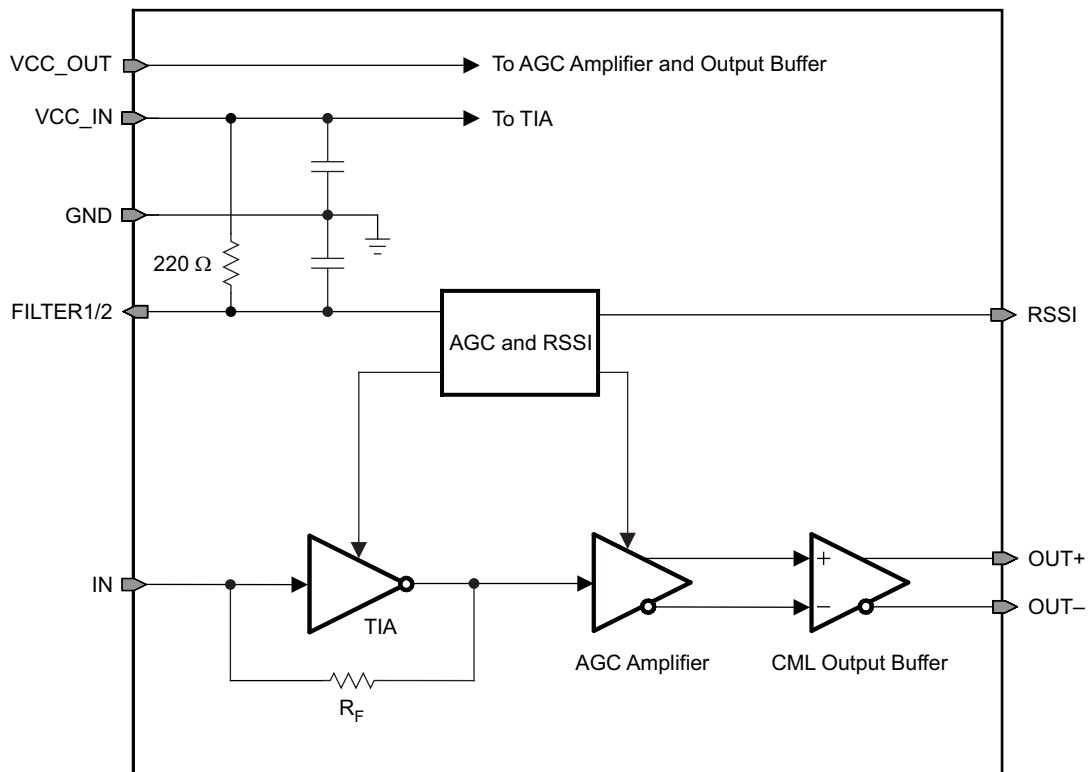
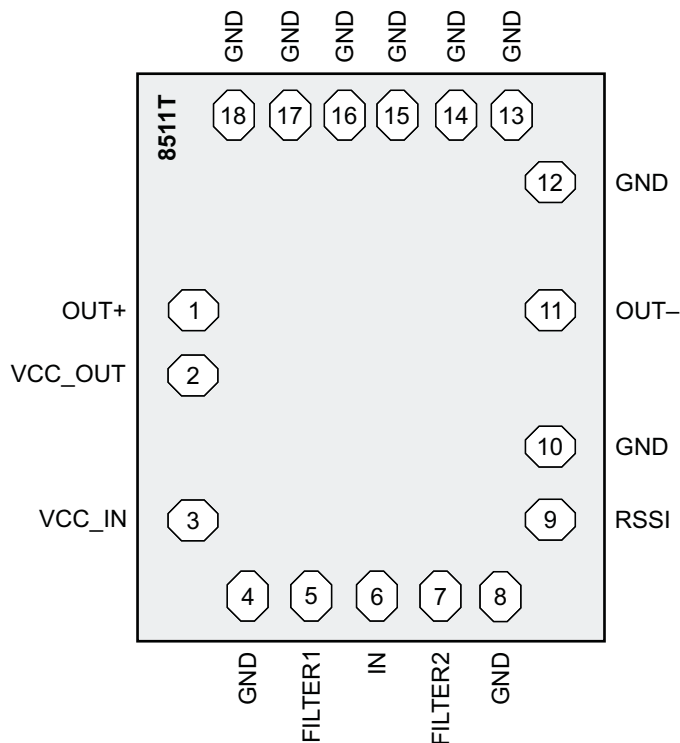


Figure 1. ONET8511T Block Diagram

## BOND PAD ASSIGNMENT

The ONET8511T is available in die form. The locations of the bond pads are shown in Figure 2.



M0094-01

Figure 2. ONET8511T Bond Pad Assignment

## TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
FILTER	5, 7	Analog	Bias voltage for photodiode cathode. These pads are internally connected to an 220 $\Omega$ resistor to $V_{CC}$ and a filter capacitor to ground (GND).
GND	4, 8, 10, 12, 13, 14, 15, 16, 17, 18	Supply	Circuit ground. All GND pads are connected on die. Bonding all pads is optional; however for optimum performance a good ground connection is mandatory.
IN	6	Analog input	Data input to TIA (photodiode anode).
OUT+	1	Analog output	Non-inverted CML data output. On-chip 50 $\Omega$ back-terminated to $V_{CC}$ .
OUT-	11	Analog output	Inverted CML data output. On-chip 50 $\Omega$ back-terminated to $V_{CC}$ .
RSSI	9	Analog output	Analog output current proportional to the input data amplitude. Indicates the strength of the received signal (RSSI). Must be sunk through an external resistor to ground (GND). The RSSI gain can be adjusted by choosing the external resistor; however, for proper operation, ensure that the voltage at the RSSI pad does not exceed $V_{CC}-0.65V$ . If the RSSI feature is not used, this pad must be bonded to ground (GND) for proper operation.
VCC_IN	3	Supply	2.95 V to 3.6 V supply voltage for input TIA stage.
VCC_OUT	2	Supply	2.95 V to 3.6 V supply voltage for the AGC amplifier.

### ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

PARAMETER		VALUE	UNIT
V <sub>CC_IN</sub> , V <sub>CC_OUT</sub>	Supply voltage <sup>(2)</sup>	–0.3 to 4.0	V
V <sub>FILTER</sub> , V <sub>OUT+</sub> , V <sub>OUT–</sub> , V <sub>RSSI</sub>	Voltage at FILTER1, FILTER2, OUT+, OUT–, RSSI <sup>(2)</sup>	–0.3 to 4.0	V
I <sub>IN</sub>	Current into IN	–0.7 to 3.5	mA
I <sub>FILTER</sub>	Current into FILTER1, FILTER2	–8 to 8	mA
I <sub>OUT+</sub> , I <sub>OUT–</sub>	Continuous current at outputs	–8 to 8	mA
ESD	ESD rating at all pins except input IN <sup>(3)</sup>	2	kV (HBM) <sup>(4)</sup>
	ESD rating at IN	0.5	
T <sub>J,max</sub>	Maximum junction temperature	125	°C
T <sub>STG</sub>	Storage temperature range	–65 to 150	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to network ground terminal.
- (3) For optimum high-frequency performance, the input pin has reduced ESD protection.
- (4) Human Body Model

### RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.95	3.3	3.6	V
T <sub>A</sub>	Operating backside die temperature	–25		100 <sup>(1)</sup>	°C
L <sub>FILTER</sub> , L <sub>IN</sub>	Wire-bond inductor at pins FILTER and IN		0.4	0.6	nH
C <sub>PD</sub>	Photodiode Capacitance		0.2		pF

- (1) 105°C junction temperature

### DC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted). Typical values are at V<sub>CC</sub> = 3.3 V and T<sub>A</sub> = 25°C.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2.95	3.3	3.6	V
I <sub>VCC</sub>	Supply current		46	70 <sup>(1)</sup>	mA
V <sub>IN</sub>	Input bias voltage		0.85	1.05	V
R <sub>OUT</sub>	Output resistance	45	50	65	Ω
R <sub>FILTER</sub>	Photodiode filter resistance		220		Ω

- (1) Includes RSSI current

## AC ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted). Typical values are at  $V_{CC} = 3.3\text{ V}$  and  $T_A = 25^\circ\text{C}$ .

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$Z_{21}$	Small signal transimpedance	Differential output; Input current $I_{IN} = 20\ \mu\text{A}_{p-p}$	3.5	5.5	8	$\text{k}\Omega$
$f_{\text{HSS},3\text{dB}}$	Small signal bandwidth	$I_{IN} = 100\ \mu\text{A}_{p-p}$ with AGC on <sup>(1)</sup>		8		GHz
$f_{\text{L},3\text{dB}}$	Low frequency –3 dB bandwidth	$I_{IN} = 100\ \mu\text{A}_{p-p}$		30	50	kHz
THD	Linear operation	100 MHz signal, 3.5 dB extinction ratio, $I_{IN} \leq 1400\ \mu\text{A}_{p-p}$		5	10	%
$\tau_{\text{AGC}}$	AGC settling time	$I_{IN} = 500\ \mu\text{A}_{p-p}$ , 3.5dB extinction ratio	7	14		$\mu\text{s}$
$I_{N,IN}$	Input referred RMS noise	unfiltered <sup>(2)</sup>		1.0	2.2	$\mu\text{A}$
	Input referred noise density	10 GHz bandwidth		10		$\text{pA}/\sqrt{\text{Hz}}$
DJ	Deterministic jitter	$I_{IN} < 1400\ \mu\text{A}_{p-p}$ (K28.5 pattern)		8	18	$\text{ps}_{p-p}$
PSNR	Power supply noise rejection <sup>(3)</sup>	$1 < f < 10\ \text{MHz}$		25		dB
$A_{\text{RSSI}}$	RSSI gain	Resistive load to GND <sup>(4)</sup>	0.95	1	1.05	A/A
	RSSI output offset current (no light)			22	32	$\mu\text{A}$
$f_{\text{H},3\text{dB},\text{RSSI}}$	RSSI bandwidth			2		MHz
$V_{\text{OUTD},\text{MAX}}$	Maximum differential output voltage	Input current $I_{IN} = 100\ \mu\text{A}_{p-p}$ , 3.5 dB extinction ratio	200	250		$\text{mV}_{p-p}$
		Input current $I_{IN} = 1400\ \mu\text{A}_{p-p}$ , 3.5 dB extinction ratio	200	270		

- (1) The small signal bandwidth is specified over process corners, temperature, and supply voltage variation. The assumed photodiode capacitance is 0.2 pF and the bond-wire inductance is 0.4 nH. The small signal bandwidth strongly depends on environmental parasitics. Careful attention to layout parasitics and external components is necessary to achieve optimal performance.
- (2) Input referred RMS noise = (RMS output noise) ÷ (gain at 100 MHz). The input referred noise is specified over process corners, temperature, and supply voltage variation.
- (3) PSNR is the differential output amplitude divided by the voltage ripple on supply; no input current at IN.
- (4) The RSSI output is a current output, which requires a resistive load to ground (GND). The voltage gain can be adjusted for the intended application by choosing the external resistor; however, for proper operation, ensure that the voltage at RSSI does not exceed  $V_{CC} - 0.65\text{ V}$ .

## DETAILED DESCRIPTION

### SIGNAL PATH

The first stage of the signal path is a transimpedance amplifier which converts the photodiode current into a voltage signal with a linear relationship. If the input signal current exceeds a certain value, the transimpedance gain is reduced by means of an AGC circuit to keep the transmit behavior linear.

The second stage is an AGC voltage amplifier that provides additional linear gain and converts the single ended input voltage into a differential data signal.

The third stage is the output buffer which provides CML outputs with an on-chip 50 $\Omega$  back-termination to  $V_{CC}$ .

### FILTER CIRCUITRY

The FILTER pins provide a filtered VCC for the photodiode bias. The on-chip low pass filter for the photodiode is implemented using a filter resistor of 220  $\Omega$  and a capacitor. The corresponding corner frequency is below 5 MHz. The supply voltages for the transimpedance amplifier are filtered by means of on-chip capacitors, thus avoiding the need for an external supply filter capacitor. The input stage has a separate VCC supply ( $V_{CC\_IN}$ ) that is not connected on the chip to the supply of the AGC/CML stages ( $V_{CC\_OUT}$ ).

### AGC AND RSSI

The voltage drop across the internal photodiode supply-filter resistor is monitored by the bias and RSSI control circuit block.

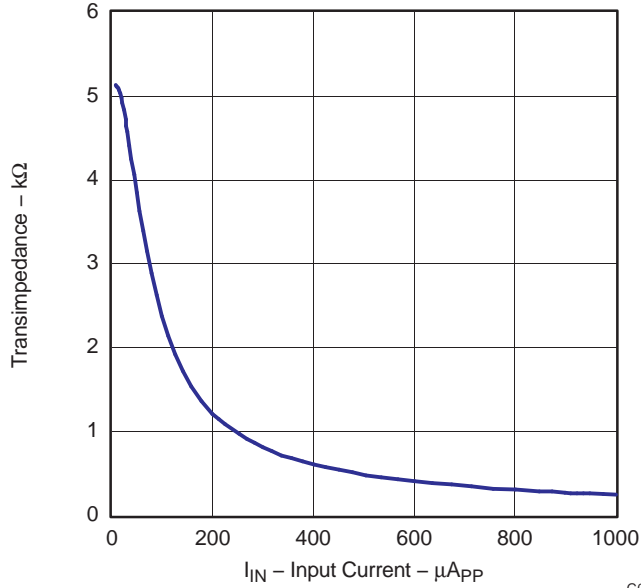
If the DC input current exceeds a specified level then it is partially cancelled by means of a controlled current source. This keeps the transimpedance amplifier stage within sufficient operating limits for optimum performance. The automatic gain control circuitry adjusts the voltage gain of the AGC amplifier to ensure linear behavior of the complete amplifier.

Finally, this circuit block senses the current through the filter resistor and generates a mirrored current that is proportional to the input signal strength. The mirrored current is available at the RSSI output and *must* be sunk to ground (GND) using an external resistor. For proper operation, ensure that the voltage at the RSSI pad does not exceed  $V_{CC}-0.65$  V.

**TYPICAL CHARACTERISTICS**

Typical operating condition is at  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$  (unless otherwise noted).

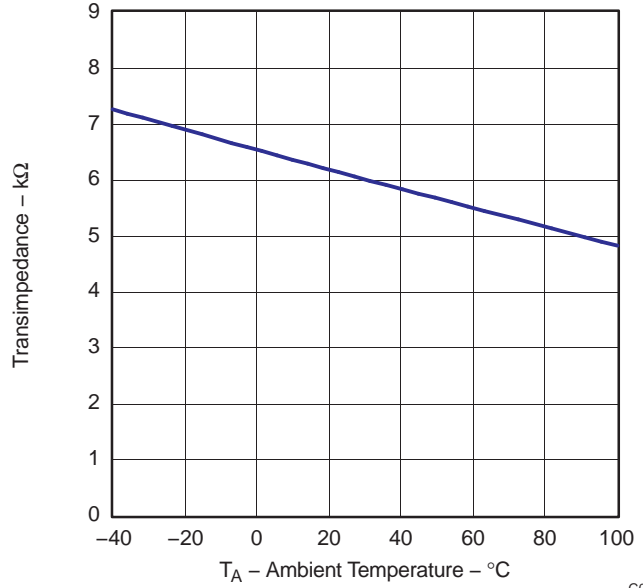
**TRANSMIMPEDANCE  
vs  
INPUT CURRENT**



**Figure 3.**

G001

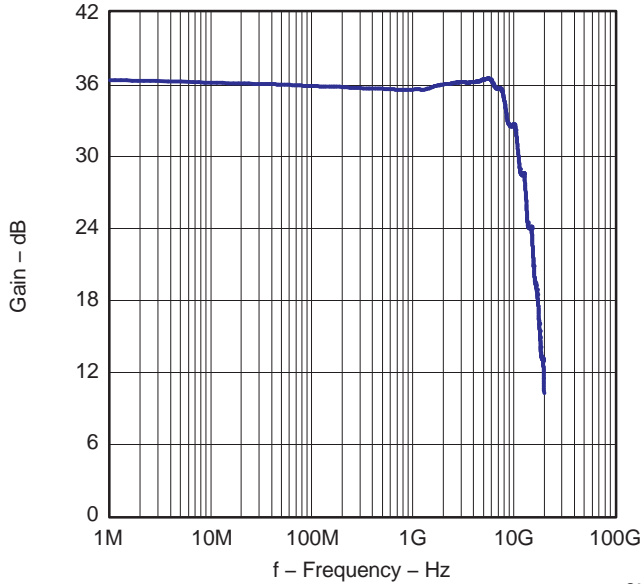
**SMALL SIGNAL TRANSMIMPEDANCE  
vs  
AMBIENT TEMPERATURE**



**Figure 4.**

G002

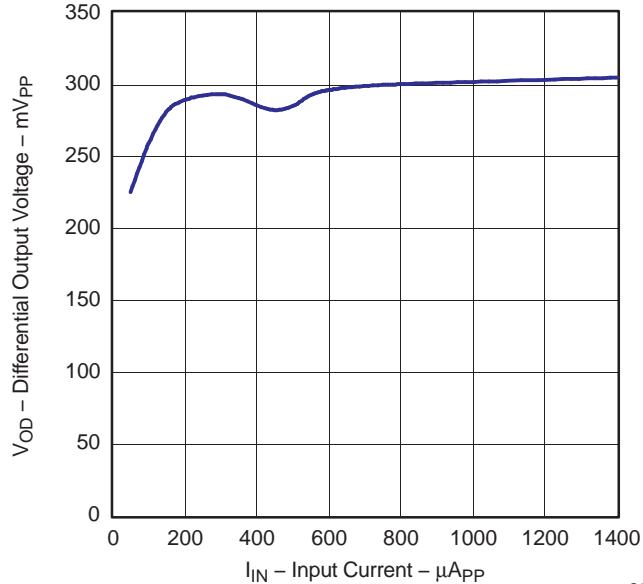
**SMALL SIGNAL TRANSFER  
CHARACTERISTICS**



**Figure 5.**

G003

**OUTPUT VOLTAGE  
vs  
INPUT CURRENT (644 MHz Signal, 3.5 dB ER)**



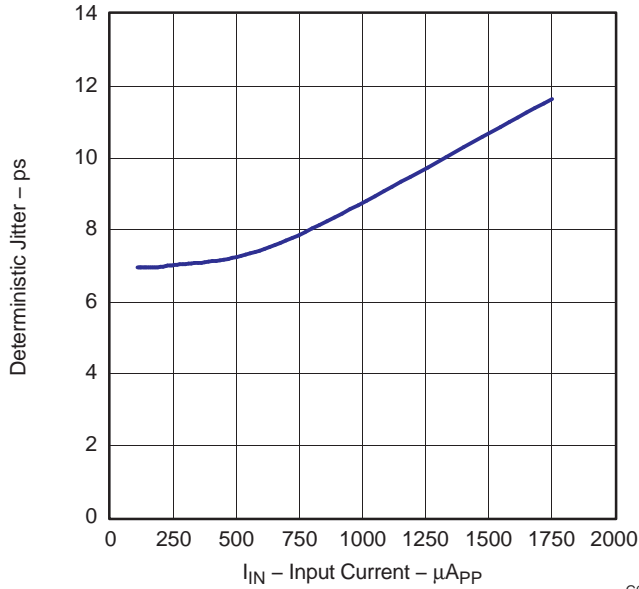
**Figure 6.**

G004

**TYPICAL CHARACTERISTICS (continued)**

Typical operating condition is at  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$  (unless otherwise noted).

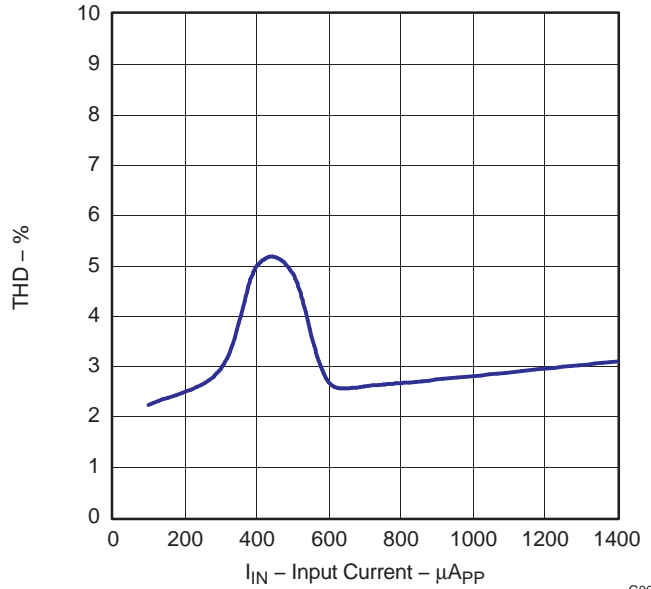
**DETERMINISTIC JITTER  
vs  
INPUT CURRENT**



**Figure 7.**

G005

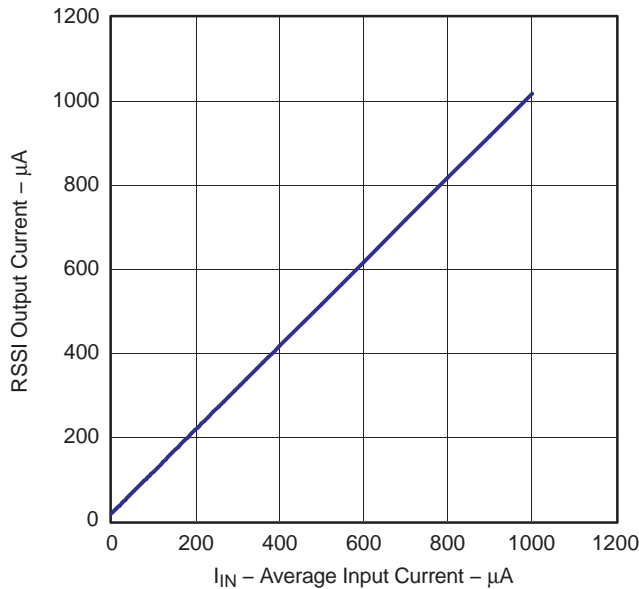
**TOTAL HARMONIC DISTORTION  
vs  
INPUT CURRENT (100 MHz Signal, 3.5 dB ER)**



**Figure 8.**

G006

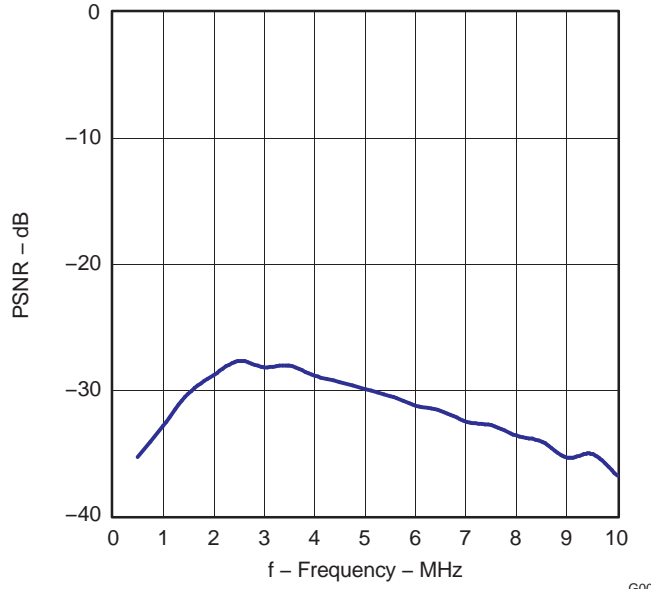
**RSSI OUTPUT CURRENT  
vs  
AVERAGE INPUT CURRENT**



**Figure 9.**

G007

**POWER SUPPLY NOISE REJECTION  
vs  
FREQUENCY**



**Figure 10.**

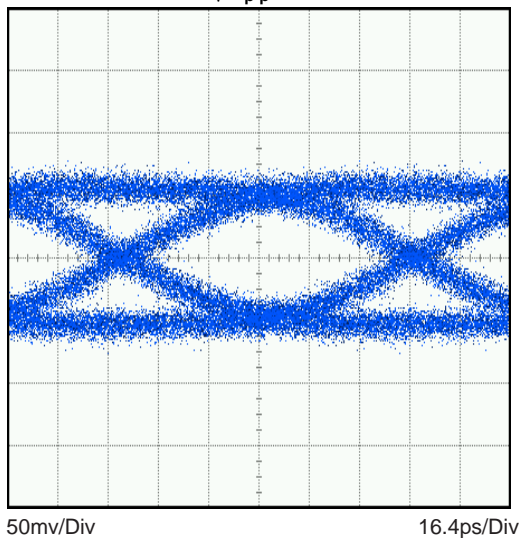
G008



**TYPICAL CHARACTERISTICS (continued)**

Typical operating condition is at  $V_{CC} = +3.3V$  and  $T_A = +25^\circ C$  (unless otherwise noted).

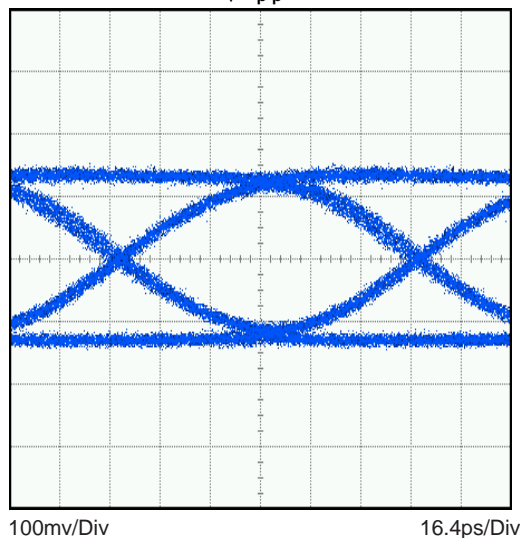
**OUTPUT EYE-DIAGRAM AT 10.3 GBPS  
AND 20  $\mu A_{p-p}$  INPUT CURRENT**



G009

**Figure 11.**

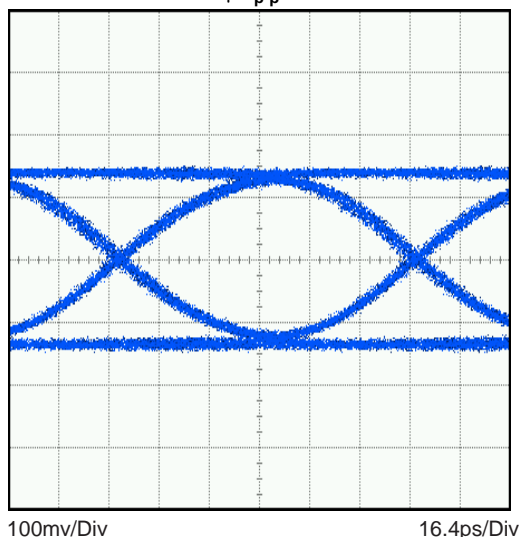
**OUTPUT EYE-DIAGRAM AT 10.3 GBPS  
AND 100  $\mu A_{p-p}$  INPUT CURRENT**



G010

**Figure 12.**

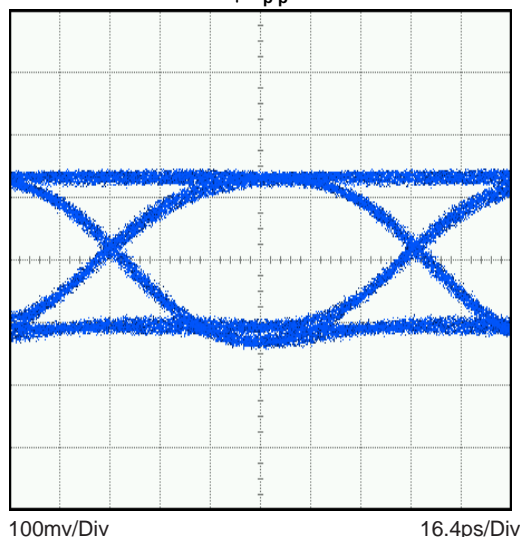
**OUTPUT EYE-DIAGRAM AT 10.3 GBPS  
AND 500  $\mu A_{p-p}$  INPUT CURRENT**



G011

**Figure 13.**

**OUTPUT EYE-DIAGRAM AT 10.3 GBPS  
AND 2000  $\mu A_{p-p}$  INPUT CURRENT**



G012

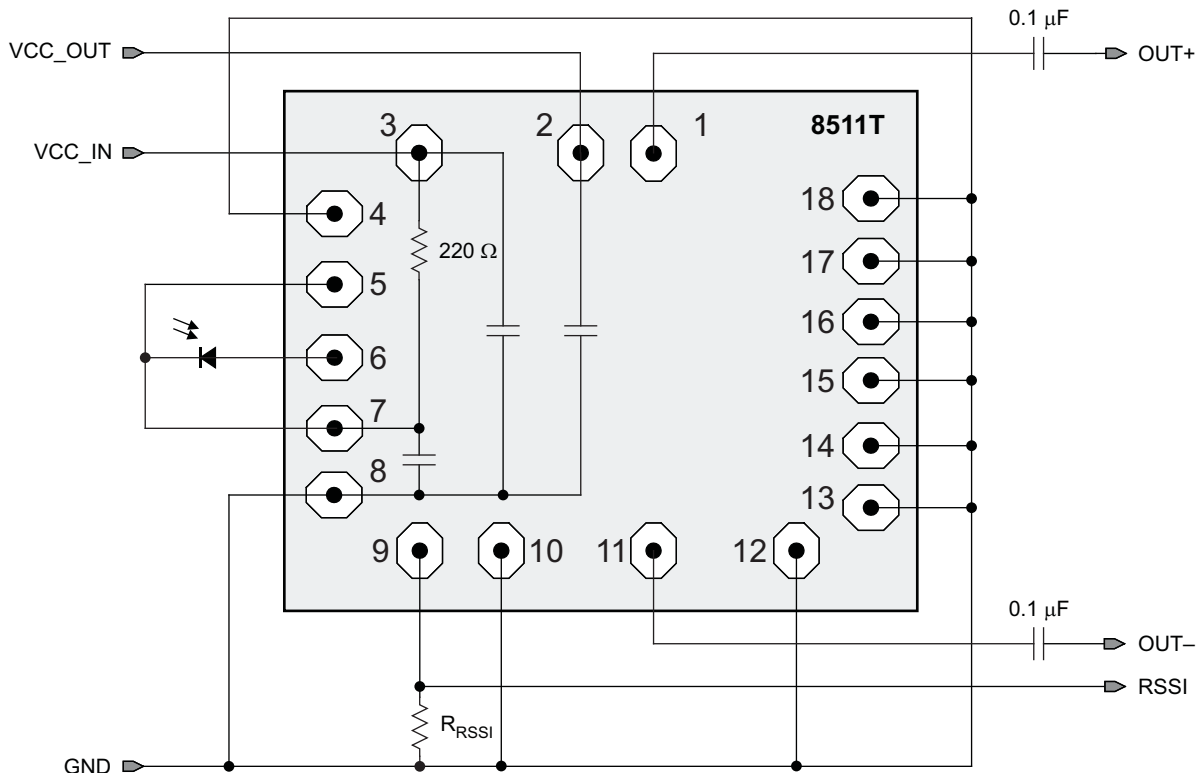
**Figure 14.**

## APPLICATION INFORMATION

Figure 15 shows the ONET8511T being used in a typical fiber optic receiver circuit using the internal photodiode bias. The ONET8511T converts the electrical current generated by the PIN photodiode into a differential output voltage. The FILTER inputs provide a DC bias voltage for the PIN that is low pass filtered by the combination of an internal  $220\ \Omega$  resistor and a capacitor. Because the voltage drop across the  $220\ \Omega$  resistor is sensed and used by the bias circuit, the photodiode must be connected to the FILTER pads for the AGC to function correctly.

The RSSI output is used to mirror the photodiode output current and *must* be connected using a resistor to GND. The voltage gain can be adjusted for the intended application by choosing the external resistor; however, for proper operation of the ONET8511T, ensure that the voltage at RSSI never exceeds  $V_{CC}-0.65\ \text{V}$ . The RSSI output must be grounded if it is unused.

The OUT+ and OUT– pins are internally terminated by  $50\ \Omega$  pull-up resistors to VCC. The outputs must be AC coupled, for example by using  $0.1\ \mu\text{F}$  capacitors, to the succeeding device.



S0332-01

Figure 15. Basic Application Circuit

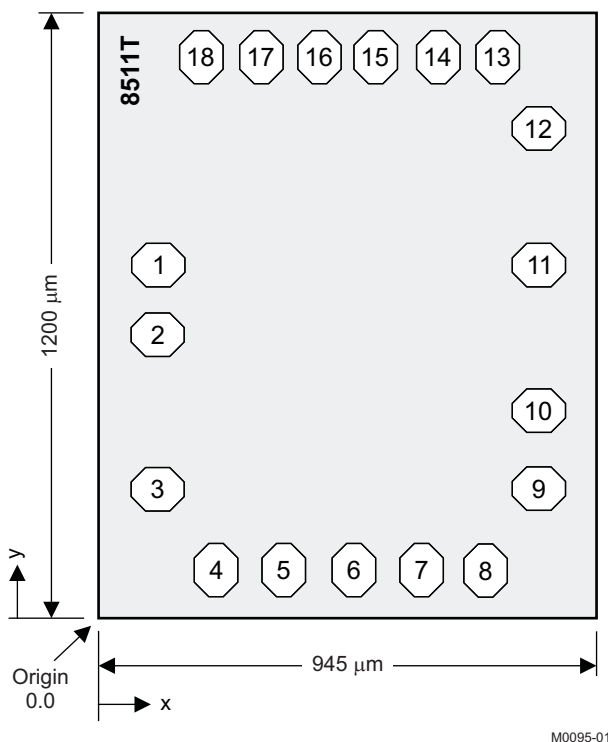
## ASSEMBLY RECOMMENDATIONS

You need to concentrate on assembly parasitics and external components to achieve optimal performance.

Recommendations that optimize performance include:

1. Minimize the total capacitance on the IN pad by using a low capacitance photodiode and compensating for stray capacitances. Place the photodiode close to the ONET8511T die in order to minimize the bond wire length and associated parasitic inductance.
2. Use identical termination and symmetrical transmission lines at the AC coupled differential output pins OUT+ and OUT–.
3. Use short bond wire connections for the supply terminals VCC\_IN, VCC\_OUT and GND. Supply voltage filtering is provided on chip but filtering may be improved by using an additional external capacitor.

## CHIP DIMENSIONS AND PAD LOCATIONS



**Die Thickness: 203 μm**

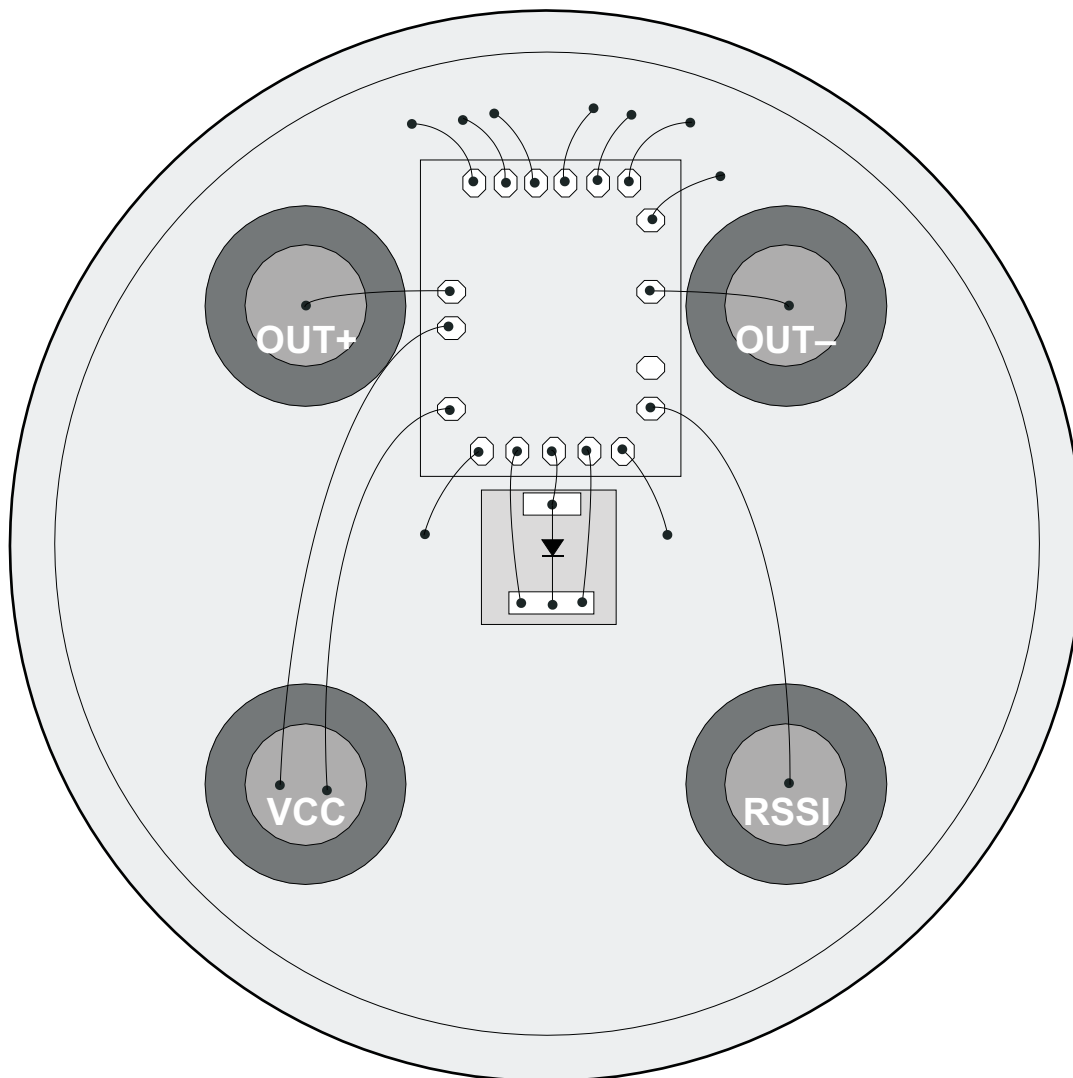
**Pad Dimensions: 105 × 65 μm**

### Bond Pad Locations and Descriptions

PAD	COORDINATES		SYMBOL	TYPE	DESCRIPTION
	x (μm)	y (μm)			
1	116	718	OUT+	Analog output	Non-inverted data output
2	116	575	VCC_OUT	Supply	3.3 V supply voltage
3	116	289	VCC_IN	Supply	3.3 V supply voltage
4	243	136	GND	Supply	Circuit ground
5	358	136	FILTER1	Analog	Bias voltage for photodiode
6	473	136	IN	Analog input	Data input to TIA
7	588	136	FILTER2	Analog	Bias voltage for photodiode
8	703	136	GND	Supply	Circuit ground
9	828	289	RSSI	Analog output	RSSI output signal
10	828	474	GND	Supply	RSSI output signal for externally biased receivers
11	828	718	OUT-	Analog output	Inverted data output
12	828	910	GND	Supply	Circuit ground
13	760	1063	GND	Supply	Circuit ground
14	645	1063	GND	Supply	Circuit ground
15	530	1063	GND	Supply	Circuit ground
16	415	1063	GND	Supply	Circuit ground
17	300	1063	GND	Supply	Circuit ground
18	185	1063	GND	Supply	Circuit ground

**TO46 LAYOUT EXAMPLE**

An example for a layout (top view) in a 5-pin TO46 can is shown in [Figure 16](#).



M0096-01

**Figure 16. TO46 5-Pin Layout Using the ONET8511T**

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
ONET8511TY	ACTIVE	DIESALE	Y	0	360	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

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**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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