Boundary Devices

Nit8M_Mini_SOM
PRODUCT MANUAL

REVISION HISTORY

DATE	REVISION	DESCRIPTION	APPROVAL
10/29/2019	0.1	First Draft	KG
3/31/2020	0.2	Added SDIO Note. Added Product Link for BD_DSIHD	KG
6/13/2020	0.3	Added SODIMM Mating Part Number Link	KG
11/10/2022	0.4	Added MTBF and storage information	GB

TABLE OF CONTENTS

TABLE OF CONTENTS

1. OVERVIEW

1.1. GENERAL INFORMATION

The Nitrogen8 family of SBCs and SOMs are the latest in Boundary Device's i.MX based embedded computing solutions.

The different Nitrogen8 series of SBCs and SOMs include offerings designed to best leverage the advantages of the i.MX 8M applications processors to fit a variety of embedded and IoT applications including: consumer/ industrial automation, aviation & aerospace, HMI, industrial control, robotics, building control, digital displays, infotainment, telematics, and more.

The Nitrogen8M_Mini SOM is designed for mass production use with a guaranteed 10-year life span, FCC Pre-scan results, and a stable supply chain. Industrial temperature and conformal coating options are available. It can also include from 2GB up to 4GB of LPDDR4 RAM.

Software Support:

Industry leading OS-Level support can be found on the Boundary Devices website via the Blog (https://boundarydevices.com/blog) and Wiki (https://boundarydevices.com/wiki). You can also find images for the latest versions of popular OS supported by the Nitrogen platforms including: Yocto, Buildroot, Ubuntu, Debian, Android, and FreeRTOS.

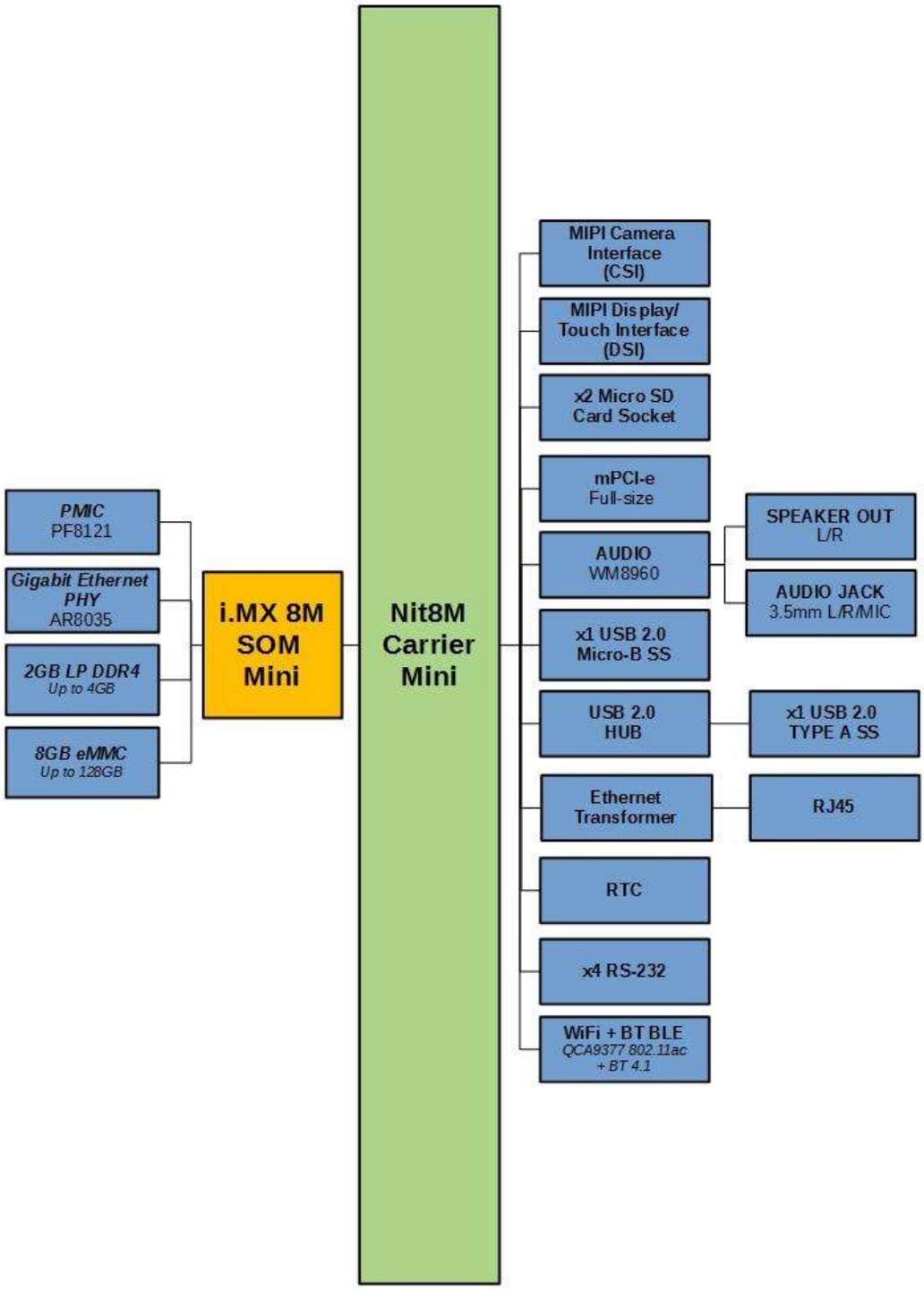
Visit: https://wiki.boundarydevices.com/index.php/Nitrogen8M_Mini_SOM/
Boundary Devices does not provide application development, but does have large list of software partners who can. You can browse our partners at https://boundarydevices.com/support

Email: info@boundarydevices.com to discuss all build options.

1.2. FEATURE SUMMARY

- Quad-Core ARM® Cortex-A53 processor at 1.6GHz
- General purpose Cortex M-4 400Mhz core processor for low-power processing
- 2GB of LPDDR4. Expandable to 4GB LPDDR4
- 16GB eMMC – Expandable to 128GB
- One MIPI DSI Display Port (4-lane up to 1080p60 via carrier board)
- One MIPI CSI Camera Interface (4-lane MIPI CSI via carrier board)
- HD Video Engine
- SDIO Interface (via carrier board)
- PCIe (via carrier board)
- 10/100/GB Ethernet (via carrier board)
- 2 High speed USB ports (1x Host, 1x OTG via carrier board)
- I2C (x3 via carrier board)
- General Purpose I/O for Device Control
- Industrial Temperature versions available
- Small Size (69.6mm x 40mm)

1.3. BLOCK DIAGRAM

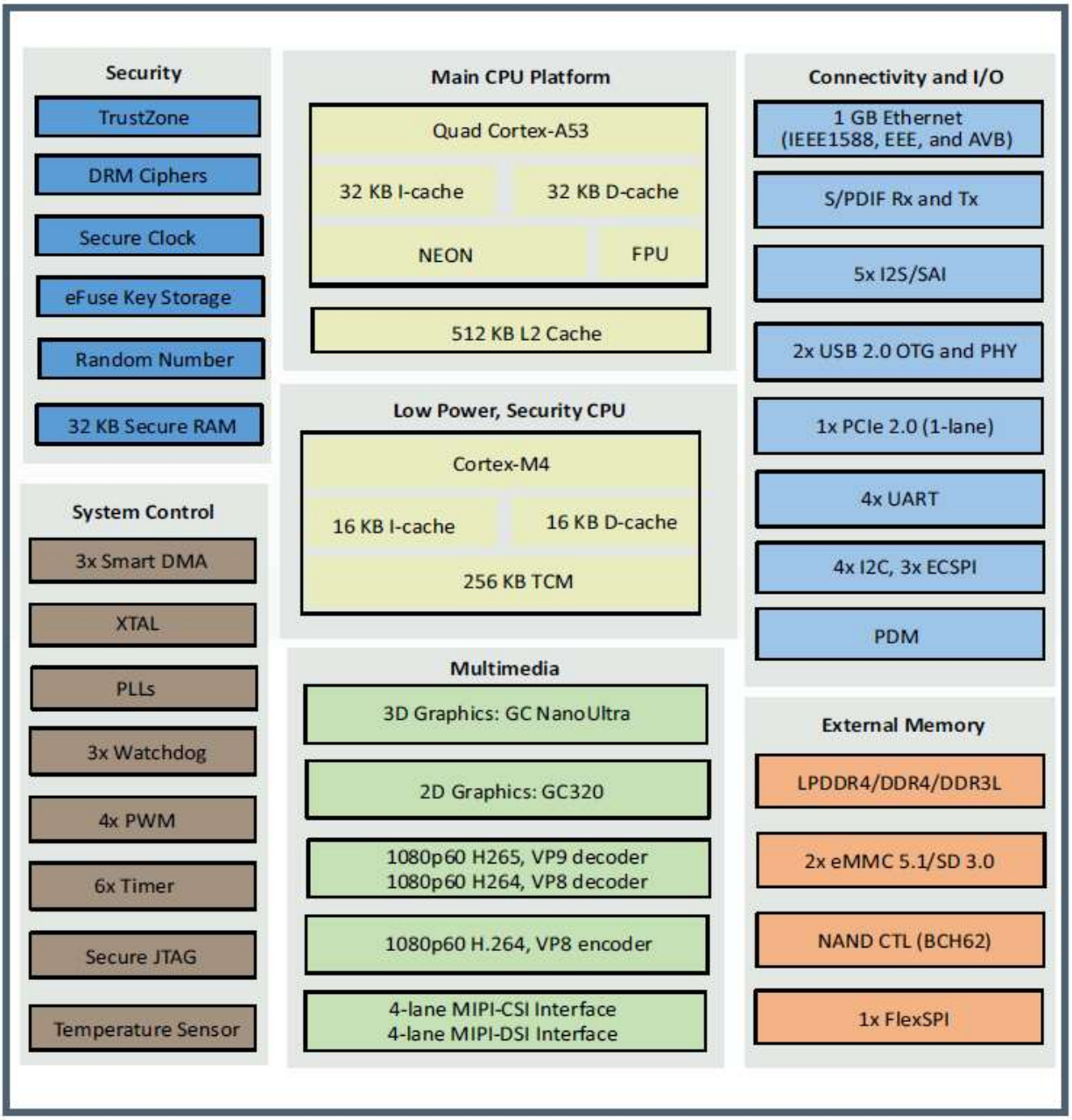


1.4. NXP I.MX 8M MINI PROCESSOR

1.4.1. OVERVIEW

The i.MX 8M Mini family of processors features advanced implementation of a quad Arm® Cortex®-A53 core, which operates at speeds of up to 1.6 GHz. A general purpose Cortex®-M4 400 MHz core processor is for low-power processing. The DRAM controller supports 32-bit/16-bit LPDDR4, DDR4, and DDR3L memory. A wide range of audio interfaces are available, including I2S, AC97, TDM, and S/PDIF. There are a number of other interfaces for connecting peripherals, such as USB, PCIe, and Ethernet.

1.4.2. I.MX 8M MINI BLOCK DIAGRAM



1.4.3. CPU

The i.MX 8M Mini applications processor represents NXP's latest video and audio experience combining state-of-the-art media-specific features with high-performance processing while optimized for lowest power consumption:

- Arm Cortex-A53 MPCore platform
- Quad symmetric Cortex-A53 processors :
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - Media Processing Engine (MPE) with NEON technology supporting the Advanced Single Instruction Multiple Data architecture:
  - Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
  - Support of 64-bit Armv8-A architecture
  - 512 KB unified L2 cache

- Arm Cortex-M4 core platform
  - 16 KB L1 Instruction Cache
  - 16 KB L1 Data Cache
  - 256 KB tightly coupled memory (TCM)

- Low power microcontroller available for customer application
  - low power microcontroller available for customer application
  - low power standby mode
  - IoT features including Weave
  - Manage IR or Wireless Remote

1.4.4. MEMORY

The on-chip memory system consists of the following:

- Boot ROM (256KB)
- On-chip RAM (256KB + 32KB)

The external memory interfaces supported on this chip include:

- 16/32-bit DRAM Interface:
  - LPDDR4-3000
- eMMC 5.0 FLASH
- SPI NOR FLASH

The i.MX 8M Mini supports the following boot devices:

- SDIO / MMC / SDXC
- eSD 3.0/eMMC 5.0 (fast boot)
- USB
- QSPI Ethernet (via plug-in mode)

1.4.5. DISPLAY

The i.MX8 video graphics subsystem consists of the following dedicated modules:

- High Performance Video Processing Unit (VPU)
- Three Graphics Processing Units (GPUs):
  - 3D GPU: accelerating the generation of 3D graphics (OpenGL/ES) and vector graphics (OpenVG)
  - 2D GPU: acceleration the generation of 2D graphics (BitBLT).
  - OpenVG: acceleration of vector graphics (OpenVG).

The chip has the following display support:

LCDIF Display Controller:

- Supports up to 2 layers of overlay
- Support up to 1080p60 display through MIPI DSI

MIPI Interface:

- 4-lane MIPI CSI interface
- 4-lane MIPI DSI interface

CSI Interface:

- CSI is a simple camera interface which is used to capture the MIPI CSI input and save the pixels into memory

1.4.6. GRAPHICS PROCESSING UNIT

The chip incorporates the following Graphics Processing Unit (GPU) features:

- 2D/3D acceleration
- Target frequency of 800 MHz
- Support OpenGL ES 1.1, 2.0, OpenVG 1.1
- TrustZone support using a local MMU to manage secure regions
- Support multi-source composition
- Support one-pass filter
- Support tile format

1.4.7. VIDEO PROCESSING UNIT

The chip incorporates the following Video Processing Unit (VPU) features:

- 1080p60 VP9 Profile 0, 2 (10 bit) Decoder (Hantro G2)
- 1080p60 HEVC/H.265 Decoder (Hantro G2)
- 1080p60 AVC/H.264 Baseline, Main, High Decoder (Hantro G1)
- 1080p60 VP8 Decoder (Hantro G1)
- 1080p60 AVC/H.264 Encoder (Hantro H1)
- 1080p60 VP8 Encoder (Hantro H1)
- TrustZone support

2. CONNECTOR DETAILS

The Nit8M_Mini_SOM exposes a 260 pin SODIMM mechanical standardinterface. The recommended mating connector for baseboard interfacing is: Tyco Electronics - TE 2309407-1

2.1. CUSTOM CONNECTORS

260 Pin SODIMM Edge Connector to Carrier Board Interface Mating Connector P/N: TE 2309407-1				
PIN#	**SOM Signal**	**SOM Voltage Domain**	**Voltage Level**	**Comments**
1	+5V	-	5V Power	
2	+5V	-	5V Power	
3	+5V	-	5V Power	
4	+5V	-	5V Power	
5	+5V	-	5V Power	
6	+5V	-	5V Power	
7	+5V	-	5V Power	
8	+5V	-	5V Power	
9	GND	-	Ground	
10	GND	-	Ground	
11	GND	-	Ground	
12	GND	-	Ground	
13	GND	-	Ground	
14	GND	-	Ground	
15	GND	-	Ground	
16	GND	-	Ground	
17	GND	-	Ground	
18	GND	-	Ground	
19	LDO3_1P8V_TO_3P3V		Power Output	DEFAULT 1.8V FOR CUSTOMER USE 350 MA MAX
20	GND	-	Ground	
21	LDO3_1P8V_TO_3P3V		Power Output	DEFAULT 1.8V FOR CUSTOMER USE 350 MA MAX
22	VDD_LICELL		3V Battery	
23	RGMII_ACT		Ethernet	
24	SAI1_RXFS	NVCC_SAI1	3.3V	
25	RGMII_LINK		Ethernet	
26	SAI1_RXC	NVCC_SAI1	3.3V	
27	GND	-	Ground	
28	SAI1_RXD0	NVCC_SAI1	3.3V	
29	TRX3_N		Ethernet	
30	SAI1_RXD1	NVCC_SAI1	3.3V	
31	TRX3_P		Ethernet	
32	SAI1_RXD2	NVCC_SAI1	3.3V	

33	GND	-	Ground	
34	SAI1_RXD3	NVCC_SAI1	3.3V	
35	TRX2_N		Ethernet	
36	SAI1_RXD4	NVCC_SAI1	3.3V	
37	TRX2_P		Ethernet	
38	SAI1_RXD5	NVCC_SAI1	3.3V	
39	GND	-	Ground	
40	SAI1_RXD6	NVCC_SAI1	3.3V	
41	TRX1_N		Ethernet	
42	SAI1_RXD7	NVCC_SAI1	3.3V	
43	TRX1_P		Ethernet	
44	GND	-	Ground	
45	GND	-	Ground	
46	SAI1_MCLK	NVCC_SAI1	3.3V	
47	TRX0_N		Ethernet	
48	GND	-	Ground	
49	TRX0_P		Ethernet	
50	SAI1_TXFS	NVCC_SAI1	3.3V	
51	GND	-	Ground	
52	SAI1_TXC	NVCC_SAI1	3.3V	
53	CLKOUT2	NVCC_CLK	1.8V	
54	SAI1_TXD0	NVCC_SAI1	3.3V	
55	CLKIN2	NVCC_CLK	1.8V	
56	SAI1_TXD1	NVCC_SAI1	3.3V	
57	GND	-	Ground	
58	SAI1_TXD2	NVCC_SAI1	3.3V	
59	CLKOUT1	NVCC_CLK	1.8V	
60	SAI1_TXD3	NVCC_SAI1	3.3V	
61	CLKIN1	NVCC_CLK	1.8V	
62	SAI1_TXD4	NVCC_SAI1	3.3V	
63	GND	-	Ground	
64	SAI1_TXD5	NVCC_SAI1	3.3V	
65	JTAG_TMS	NVCC_JTAG	3.3V	
66	SAI1_TXD6	NVCC_SAI1	3.3V	
67	JTAG_TCK	NVCC_JTAG	3.3V	
68	SAI1_TXD7	NVCC_SAI1	3.3V	
69	JTAG_TDI	NVCC_JTAG	3.3V	
70	GND	-	Ground	
71	JTAG_TDO	NVCC_JTAG	3.3V	
72	WIFI_RESET	NVCC_SD1	1.8V	
73	JTAG_MOD	NVCC_JTAG	3.3V	
74	WL_WAKE_HOST	NVCC_SAI2	3.3V	
75	JTAG_NTRST	NVCC_JTAG	3.3V	
76	SAI5_RXC	NVCC_SAI5	3.3V	

77	GND	-	Ground	
78	SD3_DATA3	NVCC_NAND	3.3V	
79	SD2_RESET_B	NVCC_SD2	1.8V/3.3V	CUSTOMER DRIVEN 1.8V OR 3.3V
80	SD3_DATA2	NVCC_NAND	3.3V	
81	SD2_CD	NVCC_SD2	1.8V/3.3V	CUSTOMER DRIVEN 1.8V OR 3.3V
82	SD3_DATA1	NVCC_NAND	3.3V	
83	SD2_DATA0	NVCC_SD2	1.8V/3.3V	CUSTOMER DRIVEN 1.8V OR 3.3V
84	SD3_DATA0	NVCC_NAND	3.3V	
85	SD2_DATA1	NVCC_SD2	1.8V/3.3V	CUSTOMER DRIVEN 1.8V OR 3.3V
86	SD3_CMD	NVCC_NAND	3.3V	
87	SD2_DATA2	NVCC_SD2	1.8V/3.3V	CUSTOMER DRIVEN 1.8V OR 3.3V
88	GND	-	Ground	
89	SD2_DATA3	NVCC_SD2	1.8V/3.3V	CUSTOMER DRIVEN 1.8V OR 3.3V
90	SD3_CLK	NVCC_NAND	3.3V	
91	SD2_CMD	NVCC_SD2	1.8V/3.3V	CUSTOMER DRIVEN 1.8V OR 3.3V
92	GND	-	Ground	
93	GND	-	Ground	
94	SAI2_TXFS	NVCC_SAI2	3.3V	
95	SD2_CLK	NVCC_SD2	1.8V/3.3V	CUSTOMER DRIVEN 1.8V OR 3.3V
96	UART1_TXD	NVCC_UART	3.3V	
97	GND	-	Ground	
98	UART1_RTS	NVCC_UART	3.3V	
99	USB_OTG2_PWR	NVCC_GPIO1	3.3V	
100	UART1_RXD	NVCC_UART	3.3V	
101	CAMERA_CLK	NVCC_GPIO1	3.3V	
102	SAI2_TXC	NVCC_SAI2	3.3V	
103	USB_OTG2_VBUS	USB POWER	5V	
104	SAI2_RXD0	NVCC_SAI2	3.3V	
105	GND	-	Ground	
106	UART1_CTS	NVCC_UART	3.3V	
107	USB_OTG2_D_P	USB_OTG2	3.3V	
108	SAI2_TXD	NVCC_SAI2	3.3V	
109	USB_OTG2_D_N	USB_OTG2	3.3V	
110	CLK_REQ_O	NVCC_SAI3	3.3V	
111	GND	-	Ground	
112	BT_WAKE_DEV	NVCC_SAI2	3.3V	
113	USB_OTG1_PWR	NVCC_GPIO1	3.3V	
114	SLOW_CLK	NVCC_GPIO1	3.3V	
115	USB_OTG1_OC	NVCC_GPIO1	3.3V	

116	BT_REG_ON	NVCC_NAND	3.3V	
117	USB_OTG1_ID	USB_OTG1	1.8V	
118	SAI2_RXC	NVCC_SAI2	3.3V	
119	GND	-	Ground	
120	GND	-	Ground	
121	USB_OTG1_D_P	USB_OTG1	3.3V	
122	PCIE_RST_B	NVCC_SAI3	3.3V	
123	USB_OTG1_D_N	USB_OTG1	3.3V	
124	PCIE_DIS_B	NVCC_GPIO1	3.3V	
125	GND	-	Ground	
126	GND	-	Ground	
127	USB_OTG1_VBUS	USB_OTG1	5V	
128	PCIE_TX_P	VDD_PCI_1P8	PCIE	
129	QSPIA_NSS0	NVCC_NAND	3.3V	
130	PCIE_TX_N	VDD_PCI_1P8	PCIE	
131	QSPIA_DATA0	NVCC_NAND	3.3V	
132	GND	-	Ground	
133	QSPIA_DATA1	NVCC_NAND	3.3V	
134	PCIE_RX_P	VDD_PCI_1P8	PCIE	
135	QSPIA_DATA2	NVCC_NAND	3.3V	
136	PCIE_RX_N	VDD_PCI_1P8	PCIE	
137	QSPIA_DATA3	NVCC_NAND	3.3V	
138	GND	-	Ground	
139	GND	-	Ground	
140	PCIE_REFCLK_P	VDD_PCI_1P8	PCIE	
141	QSPIA_SCLK	NVCC_NAND	3.3V	
142	PCIE_REFCLK_N	VDD_PCI_1P8	PCIE	
143	GND	-	Ground	
144	GND	-	Ground	
145	GND	-	Ground	
146	GND	-	Ground	
147	TP18	-	-	
148	CSI_D0_N	VDD_MIPI_1P8	MIPI 1.8V	
149	UART4_RXD	NVCC_UART	3.3V	
150	CSI_D0_P	VDD_MIPI_1P8	MIPI 1.8V	
151	UART4_TXD	NVCC_UART	3.3V	
152	GND	-	Ground	
153	GND	-	Ground	
154	CSI_D1_N	VDD_MIPI_1P8	MIPI 1.8V	
155	GND	-	Ground	
156	CSI_D1_P	VDD_MIPI_1P8	MIPI 1.8V	
157	GND	-	Ground	
158	GND	-	Ground	
159	GND	-	Ground	

160	CSI_D2_N	VDD_MIPI_1P8	MIPI 1.8V	
161	GND	-	Ground	
162	CSI_D2_P	VDD_MIPI_1P8	MIPI 1.8V	
163	GND	-	Ground	
164	GND	-	Ground	
165	GND	-	Ground	
166	CSI_D3_N	VDD_MIPI_1P8	MIPI 1.8V	
167	GND	-	Ground	
168	CSI_D3_P	VDD_MIPI_1P8	MIPI 1.8V	
169	GND	-	Ground	
170	GND	-	Ground	
171	UART2_RXD	NVCC_UART	3.3V	
172	CSI_CK_N	VDD_MIPI_1P8	MIPI 1.8V	
173	UART2_TXD	NVCC_UART	3.3V	
174	CSI_CK_P	VDD_MIPI_1P8	MIPI 1.8V	
175	GND	-	Ground	
176	GND	-	Ground	
177	GND	-	Ground	
178	I2C3_SCL	NVCC_I2C	3.3V	
179	TP20	-	-	
180	I2C3_SDA	NVCC_I2C	3.3V	
181	GND	-	Ground	
182	GND	-	Ground	
183	GND	-	Ground	
184	NAND_CLE	NVCC_NAND	3.3V	
185	I2C4_SDA	NVCC_I2C	3.3V	
186	SPDIF_EXT_CLK/PWM1	NVCC_SAI3	3.3V	
187	I2C4_SCL	NVCC_I2C	3.3V	
188	GND	-	Ground	
189	GND	-	Ground	
190	I2C2_SDA	NVCC_I2C	3.3V	
191	TP17	-	-	
192	I2C2_SCL	NVCC_I2C	3.3V	
193	GND	-	Ground	
194	GND	-	Ground	
195	TP21	-	-	
196	DSI_D0_P	VDD_MIPI_1P8	MIPI 1.8V	
197	TP22	-	-	
198	DSI_D0_N	VDD_MIPI_1P8	MIPI 1.8V	
199	TP23	-	-	
200	GND	-	Ground	
201	GND	-	Ground	
202	DSI_D1_P	VDD_MIPI_1P8	MIPI 1.8V	
203	ECSPI2_SCLK	NVCC_ECSPI	3.3V	

204	DSI_D1_N	VDD_MIPI_1P8	MIPI 1.8V	
205	GND	-	Ground	
206	GND	-	Ground	
207	ECSPI2_MOSI	NVCC_ECSPI	3.3V	
208	DSI_CLK_P	VDD_MIPI_1P8	MIPI 1.8V	
209	ECSPI2_MISO	NVCC_ECSPI	3.3V	
210	DSI_CLK_N	VDD_MIPI_1P8	MIPI 1.8V	
211	ECSPI2_SS0	NVCC_ECSPI	3.3V	
212	GND	-	Ground	
213	UART3_TXD	NVCC_UART	3.3V	
214	DSI_D2_P	VDD_MIPI_1P8	MIPI 1.8V	
215	UART3_RXD	NVCC_UART	3.3V	
216	DSI_D2_N	VDD_MIPI_1P8	MIPI 1.8V	
217	UART3_CTS	NVCC_ECSPI	3.3V	
218	GND	-	Ground	
219	UART3_RTS	NVCC_ECSPI	3.3V	
220	DSI_D3_P	VDD_MIPI_1P8	MIPI 1.8V	
221	GPIO1_IO5/M4NMI	NVCC_GPIO1	3.3V	
222	DSI_D3_N	VDD_MIPI_1P8	MIPI 1.8V	
223	USB_OTG2_OC	NVCC_GPIO1	3.3V	
224	GND	-	Ground	
225	GPIO1_IO11	NVCC_GPIO1	3.3V	
226	GPIO1_IO09	NVCC_GPIO1	3.3V	
227	ON_OFF	NVCC_SNVS_1P8	1.8V	
228	TOUCH_RESET	NVCC_GPIO1	3.3V	
229	RTC_IRQ	NVCC_GPIO1	3.3V	
230	TOUCH_INT	NVCC_GPIO1	3.3V	
231	EXT_RESET_N	NVCC_SNVS_1P8	1.8V	
232	GPIO1_IO01	NVCC_GPIO1	3.3V	
233	HP_DET	NVCC_SAI3	3.3V	
234	SPDIF_TX/PWM3	NVCC_SAI3	3.3V	
235	MIC_DET	NVCC_GPIO1	3.3V	
236	GND	-	Ground	
237	GND	-	Ground	
238	SPDIF_RX/PWM2	NVCC_SAI3	3.3V	
239	SAI3_MCLK/PWM4	NVCC_SAI3	3.3V	
240	GND	-	Ground	
241	GND	-	Ground	
242	SAI5_MCLK	NVCC_SAI5	3.3V	
243	SAI3_TXC	NVCC_SAI3	3.3V	
244	GND	-	Ground	
245	SAI3_RXD	NVCC_SAI3	3.3V	
246	SAI5_RXFS	NVCC_SAI5	3.3V	
247	SAI3_TXD	NVCC_SAI3	3.3V	

248	SAI5_RXD0	NVCC_SAI5	3.3V	
249	TP26	-	-	
250	SAI5_RXD1	NVCC_SAI5	3.3V	
251	TP25	-	-	
252	SAI5_RXD2	NVCC_SAI5	3.3V	
253	TP24	-	-	
254	SAI5_RXD3	NVCC_SAI5	3.3V	
255	GND	-	Ground	
256	GND	-	Ground	
257	GND	-	Ground	
258	GND	-	Ground	
259	GND	-	Ground	
260	GND	-	Ground	

2.2. SODIMM 260 PIN MUX

There are many pin muxing options on the i.MX 8M Mini so we recommend registering on the NXP website to get the i.MX 8M Mini Technical Reference Manual. The "**Chapter 8 Chip IO and Pinmux**" will provide all the possible combinations available.
If unsure about the capabilities, please contact us to discuss pin muxing options.

3. SOM INTERFACES

3.1. DISPLAY INTERFACES

3.1.1. OVERVIEW

The Nit8M_Mini_SOM consists of the following display interfaces:

- One MIPI/DSI port - driven by the MIPI/DSI transmitter; four data lane 1080p60 with a maximum bit rate of 1.5 Gbps.

3.1.2. DSI

Nit8M_Mini_SOM MIPI DSI Host Controller supports up to **4** D-PHY data lanes:

DSI SIGNALS:

Pin #	Signal	Description
196	DSI_D0_P	Positive DSI Data 0 Differential
198	DSI_D0_N	Negative DSI Data 0 Differential
202	DSI_D1_P	Positive DSI Data 1 Differential
204	DSI_D1_N	Negative DSI Data 1 Differential
208	DSI_CLK_P	Positive DSI Clock Differential
210	DSI_CLK_N	Negative DSI Clock Differential
214	DSI_D2_P	Positive DSI Data 2 Differential
216	DSI_D2_N	Negative DSI Data 2 Differential
220	DSI_D3_P	Positive DSI Data 3 Differential
222	DSI_D3_N	Negative DSI Data 3 Differential

3.1.3. HDMI

HDMI is available using Boundary Devices DSI to HDMI converter daughter board.

DB_8mm_DSIHD Product Link: DB_8mm_DSIHD

3.1.4. LVDS

LVDS is available using Boundary Devices DSI to LVDS converter daughter board.

DB_8mm_DSIHD Product Link: DB_8mm_DSIHD

3.2. CAMERA INTERFACES

3.2.1. MIPI CSI

MIPI CSI2 (four-lane)- This module provides one four-lane MIPI camera serial interfaces, which operates up to a maximum bit rate of 1.5 Gbps. The CSI-2 Host Controller is a digital core that implements all protocol functions defined in the MIPI CSI-2 specification, providing an interface between the system and the MIPI D-PHY, allowing communication with an MIPI CSI-2 compliant camera sensor.

MIPI CSI-2SIGNALS:

Pin #	Signal	Description
148	CSI_D0_N	Negative CSI-0 Clock Differential
150	CSI_D0_P	Positive CSI-0 Clock Differential
154	CSI_D1_N	Negative CSI-1 Clock Differential
156	CSI_D1_P	Positive CSI-1 Clock Differential
160	CSI_D2_N	Positive CSI-2 Clock Differential
162	CSI_D2_P	Negative CSI-2 Clock Differential
166	CSI_D3_N	Negative CSI-3 Clock Differential
168	CSI_D3_P	Positive CSI-3 Clock Differential
172	CSI_CK_N	Negative Clock Differential
174	CSI_CK_P	Positive Clock Differential

3.3. GIGABIT ETHERNET

GIGABIT ETHERNET FEATURES:

The Ethernet Media Access Controller (MAC) is designed to support 10/100/1000 Mbps Ethernet/IEEE 802.3 networks. An external Gigabit magnetics is required to complete the interface to the media. The i.MX8 processor also consists of HW assist for IEEE1588 standard. See the ENET chapter of the i.MX 8M Mini Applications Processor Reference Manual (IMX8MMRM) for details

GIGABIT ETHERNET:

Vendor	Part Number	Package
Qualcomm	AR8035-AL1A / KSZ9031RN	PHY Transceiver
Amphenol	RJHSE-5381	RJ45 Ethernet Jack
Link PP	LP5007NL	Ethernet Transformer

GIGABIT ETHERNET SIGNALS:

Pin #	Signal
23	RGMII_ACT
25	RGMII_LINK
29	TRX3_N
31	TRX3_P
35	TRX2_N
37	TRX2_P
41	TRX1_N
43	TRX1_P
47	TRX0_N
49	TRX0_P

3.4. WI-FI &BLUETOOTH

The Nit8M_Mini_SOM does not contain WiFi+BT directly on the SOM. The WiFi+BT functionality is available on the carrier board via the SDIO + BT interfaces. Please see the Nitrogen8M_Mini Carrier board schematics for connection details as well as the recommended BD_SDMAC WiFi+BT module.

3.5. USB HOST2.0

The USB controller block provides high performance USB functionality that conforms to the USB 2.0 specification.

USB HOST SIGNALS:

Pin #	Signal	Description
99	USB_OTG2_PWR	USB OTG Power Enable
101	USB_OTG2_OC	USB OTG Over Current
103	USB_OTG2_VBUS	USB 2.0 OTG VBUS Indicator (5V)
107	USB_OTG2_D_P	Positive USB OTG Data
109	USB_OTG2_D_N	Negative USB OTG Data

3.6. USB 2.0OTG

USB 2.0 ON-THE-GO FEATURES:

High-speed OTG core:

- HS/FS/LS UTMI compliant interface
- High speed, full speed and low speed operation in host mode (with UTMI transceiver)
- High speed, and full speed operation in peripheral mode (with UTMI transceiver)
- Hardware support for OTG signaling, session request protocol, and host negotiation protocol
- Up to 8 bidirectional end points
- Integrated HS USBPHY

OTG SIGNALS:

Pin #	Signal	Description
113	USB_OTG1_PWR	USB OTG Power Enable
115	USB_OTG1_OC	USB OTG Over Current
117	USB_OTG1_ID	USB ID /3.3V
121	USB_OTG1_D_P	Positive USB OTG Data
123	USB_OTG1_D_N	Negative USB OTG Data
127	USB_OTG1_VBUS	USB 2.0 OTG VBUS Indicator (5V)

3.7. MMC/SD/SDIO

i.MX 8M Mini SoC characteristics:
All the MMC/SD/SDIO controller IPs are based on the uSDHC IP.

They are designed to support:

- SD/SDIO standard, up to version 3.0.
- MMC standard, up to version 5.1.
- Support for SDXC (extended capacity)
- 1.8 V and 3.3 V operation, but do not support 1.2 V operation.
- 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit/8-bit MMC mode.

Two uSDHC controllers (SDHC1 and SDHC3) can support up to an 8-bit interface, the other controller (SDHC2) can only support up to a 4-bit interface.

SDMMC2 SIGNALS:

Pin #	Signal	Description
79	SD2_RESET_B	Connect to SD2 Reset Pin on SD CACARD
81	SD2_CD	Connect to SD2 CD Pin on SD Card
83	SD2_DATA0	SD2 Data 0 Line
85	SD2_DATA1	SD2 Data 1 Line
87	SD2_DATA2	SD2 Data 2 Line
89	SD2_DATA3	SD2 Data 3 Line
91	SD2_CMD	CMD Line Connect To Card
95	SD2_CLK	Clock

Note: SDIO does not require pull-ups

3.8. AUDIO

The Nit8M_Mini_SOM features these audio interfaces:

- WM8960CGEFL/V Audio codec interfaces
    1. Analog outputs/inputs:
        - Stereo HP out
        - Lineout L/R
        - Built-In 2W Amplifier

    *Reference the Cirrus Website for technical specifications.
    https://statics.cirrus.com/pubs/proDatasheet/WM8960_v4.4.pdf

AUDIO SIGNALS:

Pin #	Signal	Description
28	SAI1_RXD0	GPIO or SAI Audio 3.3V
46	SAI1_MCLK	GPIO or SAI Audio 3.3V
50	SAI1_TXFS	GPIO or SAI Audio 3.3V
52	SAI1_TXC	GPIO or SAI Audio 3.3V
54	SAI1_TXD0	GPIO or SAI Audio 3.3V

3.9. UARTINTERFACES

All 4 UART interfaces are supported, based on pin mux configurations of the UART interface.

UART FEATURES:

• High-speed TIA/EIA-232-F compatible, up to Mbit/s
• Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
• 9-bit or Multidrop mode (RS-485) support (automatic slave address detection)
• 7 or 8 data bits for RS-232 characters, or 9 bit RS-485 format
• 1 or 2 stop bits
• Programmable parity (even, odd, and no parity)
• Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals
• RS-485 driver direction control via CTS_B signal
• Edge-selectable RTS_B and edge-detect interrupts
• Status flags for various flow control and FIFO states
• Voting logic for improved noise immunity (16x oversampling)
• Transmitter FIFO empty interrupt suppression
•UART internal clocks enable/disable
• Auto baud rate detection (up to 115.2 Kbit/s)
• Receiver and transmitter enable/disable for power saving
• RX_DATA input and TX_DATA output can be inverted respectively in RS-232/ RS-485 mode
• DCE/DTE capability
• RTS_B, IrDA asynchronous wake (AIRINT), receive asynchronous wake (AWAKE) interrupts wake the processor from STOP mode
• Maskable interrupts
• Two DMA Requests (TxFIFO DMA Request and RxFIFO DMA Request)
• Escape character sequence detection
• Software reset (SRST_B)
• Two independent, 32-entry FIFOs for transmit and receive
• The peripheral clock can be totally asynchronous with the module clock. The module clock determines baud rate. This allows frequency scaling on peripheral clock (such as during DVFS mode) while remaining the module clock frequency and baud rate

UART1 SIGNALS:

Pin #	Signal	Description
96	UART1_TXD	UART1Transmit
98	UART1_RTS	UART1 HW Flow Control RTS
100	UART1_RXD	UART1 Receive
106	UART1_CTS	UART1 HW Flow Control CTS

UART2 SIGNALS:

Pin #	Signal	Description
171	UART2_RXD	UART2 Receive
173	UART2_TXD	UART2 Transmit

UART3 SIGNALS:

Pin #	Signal	Description
213	UART3_TXD	UART3 Transmit
215	UART3_RXD	UART3 Receive
217	UART3_CTS	UART3 HW Flow Control CTS
219	UART3_RTS	UART3 HW Flow Control RTS

UART4 SIGNALS:

Pin #	Signal	Description
149	UART2_RXD	UART2 Receive
151	UART2_TXD	UART2 Transmit

Note: UART4 is used as default boot debug port. (Console/Debug Port)

3.10. FLEXIBLE SPI

FlexSPI with support for XIP (for ME in low-power mode) and parallel read mode of two identical FLASH devices

The FlexSPI module acts as an interface to external serial flash devices. This module contains the following features:

- Flexible sequence engine to support various flash vendor devices
- Single pad/Dual pad/Quad pad mode of operation
- Single Data Rate/Double Data Rate mode of operation
- Parallel Flash mode
- DMA support
- Memory mapped read access to connected flash devices
- Multi master access with priority and flexible and configurable buffer for each master GIC Generic Interrupt Controller The GIC handles all interrupts

3.11. ECSPI KEY FEATURES

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a Full-duplex enhanced Synchronous Serial Interface, with data rate up to 52 Mbit/s. Configurable to support Master/Slave modes, four chip selects to support multiple peripherals.

- Full-duplex synchronous serial interface

- Master/slave configurable
- Four chip select (SS) signals to support multiple peripherals
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmitting and receiving data
- 32-bit wide by 16-entry FIFO for HT message data
- Polarity and phase of the chip select (SS) and SPI clock (SCLK) are configurable
- Direct Memory Access (DMA)support
- Max operation frequency up to the reference clock frequency

SPI isMuxed with SD2 a CSI Signals and is supported as follows:

Table 6-22. SD/MMC IOMUX pin configuration

Signal	USDHC1	USDHC2	USDHC3
CLK	SD1_CLK.alt0	SD2_CLK.alt0	SD3_CLK.alt0
CMD	SD1_CMD.alt0	SD2_CMD.alt0	SD3_CMD.alt0
DATA0	SD1_DATA0.alt0	SD2_DATA0.alt0	SD3_DATA0.alt0
DATA1	SD1_DATA1.alt0	SD2_DATA1.alt0	SD3_DATA1.alt0
DATA2	SD1_DATA2.alt0	SD2_DATA2.alt0	SD3_DATA2.alt0

3.12. PCIE

Nit8M_Mini_SOM PCI Express functionality has the following parts:

PCI Express includes the following cores:

- PCI Express Dual Mode (DM)core
- PCI Express Root Complex (RC)core
- PCI Express Endpoint (EP)core

PCI Express 2.0 PHY:

- PCIe 2.0 PHY is a complete mixed-signal semiconductor intellectual property (IP) solution, designed for single-chip integration into computer applications
- The PCIe 2.0 PHY supports both the 5 Gbps data rate of the PCI Express Gen 2.0 specifications as well as being backwards compatible to the 2.5Gb/s Gen 1.1 specification

PCIE SIGNALS:

Pin #	Signal	Description
122	PCIE_RST_B	Reset PCIE Module 3.3V
124	PCIE_DIS_B	Disable PCIE Signal 3.3V
128	PCIE_TX_P	Positive PCI TX Differential
130	PCIE_TX_N	Negative PCI TX Differential
134	PCIE_RX_P	Positive PCI RX Differential
136	PCIE_RX_N	Negative PCI RX Differential
140	PCIE_REFCLK_P	PCIE Clock
142	PCIE_REFCLK_N	PCIE Clock

3.13. I2C

I2C-1, 2,3, 4 Interface connectivity peripherals provide serial interface for external devices.
The I2C operates primarily in two functional modes: Standard mode and Fast mode.

- In Standard mode, I2C supports the data transfer rates up to 100 kbits/s.
- In Fast mode, data transfer rates up to 400 kbits/s can be achieved. Per blockoperation, there is no special configuration required for Fast or Standard mode. It isthe data transfer rate that distinguishes Standard and Fast mode.

I2C1 SIGNALS: I2C1 IS RESERVED FOR PMIC

I2C2 SIGNALS:

Pin #	Signal	Description
190	I2C1_SDA	I2C Signal
192	I2C1_SCL	I2C Signal

I2C3 SIGNALS:

Pin #	Signal	Description
178	I2C2_SCL	I2C Signal
180	I2C2_SDA	I2C Signal

I2C4 SIGNALS:

Pin #	Signal	Description
185	I2C3_SDA	I2C Signal
187	I2C3_SCL	I2C Signal

3.14. GENERAL PURPOSE I/O

Most of the SOM's IO pins can be used as GPIOs. If you need more GPIO, or need other signals, please contact us to discuss pin muxing options.

3.15. GENERAL SYSTEM CONTROL

3.15.1. RESET

'0' logic will reset Nit8M_Mini_SOM

3.16. REFERENCE CLOCK OUT

Nit8M_Mini_SOM output clock is controlled by the i.MX8 Mini CCM module. Please refer to the i.MX8 Mini User Manual regarding the configuration option for this clock.

3.17. POWER

3.17.1. POWER SUPPLY

Pin #	Signal	Description
1, 2, 3, 4, 5, 6, 7, 8	5VIN	DC Supply Voltage (5 Volt)

3.17.2. GROUND

Pin #	Signal	Description
9, 10, 11, 12, 13, 14, 15, 16, 17, 18, 20, 27, 33, 39, 44, 45, 48, 51, 57, 63, 70, 77, 88, 92, 93, 97, 105, 111, 119, 120, 125, 126, 132, 138, 139, 143, 144, 145, 146, 152, 153, 155, 157, 158, 159, 161, 163, 164, 165, 167, 169, 170, 175, 176, 177, 181, 182, 183, 188, 189, 193, 194, 200, 201, 205, 206, 212, 218, 224, 236, 237, 240, 241, 244, 255, 256, 257, 258, 259, 260	GND	Digital Ground

4. OPERATIONAL CHARACTERISTICS

4.1. POWER SUPPLY

Description	Signal	Description	Typical	Tolerance	Unit
Main Power Supply, DC-IN	5VIN	DC Supply Voltage	5	+/- 5%	V

4.2. POWER CONSUMPTION

Parameter	Min	Typical	Max	Unit
Main Input Voltage	-	5	-	V
Power Consumption*	-	1300	2700	mW
CPU Clock	1.2	-	1.8	GHz

*Reference the NXP Website to get the i.MX8 reference manual for power consumption and CPU clock speed specifications

5. ENVIRONMENTAL SPECIFICATIONS

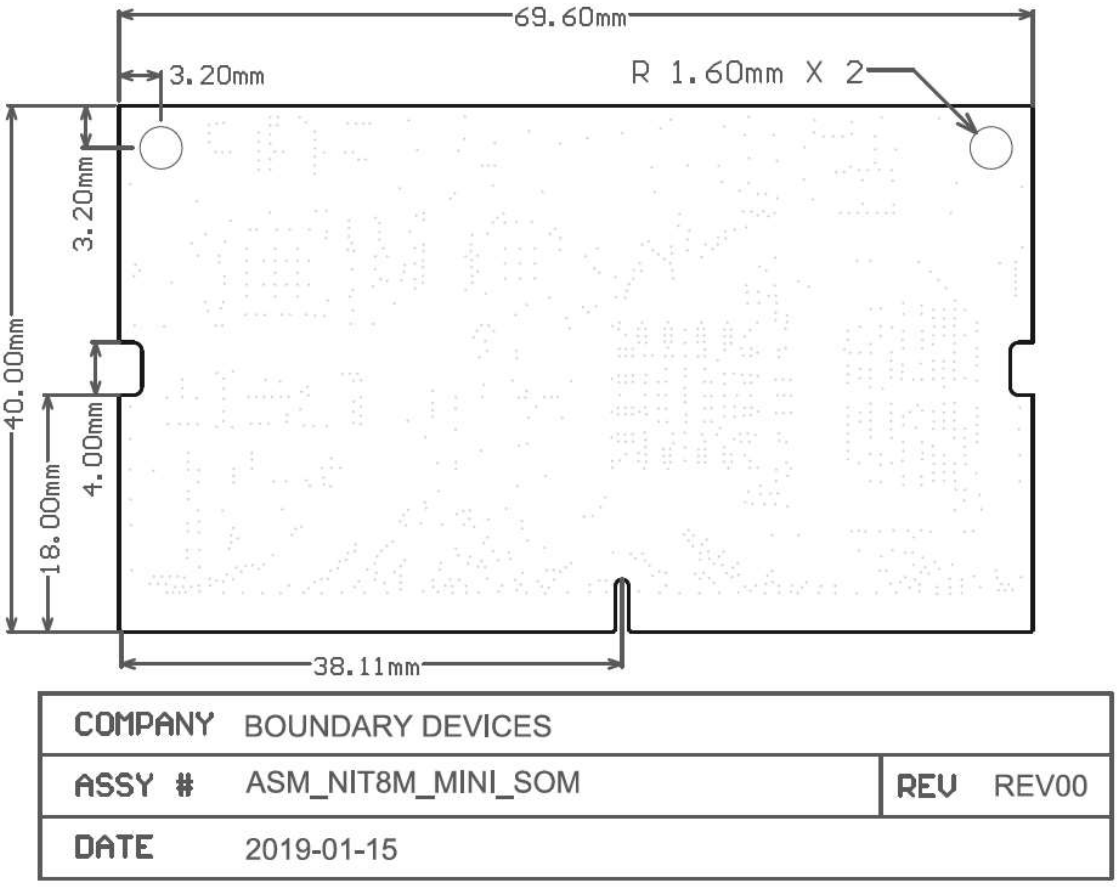
Operating Rating	Min.	Max.
Commercial Operating Temperature Range	0 °C	+70 °C
Industrial Operating Temperature Range	-40 °C	+85 °C
Relative humidity, Operational	10%	90%
Relative humidity, Storage	5%	95%
MTBF	215 kHours	-

Notes:

1. Commercial and Industrial Temperature is based on the operating temperature grade of the SOM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.
2. WiFi+BT module is only rated to -20 to +70 °C.

6. MECHANICALDRAWINGS

TOP VIEW



7. ORDERABLE PART NUMBERS

SKU	CPU	DDR Memory	eMMC Storage Size	Operating Rating	Operating Temperature Range
NIT8MQ_Mini_SOM_2r16e	i.MX8 Mini Quad	2GB	16GB	Commercial	0° to 70°C
NIT8MQ_Mini_SOM_4r16e	i.MX8 Mini Quad	4GB	16GB	Commercial	0° to 70°C
NIT8MQ_Mini_SOM_2r16e_i	i.MX8 Mini Quad	2GB	16GB	Industrial	-40° to 85°C
NIT8MQ_Mini_SOM_4r16e_i	i.MX8 Mini Quad	4GB	16GB	Industrial	-40° to 85°C

*Please contact us to discussother custom options

8. WARRANTY TERMS

Seller warrants to Buyer that goods and merchandise sold to Buyer will be free from liens and encumbrances when shipped to Buyer and will be free from defects in material and workmanship for a period of one year from the date of shipments to Buyer provided that:

(a) Seller is promptly notified (within the warranty period) of any warranty claim

(b) The goods and merchandise are returned to Seller, freight prepaid, after Buyer has received a return authorization number from Seller. Seller will credit Buyer for reasonable freight charges paid to return such goods and merchandise

(c) Seller's examination of such items shall disclose to its reasonable satisfaction that the claimed defect in the goods and merchandise was not caused by misuse, static discharge, abuse, neglect, improper handling, installation, unauthorized repair, alteration or accident. Modification of goods and merchandise by Buyer, or at Buyer's direction, or by any subsequent purchaser or user, unless specifically authorized in writing by Seller, shall invalidate the above warranty.

Seller's liability under this warranty is limited to repairing, replacing, or issuing a credit in the amount of the unit contract price, at its election, for any such claim. Any repair or replacement shall not extend the warranty period. Because identical parts may not be available upon return of a device, Seller may replace components with functionally equivalent parts. Buyer will be notified of any replacement which is known to require modifications to software installed on the device.

This warranty is extended to Buyer and subsequent purchasers or users of such goods and merchandise. Buyer is the sole entity entitled to exercise this warranty and may act as an agent on behalf of subsequent purchasers. Seller will not honor any claims under this warranty directly from subsequent purchasers or third parties. This warranty is given in lieu of all other warranties, express or implied, including implied warranties of merchantability and fitness for a particular purpose.

9. CONTACT INFORMATION

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