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MOSFET - Power, Single N-Channel, SO8-FL
25 V, 4.2 mΩ, 75 A

NTMFS4D8N02H

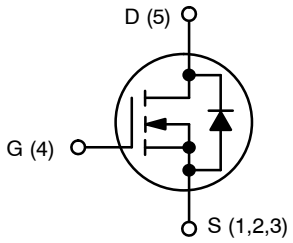
ON Semiconductor®

www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
25 V	4.2 mΩ @ 10 V	75 A
	7.0 mΩ @ 4.5 V	

Features
- Advanced Package (5x6 mm) with Excellent Thermal Conduction
- Ultra Low $R_{DS(on)}$ to Improve System Efficiency
- Optimized Design to Minimize Conduction and Switching Losses
- These Devices are Pb−Free, Halogen−Free/BFR−Free and are RoHS Compliant

Typical Applications
- High Performance DC−DC Converters
- System Voltage Rails
- Netcom, Telecom
- Servers & Point of Load



N−CHANNEL MOSFET

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

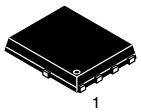
Parameter			Symbol	Value	Unit
Drain−to−Source Voltage			V_{DSS}	25	V
Gate−to−Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	I_D	75	A
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	T_C = 25°C	P_D	41	W
Continuous Drain Current $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	I_D	21	A
Power Dissipation $R_{\theta JA}$ (Note 1)	Steady State	T_A = 25°C	P_D	3.2	W
Pulsed Drain Current	T_A = 25°C, t_p = 10 μs		I_{DM}	216	A
Single Pulse Drain−to−Source Avalanche Energy ($I_{L(pk)}$ = 32 A, L = 0.1 mH) (Note 2)			E_{AS}	51	mJ
Operating Junction and Storage Temperature Range			T_J, T_{stg}	−55 to +150	°C
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

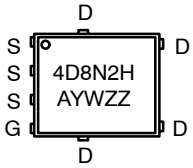
Parameter	Symbol	Value	Unit
Junction−to−Case − Steady State (Note 1)	$R_{\theta JC}$	3.7	°C/W
Junction−to−Ambient − Steady State (Note 1)	$R_{\theta JA}$	47.3	

1. Surface−mounted on FR4 board using a 1 in^2, 2 oz. Cu pad.
2. This is the absolute maximum rating. Parts are 100% UIS tested at T_J = 25°C, V_{GS} = 10 V, I_L = 21 A, E_{AS} = 22 mJ.



DFN5
(SO−8FL)
CASE 488AA
STYLE 1

MARKING DIAGRAM



4D8N2H = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
ZZ = Lot Traceability

ORDERING INFORMATION
See detailed ordering, marking and shipping information on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain−to−Source Breakdown Voltage	$V_{(BR)DSS}$	V_{GS} = 0 V, I_D = 250 μA		25			V
Drain−to−Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	I_D = 250 μA, ref to 25°C			10.6		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	V_{GS} = 0 V, V_{DS} = 20 V	T_J = 25°C			1.0	μA
			T_J = 125°C			10	
Gate−to−Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 20 V				100	nA
ON CHARACTERISTICS (Note 3)							
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}, I_D = 250 μA		1.2		2.1	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$	I_D = 250 μA, ref to 25°C			−4.2		mV/°C
Drain−to−Source On Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 20 A		3.4	4.2	mΩ
		V_{GS} = 4.5 V	I_D = 15 A		5.4	7.0	
Forward Transconductance	g_{FS}	V_{DS} = 5 V, I_D = 15 A			54		S
Gate Resistance	R_G	T_A = 25°C			0.9		Ω
CHARGES & CAPACITANCES							
Input Capacitance	C_{ISS}	V_{GS} = 0 V, V_{DS} = 12 V, f = 1 MHz			780		pF
Output Capacitance	C_{OSS}				530		
Reverse Transfer Capacitance	C_{RSS}				39		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 4.5 V, V_{DS} = 12 V; I_D = 30 A			6.2		nC
Threshold Gate Charge	$Q_{G(TH)}$				1.4		
Gate−to−Source Charge	Q_{GS}				2.5		
Gate−to−Drain Charge	Q_{GD}				1.5		
Total Gate Charge	$Q_{G(TOT)}$	V_{GS} = 10 V, V_{DS} = 12 V; I_D = 30 A			13.4		nC
SWITCHING CHARACTERISTICS, V_{GS} = 4.5 V (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 4.5 V, V_{DS} = 12 V, I_D = 30 A, R_G = 3 Ω			9.7		ns
Rise Time	t_r				7.4		
Turn−Off Delay Time	$t_{d(OFF)}$				13		
Fall Time	t_f				5.2		
SWITCHING CHARACTERISTICS, V_{GS} = 10 V (Note 4)							
Turn−On Delay Time	$t_{d(ON)}$	V_{GS} = 10 V, V_{DS} = 12 V, I_D = 30 A, R_G = 3 Ω			6.9		ns
Rise Time	t_r				2.6		
Turn−Off Delay Time	$t_{d(OFF)}$				18		
Fall Time	t_f				2.7		
DRAIN−SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	V_{GS} = 0 V, I_S = 10 A	T_J = 25°C		0.8	1.0	V
			T_J = 125°C		0.65		
Reverse Recovery Time	t_{RR}	V_{GS} = 0 V, dI_S/dt = 100 A/μs, I_S = 10 A			28		ns
Charge Time	t_a				14		
Discharge Time	t_b				14		
Reverse Recovery Charge	Q_{RR}				11		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

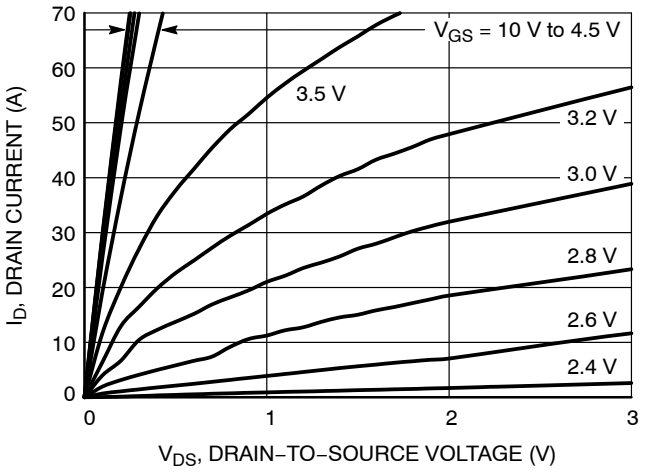


Figure 1. On−Region Characteristics

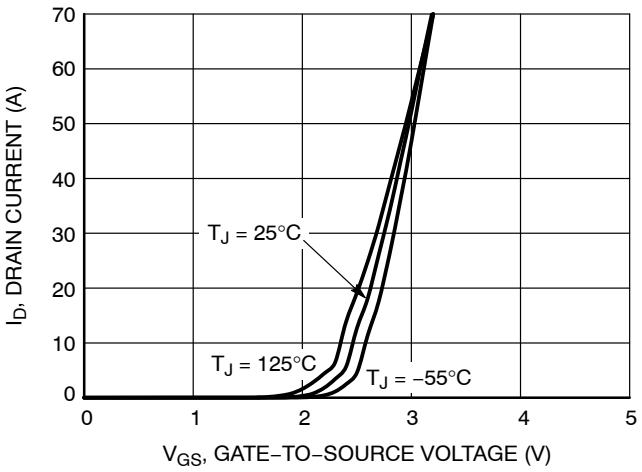


Figure 2. Transfer Characteristics

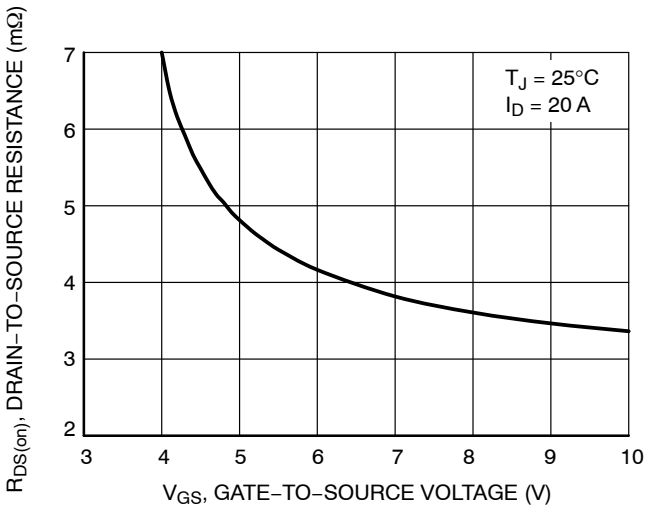


Figure 3. On−Resistance vs. Gate−to−Source Voltage

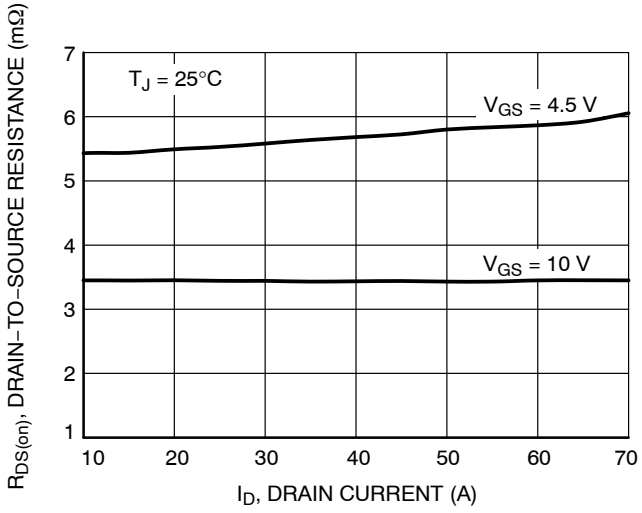


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

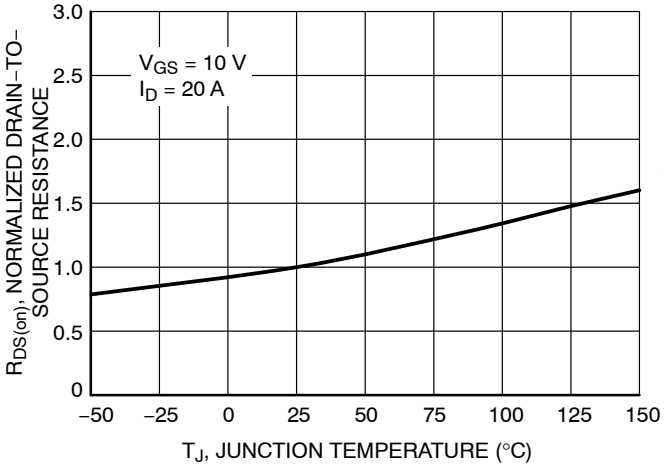


Figure 5. On−Resistance Variation with Temperature

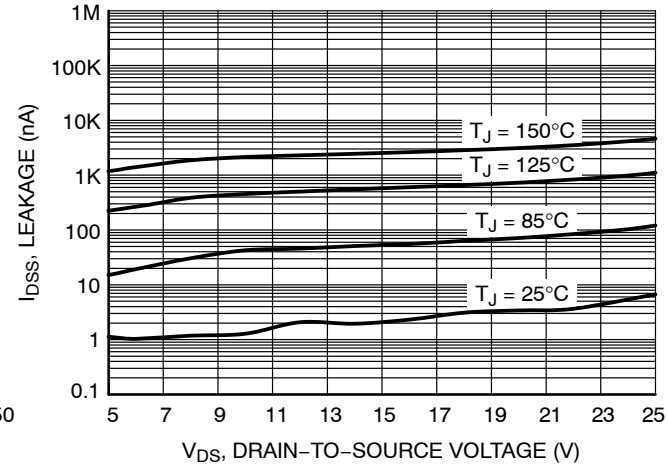


Figure 6. Drain−to−Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS

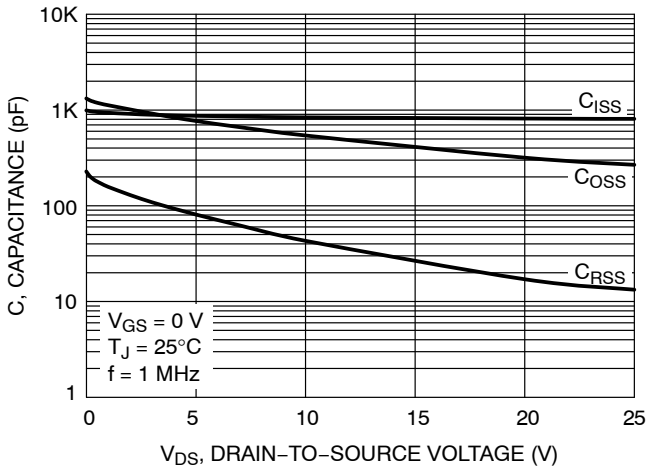


Figure 7. Capacitance Variation

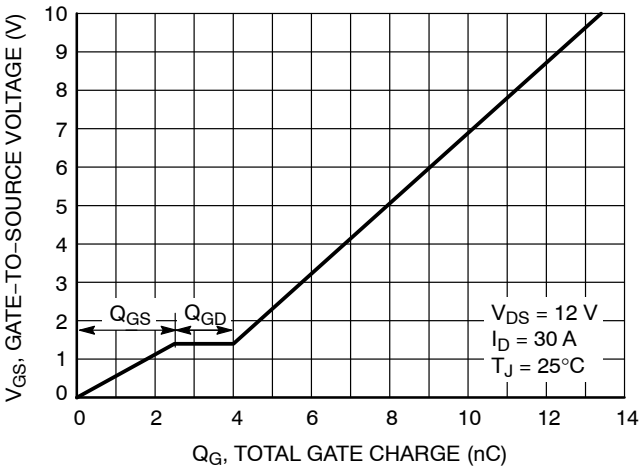


Figure 8. Gate−to−Source vs. Total Charge

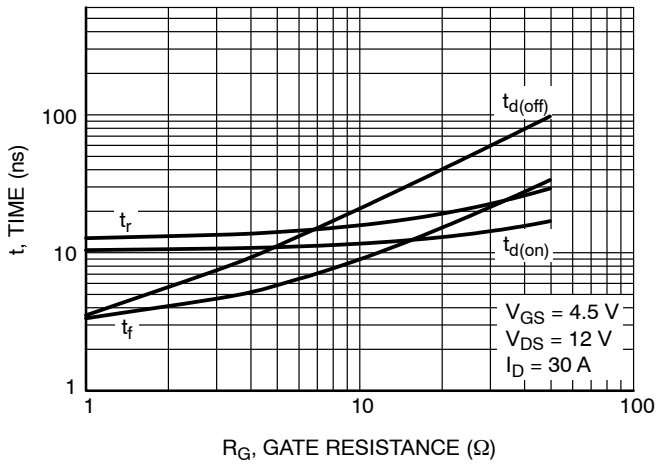


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

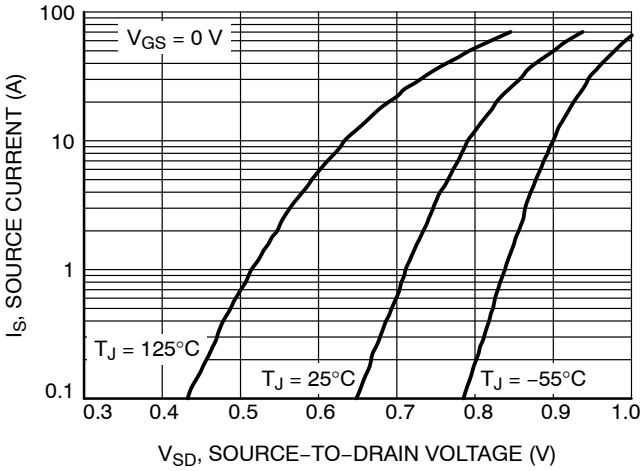


Figure 10. Diode Forward Voltage vs. Current

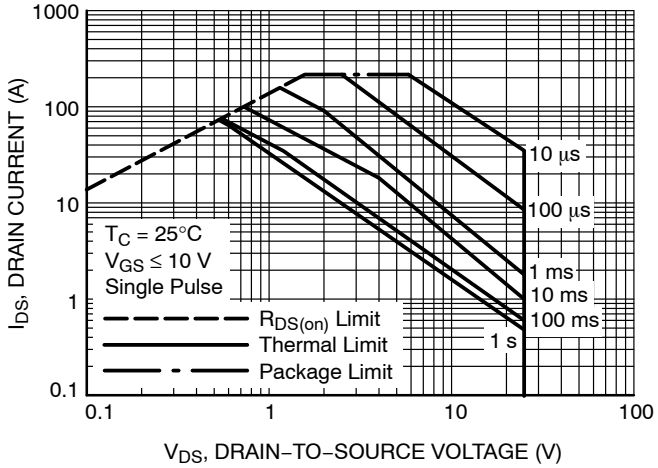


Figure 11. Maximum Rated Forward Biased Safe Operating Area

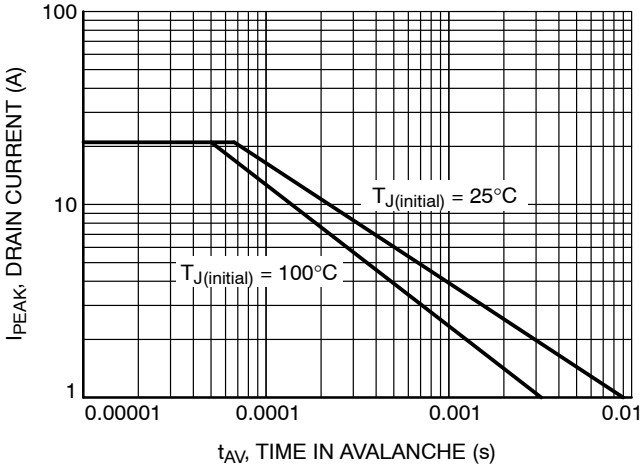


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS

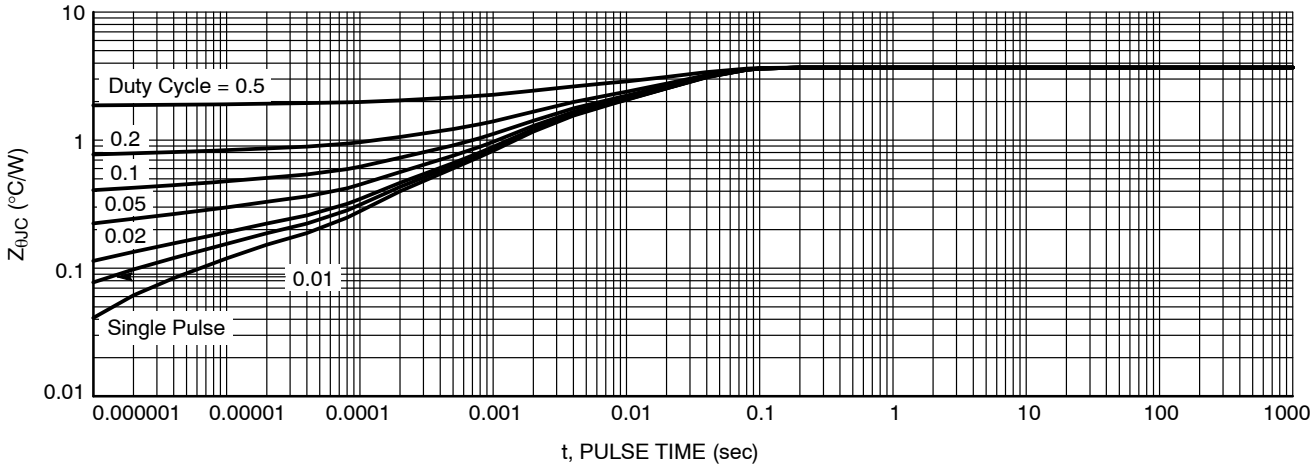


Figure 13. Transient Thermal Impedance

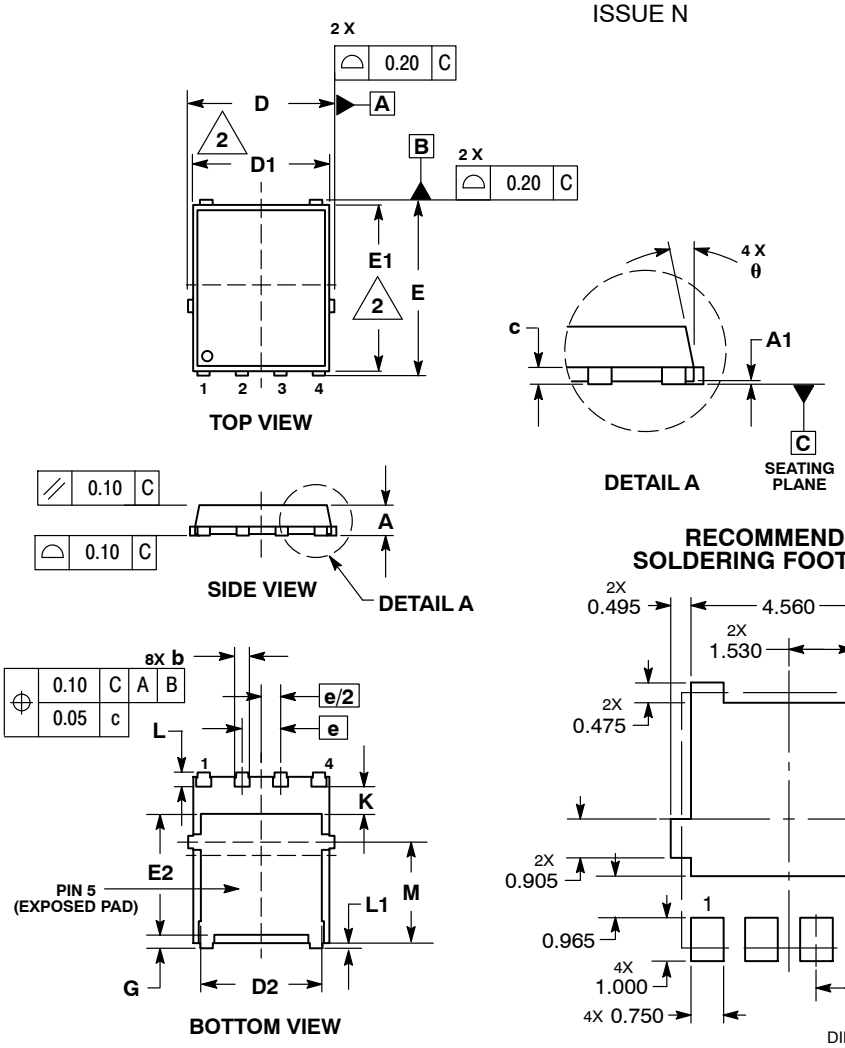
DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMFS4D8N02HT1G	4D8N2H	DFN5 (Pb−Free)	1500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO−8FL)
CASE 488AA
ISSUE N



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

	MILLIMETERS		
DIM	MIN	NOM	MAX
A	0.90	1.00	1.10
A1	0.00	–––	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.00	5.15	5.30
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.00	6.15	6.30
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.575	0.71
K	1.20	1.35	1.50
L	0.51	0.575	0.71
L1	0.125 REF		
M	3.00	3.40	3.80
θ	0 °	–––	12 °

STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

RECOMMENDED SOLDERING FOOTPRINT*

DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
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