

## Internal 3.5A MOSFET Switching Regulator IC for Buck Converter

### FEATURES

- Fast transient response at recovering from voltage drop
- External clock synchronization
- Operating voltage range      4.45V to 40V
- Switching current                5A min.
- Oscillating frequency        C ver. 450kHz  
J ver. 100k to 1000kHz
- PWM control
- Maximum 100% duty cycle
- Adjustable soft start function
- Corresponds to MLCC
- UVLO function
- Over Current Protection (Hiccup type)
- Thermal shutdown protection
- Power Good function
- Standby function
- Package outline                 HSOP8

### GENERAL DESCRIPTION

The NJW4196 is a buck converter with 40V/3.5A MOSFET.

It improves transient response at recovering from voltage drop compare with conventional current mode products. Therefore the NJW4196 provides excellent stable regulation even under condition of large voltage fluctuations.

Oscillating frequency can be synchronized with an externally input clock.

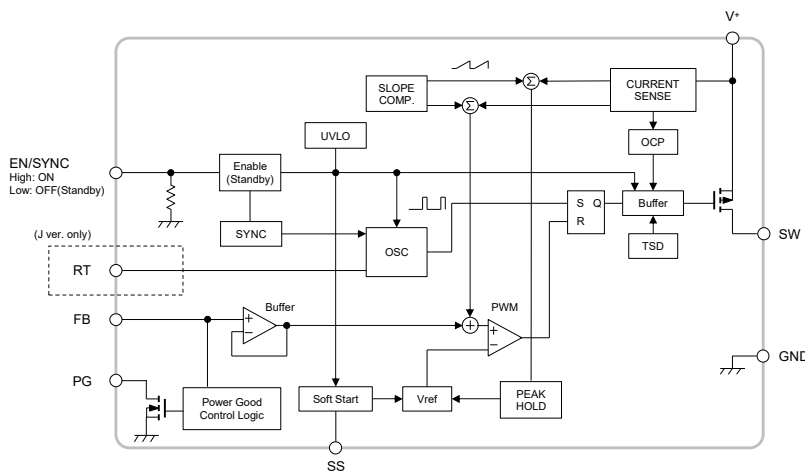
Also, it has a soft start function, an over current protection and a thermal shutdown circuit.

It is suitable for power supply for Car Accessory, Office Automation Equipment, Industrial Instrument and so on.

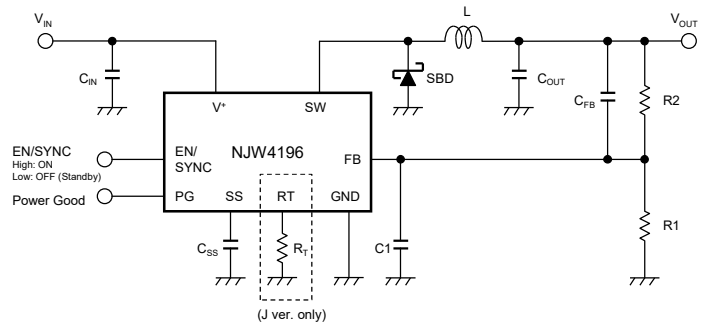
### APPLICATION

- Car accessory
- Industrial equipment
- OA equipment

### BLOCK DIAGRAM



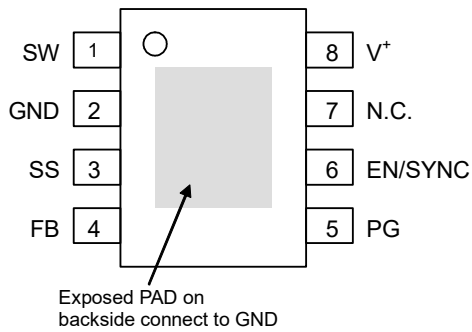
### TYPICAL APPLICATION



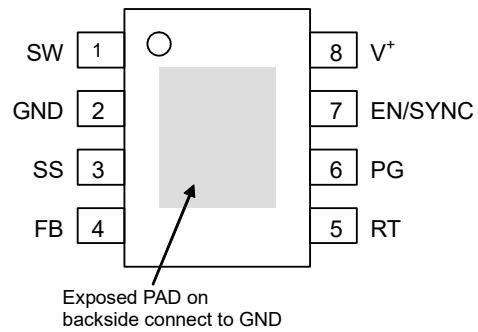
## ■PRODUCT CLASSIFICATION

Part Number	Version	Oscillating Frequency
NJW4196GM1-C	C	Fixed 450kHz
NJW4196GM1-J	J	Adjustable 100k to 1000kHz

## ■PIN CONFIGURATION



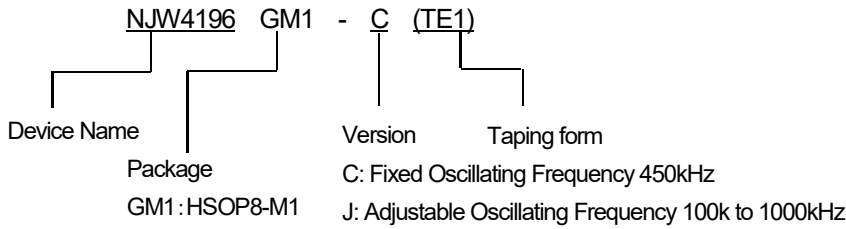
**NJW4196GM1-C**



**NJW4196GM1-J**

SYMBOL	Pin NO.		DESCRIPTION
	C ver.	J ver.	
SW	1	1	Switch output pin of Power MOSFET
GND	2	2	GND pin
SS	3	3	Soft Start time setting pin. Soft start time is set by an external capacitor.
FB	4	4	Output voltage detecting pin Connects output voltage through the resistor divider tap to this pin in order to voltage of the FB pin become 1V.
RT	-	5	Oscillating frequency setting pin with an external timing resistor. Oscillating frequency should set between 100kHz and 1000kHz.(Only J version)
PG	5	6	Power Good pin. An open drain output that goes high impedance when the FB pin voltage is stable around $\pm 15\%$ .
EN/SYNC	6	7	Standby control pin It is internally pulled down with 500k $\Omega$ . Normal operation at the time of high level. Standby Mode at the time of low level or OPEN. Moreover, it operates by inputting clock signal at the oscillatory frequency that synchronized with the input signal.
N.C.	7	-	Non connection(Only C version)
V <sup>+</sup>	8	8	Power supply pin
Exposed PAD	-	-	Connect to GND

## MARK INFORMATION



## ORDERING INFORMATION

PART NUMBER	PACKAGE OUTLINE	Oscillating Frequency	RoHS	HALOGEN-FREE	TERMINAL FINISH	MARKING	WEIGHT (mg)	MOQ (pcs)
NJW4196GM1-C(TE1)	HSOP8	Fixed	yes	yes	Sn100%	4196C	81	3000
NJW4196GM1-J(TE1)	HSOP8	Adjustable	yes	yes	Sn100%	4196J	81	3000

## ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V^+$	-0.3 to +45	V
$V^+$ - SW pin Voltage	$V_{V-SW}$	+45	V
FB pin Voltage	$V_{FB}$	-0.3 to +6	V
PG pin Voltage	$V_{PG}$	-0.3 to +6	V
EN/SYNC pin Voltage	$V_{EN/SYNC}$	-0.3 to +45	V
Power Dissipation ( $T_a=25^\circ\text{C}$ ) HSOP8	$P_D$	(2 Layer / 4 Layer) 860 <sup>(1)</sup> / 2900 <sup>(2)</sup>	mW
Junction Temperature	$T_j$	-40 to +150	$^\circ\text{C}$
Operating Temperature	$T_{opr}$	-40 to +125	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-50 to +150	$^\circ\text{C}$

(1): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

(2): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)

(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

Depending on conditions of the application, NJW4196 may not apply a max output current of it by a limit of the power consumption.

## RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V^+$	4.45 to 40	V
PG pin Voltage	$V_{PG}$	0 to 5.5	V
Timing Resistor <sup>(3)</sup>	$R_T$	10 to 120	k $\Omega$
Oscillating Frequency <sup>(3)</sup>	$f_{OSC}$	100 to 1000	kHz
External Clock Input Range	$f_{SYNC}$	C ver. 440 to 600 J ver. $f_{osc} \times 0.9$ (250kHz min.) to $f_{osc} \times 1.3$	kHz

(3): Apply only the J version.

**■ ELECTRICAL CHARACTERISTICS**

 Unless otherwise noted,  $V^+ = V_{EN,SYNC} = 12V$ , ( $R_T = 39k\Omega$ : J version only),  $T_a = 25^\circ C$ 

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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**Under Voltage Lockout Block**

ON Threshold Voltage	$V_{T\_ON}$	$V^+ = L \rightarrow H$	4.05	4.25	4.45	V
OFF Threshold Voltage	$V_{T\_OFF}$	$V^+ = H \rightarrow L$	4.0	4.15	4.3	V
Hysteresis Voltage	$V_{HYS}$		70	100	-	mV

**Soft Start Block**

Charge Current	$I_{CHG}$		3.5	4.0	4.5	$\mu A$
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**Oscillator Block**

Oscillating Frequency	$f_{OSC\_C}$	C version <sup>(4)</sup>	405	450	495	KHz
	$f_{OSC\_J}$	J version, $R_T = 39k\Omega$ <sup>(5)</sup>	270	300	330	KHz
Oscillating Frequency deviation (Supply voltage)	$f_{DV}$	$V^+ = 4.45V$ to 40V	-	1	-	%
Oscillating Frequency deviation (Temperature)	$f_{DT}$	$T_a = -40^\circ C$ to $+85^\circ C$	-	5	-	%

(4): Apply only the C ver.

(5): Apply only the J ver.

**Buffer Block**

Reference Voltage	$V_B$		-1.0%	1	+1.0%	V
Threshold Voltage	$V_{TH}$	$I_{SW} = 3A$	-2.0%	1	+2.0%	V
Input Bias Current	$I_B$		-0.1	-	0.1	$\mu A$

**PWM Comparete Block**

Maximum Duty Cycle	$M_{AX}D_{UTY}$	$V_{FB} = 0.9V$	-	-	100	%
Minimum ON Time	$t_{ON-min}$		-	125	185	ns

**OCP Block**

COOL DOWN Time	$t_{COOL}$		-	75	-	ms
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**Output Block**

Output ON Resistance	$R_{ON}$	$I_{SW} = 3A$	-	0.125	0.25	$\Omega$
Switching Current Limit	$I_{LIM}$		5	6.5	8	A
SW Leak Current	$I_{LEAK}$	$V_{EN,SYNC} = 0V$ , $V^+ = 40V$ , $V_{SW} = 0V$	-	-	5	$\mu A$

**■ ELECTRICAL CHARACTERISTICS**

 Unless otherwise noted,  $V^+ = V_{EN/SYNC} = 12V$ , ( $R_T = 39k\Omega$ : J version only),  $T_a = 25^\circ C$ 

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
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**Standby Control / Sync Block**

EN/SYNC pin High Threshold Voltage	$V_{THH\_EN/SYNC}$	$V_{EN/SYNC} = L \rightarrow H$	1.6	-	$V^+$	V
EN/SYNC pin Low Threshold Voltage	$V_{THL\_EN/SYNC}$	$V_{EN/SYNC} = H \rightarrow L$	0	-	0.5	V
Input Bias Current (EN/SYNC pin)	$I_{EN/SYNC}$	$V_{EN/SYNC} = 12V$	-	235	340	$\mu A$

**Power Good Block**

High Level Detection Voltage	$V_{THH\_PG}$	Measured at FB pin	110	115	120	%
Low Level Detection Voltage	$V_{THL\_PG}$	Measured at FB pin	80	85	90	%
Hysteresis Region	$V_{HYS\_PG}$		-	2	-	%
Power Good ON Resistance	$R_{ON\_PG}$	$I_{PG} = 10mA$	-	45	60	$\Omega$
Leak Current at OFF State	$I_{LEAK\_PG}$	$V_{PG} = 6V$	-	-	0.1	$\mu A$

**General Characteristics**

Quiescent Current	$I_{DD}$	$R_L = \text{no load}, V_{FB} = 0.9V$	-	3.5	4.2	mA
Standby Current	$I_{DD\_STB}$	$V_{EN/SYNC} = 0V$	-	-	3	$\mu A$

## ■ THERMAL CHARACTERISTICS

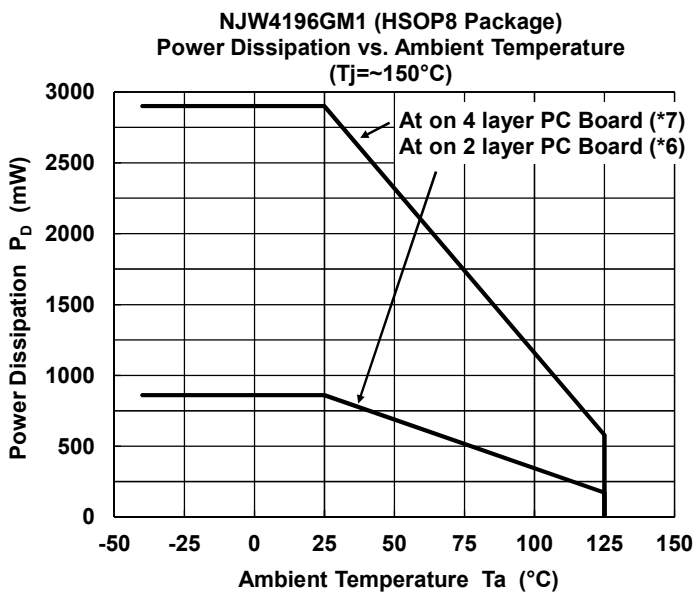
PARAMETER	SYMBOL	VALUE	UNIT
Junction-to-ambient thermal resistance	$\theta_{ja}$	145 <sup>(6)</sup>	°C/W
		43 <sup>(7)</sup>	
Junction-to-Top of package characterization parameter	$\psi_{jt}$	28 <sup>(6)</sup>	°C/W
		12 <sup>(7)</sup>	

(6): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 2Layers)

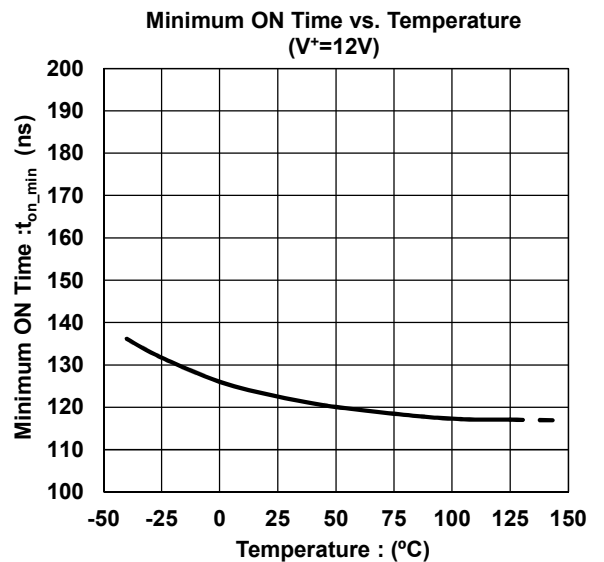
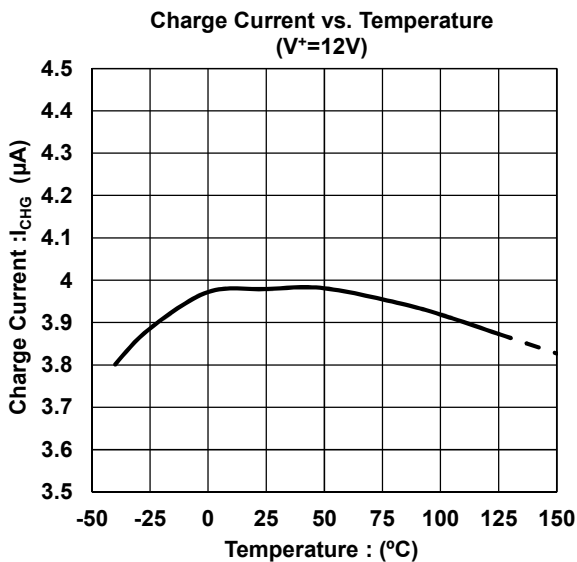
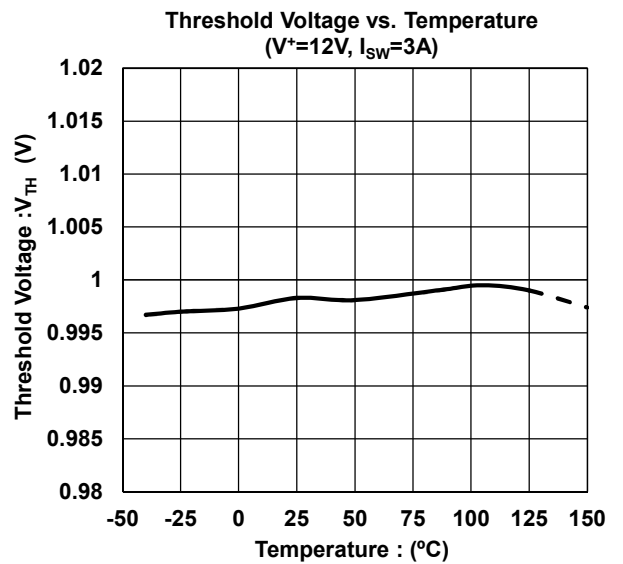
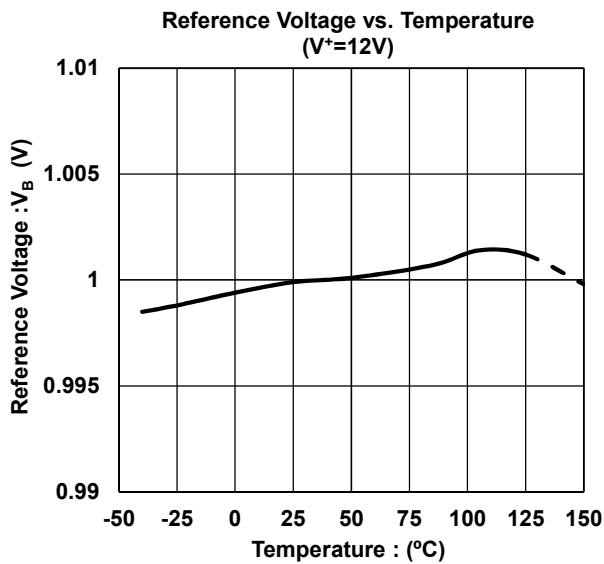
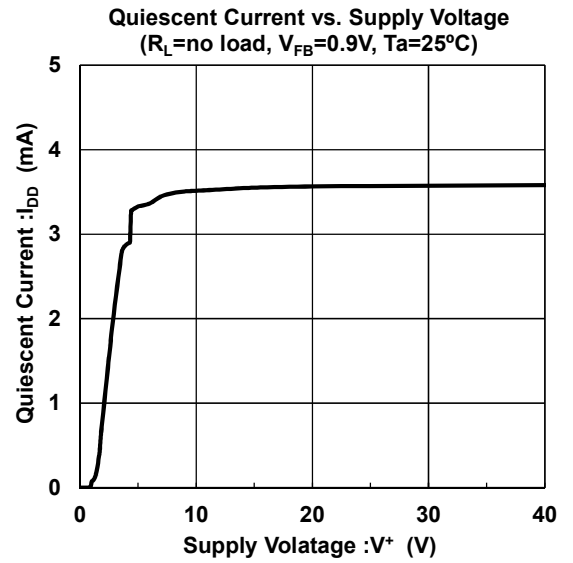
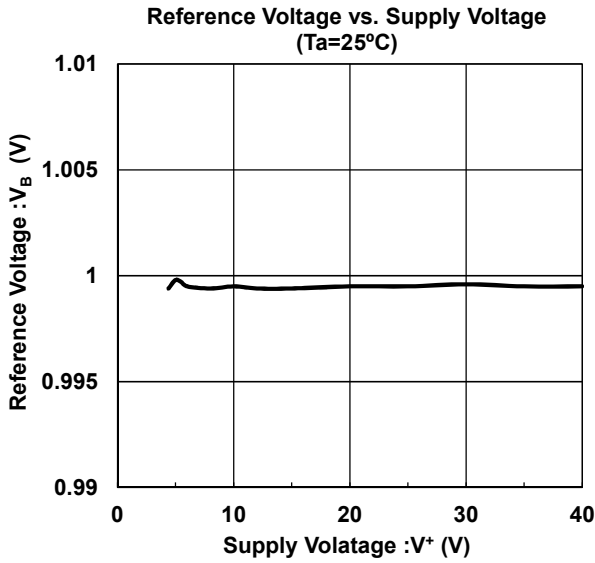
(7): Mounted on glass epoxy board. (76.2×114.3×1.6mm:based on EIA/JDEC standard, 4Layers)

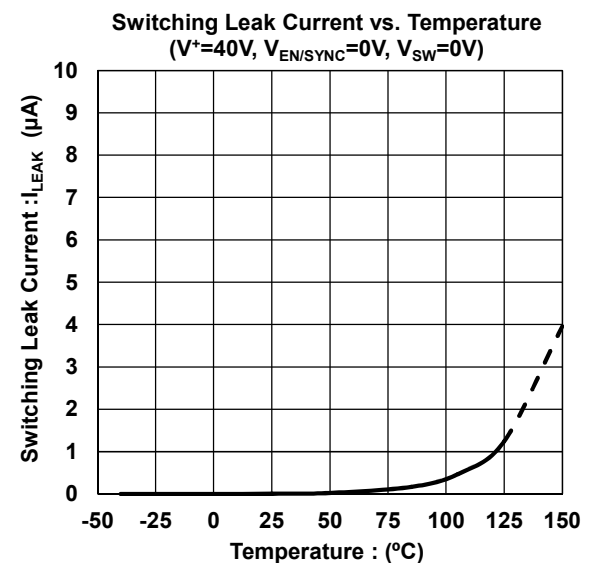
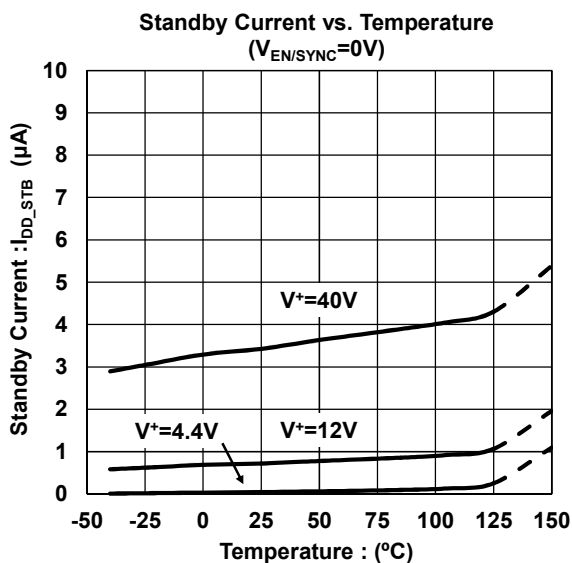
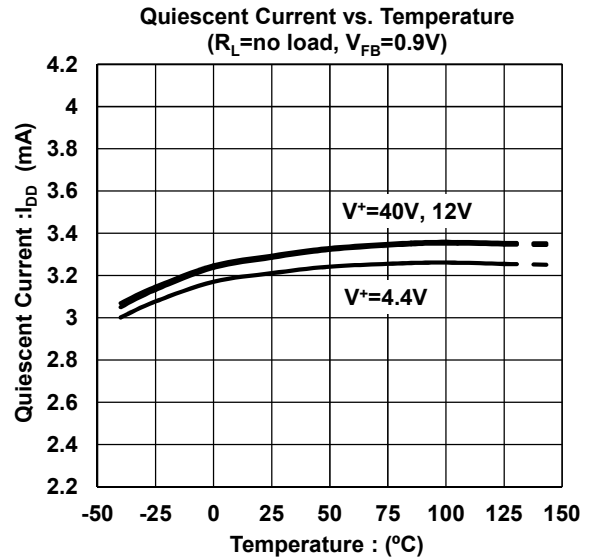
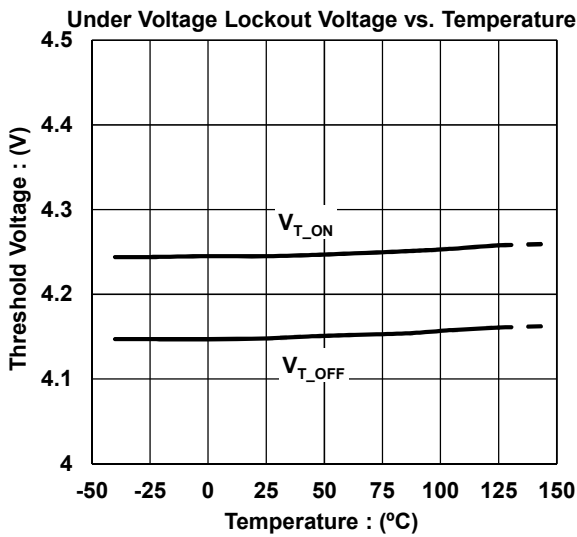
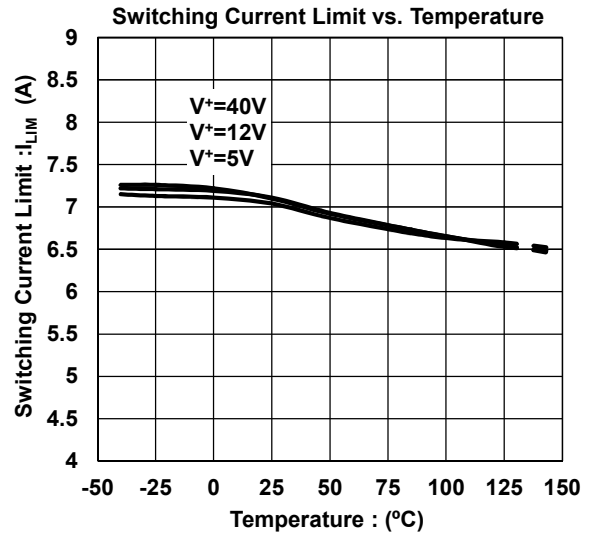
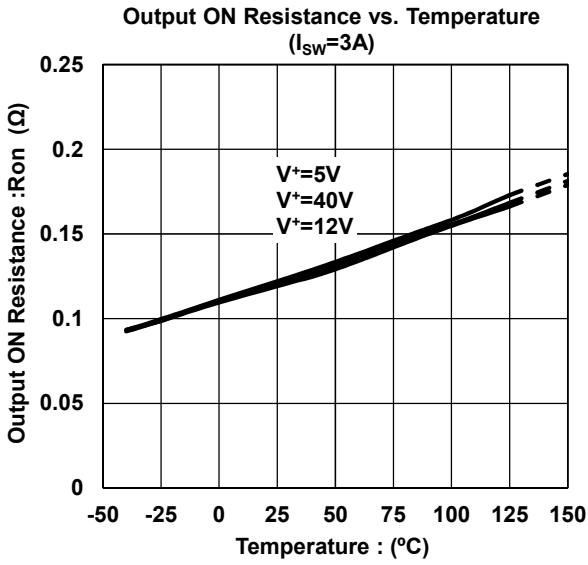
(For 4Layers: Applying 74.2×74.2mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5)

## ■ POWER DISSIPATION vs. AMBIENT TEMPERATURE

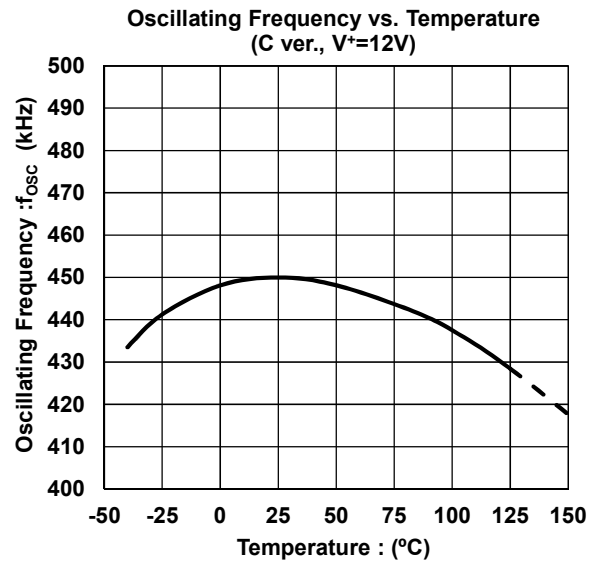
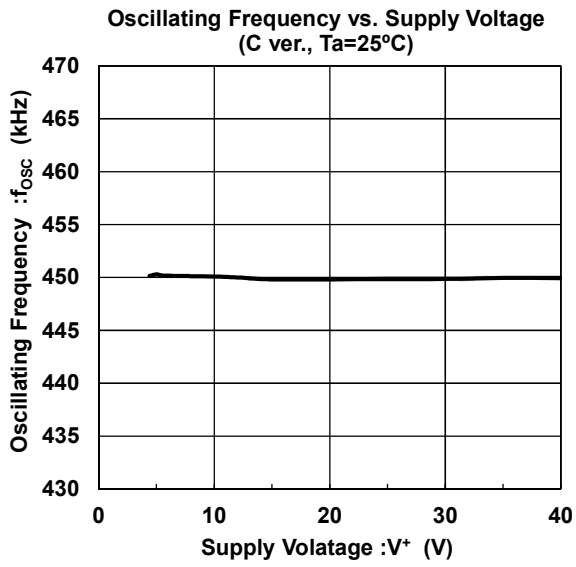


## ■ TYPICAL CHARACTERISTICS









## Technical Information

### ■DESCRIPTION OF BLOCK FEATURES

- Power MOSFET (SW Output Section)

The power is stored in the inductor by the switch operation of built-in power MOSFET. The output current is limited to 5A(min.) by overcurrent protection function. In case of buck converter, the forward direction bias voltage is generated with inductance current that flows into the external regenerative diode when MOSFET is turned off.

Although the SW pin accept a voltage between the V<sup>+</sup> pin and the SW pin up to +45V, use a Schottky diode that has low saturation voltage.

- Power Supply, GND pin (V<sup>+</sup> and GND)

In line with switching element drive, current flows into the IC according to frequency. If the power supply impedance provided to the power supply circuit is high, it will not be possible to take advantage of IC performance due to input voltage fluctuation. Therefore insert a bypass capacitor close to the V<sup>+</sup> pin – the GND pin connection in order to lower high frequency impedance.

- Under Voltage Lockout (UVLO)

The UVLO is released above ON Threshold Voltage (4.25V typ.) and IC operation starts. Then, supply voltage decrease below OFF Threshold Voltage (4.15V typ.), IC stops operate because the UVLO circuit . There is 100mV(typ.) width hysteresis voltage between detect and release.

Hysteresis prevents the malfunction near the UVLO threshold voltage.

- Soft Start Function (Soft Start)

The output voltage of the converter gradually rises to a set value by the soft start function.

The soft start time is adjustable by the capacitor C<sub>SS</sub> of the SS pin.

$$t_{SS} = C_{SS} \times \frac{1.0}{I_{CHG}} \text{ [s]}$$

I<sub>CHG</sub>: Soft Start Block Charge Current

When switching stopped by standby, UVLO, Hiccup by the OCP and TSD(Thermal Shut Down), NJW4196 discharges the capacitor of the SS pin.

When the rebooting, output voltage raises again with soft start.

# Technical Information

## DESCRIPTION OF BLOCK FEATURES (Continued)

### Over Current Protection Circuit (OCP)

NJW4196 contains hiccup type over current protection(OCP). The hiccup OCP circuit is able to decrease heat generation at the overload.

If a current exceeding  $I_{LIM}$  flows in the built-in power MOSFET, the power MOSFET is turned off by the OCP, and the switching operation is resumed at next cycle.

If the overcurrent detection continues for 128 pulses when the FB pin voltage is 0.5V or less, the switching operation stops.

When the FB pin voltage is 0.5V or lower(less), the switching operation stops after the overcurrent detection continued 128 pulses.

Then, after a cool-down time of about 75ms typ., restart with soft start.

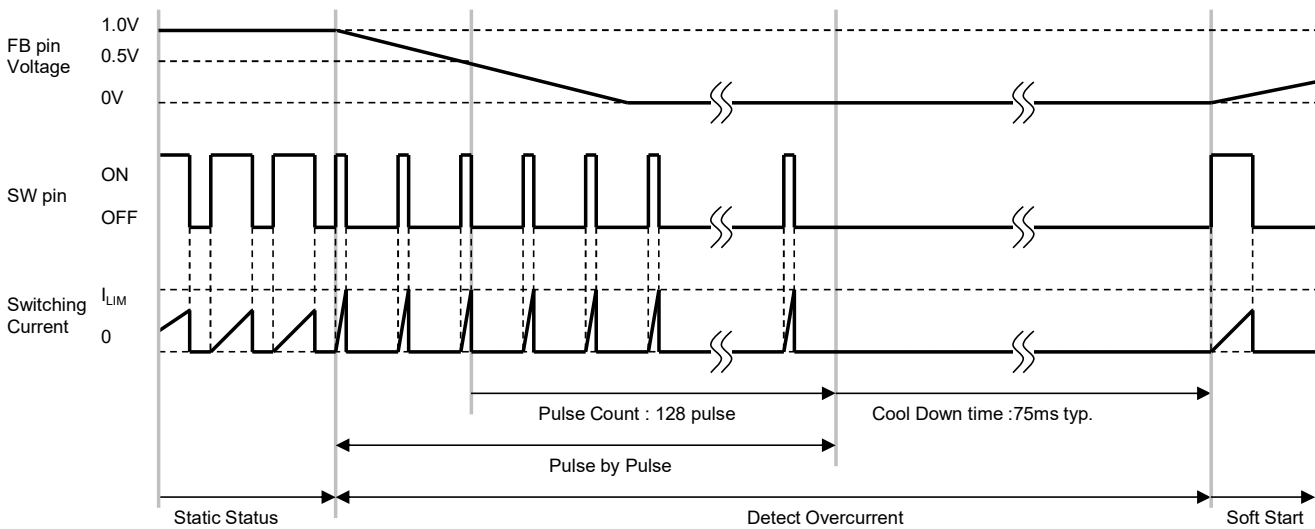


Fig. 1. Timing Chart at Over Current Detection

### Thermal Shutdown Function (TSD)

When Junction temperature exceeds the  $165^{\circ}\text{C}^*$ , thermal shutdown(TSD) circuit function stops SW function. When junction temperature decreases to  $145^{\circ}\text{C}^*$  or less, SW operation returns with soft start operation.

The TSD circuit is preliminary function to prevent malfunctioning of IC at the high junction temperature and is not intended to compensate for improper thermal design. It is recommended to operate within the IC junction temperature range (up to  $+150^{\circ}\text{C}$ ). \* Design value

### Standby Function

The NJW4196 stops the operating and becomes standby status when the EN/SYNC pin becomes less than 0.5V.

The EN/SYNC pin internally pulls down with  $500\text{k}\Omega$ , therefore the NJW4196 becomes standby mode when the EN/SYNC pin is OPEN. When not using the standby function, connect the EN / SYNC pin to  $V^+$ .

# Technical Information

## ■ DESCRIPTION OF BLOCK FEATURES (Continued)

### ● External Clock Synchronization

By inputting a square wave to EN/SYNC pin, can be synchronized to an external clock frequency.

The square wave must meet the specifications in Table 1.

Table 1. The input square wave to an EN/SYNC pin.

	C version ( $f_{OSC} = 450\text{kHz}$ )	J version ( $f_{OSC} = 100\text{k to } 1000\text{kHz}$ )
Input Frequency	440kHz to 600kHz	$f_{OSC} \times 0.9(250\text{kHz min.})$ to $f_{OSC} \times 1.3$
Duty Cycle	25% to 75%	40% to 60%
Voltage swing	1.6V or more at High level 0.5V or less at Low level	

Switching operation during external synchronization is triggered by the rising edge of the input signal.

In the standby state and switching between asynchronous operation and external synchronous operation, it is set to delay time of 30 $\mu\text{s}$  to prevent malfunction. (Fig. 2.)

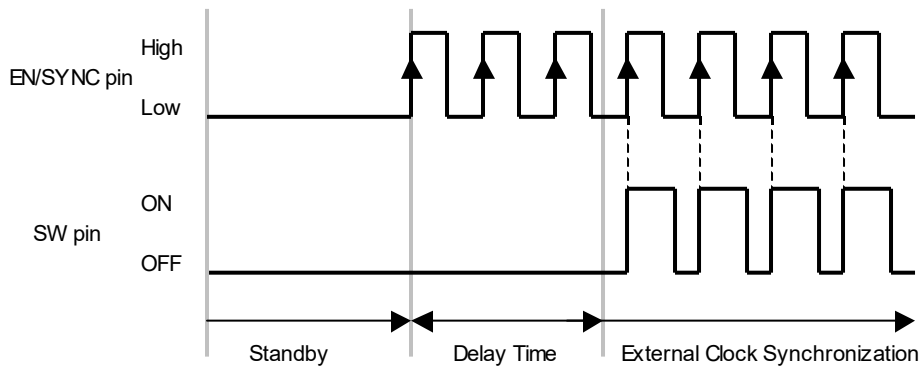


Fig. 2. Switching Operation by External Synchronized Clock

### ● Power Good Function

It monitors the output status and outputs a signal from PG pin that internally connected to open drain MOSFET.

The PG pin goes high impedance when the FB pin voltage is stable around reference voltage  $1.0\text{V} \pm 15\%$  (typ.) When the FB pin voltage is out of the range of  $1.0\text{V} \pm 15\%$ , the PG pin goes low.

In order to prevent malfunction of the power good output, it is set to 2.0% typ. of hysteresis and a delay time of 20 $\mu\text{s}$ -30 $\mu\text{s}$  for the FB pin voltage changes.

## Technical Information

### ■ Application Information

#### ● Oscillating Frequency Setting

When the switching frequency is high, the application can use a small inductor and capacitor. However, it should be considered reducing application efficiency and limiting minimum ON time.

The J version of NJW4196 sets the oscillating frequency by connecting a resistor between the RT pin and GND.

Figure 3 shows the oscillating frequency vs. timing resistance characteristics. Set the oscillation frequency between 100kHz and 1000kHz.

In addition, since the minimum ON time ( $t_{ON-min}$ ) of NJW4196 is set to 125ns typ., It is necessary to select an oscillating frequency at which the ON time of the buck converter circuit is 125ns typ. or more.

The ON time of the buck converter circuit is determined by the following equation.

$$t_{on} = \frac{V_{OUT}}{V_{IN} \times f_{OSC}} [s]$$

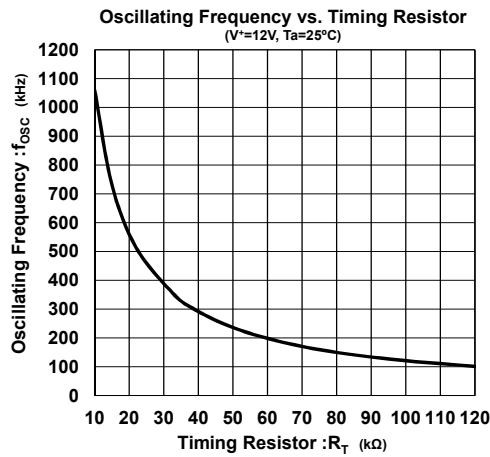


Fig.3. Oscillating frequency vs. timing resistor

## Technical Information

### ■ Application Information (Continued)

#### ● Inductors

Since large current flows through the inductor, it must have a current capability that does not saturate.

In case of NJW4196, optimized inductor value is determined by the input voltage and output voltage.

As the L value decreases, the peak current for the output current increases and conversion efficiency tends to decrease.

(Fig. 4.) Also note that the output current is limited so that the overcurrent limit is not exceeded.

The peak current is decided the following equation.

$$\Delta I_L = \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{L \times V_{IN} \times f_{OSC}} \text{ [A]}$$

$$I_{pk} = I_{OUT} + \frac{\Delta I_L}{2} \text{ [A]}$$

The optimum value varies depending on the application specifications, parts, etc., so make fine adjustments with the actual machine.

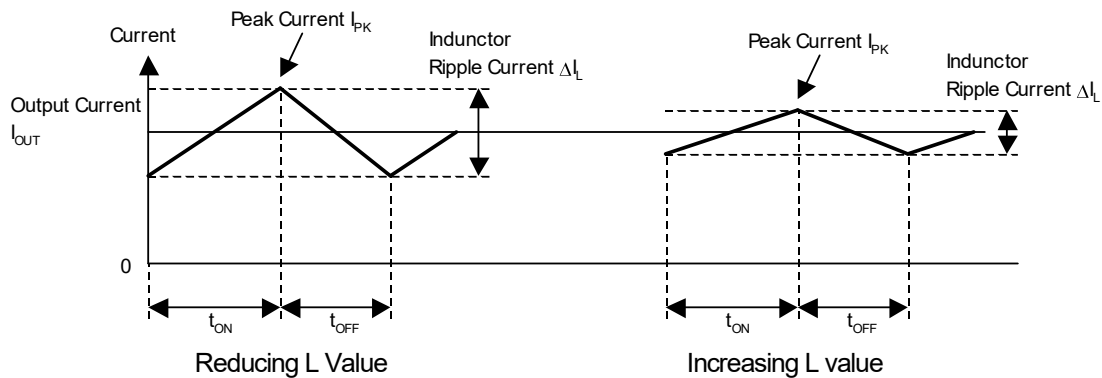


Fig. 4. Inductor Current State Transition (Continuous Conduction Mode)

## Technical Information

### ■ Application Information (Continued)

#### ● Input Capacitor

In the input section of switching regulator, flows transient current according to oscillation frequency. If the power supply impedance is large, the input voltage will fluctuate and the NJW4196 may not deliver good performance.

Therefore, insert the input capacitor as close to the IC as possible. A ceramic capacitor is the optimal for input capacitor.

The effective input current can be calculated by the following equation.

$$I_{\text{RMS}} = I_{\text{OUT}} \times \frac{\sqrt{V_{\text{OUT}} \times (V_{\text{IN}} - V_{\text{OUT}})}}{V_{\text{IN}}} \text{ [A]}$$

In the above equation, the maximum current is obtained when  $V_{\text{IN}} = 2 \times V_{\text{OUT}}$ , and the result in this case is

$$I_{\text{RMS}} = I_{\text{OUT (MAX)}} \div 2.$$

When selecting the input capacitor, use one with sufficient margin after evaluation.

#### ● Output Capacitor

An output capacitor stores power from the inductor, and stabilizes voltage provided to the output.

NJW4196 corresponds to a low ESR (Equivalent Series Resistance) output capacitor, so the ceramic capacitor is the optimal for compensation.

When selecting an output capacitor, it is necessary to consider the ESR characteristics, ripple current and maximum voltage. If it is a low ESR type capacitor, the ripple voltage can be lowered.

The ripple voltage can be calculated by the following equation.

$$V_{\text{ripple(p-p)}} = \Delta I_L \times \left( \text{ESR} + \frac{1}{8 \times f_{\text{OSC}} \times C_{\text{OUT}}} \right) \text{ [V]}$$

The effective ripple current that flows in a capacitor ( $I_{\text{rms}}$ ) is calculated by the following equation.

$$I_{\text{rms}} = \frac{\Delta I_L}{2\sqrt{3}} \text{ [Arms]}$$

Since a ceramic capacitor capacitance decreases due to DC voltage application or temperature change, check the characteristics with a spec sheet.

## Technical Information

### ■ Application Information (Continued)

#### ● Catch Diode

When the power MOSFET is in OFF cycle, the power stored in the inductor flows to output capacitor through the catch diode. Therefore, a current corresponding to the load current flows through the diode every cycle. Because diode's forward saturation voltage and current accumulation cause power loss, a Schottky Barrier Diode (SBD) which has a low forward saturation voltage is ideal.

A SBD also has a short reverse recovery time. If the reverse recovery time becomes longer, through current will flow at the power MOSFET switches to ON cycle from OFF cycle. This current may reduce efficiency and cause noise.

#### ● Setting Output Voltage, Noise Bypass Capacitor

The output voltage is determined by the relative resistances of R1 and R2. The current flowing through R1 and R2 should be large enough to ignore the bias current.

$$V_{\text{OUT}} = \left( \frac{R2}{R1} + 1 \right) \times V_B \text{ [V]}$$

Connect C1=100pF to 1,000pF to an FB pin as a noise bypass capacitor.

R2 and C<sub>FB</sub> form a zero (f<sub>Z1</sub>) and compensate for the phase of the switching regulator.

The pole generated by the noise bypass capacitor is compensated by R2 and C<sub>FB</sub>.

$$f_p = \frac{1}{2 \times \pi \times R1 \times C1} \text{ [Hz]}$$

$$f_{z1} = \frac{1}{2 \times \pi \times R2 \times C_{FB}} \text{ [Hz]}$$

Adjust with the actual machine so that it becomes  $0.5 < \frac{f_{z1}}{f_p} < 2.5$ .



## Technical Information

### ■ Application Information (Continued)

#### ● Board Layout

The switching regulator supplies power to the load by charging and discharging the inductor

In the switching regulator application, because the current flow corresponds to the oscillation frequency, the substrate (PCB) layout becomes an important.

You should attempt the transition voltage decrease by making a current loop area minimize as much as possible. Therefore, you should make a current flowing line thick and short as much as possible. Fig.5. shows a current loop at buck converter. Especially, should lay out high priority the loop of  $C_{IN}$ -SW-SBD that occurs rapid current change in the switching. It is effective in reducing noise spikes caused by parasitic inductance.

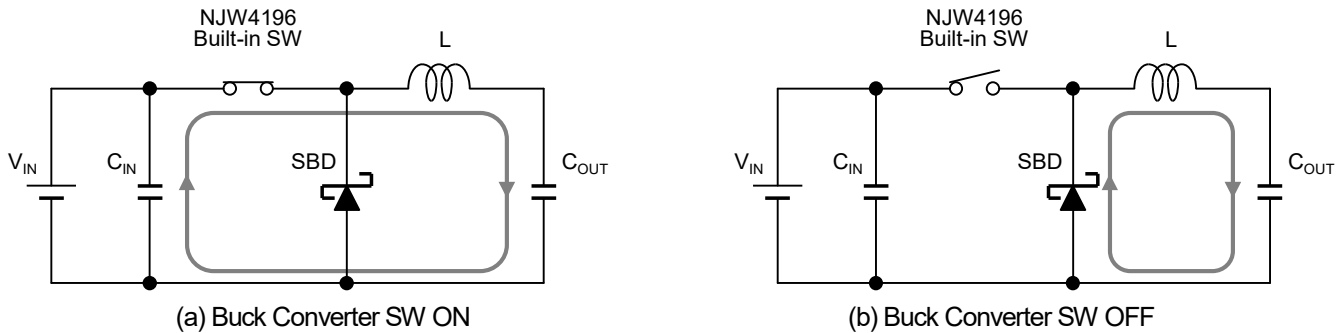


Fig. 5. Current Loop at Buck Converter

Concerning the GND line, it is preferred to separate the power system and the signal system, and use single ground point.

The voltage sensing feedback line should be as far away as possible from the inductance. Because this line has high impedance, it is laid out to avoid the influence noise caused by flux leaked from the inductance.

Fig. 6. shows example of wiring at buck converter.

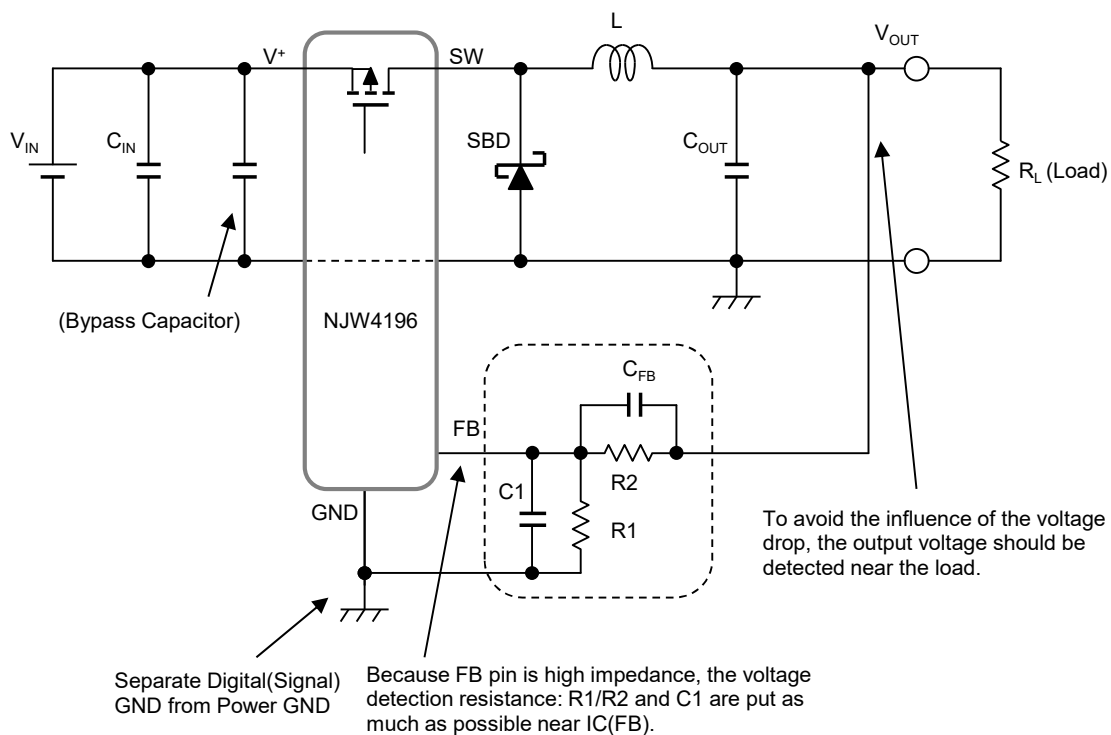


Fig. 6. Board Layout at Buck Converter

## Technical Information

### ■ Calculation of Package Power

A lot of the power consumption of buck converter occurs from the internal switching element (Power MOSFET). Power consumption of NJW4196 is roughly estimated as follows.

$$\begin{aligned} \text{Input Power:} & \quad P_{\text{IN}} = V_{\text{IN}} \times I_{\text{IN}} \quad [\text{W}] \\ \text{Output Power:} & \quad P_{\text{OUT}} = V_{\text{OUT}} \times I_{\text{OUT}} \quad [\text{W}] \\ \text{Diode Loss:} & \quad P_{\text{DIODE}} = V_{\text{F}} \times I_{\text{L(avg)}} \times \text{OFF duty} \quad [\text{W}] \\ \text{NJW4196 Power Consumption:} & \quad P_{\text{LOSS}} = P_{\text{IN}} - P_{\text{OUT}} - P_{\text{DIODE}} \quad [\text{W}] \end{aligned}$$

Where:

$V_{\text{IN}}$	: Input Voltage for Converter	$I_{\text{IN}}$	: Input Current for Converter
$V_{\text{OUT}}$	: Output Voltage of Converter	$I_{\text{OUT}}$	: Output Current of Converter
$V_{\text{F}}$	: Diode's Forward Saturation Voltage	$I_{\text{L(avg)}}$	: Inductor Average Current
OFF duty	: Switch OFF Duty		

Efficiency ( $\eta$ ) is calculated as follows.

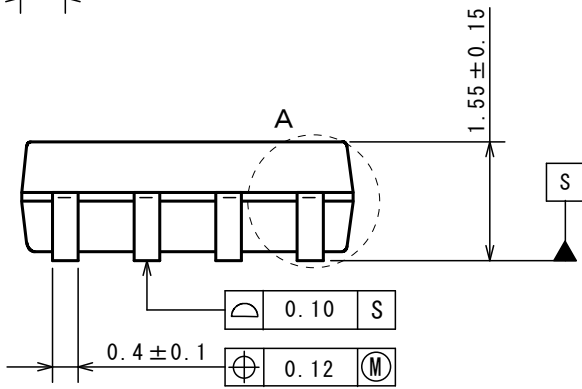
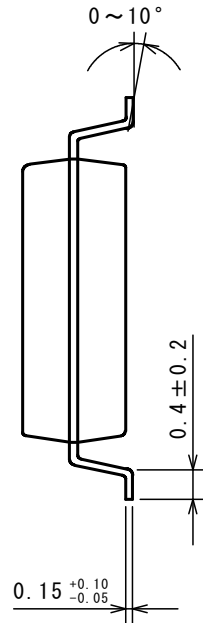
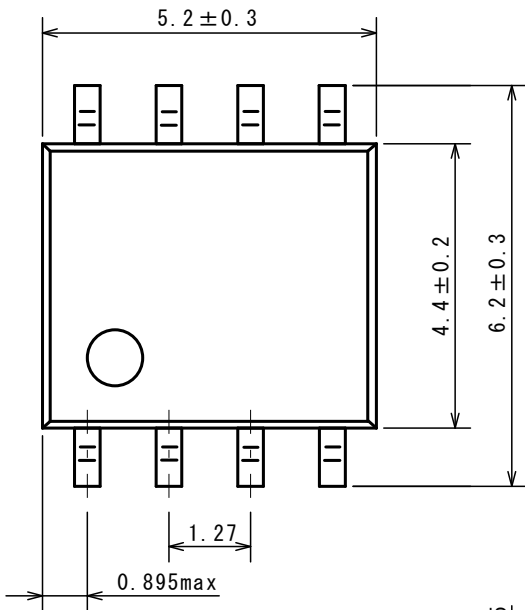
$$\eta = (P_{\text{OUT}} \div P_{\text{IN}}) \times 100 \quad [\%]$$

You should consider temperature derating to the calculated power consumption:  $P_{\text{D}}$ .

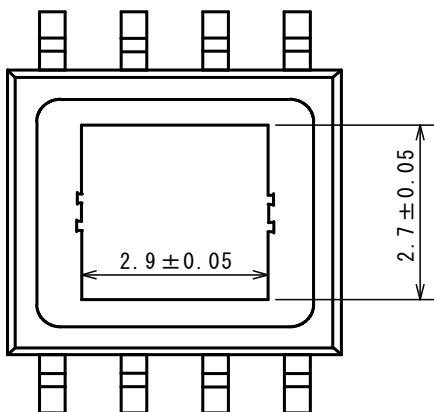
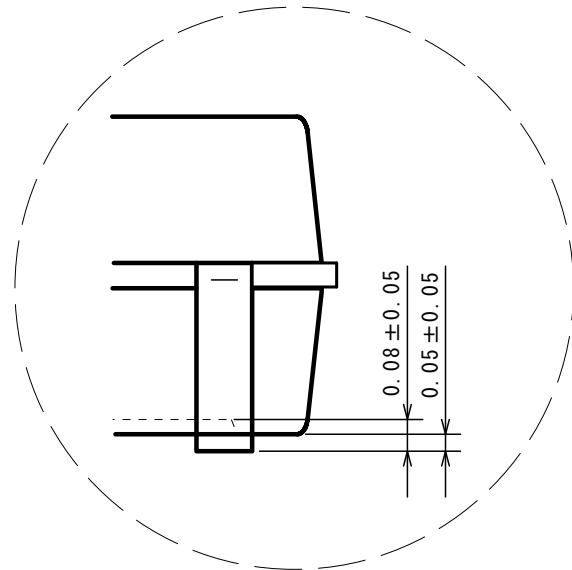
You should design power consumption in rated range referring to the power dissipation vs. ambient temperature characteristics.

### PACKAGE OUTLINE

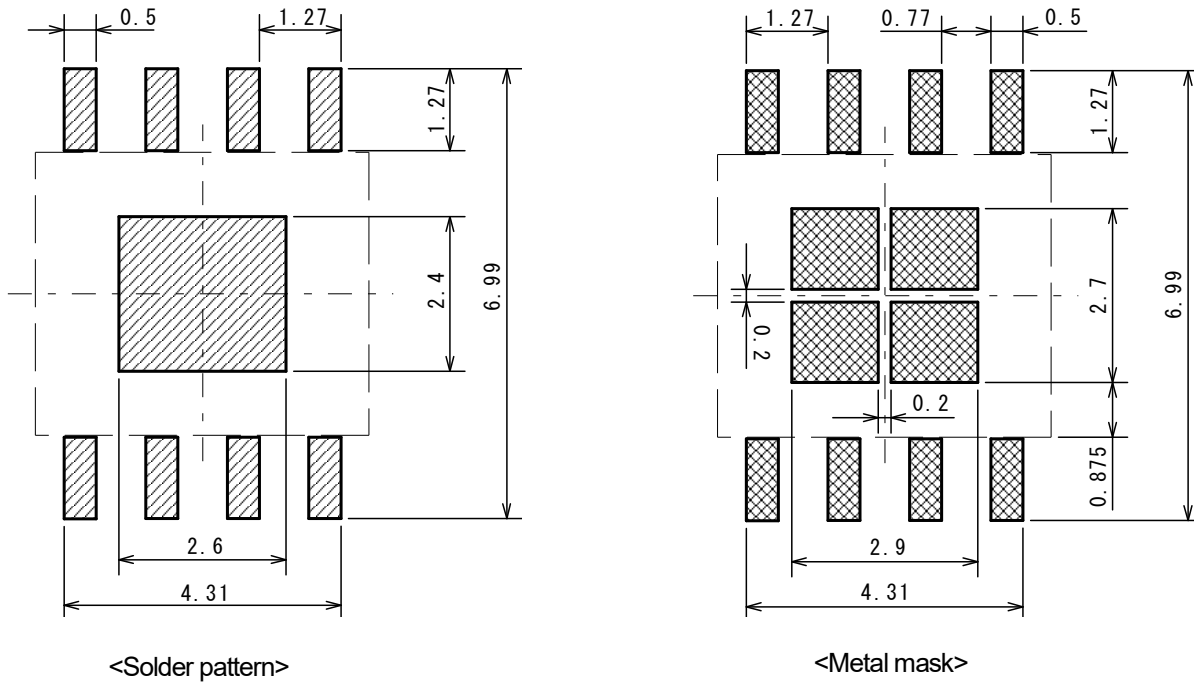
Unit: mm



Detail drawing of part A



### EXAMPLE OF SOLDER PADS DIMENSIONS



### <Instructions for mounting>

Please note the following points when you mount HSOP-8 package IC because there is a standoff on the backside electrode.

(1) Temperature profile of lead and backside electrode.

It is necessary that both re-flow temperature profile of lead and backside electrode are higher than preset temperature.

When solder wet temperature is lower than lead/backside electrode temperature, there is possibility of defect mounting.

(2) Design of foot pattern / metal mask

Metal mask thickness of solder pattern print is more than 0.13mm.

(3) Solder paste

The mounting was evaluated with following solder paste, foot pattern and metal mask.

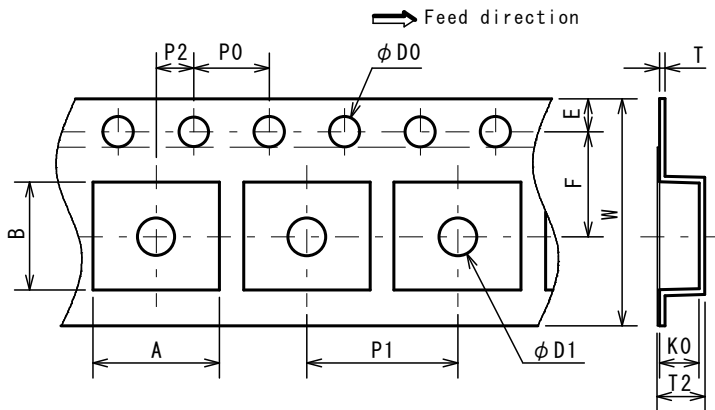
Because mounting might be greatly different according to the manufacturer and the product number even if the solder composition is the same.

We will strongly recommend to evaluate mounting previously with using foot pattern, metal mask and solder paste.

Solder paste composition	Sn37Pb (Senju Metal Industry Co., Ltd: OZ7053-340F-C)
	Sn3Ag0.5Cu (Senju Metal Industry Co., Ltd: M705-GRN350-32-11)

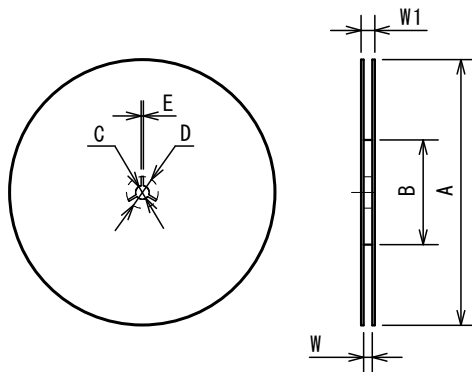
### PACKING SPEC

#### TAPING DIMENSIONS



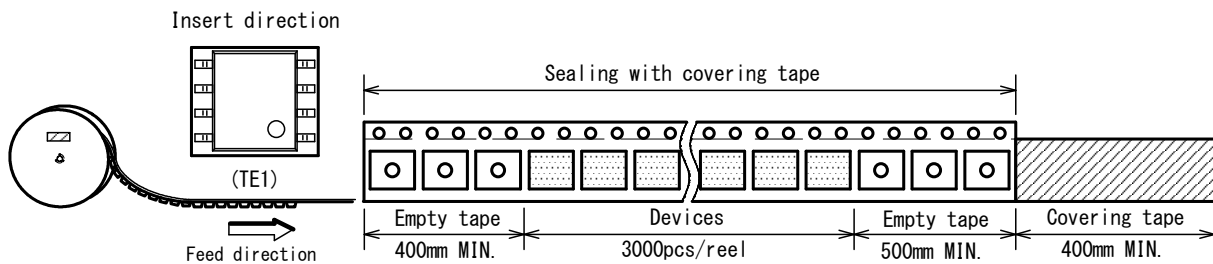
SYMBOL	DIMENSION	REMARKS
A	6.7±0.1	
B	5.55±0.1	
D0	1.55±0.05	
D1	2.05±0.05	
E	1.75±0.1	
F	5.5±0.05	
P0	4.0±0.1	
P1	8.0±0.1	
P2	2.0±0.05	
T	0.3±0.05	
T2	2.47	
K0	2.1±0.1	
W	12.0±0.2	

#### REEL DIMENSIONS

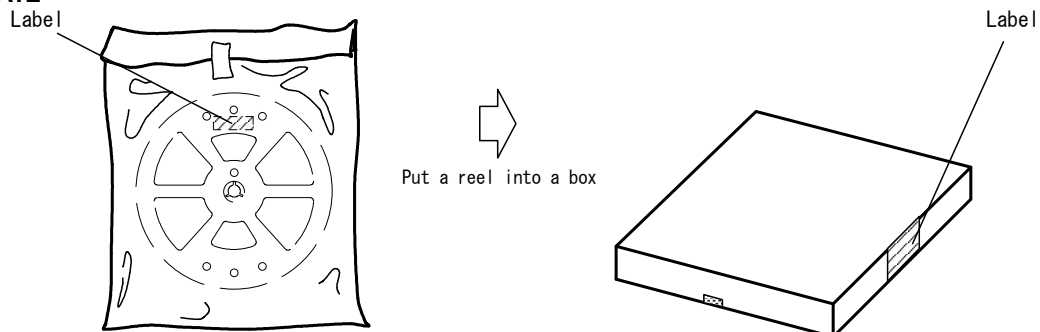


SYMBOL	DIMENSION
A	φ 330±2
B	φ 80±1
C	φ 13±0.2
D	φ 21±0.8
E	2±0.5
W	13.5±0.5
W1	17.5±1

#### TAPING STATE



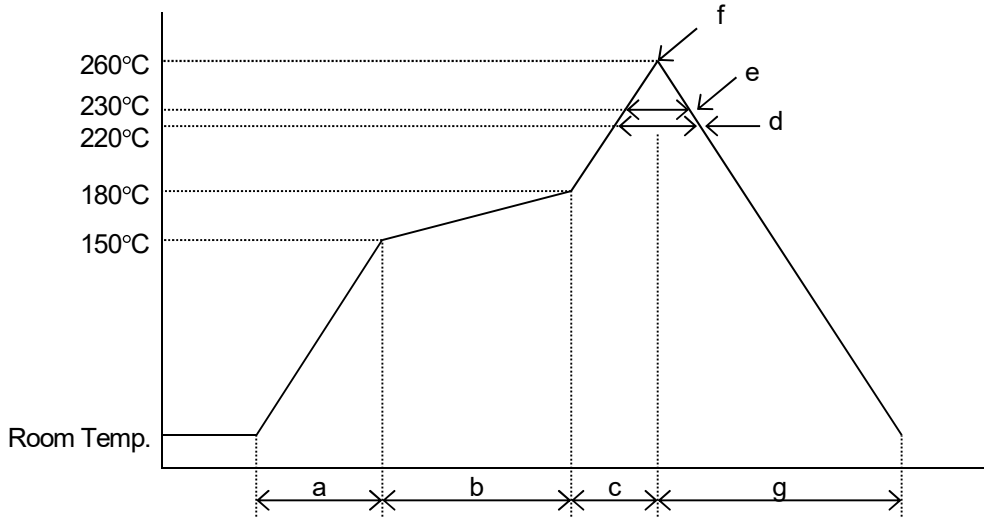
#### PACKING STATE



■ **RECOMMENDED MOUNTING METHOD**  
**INFRARED REFLOW SOLDERING METHOD**

EAE-D1006-000-02

\* Recommended reflow soldering procedure



- |                                 |                                |
|---------------------------------|--------------------------------|
| a: Temperature ramping rate     | : 1 to 4°C/s                   |
| b: Pre-heating temperature time | : 150 to 180°C<br>: 60 to 120s |
| c: Temperature ramp rate        | : 1 to 4°C/s                   |
| d: 220°C or higher time         | : Shorter than 60s             |
| e: 230°C or higher time         | : Shorter than 40s             |
| f: Peak temperature             | : Lower than 260°C             |
| g: Temperature ramping rate     | : 1 to 6°C/s                   |

The temperature indicates at the surface of mold package.

**■REVISION HISTORY**

Date	Revision	Changes
29. Nov.2019.	Ver.1.0	New Release C version and J version

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