Low phase noise Fundamental Quartz Crystal Oscillator IC

■FEATURES(V_{DD}=3.3V, f=49.152MHz, Ta=25°C)

- ●Oscillation Frequency 20MHz to 50MHz(Fundamental)
- ●Phase noise -103dBc/Hz(Typ.) @10Hz Offset
  -163dBc/Hz(Typ.) @1kHz Offset
- ●RMS Jitter 0.05psec(Typ.) @12kHz to 20MHz
- ●Operating Voltage 1.62V to 3.63V
- ●Operating Current 3.1mA(Typ.) @49.152MHz, C_L=15pF
- ●Built In Divider f_0, f_0/2 (Factory set)
- ●Stand-by Function (CONT Terminal: L)
  Oscillation Stop and High Impedance F_{OUT} terminal.
- ●3-State Output Buffer
- ●Built-in Variable Pull-up Resistance (CONT: Pull-up Resistance large at the Stand-by mode.)
- ●Oscillation Capacitors Cg and Cd
- ●Operation Temperature -40°C to 125°C
- ●Package Outline Die / 8-inch wafer

■GENERAL DESCRIPTION

The NJU6222 series is a C-MOS quartz crystal oscillator IC (20MHz to 50MHz) realized very low phase noise. It is consisted of an oscillation amplifier, divider (f_0, f_0/2), and 3-state output buffer.
There are 2-type of pad location for Flip chip and Wire bonding that apply SMD's 2016-package and more miniature.
The NJU6222 in low voltage operation features low phase noise, it is suitable for high quality Hi-Fi sound device, Communication device, and others by battery drive.

■APPLICATION

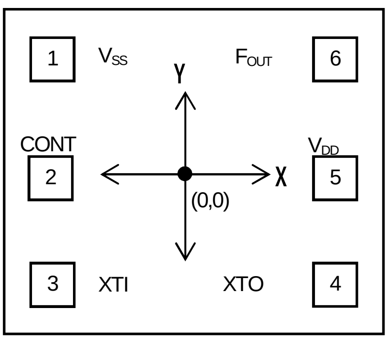
- ●Low Noise Crystal Oscillator

■LINE-UP TABLE

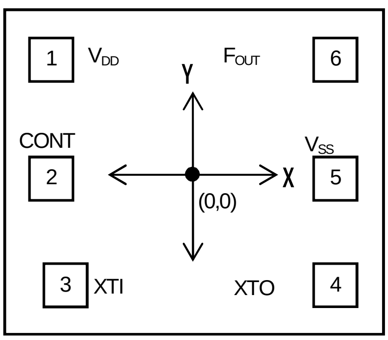
Type No	F_{OUT}	Version	
		Type A	Type C
NJU6222	f_0	A1	C1
	f_0/2	A2	C2

■PAD LOCATION

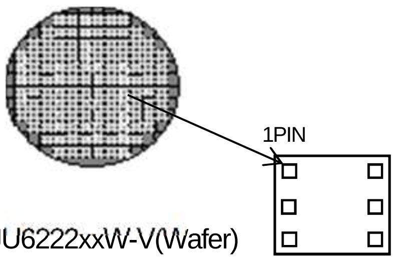
A Type
(For Flip Chip Assembly)



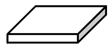
C Type
(For Wire Bonding Assembly)



■PACKAGE OUTLINE



NJU6222xxW-V(Wafer)



NJU6222xxC-V(Die)

■CORDINATES

Pad No.	X	Y
1	-174	190
2	-186	0
3	-174	-190
4	174	-190
5	186	0
6	174	190

Starting Point: Die Center Unit[µm]
Die Size: 0.580x0.588mm
Die Thickness (C-V): 130 ± 15µm
Wafer Thickness (W-V): 130 ± 20µm
Pad size: 80x80µm
Die Substrate: V_{SS} level

■PRODUCT NUMBER

NJU6222 □□ □-□

- NJU6222: Part Number
- □□: Version
- □-□: W-V :Wafer 130µm / C-V :Die 130µm

■ORDER INFORMATION

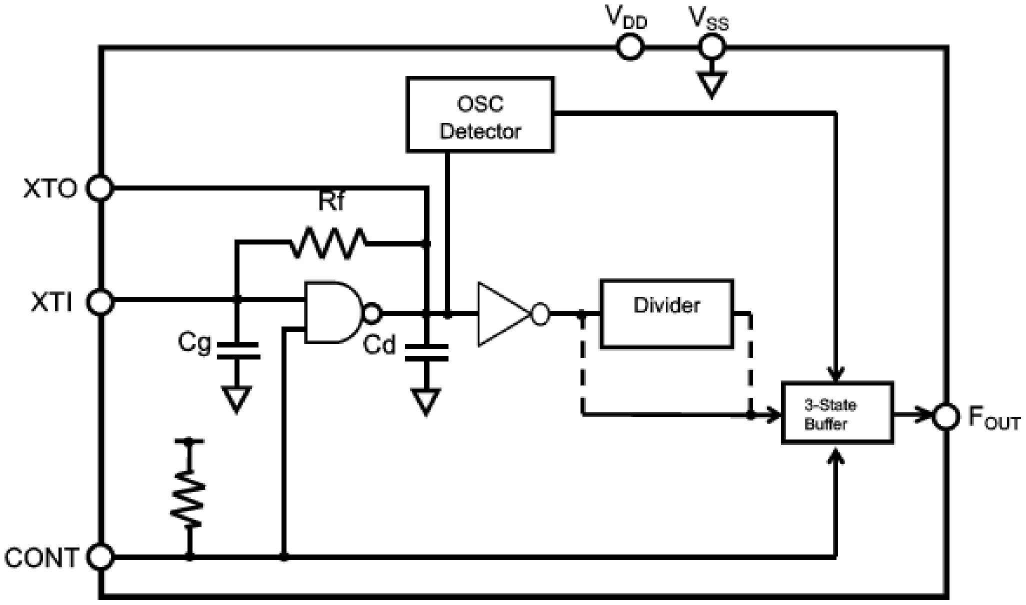
TYPE No.	OUT LINE	MOQ
NJU6222 A x W -V	Wafer	1Wafer (Around 75000pcs)
NJU6222 C x W -V		
NJU6222 A x C - V	Die	75000pcs (5000pcs x 15pack)
NJU6222 C x C - V		5000pcs/pack

■TERMINAL DISCREPTION

SYMBOL	FUNCTION
CONT	Oscillation and 3-state Output Buffer Control CONT / F_{OUT}: H or OPEN: Output one frequency selected out of f_0 and f_0/2 Note1) L: Oscillation Stop and High impedance Output
XTI	Quartz Crystal Connection terminals
XTO	
V_{SS}	GND terminal (V_{SS}=0V)
F_{OUT}	Frequency Output terminal (3-State Output Buffer)
V_{DD}	Power Supply terminal V_{DD}=1.62 to 3.63V

Note 1) Refer to the line-up table.

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{DD}	-0.6 to 6.0	V
Input Voltage	V_{IN}	-0.6 to $+V_{DD}$+0.6 and ≦6.0V	V
Output Voltage	V_O	-0.6 to V_{DD}+0.6	V
Input Current	I_{IN}	±10	mA
Output Terminal Current	I_O	±25	mA
Storage Temperature Range	T_{stg}	- 55 to 150	°C
Maximum Junction Temperature	T_{jmax}	150	°C

Note2) If the LSI used condition above the absolute maximum ratings, the LSI may be destroyed.
Use beyond the electric characteristics conditions will cause mal-function and poor reliability.

■RECOMMEND OPERATING CONDITIONS

PARAMETER	SYMBOL	CONDITIONS	VALUE	UNIT
Supply Voltage	V_{DD}	Ta=25°C	1.62 to 3.63	V
Operating Temperature Range	T_{opr}		-40 to 125	°C
Input Voltage	V_{IN}	CONT	0 to 3.63	V
Output Voltage	V_{OUT}	F_{OUT}	0 to V_{DD}	V
Output Frequency	df/f	$V_{DD}\pm10\%$	±1	ppm

■ELECTRICAL CHARACTERISTICS

(V_{DD}=1.62 to 3.63V, V_{SS}=0V, Ta=25°C)

PARAMETER	SYMBOL	TEST CONDITION		MIN	TYP	MAX	UNIT
Operating Current	I_{DD}	x1 version (f_0) No load TEST CIRCUIT (1)(3) f_0=49.152MHz Fout=49.152MHz	V_{DD}=1.8V	-	1.8	2.9	mA
			V_{DD}=2.5V	-	3.3	4.8	
			V_{DD}=3.3V	-	5.5	7.7	
		x2 version (f_0/2) No load TEST CIRCUIT (1)(3) f_0=49.152MHz Fout=24.576MHz	V_{DD}=1.8V	-	1.4	2.4	
			V_{DD}=2.5V	-	2.7	4.1	
			V_{DD}=3.3V	-	4.8	6.6	
		x1 version (f_0) C_L=15pF TEST CIRCUIT (1)(3) f_0=49.152MHz Fout=49.152MHz	V_{DD}=1.8V	-	3.1	4.1	
			V_{DD}=2.5V	-	5.1	6.6	
			V_{DD}=3.3V	-	7.9	9.9	
		x2 version CL=15pF TEST CIRCUIT (1)(3) f_0=49.152MHz Fout=24.576MHz	V_{DD}=1.8V	-	2.0	3.0	
			V_{DD}=2.5V	-	3.6	4.9	
			V_{DD}=3.3V	-	5.9	7.7	
Stand-by Current	I_{STB}	TEST CIRCUIT(1)(3) CONT=V_{SS}	V_{DD}=1.8V	-	3.0	25.0	μA
			V_{DD}=2.5V	-	5.0	30.0	
			V_{DD}=3.3V	-	9.0	35.0	
H Level Output Voltage	V_{OH}	TEST CIRCUIT(2)(3)		V_{DD}-0.4	-	-	V
L Level Output Voltage	V_{OL}	TEST CIRCUIT(2)(3)		-	-	0.4	V
H Level Input Voltage	V_{IH}	TEST CIRCUIT(3)(3)		0.7V_{DD}	-	-	V
L Level Input Voltage	V_{IL}	TEST CIRCUIT(3)(3)		-	-	0.3V_{DD}	V
Input Current	I_{IN}	TEST CIRCUIT(4)(3), V_{DD}=1.62V, CONT=V_{DD}		-	-	0.065	μA
		TEST CIRCUIT(4)(3), V_{DD}=1.62V, CONT=V_{SS}		-	-	-0.5	
		TEST CIRCUIT(4)(3), V_{DD}=3.63V, CONT=V_{DD}		-	-	0.150	
		TEST CIRCUIT(4)(3), V_{DD}=3.63V, CONT=V_{SS}		-10	-	-	
3-state off leakage current	I_{OZ}	TEST CIRCUIT(5)(3), F_{OUT}= V_{DD} or V_{SS}		-	-	±0.1	μA

(V_{DD}=1.62 to 3.63V, V_{SS}=0V, Ta=25°C)

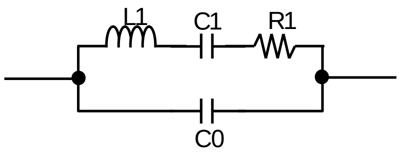
PARAMETER	SYMBOL	TEST CONDITION		MIN	TYP	MAX	UNIT
Feedback Resistance	Rf			-	50	-	kΩ
Built-In Oscillator Capacitance	Cg	f_{OSC}=50MHz		-	8	-	pF
	Cd	f_{OSC}=50MHz		-	17	-	pF
Oscillation Frequency	F_{OSC}	Recommendation(5)		-	-	50	MHz
Output Signal Symmetry	SYM	C_L=15pF, @V_{DD}/2		45	50	55	%
Phase Noise	SSB	x1 version (f_0) f_{OSC}=49.152MHz V_{DD}=1.8V	10Hz Offset	-	-103	-	dBc/Hz
			1kHz Offset	-	-158	-	
			Floor	-	-166	-	
		x1 version (f_0) f_{OSC}=49.152MHz V_{DD}=3.3V	10Hz Offset	-	-103	-	
			1kHz Offset	-	-163	-	
			Floor	-	-172	-	
Output Signal rise Time	tr	TEST CIRCUIT(1)(3) 0.1V_{DD} to 0.9V_{DD}	V_{DD}=1.8V	-	3.1	4.7	ns
			V_{DD}=2.5V	-	1.8	2.7	ns
			V_{DD}=3.3V	-	1.3	2.0	ns
Output Signal fall Time	tf	TEST CIRCUIT(1)(3) 0.9V_{DD} to 0.1V_{DD}	V_{DD}=1.8V	-	2.8	4.2	ns
			V_{DD}=2.5V	-	1.8	2.7	ns
			V_{DD}=3.3V	-	1.4	2.1	ns
Output Disable Time	t_{POZ}	TEST CIRCUIT (6)(3)		-	-	200	ns
Output Enable Time	t_{PZO}	TEST CIRCUIT (6)(3)		-	-	1.0	ms
Oscillation Start Up Time	t_{OSC}	TEST CIRCUIT (1)(3)		-	-	1.0	ms

Note 3) Decupling capacitor over than 0.01µF ceramic capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the circuit.

Note 4) The Phase noise characteristics is applied to NJU6222A1/C1 (f_0).

Note 5) NJR's standard crystal is used for measurement of the oscillation frequency range and it does not guarantee oscillation. (Refer to EXAMPLE OF CRYSTAL PARAMETERS FOR MEASUREMENT CIRCUITS)

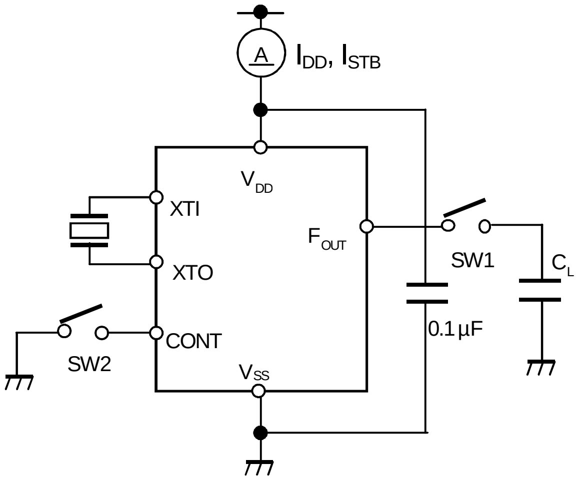
■**EXAMPLE OF CRYSTAL PARAMETERS FOR MEASUREMENT CIRCUITS**



f[MHz]	R1[Ω]	L1[mH]	C1[fF]	C0[pF]
49.152	17.7	3.83	2.74	1.23

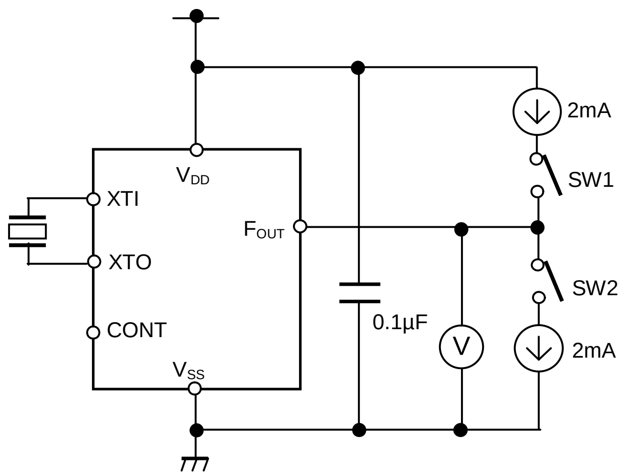
■TYPICAL TEST CIRCUIT

(1) Operating Current, Stand-by Current, Output Signal Symmetry, Output Signal rise / Fall Time, Oscillation Start-Up Time



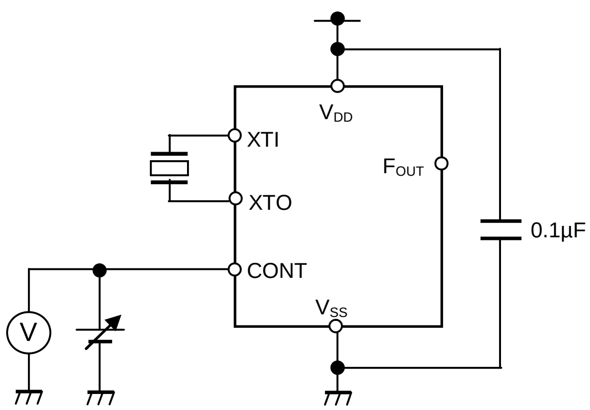
PARAMETER	SW1	SW2
I_{DD} (C_L=0pF)	OFF	OFF
I_{DD} (C_L=15pF)	ON	OFF
I_{STB}	ON or OFF	ON
SYM, tr, tf	ON	OFF
t_{OSC}	ON	OFF

(2) High-level / Low-level Output Voltage (V_{OH}/ V_{OL})



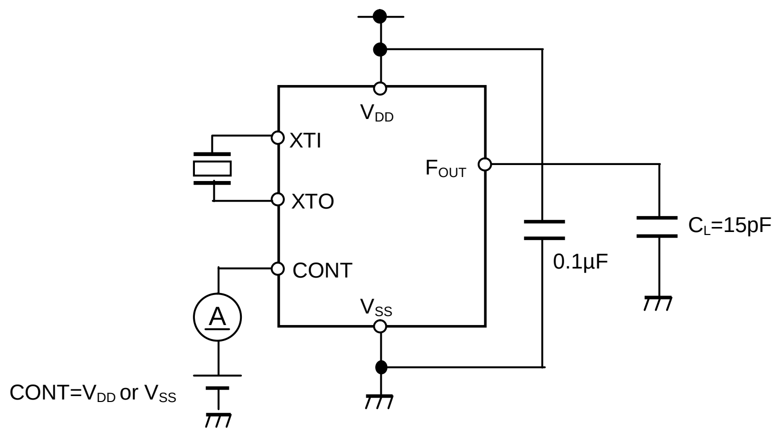
PARAMETER	SW1	SW2
V_{OH}	ON	OFF
V_{OL}	OFF	ON

(3) High-level / Low-level Input Voltage (V_{IH}/ V_{IL})

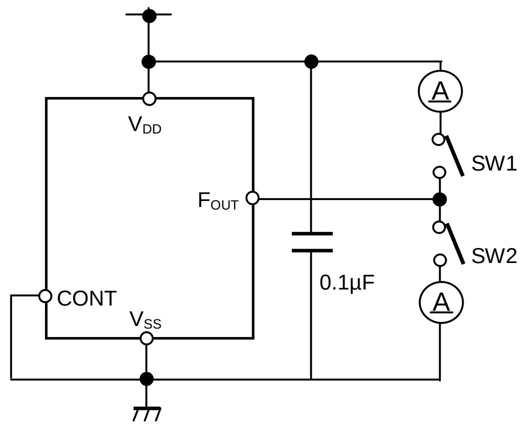


PARAMETER	F_{OUT}
CONT > $0.7V_{DD}$	Oscillation
CONT < $0.3V_{DD}$	Stop

(4) Input Current (I_{IN})

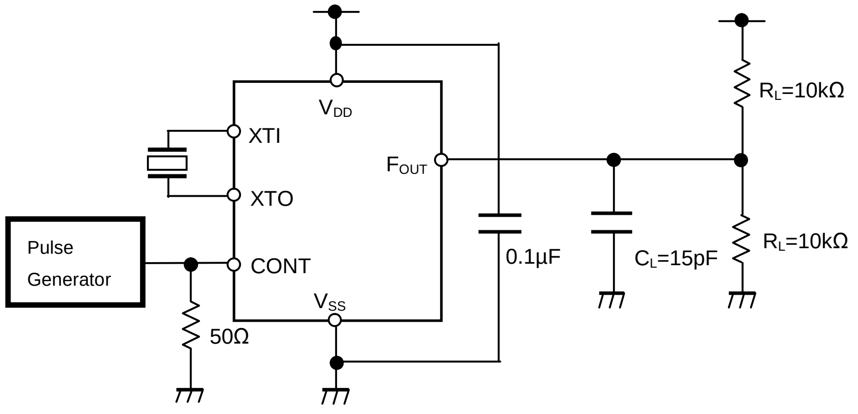


(5) 3-State Off Leakage Current (I_{IOZ})



PARAMETER	SW1	SW2
I_{OZH}	ON	OFF
I_{OZL}	OFF	ON

(6) Output Disable Time, Output Enable Time (T_{POZ}/T_{PZO})



■TIMING CHART

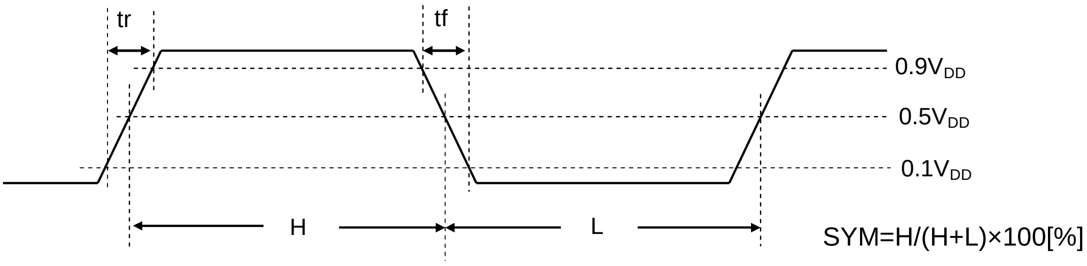


Fig.1 Output Signal Rise Time: tr, Output Signal Fall Time: tf, Output Symmetry: SYM

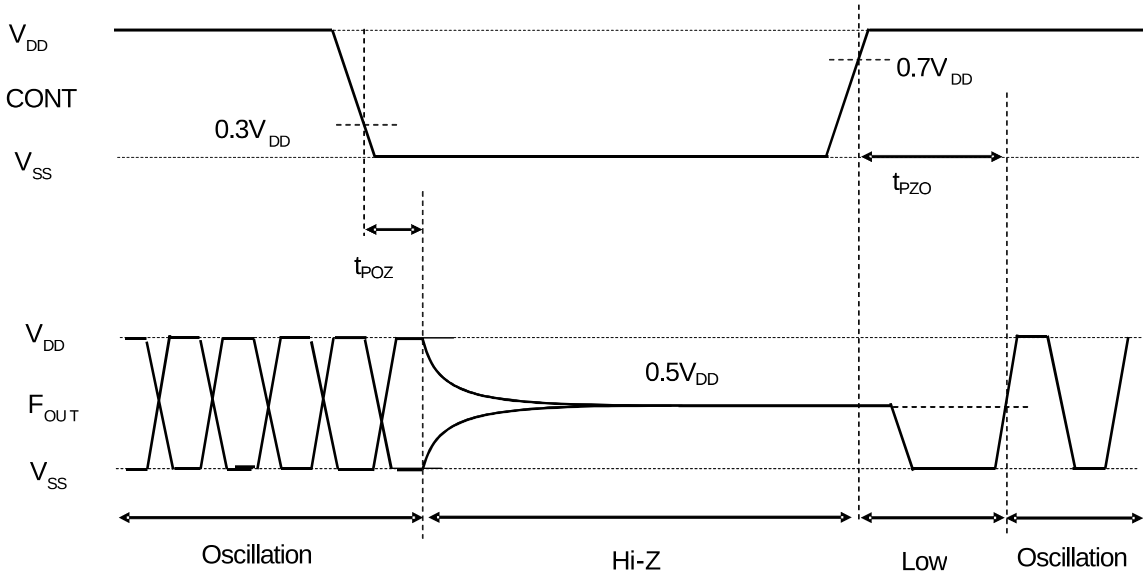


Fig.2 Output Disable time: t_{POZ}, Output Enable time: t_{PZO}, Timing Chart

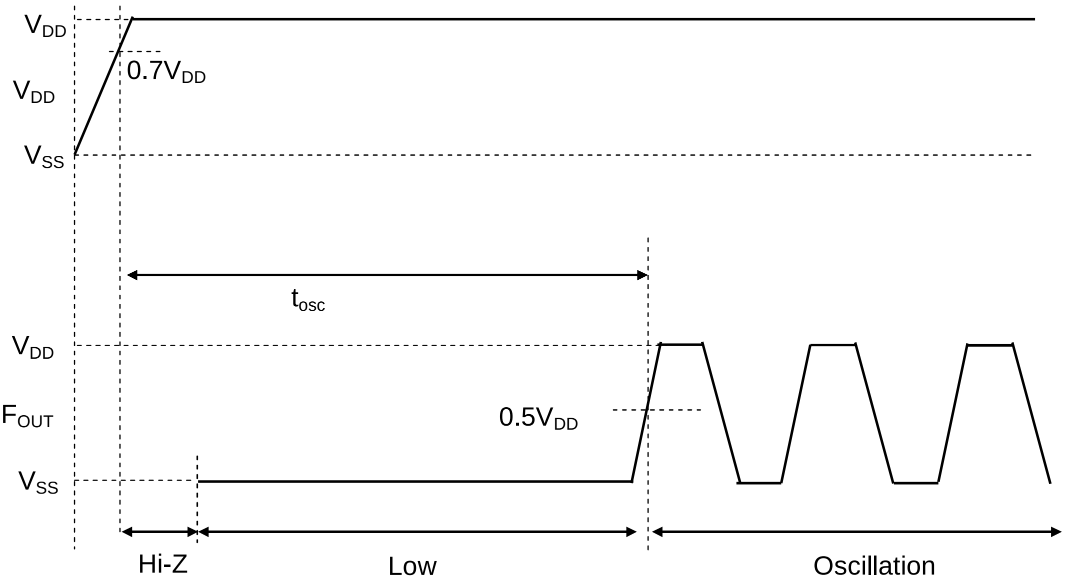
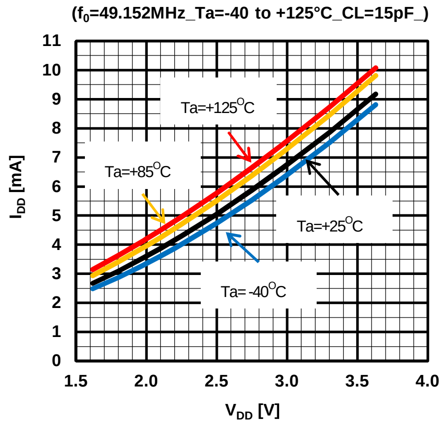


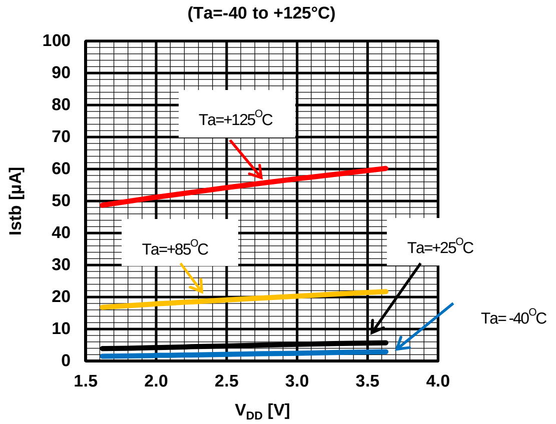
Fig.3 Oscillation Start time: t_{OSC}

■TYPICAL CHARACTERISTICS

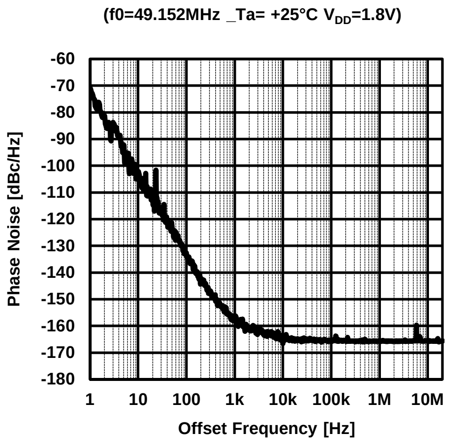
・Operation Current

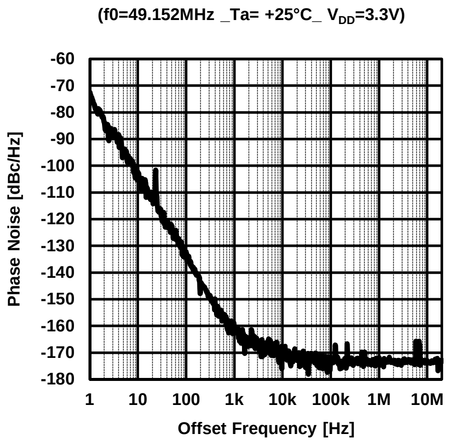


・Stand-by Current

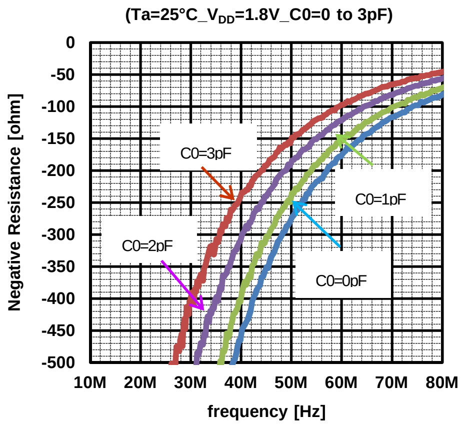


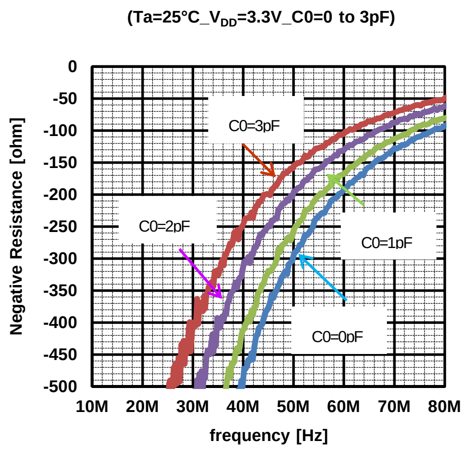
・Phase Noise





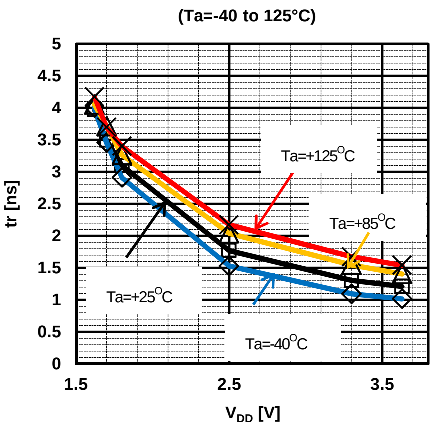
・Negative Resistance



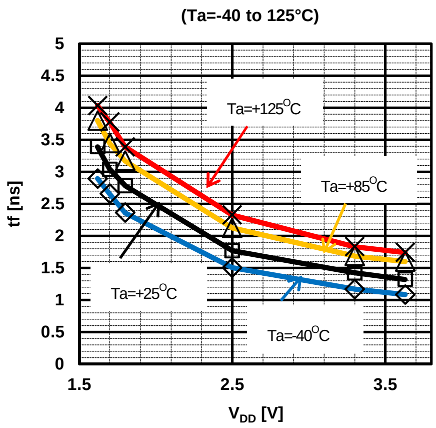


Note; A negative resistance 3 to 5 times the equivalent series resistance is said to be required for sufficient oscillation margin.

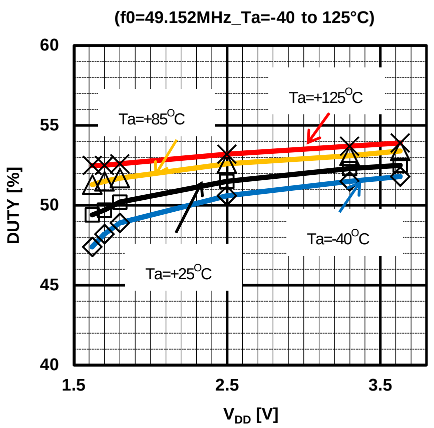
·Output Signal rise Time



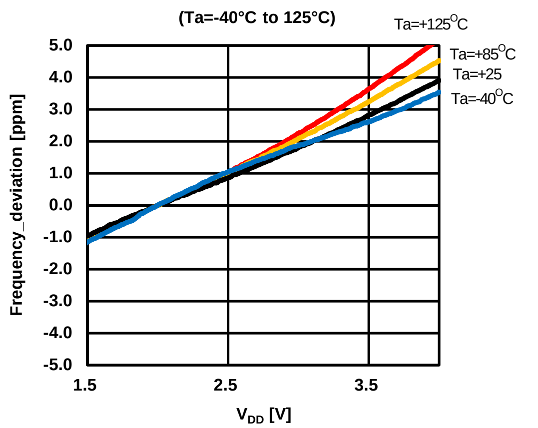
·Output Signal fall Time



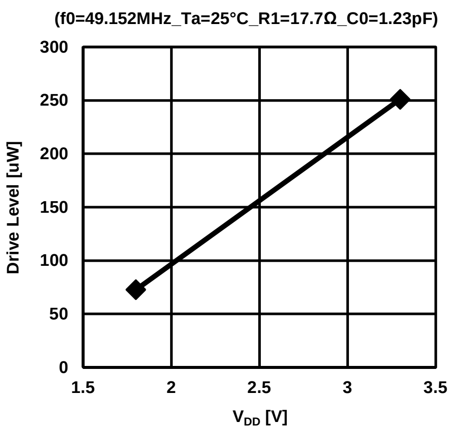
·Output Signal Symmetry



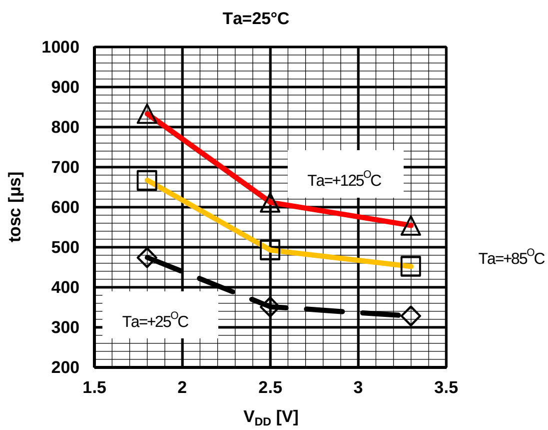
·Output Frequency Stability



· Drive Level



· Oscillation Start-Up Time



■Application Note

■FUNCTIONAL DESCRIPTION

•Standby Function

When CONT Terminal is “Low”, the F_{OUT} Terminal output is High impedance.

CONT	F_{OUT}	Oscillator
High(Open)	Frequency output	Normal operation
Low	High impedance	Stop

When not using Stand-by function, CONT terminal is recommended to connect to V_{DD}.

•Built-in Variable Pull-up Resistance of CONT terminal

The built-in pull-up resistance value of CONT Terminal changes in response to the input level. When CONT is “Low” level, the pull-up resistance value is large to reduce the current consumption by the resistance. When CONT is open or connected to V_{DD}, the pull-up resistance value is small to decrease the input susceptibility to external noise. It works to prevent an unexpectedly stopping of the output by external noise.

•VIRSION DISCRIMINATION INTERNAL COMPONENTS

PAD layout version of the NJU6222 series is determined by the version name in chip. Divide version of the NJU6222 series is determined by the internal fuse trimming.

Laser-trimmed versions are identified externally by the combination of the version name marking (1) and the locations of trimmed fuses (2). (Table 1 shows the chip version identification)

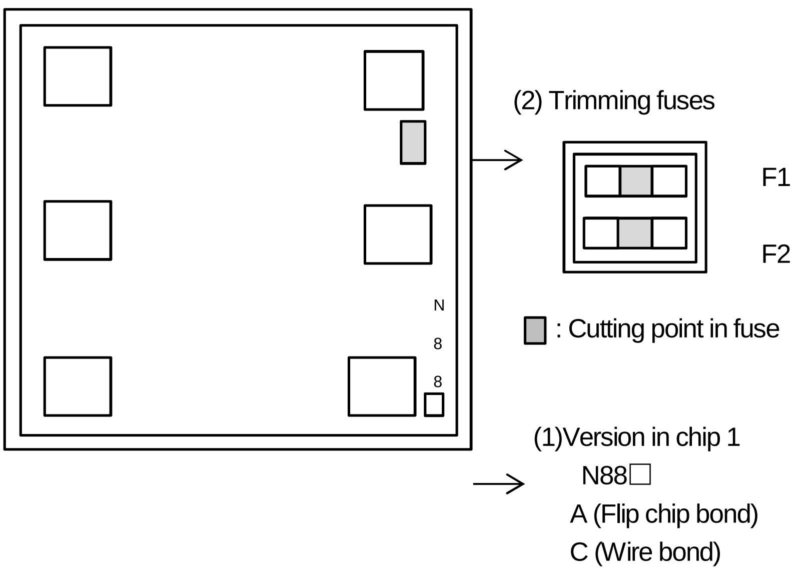


Table 1: Frequency version and Cutting point in fuse.

Version name	Mask / Version set by trimming fuses		
	Mask	Trimming fuses	
	Version	F1	F2
NJU6222A1	A	-	-
NJU6222A2	A	*	-
NJU6222C1	C	-	-
NJU6222C2	C	*	-

Note 1) “-“: Uncut, “*”: Cutting

[CAUTION]

1. NJR strives to produce reliable and high quality semiconductors. NJR's semiconductors are intended for specific applications and require proper maintenance and handling. To enhance the performance and service of NJR's semiconductors, the devices, machinery or equipment into which they are integrated should undergo preventative maintenance and inspection at regularly scheduled intervals. Failure to properly maintain equipment and machinery incorporating these products can result in catastrophic system failures

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   All other trademarks mentioned herein are the property of their respective companies.

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   The introduction of external contaminants (e.g. dust, oil or cosmetics) can result in failures of semiconductor products.

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5. Special care is required in designing devices, machinery or equipment which demand high levels of reliability. This is particularly important when designing critical components or systems whose failure can foreseeably result in situations that could adversely affect health or safety. In designing such critical devices, equipment or machinery, careful consideration should be given to amongst other things, their safety design, fail-safe design, back-up and redundancy systems, and diffusion design.

6. The products listed in this datasheet may not be appropriate for use in certain equipment where reliability is critical or where the products may be subjected to extreme conditions. You should consult our sales office before using the products in any of the following types of equipment.

   ・Aerospace Equipment
   ・Equipment Used in the Deep Sea
   ・Power Generator Control Equipment (Nuclear, steam, hydraulic, etc.)
   ・Life Maintenance Medical Equipment
   ・Fire Alarms / Intruder Detectors
   ・Vehicle Control Equipment (Airplane, railroad, ship, etc.)
   ・Various Safety Devices

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9. The product specifications and descriptions listed in this datasheet are subject to change at any time, without notice.