

NHD-4.3-480272MF-20 Controller Board

TFT Controller Evaluation Board

NHD-	Newhaven Display
4.3-	4.3" Diagonal
480272-	480xRGBx272 pixels
MF-	Model
20-	20-POS FFC interface (8-bit data) SSD1963 Controller

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Additional Resources

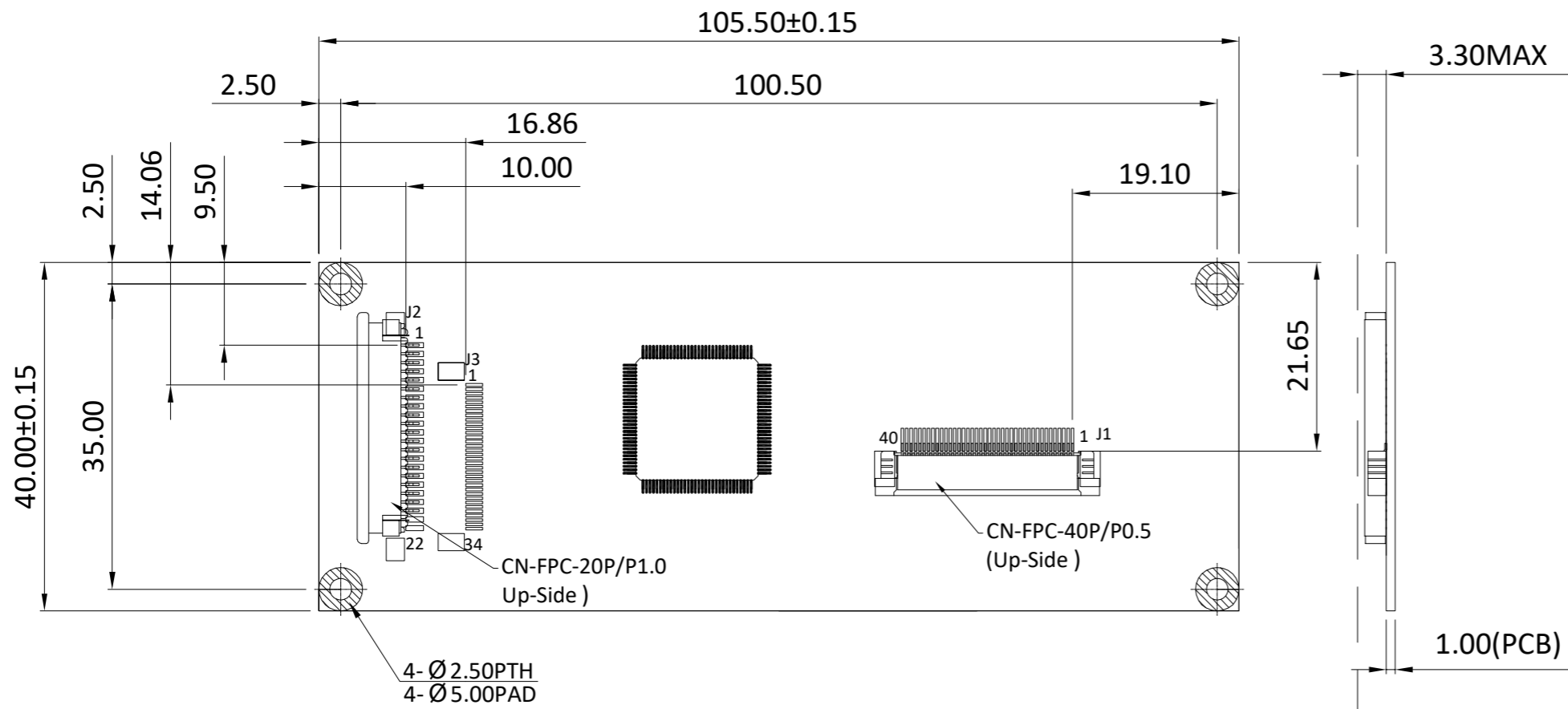
- **Support Forum:** <https://support.newhavendisplay.com/hc/en-us/community/topics>
- **GitHub:** <https://github.com/newhavendisplay>
- **Example Code:** <https://support.newhavendisplay.com/hc/en-us/categories/4409527834135-Example-Code/>
- **Knowledge Center:** https://www.newhavendisplay.com/knowledge_center.html
- **Quality Center:** https://www.newhavendisplay.com/quality_center.html
- **Precautions for using LCDs/LCMs:** <https://www.newhavendisplay.com/specs/precautions.pdf>
- **Warranty / Terms & Conditions:** <https://www.newhavendisplay.com/terms.html>



Document Revision History

Revision	Date	Description	Changed By
0	05/14/2007	Initial Release	CL
1	04/27/2012	J2 Pin Description Updated	AK
2	04/19/2019	LED Driver IC Updated	SB
3	03/04/2021	2D Mechanical Drawing Redesign; Revised Compatibility to NHD-4.3-480272MF-ATXL# Models	AS
4	11/04/2022	Backlight Driver Information Added and Mechanical Drawing Updated	KL
5	04/05/2023	Updated Electrical Characteristics	KL
6	08/16/2023	J1/J2 Pin Description Updated	KL

Mechanical Drawing

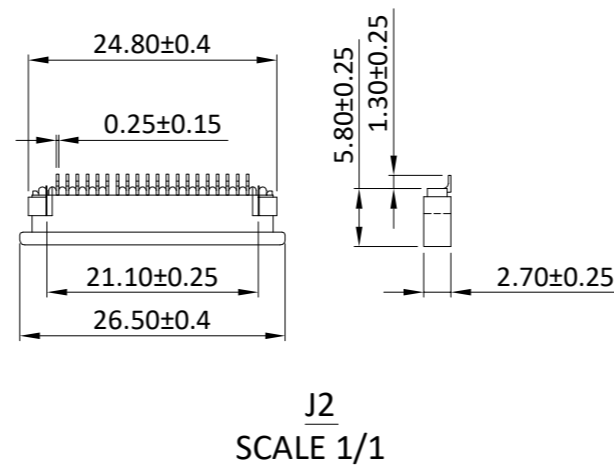
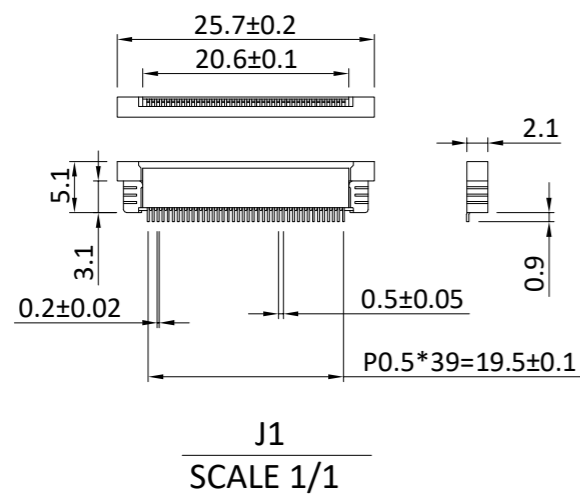


J1

PIN NO.	SYMBOL	PIN NO.	SYMBOL
1	VLED-	21	GND
2	VLED+	22	GND
3	GND	23	B0
4	VDD	24	B1
5	GND	25	B2
6	GND	26	B3
7	R0	27	B4
8	R1	28	B5
9	R2	29	GND
10	R3	30	PCLK
11	R4	31	DIP_ON
12	R5	32	HS
13	GND	33	VS
14	GND	34	DE
15	G0	35	NC
16	G1	36	GND
17	G2	37	NC
18	G3	38	NC
19	G4	39	NC
20	G5	40	NC

J2

PIN NO.	SYMBOL	PIN NO.	SYMBOL
1	GND		
2	VDD		
3	BL_E		
4	RS		
5	WR		
6	RD		
7	DB0		
8	DB1		
9	DB2		
10	DB3		
11	DB4		
12	DB5		
13	DB6		
14	DB7		
15	CS		
16	RES		
17	NC		
18	NC		
19	DIP_ON		
20	NC		



Standard Tolerance: (Unless otherwise specified) Linear: ±0.3mm		
	Drawing/Part Number: NHD-4.3-480272MF-20 Controller Board	Revision: 1A
Unless otherwise specified: • Dimensions are in Millimeters • Third Angle Projection	Drawn By: K. Lewis	Approved By: K. Lewis
	Drawn Date: 04/05/2023	Approved Date: 04/05/2023
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Pin Description

J1 (SSD1963 output to display panel)

Pin No.	Symbol	External Connection	Function Description
1	LED-	LED Power Supply	Backlight GND
2	LED+	LED Power Supply	Backlight Power
3	GND	Power Supply	GND
4	VDD	Power Supply	Power supply for LCD and logic (3.3V)
5-6	GND	Power Supply	GND
7-12	[R0-R5]	MPU	Red Data Signals
13-14	GND	Power Supply	GND
15-20	[G0-G5]	MPU	Green Data Signals
21-22	GND	Power Supply	GND
23-28	[B0-B5]	MPU	Blue Data Signals
29	GND	Power Supply	GND
30	PCLK	MPU	Data sample Clock signal
31	DISP	MPU	Display ON/OFF signal
32	HSYNC	MPU	Line synchronization signal
33	VSYNC	MPU	Frame synchronization signal
34	DEN	MPU	Data Enable signal
35	NC	-	No Connect
36	GND	Power Supply	GND
37	NC	-	No Connect
38	NC	-	No Connect
39	NC	-	No Connect
40	NC	-	No Connect

J2 (SSD1963 input from user's MPU)

Pin No.	Symbol	External Connection	Function Description
1	GND	Power Supply	GND
2	V _{DD}	Power Supply	Power supply for LCD and logic (3.3V)
3	BL_E	Power Supply	Backlight Enable and PWM Signal
4	D/C#	MPU	Data/Command Select signal. D/C#=0: Command, D/C#=1: Data
5	WR#	MPU	8080 MPU Write Signal active LOW
6	RD#	MPU	8080 MPU Read Signal active LOW
7-14	DB0-DB7	MPU	8-bit bidirectional data bus
15	CS#	MPU	Active LOW Chip Select signal
16	RESET#	MPU	Active LOW Reset signal
17	NC	-	No Connect
18	NC	-	No Connect
19	DISP	MPU	Display ON/OFF signal
20	NC	-	No Connect

Electrical Characteristics

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating Temperature Range	T _{OP}	Absolute Max	-20	-	+70	°C
Storage Temperature Range	T _{ST}	Absolute Max	-30	-	+80	°C
Supply Voltage	V _{DD}	-	3.0	3.3	3.6	V
Supply Current	I _{DD}	-	-	500	-	mA
Input High Voltage	V _{IH}	-	0.8 * V _{CC}	-	V _{CC}	V
Input Low Voltage	V _{IL}	-	GND	-	0.2 * V _{CC}	V
Backlight Supply Current	I _{LED}	-	30	40	50	mA
Backlight Supply Voltage	V _{LED}	I _{LED} = 40mA	22.4	25.6	27.2	V

Controller Information

Built-in SSD1963 Controller: <https://support.newhavendisplay.com/hc/en-us/articles/4414860003351-SSD1963>

Pixel Data Format

The 8080 mode MCU interface supports 8-bit, 9-bit, 16-bit and 18-bit data bus. Depending on the width of the data bus, the display data are packed into the data bus in different ways.

Interface	Cycle	D[23]	D[22]	D[21]	D[20]	D[19]	D[18]	D[17]	D[16]	D[15]	D[14]	D[13]	D[12]	D[11]	D[10]	D[9]	D[8]	D[7]	D[6]	D[5]	D[4]	D[3]	D[2]	D[1]	D[0]
24 bits	1 st	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
18 bits	1 st							R5	R4	R3	R2	R1	R0	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1	B0
16 bits (565 format)	1 st									R5	R4	R3	R2	R1	G5	G4	G3	G2	G1	G0	B5	B4	B3	B2	B1
16 bits	1 st									R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0
	2 nd									B7	B6	B5	B4	B3	B2	B1	B0	R7	R6	R5	R4	R3	R2	R1	R0
	3 rd									G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
12 bits	1 st													R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4
	2 nd												G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0	
9 bits	1 st															R5	R4	R3	R2	R1	R0	G5	G4	G3	
	2 nd														G2	G1	G0	B5	B4	B3	B2	B1	B0		
8 bits	1 st																	R7	R6	R5	R4	R3	R2	R1	R0
	2 nd																	G7	G6	G5	G4	G3	G2	G1	G0
	3 rd																	B7	B6	B5	B4	B3	B2	B1	B0

Timing Characteristics

Table 13-6: Parallel 8080-series Interface Timing Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
f_{MCLK}	System Clock Frequency*	1	-	110	MHz
t_{MCLK}	System Clock Period*	$1/f_{MCLK}$	-	-	ns
t_{PWCSL}	Control Pulse High Width Write	13	$1.5 * t_{MCLK}$	-	ns
	Control Pulse High Width Read	30	$3.5 * t_{MCLK}$	-	
t_{PWCSH}	Control Pulse Low Width Write (next write cycle)	13	$1.5 * t_{MCLK}$	-	ns
	Control Pulse Low Width Write (next read cycle)	80	$9 * t_{MCLK}$		
	Control Pulse Low Width Read	80	$9 * t_{MCLK}$		
t_{AS}	Address Setup Time	1	-	-	ns
t_{AH}	Address Hold Time	2	-	-	ns
t_{DSW}	Write Data Setup Time	4	-	-	ns
t_{DHW}	Write Data Hold Time	1	-	-	ns
t_{PWLW}	Write Low Time	12	-	-	ns
t_{DHR}	Read Data Hold Time	1	-	-	ns
t_{ACC}	Access Time	32	-	-	ns
t_{PWLr}	Read Low Time	36	-	-	ns
t_R	Rise Time	-	-	0.5	ns
t_F	Fall Time	-	-	0.5	ns
t_{CS}	Chip select setup time	2	-	-	ns
t_{CSH}	Chip select hold time to read signal	3	-	-	ns

* System Clock denotes external input clock (PLL-bypass) or internal generated clock (PLL-enabled)

Figure 13-3: Parallel 8080-series Interface Timing Diagram (Write Cycle)

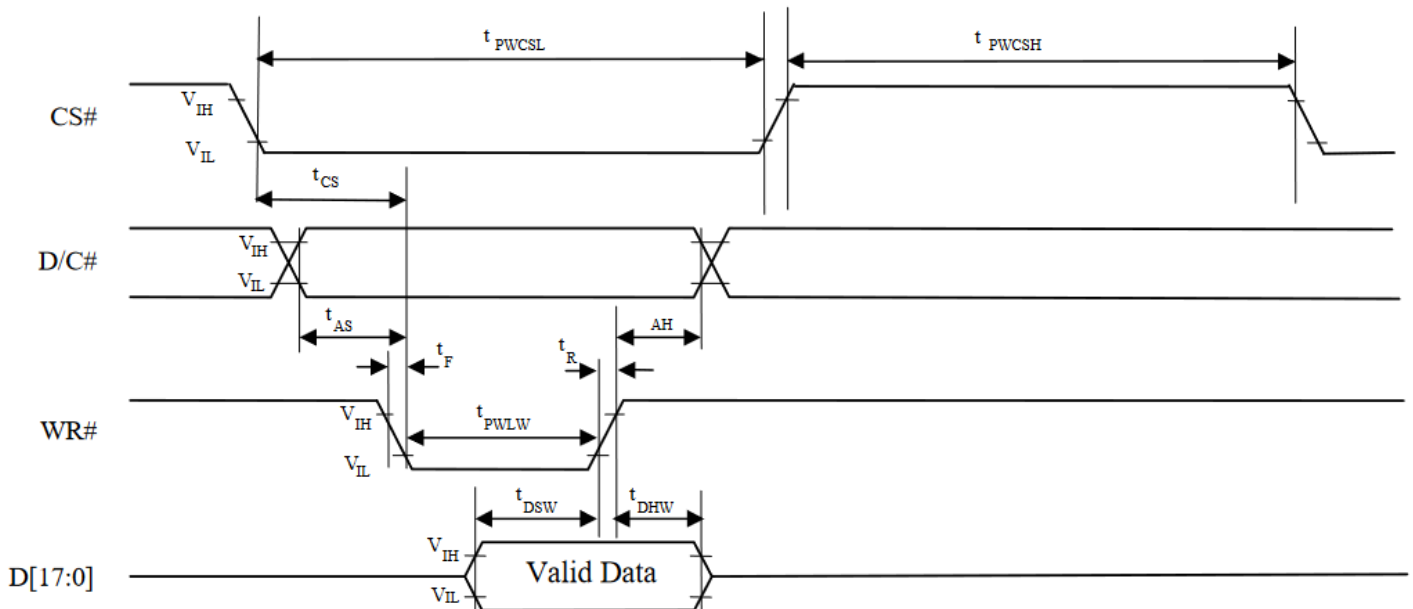
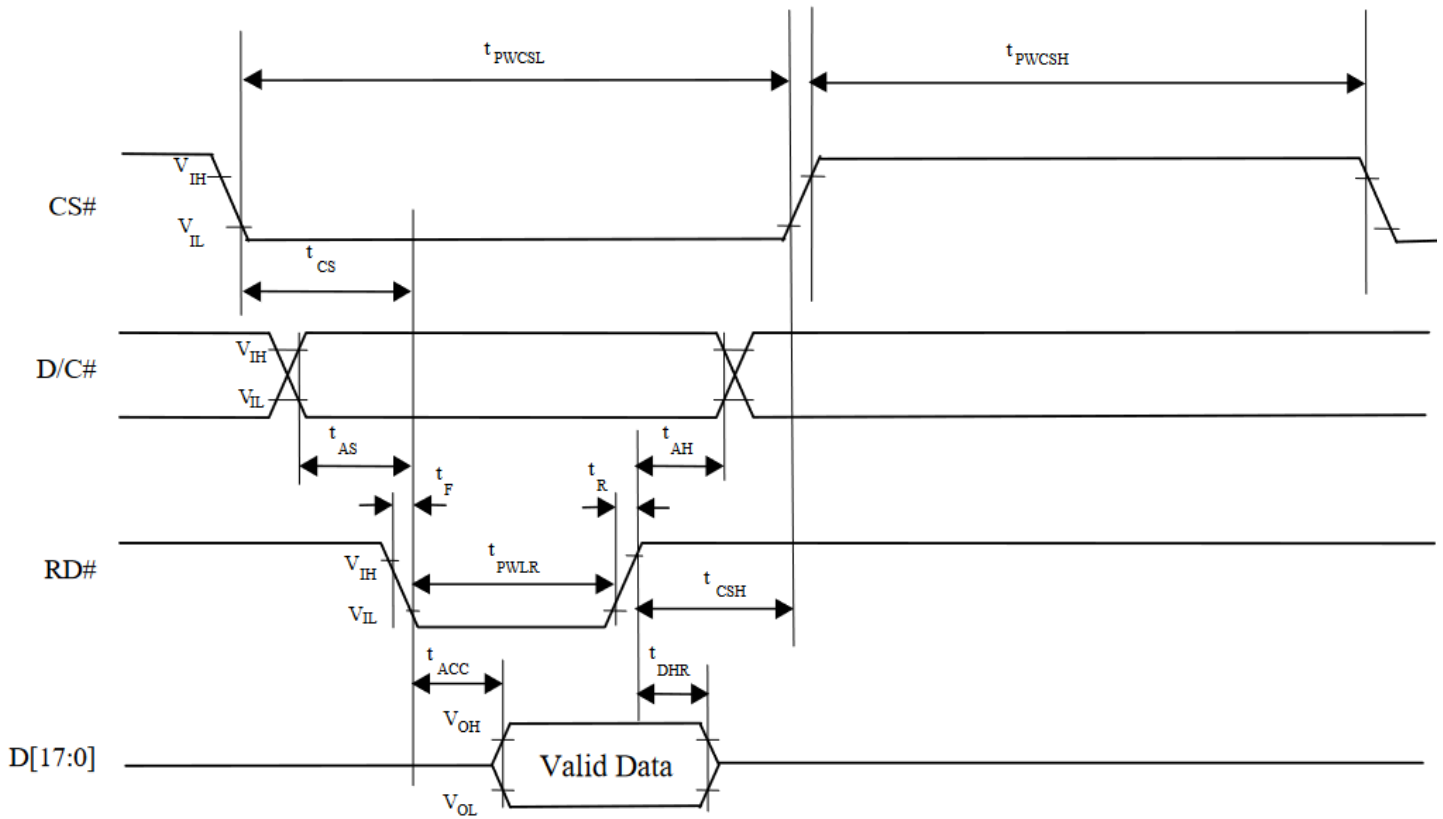


Figure 13-4: Parallel 8080-series Interface Timing Diagram (Read Cycle)



Quality Information

Test Item	Content of Test	Test Condition	Note
High Temperature storage	Endurance test applying the high storage temperature for a long time.	+80°C , 200hrs	2
Low Temperature storage	Endurance test applying the low storage temperature for a long time.	-30°C , 200hrs	1,2
High Temperature Operation	Endurance test applying the electric stress (voltage & current) and the high thermal stress for a long time.	+70°C 200hrs	2
Low Temperature Operation	Endurance test applying the electric stress (voltage & current) and the low thermal stress for a long time.	-20°C , 200hrs	1,2
High Temperature / Humidity Storage	Endurance test applying the electric stress (voltage & current) and the high thermal with high humidity stress for a long time.	+60°C , 90% RH , 96hrs	1,2
Thermal Shock resistance	Endurance test applying the electric stress (voltage & current) during a cycle of low and high thermal stress.	-20°C,30min -> 25°C,5min -> 70°C,30min = 1 cycle 10 cycles	
Vibration test	Endurance test applying vibration to simulate transportation and use.	10-55Hz , 1.5mm amplitude. 60 sec in each of 3 directions X,Y,Z For 15 minutes	3
Static electricity test	Endurance test applying electric static discharge.	VS=800V, RS=1.5kΩ, CS=100pF One time	

Note 1: No condensation to be observed.

Note 2: Conducted after 4 hours of storage at 25°C, 0%RH.

Note 3: Test performed on product itself, not inside a container.