

NDDL01N60Z, NDTL01N60Z

N-Channel Power MOSFET 600 V, 15 Ω

Features

- 100% Avalanche Tested
- Gate Charge Minimized
- Zener-protected
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	NDD	NDT	Unit
Drain-to-Source Voltage	V_{DSS}	600		V
Gate-to-Source Voltage	V_{GS}	± 30		V
Continuous Drain Current Steady State, $T_C = 25^\circ\text{C}$ (Note 1)	I_D	0.8	0.25	A
Continuous Drain Current Steady State, $T_C = 100^\circ\text{C}$ (Note 1)	I_D	0.5	0.15	A
Power Dissipation Steady State, $T_C = 25^\circ\text{C}$	P_D	26	2	W
Pulsed Drain Current, $t_p = 10 \mu\text{s}$	I_{DM}	3.4		A
Source Current (Body Diode)	I_S	2.5	1.7	A
Single Pulse Drain-to-Source Avalanche Energy ($I_D = 0.8 \text{ A}$)	EAS	12		mJ
Peak Diode Recovery (Note 2)	dv/dt	4.5		V/ns
Lead Temperature for Soldering Leads	T_L	260		$^\circ\text{C}$
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to +150		$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Limited by maximum junction temperature
2. $I_S = 1.5 \text{ A}$, $di/dt \leq 100 \text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$

THERMAL RESISTANCE

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) NDDL1N60Z	$R_{\theta JC}$	4.8	$^\circ\text{C}/\text{W}$
Junction-to-Ambient (Note 4) NDDL1N60Z (Note 3) NDDL1N60Z-1 (Note 4) NDTL1N60Z (Note 5) NDTL1N60Z	$R_{\theta JA}$	42 96 62 151	$^\circ\text{C}/\text{W}$

3. Insertion mounted.
4. Surface-mounted on FR4 board using 1" sq. pad size (Cu area = 1.127" sq. [2 oz] including traces).
5. Surface-mounted on FR4 board using minimum recommended pad size (Cu area = 0.026" sq. [2 oz]).

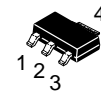
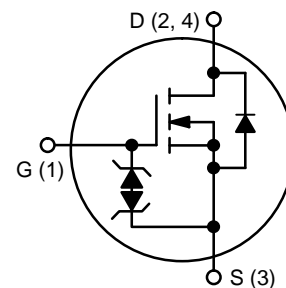


ON Semiconductor®

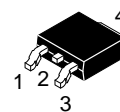
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(ON) MAX}$
600 V	15 Ω @ 10 V

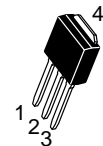
N-Channel MOSFET



SOT-223
CASE 318E
STYLE 3



DPAK
CASE 369C
STYLE 2



IPAK
CASE 369D
STYLE 2

MARKING & ORDERING INFORMATION

See detailed ordering, marking and shipping information in the package dimensions section on page 3 of this data sheet.

NDDL01N60Z, NDTL01N60Z

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
----------------	--------	-----------------	-----	-----	-----	------

OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	600			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$	Reference to $25^\circ\text{C}, I_D = 1\text{ mA}$		610		mV/ $^\circ\text{C}$
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$		1	μA
			$T_J = 125^\circ\text{C}$		50	
Gate-to-Source Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 6)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{DS} = V_{GS}, I_D = 50\text{ }\mu\text{A}$	3	4.0	4.5	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			9.6		mV/ $^\circ\text{C}$
Static Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 0.4\text{ A}$		12.2	15	Ω
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 0.4\text{ A}$		0.7		S

CHARGES, CAPACITANCES & GATE RESISTANCES

Input Capacitance (Note 7)	C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		92		μF
Output Capacitance (Note 7)	C_{oss}			13		
Reverse Transfer Capacitance (Note 7)	C_{rss}			3		
Effective output capacitance, energy related (Note 9)	$C_{o(er)}$	$V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }480\text{ V}$		5.5		μF
Effective output capacitance, time related (Note 10)	$C_{o(tr)}$	$I_D = \text{constant}, V_{GS} = 0\text{ V}, V_{DS} = 0\text{ to }480\text{ V}$		8.1		
Total Gate Charge (Note 7)	Q_g	$V_{DS} = 300\text{ V}, I_D = 0.4\text{ A}, V_{GS} = 10\text{ V}$		4.9		nC
Gate-to-Source Charge (Note 7)	Q_{gs}			1.2		
Gate-to-Drain Charge (Note 7)	Q_{gd}			2.4		
Plateau Voltage	V_{GP}			5.8		V
Gate Resistance	R_g			6.6		Ω

SWITCHING CHARACTERISTICS (Note 8)

Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 0.4\text{ A}, V_{GS} = 10\text{ V}, R_G = 0\text{ }\Omega$		10		ns
Rise Time	t_r			5		
Turn-off Delay Time	$t_{d(off)}$			13		
Fall Time	t_f			18		

DRAIN-SOURCE DIODE CHARACTERISTICS

Diode Forward Voltage	V_{SD}	$I_S = 0.4\text{ A}, V_{GS} = 0\text{ V}$	$T_J = 25^\circ\text{C}$		0.8	1.2	V
			$T_J = 100^\circ\text{C}$		0.7		
Reverse Recovery Time	t_{rr}	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}, I_S = 1\text{ A}, d_i/d_t = 100\text{ A}/\mu\text{s}$		183		ns	
Charge Time	t_a			33			
Discharge Time	t_b			150			
Reverse Recovery Charge	Q_{rr}			255			nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

6. Pulse Width $\leq 300\text{ }\mu\text{s}$, Duty Cycle $\leq 2\%$.

7. Guaranteed by design.

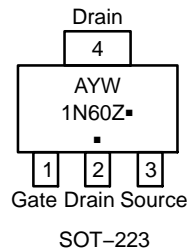
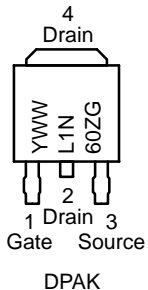
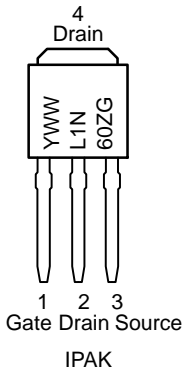
8. Switching characteristics are independent of operating junction temperatures.

9. $C_{o(er)}$ is a fixed capacitance that gives the same stored energy as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

10. $C_{o(tr)}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 to 80% $V_{(BR)DSS}$

NDDL01N60Z, NDTL01N60Z

MARKING DIAGRAMS



A = Assembly Location
 Y = Year
 W, WW = Work Week
 L1N60Z, 1N60Z = Specific Device Codes
 G or ■ = Pb-Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
NDDL01N60Z-1G	IPAK (Pb-Free, Halogen-Free)	75 Units / Rail
NDDL01N60ZT4G	DPAK (Pb-Free, Halogen-Free)	2500 / Tape & Reel
NDTL01N60ZT1G	SOT-223 (Pb-Free, Halogen-Free)	1000 / Tape & Reel
NDTL01N60ZT3G	SOT-223 (Pb-Free, Halogen-Free)	4000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TYPICAL CHARACTERISTICS

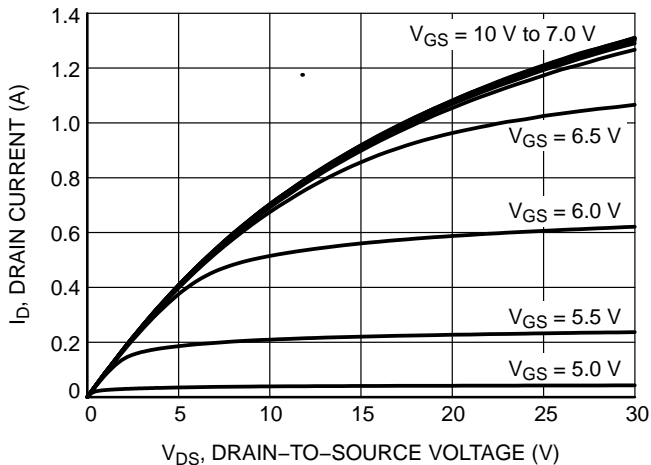


Figure 1. On-Region Characteristics

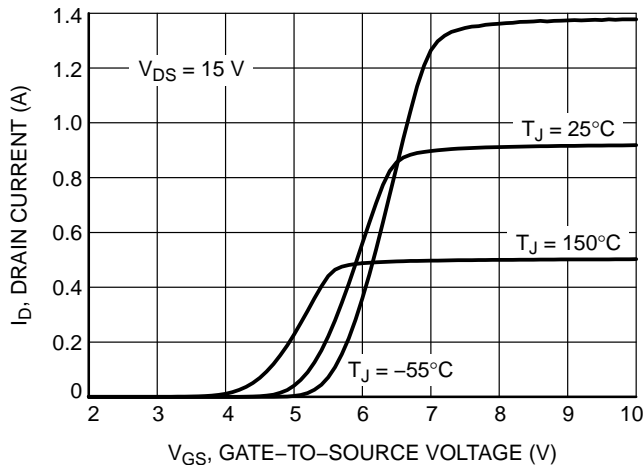


Figure 2. Transfer Characteristics

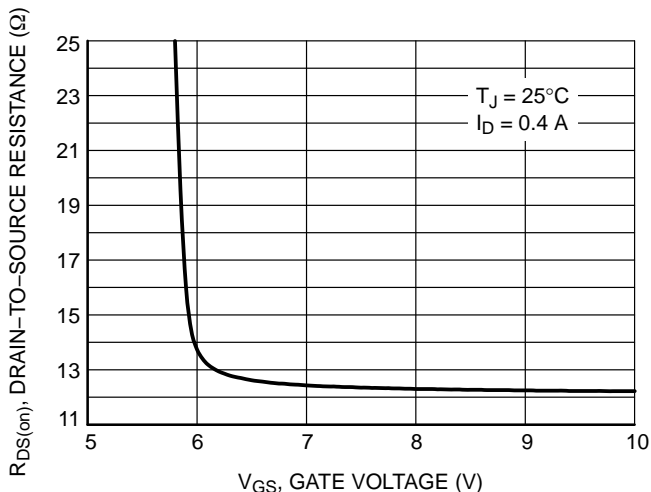


Figure 3. On-Resistance vs. Gate-to-Source Voltage

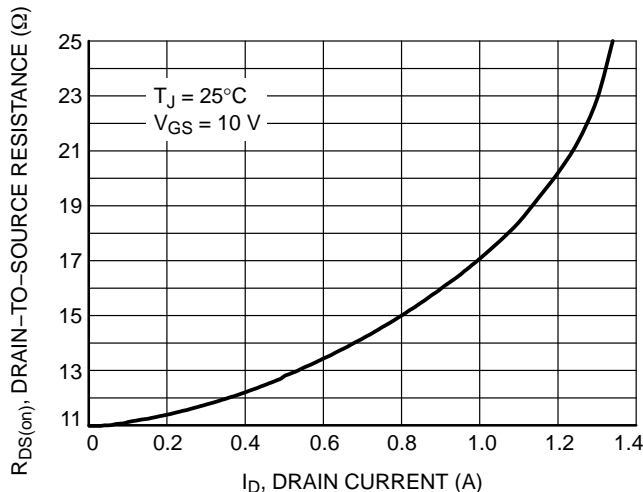


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

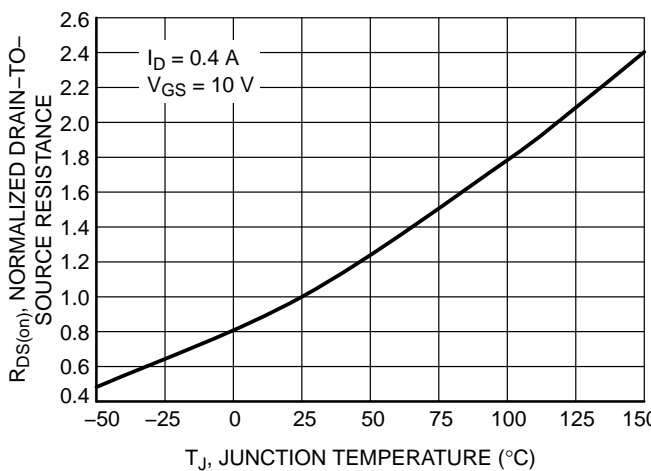


Figure 5. On-Resistance Variation with Temperature

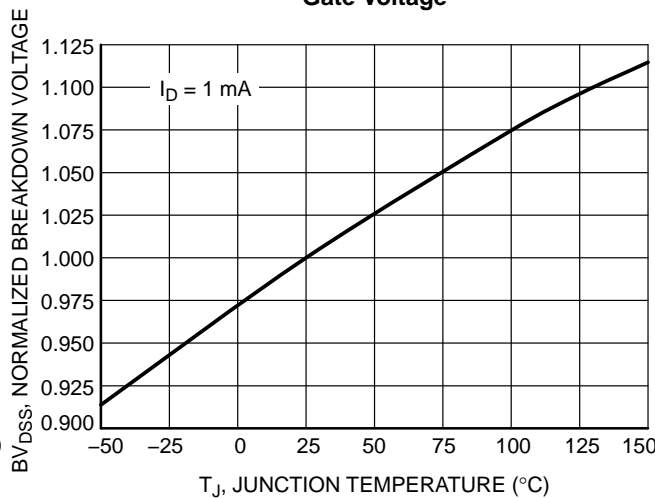


Figure 6. Breakdown Voltage Variation with Temperature

NDDL01N60Z, NDTL01N60Z

TYPICAL CHARACTERISTICS

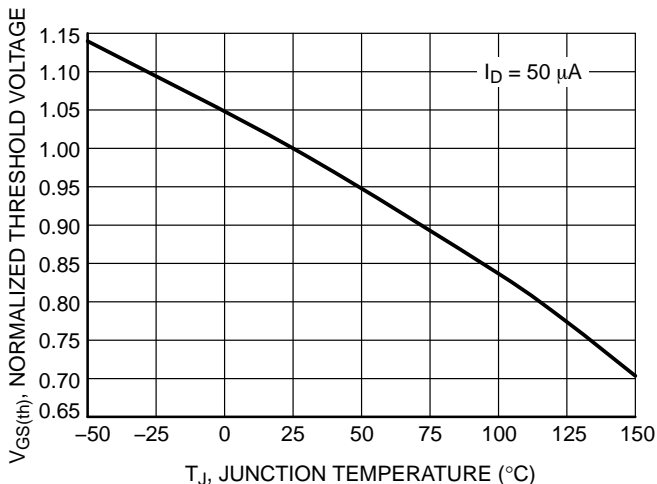


Figure 7. Threshold Voltage Variation with Temperature

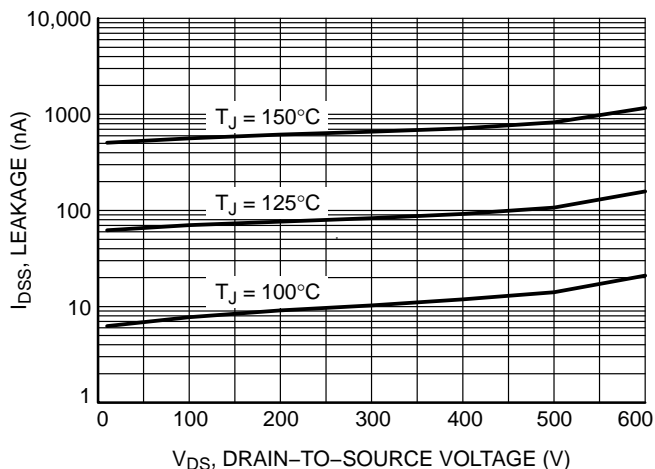


Figure 8. Drain-to-Source Leakage Current vs. Voltage

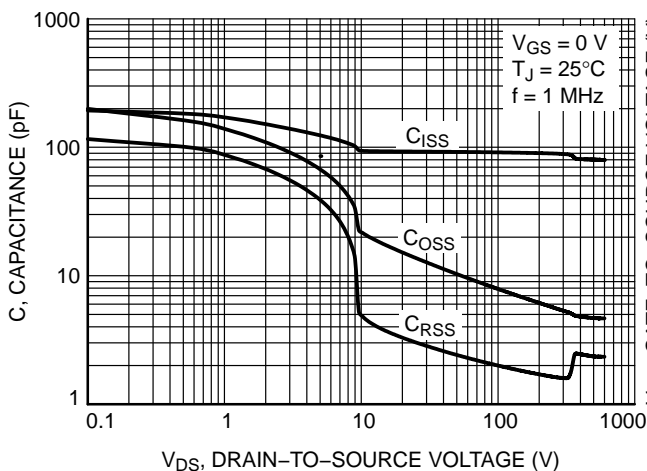


Figure 9. Capacitance Variation

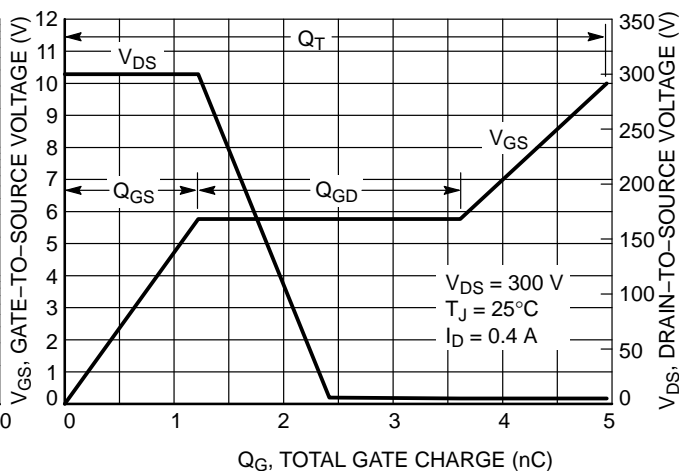


Figure 10. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

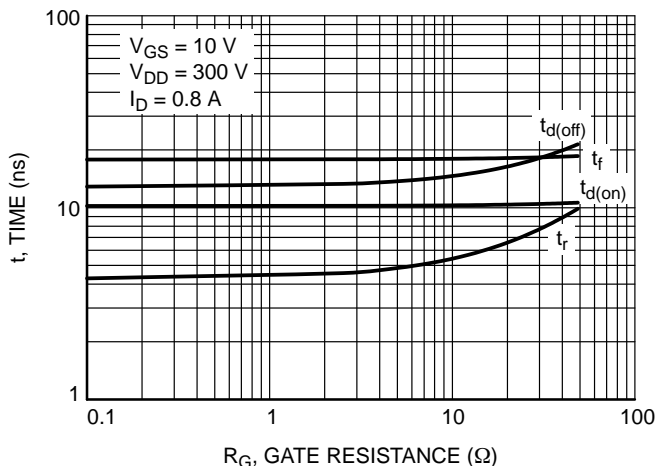


Figure 11. Resistive Switching Time Variation vs. Gate Resistance

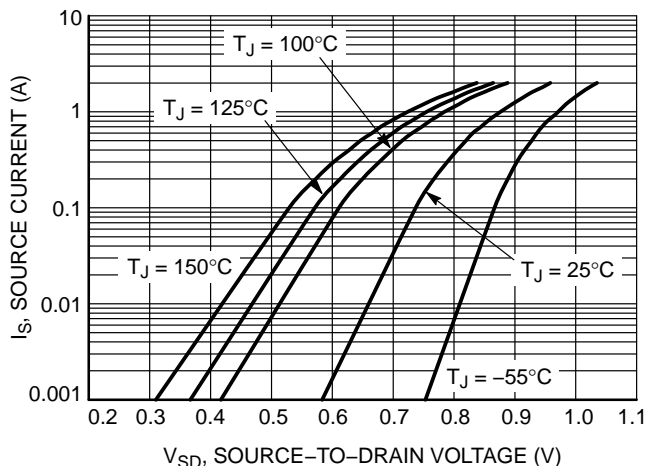


Figure 12. Diode Forward Voltage vs. Current

NDDL01N60Z, NDTL01N60Z

TYPICAL CHARACTERISTICS

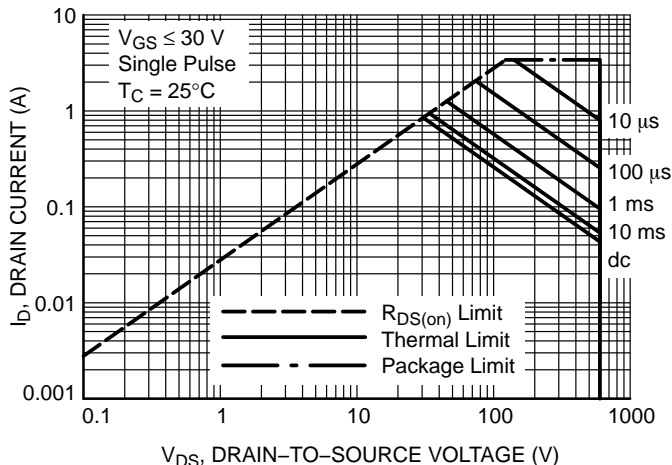


Figure 13. Maximum Rated Forward Biased Safe Operating Area for NDDL01N60Z

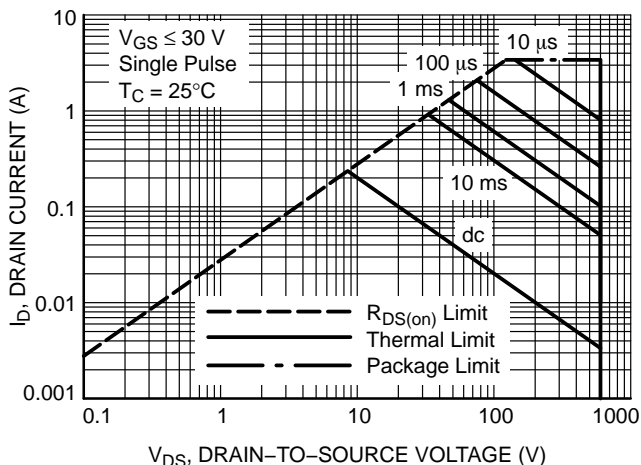


Figure 14. Maximum Rated Forward Biased Safe Operating Area for NDTL01N60Z

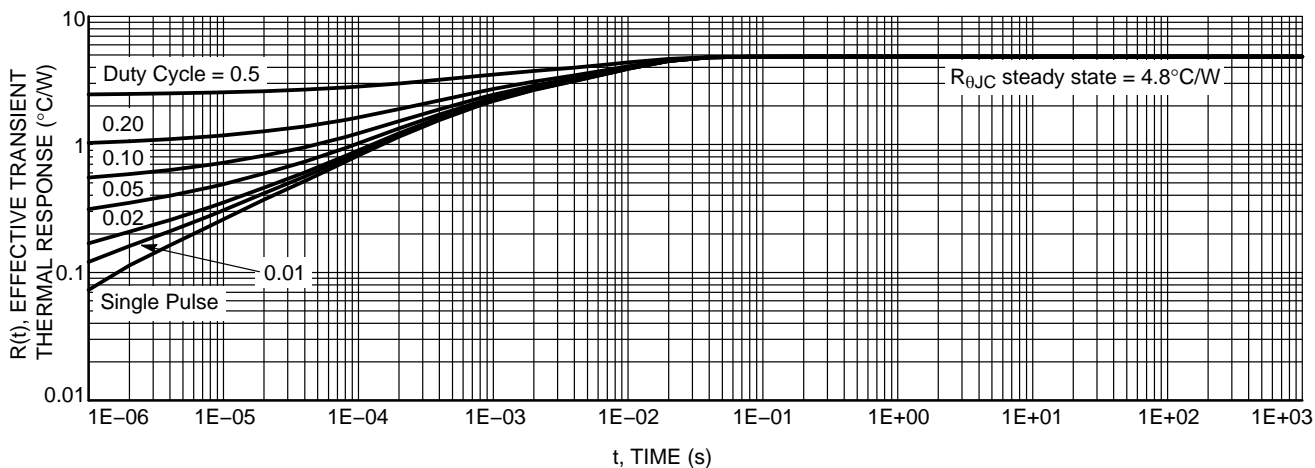


Figure 15. Thermal Impedance (Junction-to-Case) for NDDL01N60Z

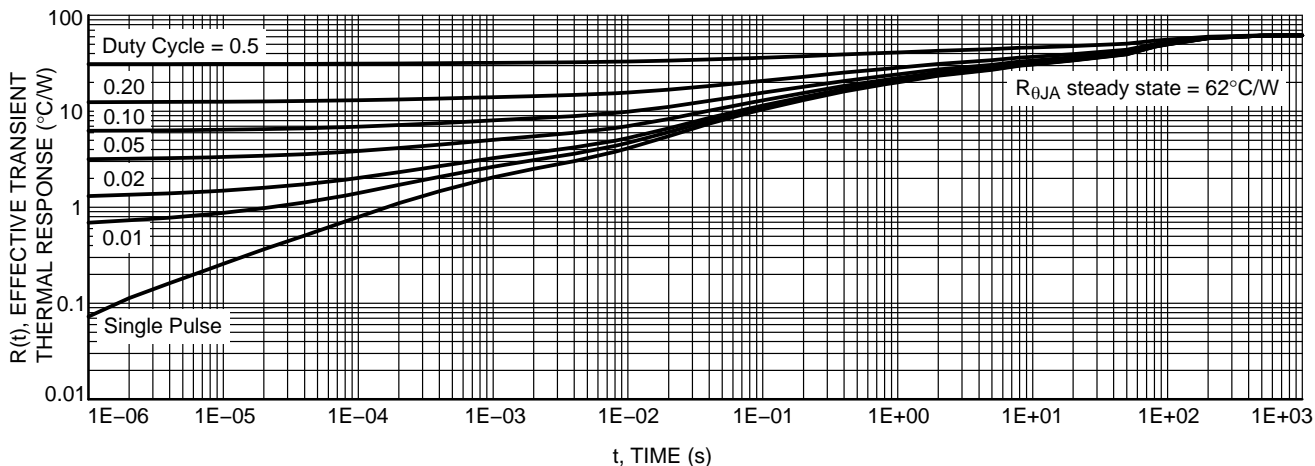
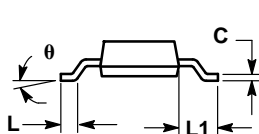
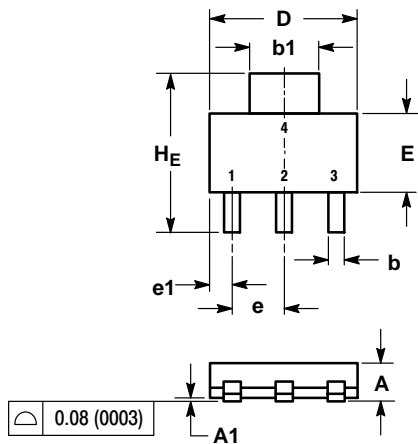


Figure 16. Thermal Impedance (Junction-to-Ambient) for NDTL01N60Z

NDDL01N60Z, NDTL01N60Z

PACKAGE DIMENSIONS

SOT-223 (TO-261)
CASE 318E-04
ISSUE N

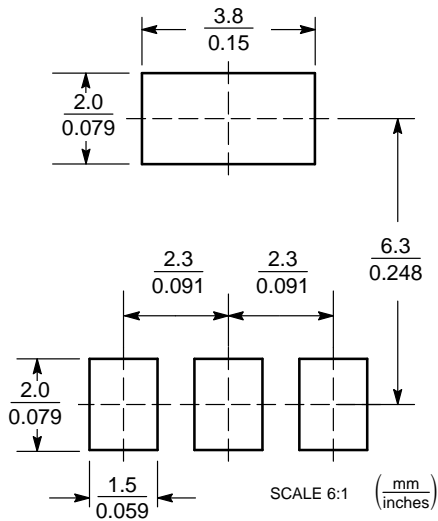


NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.63	1.75	0.060	0.064	0.068
A1	0.02	0.06	0.10	0.001	0.002	0.004
b	0.60	0.75	0.89	0.024	0.030	0.035
b1	2.90	3.06	3.20	0.115	0.121	0.126
c	0.24	0.29	0.35	0.009	0.012	0.014
D	6.30	6.50	6.70	0.249	0.256	0.263
E	3.30	3.50	3.70	0.130	0.138	0.145
e	2.20	2.30	2.40	0.087	0.091	0.094
e1	0.85	0.94	1.05	0.033	0.037	0.041
L	0.20	---	---	0.008	---	---
L1	1.50	1.75	2.00	0.060	0.069	0.078
HE	6.70	7.00	7.30	0.264	0.276	0.287
θ	0°	---	10°	0°	---	10°

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

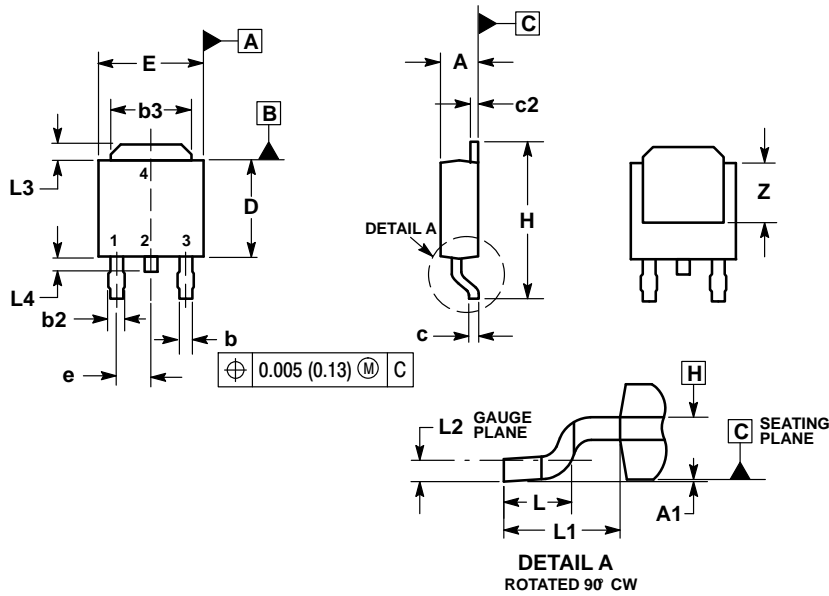
SOLDERING FOOTPRINT



NDDL01N60Z, NDTL01N60Z

PACKAGE DIMENSIONS

DPAK (SINGLE GAUGE) CASE 369C-01 ISSUE D



NOTES:

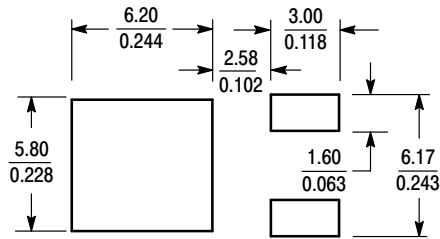
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

SOLDERING FOOTPRINT*



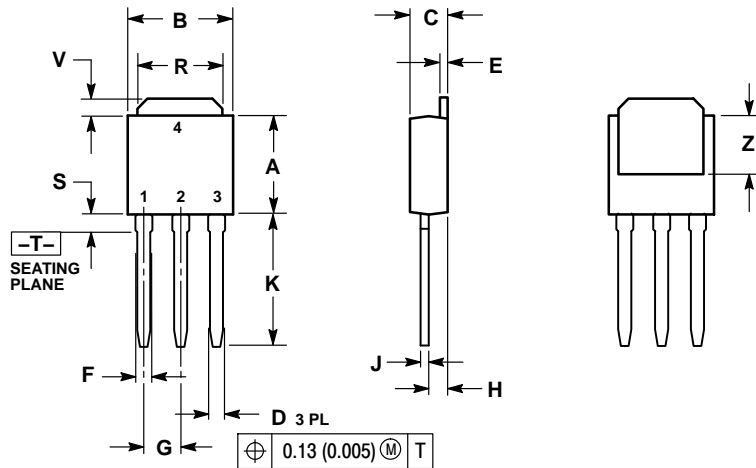
SCALE 3:1 $\left(\frac{\text{mm}}{\text{inches}}\right)$

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NDDL01N60Z, NDTL01N60Z

PACKAGE DIMENSIONS

IPAK CASE 369D ISSUE C



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

STYLE 2:

- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

ON Semiconductor and **ON** are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative