MEDIATEK

MT3620

A highly integrated, high performance IoT MCU with a security design focus necessary for modern, robust internet-connected devices.

Document Revision History

Revision	Date	Description
1.0	12 October 2017	Initial customer release.
1.1	4 April 2018	Additional information added.

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1. System Overview

1.1 General Description

MT3620 is a highly integrated single chip tri-core MCU designed to meet the requirements of modern, robust internet-connected devices. It leverages the Microsoft Azure Sphere security architecture to provide an unprecedented level of security to connected device manufacturers. For the lifetime of the device the Azure Sphere solution provides device authentication and attestation, supports remote over-the-air software updates to maintain security in the face of evolving attacks, and automates error logging and reporting. Please refer to the "Azure Sphere Solution Overview" document from Microsoft for more information.

MT3620 features an application processor subsystem based on an ARM Cortex-A7 core which runs at up to 500MHz. The chip also includes two general purpose ARM Cortex-M4F I/O subsystems, each of which runs at up to 200MHz. These subsystems were designed to support real-time requirements when interfacing with a variety of on-chip peripherals including UART, I2C, SPI, I2S, and ADC. They are completely general-purpose Cortex-M4F units which may be tailored to specific application requirements. On-chip peripherals may be mapped to any of the three end-user accessible cores, including the CA7.

In addition to these three end-user accessible cores, MT3620 contains a security subsystem with its own dedicated CM4F core for secure boot and secure system operation. There is also a Wi-Fi subsystem controlled by a dedicated N9 32-bit RISC core. This contains a 1x1 dual-band 802.11a/b/g/n radio, baseband and MAC designed to support both low power and high throughput applications without placing computational load on the user-accessible cores.

MT3620 also includes over 5MB of embedded RAM, split among the various cores. There is a fully-integrated PMU and a real-time clock. Flash memory is integrated in the MT3620 package; see section 3.2 for ordering information. Please refer to the "Azure Sphere MT3620 Support Status" document from Microsoft for information about how much memory and which hardware features are available to end-user applications. Only hardware features supported by the Azure Sphere solution are available to MT3620 end-users.

1.2 Main Features

1.2.1 Platform

- ARM Cortex A7 with NEON and FPU support and 64kB L1 instruction cache, 32kB L1 data cache, 256kB L2 cache, and 4MB system memory for the Azure Sphere operating system and user applications; ideal for high-level user code
- Two general purpose ARM Cortex M4 cores, each with 192kB TCM, 64kB SRAM, and integrated FPU; ideal for real-time control requirements
- In-package serial flash; see Section 3.2 for details
- User-accessible cores support execute-in-place (XIP) from flash
- Five "ISU" serial interface blocks which can be configured as I2C master. I2C slave, SPI master, SPI slave, or UART; I2C runs at up to 1MHz, SPI at up to 40MHz, and UARTs at up to 3Mbps
- Two I2S interfaces supporting slave and TDM slave modes
- Eight-channel, 12-bit, 2MS/s single-ended successive approximation ADC using internal 2.5V or external 1.8V reference
- 76 programmable GPIO pins with programmable drive strength (some multiplexed with other functions)
- 12 PWM outputs
- 24 external interrupt inputs
- Six hardware counter blocks which can count and measure pulses and perform quadrature decoding
- RTC can run from dedicated 32 kHz external input, from on-die 32 kHz oscillator, from on-die ring oscillator, or from main oscillator
- One-time programmable e-fuse block for storing chip-specific information
- Two additional, dedicated UARTs, one for each CM4F I/O subsystem
- Per-core watchdog timers
- Per-core general-purpose timers

1.2.2 Pluton Security Subsystem

- Provides security and secure power management for entire chip
- Dedicated ARM Cortex-M4F security processor with 128kB secured TCM and 64kB secured mask ROM bootloader
- Microsoft Azure Sphere Pluton security engine provides cryptographic engines and hardware root of trust
- Hardware random number generator with entropy monitoring system to ensure true random numbers
- Side-channel attack and tampering counter-measures

1. System Overview (continued)

- Dedicated, secure one-time programmable e-fuse block for storing security-related configuration information
- Provides secure boot via ECDSA, hardware support for remote attestation and certificate-based security

1.2.3 Wi-Fi

- Dedicated high-performance N9 32-bit RISC core
- Dedicated one-time programmable e-fuse block for storing Wi-Fi specific calibration and configuration information
- IEEE 802.11 a/b/g/n compliant
- Supports 20MHz bandwidth in 2.4GHz band and 5GHz band
- Dual-band 1T1R mode
- Supports STBC, LDPC, explicit beamforming as the beamformee
- Greenfield, mixed mode, legacy modes support
- IEEE 802.11 d/e/h/i/k/r/w support
- Security support for WFA WPA/WPA2 personal, WPS2.0, WAPI
- Supports 802.11w protected managed frames
- QoS support of WFA WMM, WMM PS
- Integrated LNA, PA, and T/R switch
- Built-in RX diversity support
- Full TX/RX antenna diversity support via external DPDT switch
- Optional external LNA and PA support
- Multiple external support component configuration options for BoM flexibility

1.2.4 Power Management and Clock Sources

- Integrated high efficiency power management unit with single 3.3V power supply input
- Integrated under-voltage lockout, three low drop-out (LDO) regulators and a high efficiency buck converter
- Integrated comparator for supply brown-out detection with configurable threshold
- 20/40/26/52MHz crystal clock support with low power operation mode
- 32kHz crystal real-time clock with external battery-backup supply

1.2.5 Management Interfaces

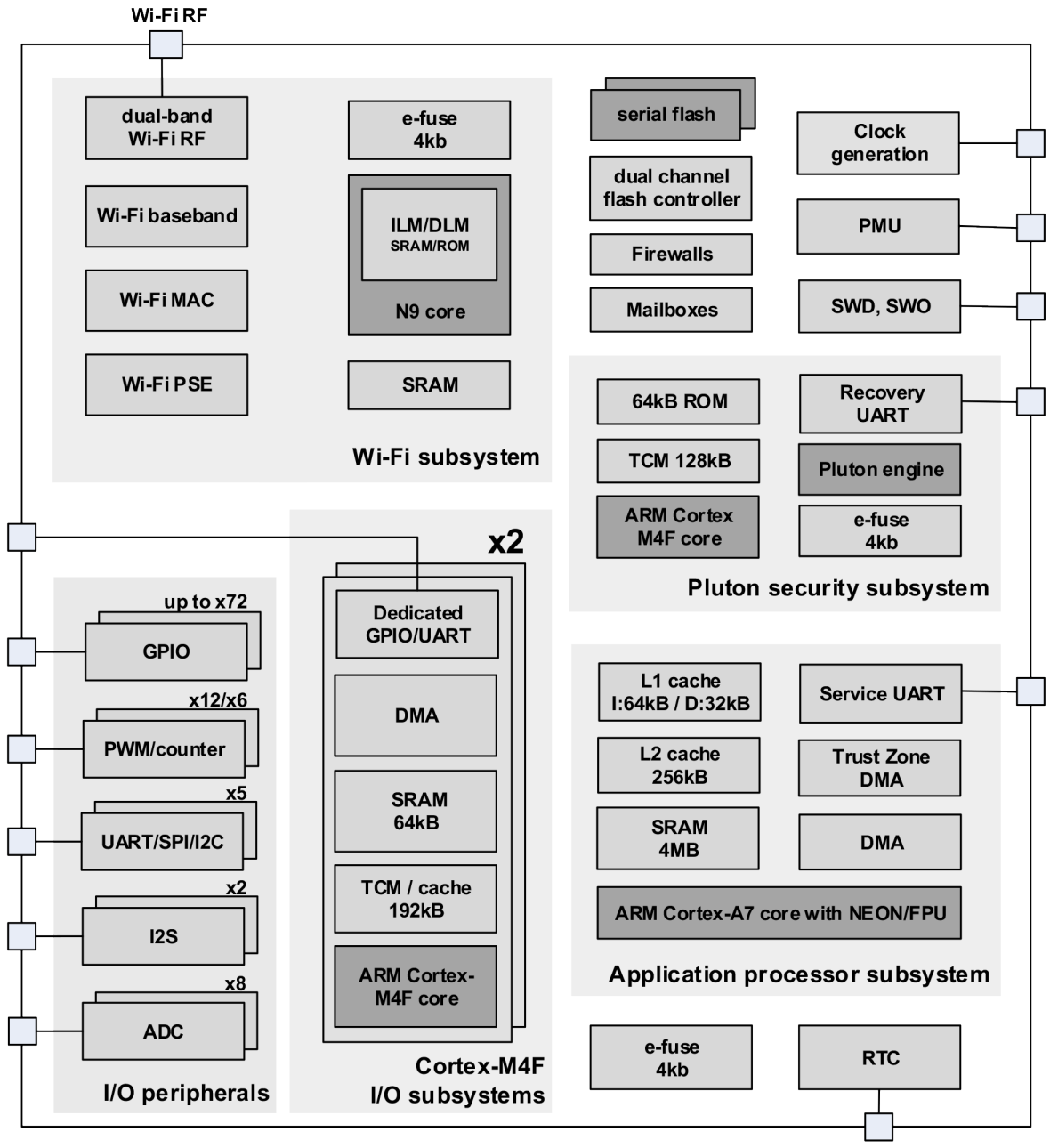
- 'Recovery' UART for re-loading device firmware
- 'Service' UART for in-production and in-field firmware update and device management

1.2.6 Technology and Package

- Highly integrated 40nm RFCMOS technology
- System-in-package (SIP) serial flash
- 12mm x 12mm 164 pin DR-QFN package
- Designed to support 4-layer PCB construction based on widely supported PCB design rules

1. System Overview (continued)

1.3 MT3620 Block Diagram



PSE	Wi-Fi packet switch engine	**PMU**	Power management unit	**PWM**	Pulse-width modulation
TCM	Tightly-coupled memory	**RTC**	Real-time clock	**GPIO**	General purpose input/output
ILM	Instruction local memory	**DMA**	Direct memory access	**FPU**	Floating point unit
DLM	Data local memory	**I2C**	Inter-IC communications	**I2S**	Inter-IC sound
ADC	Analog to digital converter	**NEON**	Arm's single instruction multiple data architecture	**UART**	Universal asynchronous receiver/transmitter

2. Application Support

2.1 Application development

MT3620 was designed in close cooperation with Microsoft as part of the Microsoft Azure Sphere solution. Whilst the Cortex-A7 application processor must always run the Azure Sphere secure OS supplied by Microsoft, it is also available for running a custom user-mode application hosted by the secure OS. Microsoft provides a powerful development environment based on the gcc compiler which includes a Visual Studio extension, allowing this application to be developed in C. Visual Studio debugging, including features such as single-step execution, breakpoints, and watchpoints are supported using a SLIP interface to the CA7 via a dedicated Azure Sphere service UART.

In addition to the Cortex-A7 application processor subsystem, MT3620 includes two Cortex-M4F I/O subsystems. The two M4F I/O subsystems are primarily intended to support real-time I/O processing but can also be used for general purpose computation and control. The M4F cores may run any end-user-provided operating system, or run a 'bare metal app' with no operating system.

Debugging on the I/O subsystems is supported through a shared multi-core SWD channel with SWO support. There is also optional support for higher bandwidth trace via a 16-bit ARM TPIU interface. Each Cortex-M4F core also has a dedicated UART which can be used to support debugging if necessary.

Operation of MT3620 security features and Wi-Fi networking is isolated from, and runs independently of, end user applications. As such, security features and Wi-Fi are only accessible via defined APIs and are robust to programming errors in end-user applications regardless of whether these applications run on the CA7 or the user-accessible CM4F cores.

2.2 Hardware config & control

Microsoft-provided libraries support a variety of functions including hardware configuration, network communication, and use of the MT3620 peripherals. Please refer to the latest "Azure Sphere MT3620 Support Status" document from Microsoft for information about currently supported hardware configurations, network communications, and peripherals. Note that due to the secure nature of the Azure Sphere solution, features not yet supported by Microsoft are not available by any other means.

2.3 RF testing support

MT3620 can enter a radio test mode that allows test lab personnel or automated test equipment to set low-level radio parameters and transmit and receive custom test signals and packets. This functionality is suitable for radio emissions compliance testing of an MT3620-based product.

The MT3620 radio test mode can also be used to support per-device production line Wi-Fi calibration and test. Production test RF equipment from test equipment suppliers such as LitePoint will include support for MT3620.

2.4 Manufacturing test support

MT3620 allows manufacturers to create custom manufacturing test applications using the same application development tools used to create end-user applications. These test applications support in-circuit functional testing during manufacturing. Microsoft will provide documentation and utilities to allow these tests to integrate with factory processes.

3. Chip Specification

3.1 Pinout

For the 'Type' column, P = power, I = input, O = output, A = analog, D = digital, RF = radio frequency.

Pins named 'RESERVED' should not be connected. Pins named 'TEST' much be connected in the manner described. Pins named 'NC' are not connected inside the chip and may be left unconnected on the PCB.

Pin #	Pin Name	Major Functions	Type	Description
1	GND		P	Ground
2	AVDD_3V3_WF_A_PA		PI	3.3V power rail for 5GHz Wi-Fi power amplifier
3	AVDD_3V3_WF_A_PA		PI	3.3V power rail for 5GHz Wi-Fi power amplifier
4	NC			
5	NC			
6	AVDD_1V6_WF_TRX		PI	1.6V power rail for Wi-Fi transmit/receive
7	AVDD_1V6_WF_AFE		PI	1.6V power rail for Wi-Fi analog front end
8	NC			
9	AVDD_1V6_XO		PI	1.6V power rail for main crystal oscillator
10	MAIN_XIN		AI	Main crystal oscillator input
11	WF_ANTSEL0		DO	Wi-Fi antenna select for external DPDT switch
12	WF_ANTSEL1		DO	Wi-Fi antenna select for external DPDT switch
13	GPIO0	GPIO0/PWM0	DIO	Interrupt-capable GPIO multiplexed with PWM output
14	GPIO1	GPIO1/PWM1	DIO	Interrupt-capable GPIO multiplexed with PWM output
15	GPIO2	GPIO2/PWM2	DIO	Interrupt-capable GPIO multiplexed with PWM output
16	GPIO3	GPIO3/PWM3	DIO	Interrupt-capable GPIO multiplexed with PWM output
17	GPIO4	GPIO4/PWM4	DIO	Interrupt-capable GPIO multiplexed with PWM output
18	GPIO5	GPIO5/PWM5	DIO	Interrupt-capable GPIO multiplexed with PWM output
19	GPIO6	GPIO6/PWM6	DIO	Interrupt-capable GPIO multiplexed with PWM output
20	GPIO7	GPIO7/PWM7	DIO	Interrupt-capable GPIO multiplexed with PWM output
21	GPIO8	GPIO8/PWM8	DIO	Interrupt-capable GPIO multiplexed with PWM output
22	GPIO9	GPIO9/PWM9	DIO	Interrupt-capable GPIO multiplexed with PWM output
23	DVDD_1V15		PI	1.15V power rail
24	DVDD_3V3		PI	3.3V power rail
25	GPIO10	GPIO10/PWM10	DIO	Interrupt-capable GPIO multiplexed with PWM output
26	GPIO11	GPIO11/PWM11	DIO	Interrupt-capable GPIO multiplexed with PWM output

3.1 Pinout (continued)

Pin #	Pin Name	Major Functions	Type	Description
27	GPIO12		DIO	Interrupt-capable GPIO
28	GPIO13		DIO	Interrupt-capable GPIO
29	GPIO14		DIO	Interrupt-capable GPIO
30	GPIO15		DIO	Interrupt-capable GPIO
31	GPIO16		DIO	Interrupt-capable GPIO
32	GPIO17		DIO	Interrupt-capable GPIO
33	GPIO18		DIO	Interrupt-capable GPIO
34	GPIO19		DIO	Interrupt-capable GPIO
35	GPIO20		DIO	Interrupt-capable GPIO
36	GPIO21		DIO	Interrupt-capable GPIO
37	GPIO22		DIO	Interrupt-capable GPIO
38	GPIO23		DIO	Interrupt-capable GPIO
39	GPIO26	GPIO26/SCLK0/TXD0	DIO	GPIO multiplexed with ISU 0 functions
40	GPIO27	GPIO27/MOSI0/RTS0/ SCL0	DIO	GPIO multiplexed with ISU 0 functions
41	GND		P	Ground
42	GPIO28	GPIO28/MISO0/RXD0/ SDA0	DIO	GPIO multiplexed with ISU 0 functions
43	GPIO29	GPIO29/CSA0/CTS0	DIO	GPIO multiplexed with ISU 0 functions
44	DVDD_1V15		PI	1.15V power rail
45	GPIO30	GPIO30/CSB0	DIO	GPIO multiplexed with ISU 0 functions
46	GPIO31	GPIO31/SCLK1/TXD1	DIO	GPIO multiplexed with ISU 1 functions
47	GPIO32	GPIO32/MOSI1/RTS1/ SCL1	DIO	GPIO multiplexed with ISU 1 functions
48	GPIO33	GPIO33/MISO1/RXD1/ SDA1	DIO	GPIO multiplexed with ISU 1 functions
49	GPIO34	GPIO34/CSA1/CTS1	DIO	GPIO multiplexed with ISU 1 functions
50	GPIO35	GPIO35/CSB1	DIO	GPIO multiplexed with ISU 1 functions
51	GPIO36	GPIO36/SCLK2/TXD2	DIO	GPIO multiplexed with ISU 2 functions
52	GPIO37	GPIO37/MOSI2/RTS2/ SCL2	DIO	GPIO multiplexed with ISU 2 functions
53	GPIO38	GPIO38/MISO2/RXD2/ SDA2	DIO	GPIO multiplexed with ISU 2 functions
54	GPIO39	GPIO39/CSA2/CTS2	DIO	GPIO multiplexed with ISU 2 functions
55	GPIO40	GPIO40/CSB2	DIO	GPIO multiplexed with ISU 2 functions
56	DVDD_3V3		PI	3.3V power rail
57	DVDD_1V15		PI	1.15V power rail
58	GPIO41	GPIO41/ADC0	ADIO	GPIO multiplexed with ADC input
59	GPIO42	GPIO42/ADC1	ADIO	GPIO multiplexed with ADC input
60	GPIO43	GPIO43/ADC2	ADIO	GPIO multiplexed with ADC input
61	GPIO44	GPIO44/ADC3	ADIO	GPIO multiplexed with ADC input

3.1 Pinout (continued)

Pin #	Pin Name	Major Functions	Type	Description
62	GPIO45	GPIO45/ADC4	ADIO	GPIO multiplexed with ADC input
63	GPIO46	GPIO46/ADC5	ADIO	GPIO multiplexed with ADC input
64	GPIO47	GPIO47/ADC6	ADIO	GPIO multiplexed with ADC input
65	GPIO48	GPIO48/ADC7	ADIO	GPIO multiplexed with ADC input
66	AVDD_2V5_ADC		PI	2.5V power rail for ADC
67	VREF_ADC		AI	Reference voltage for ADC
68	AVSS_2V5_ADC		P	Ground for ADC
69	EXT_PMU_EN		DO	External power supply enable output
70	WAKEUP		DI	External wakeup from deepest sleep mode
71	AVDD_3V3_RTC		PI	3.3V power rail for real-time clock
72	RTC_XIN		AI	Realtime clock crystal oscillator input
73	RTC_XOUT		AO	Realtime clock crystal oscillator output
74	AVDD_3V3_XPLL		PI	3.3V power rail for internal phase-locked loop
75	I2S_MCLK0_ALT		AO	Analog alternative to MCLK0
76	I2S_MCLK1_ALT		AO	Analog alternative to MCLK1
77	DVDD_1V15		PI	1.15V power rail
78	DVDD_1V15		PI	1.15V power rail
79	VOUT_2V5		PO	Output from internal 2.5V LDO
80	AVDD_3V3		PI	3.3V power rail
81	PMU_EN		DI	Internal PMU override
82	RESERVED			
83	GND		P	Ground
84	SENSE_1V15		AI	Sense input to stabilise the 1.15V power supply
85	VOUT_1V15		PO	Output from internal 1.15V LDO
86	AVDD_1V6_CLDO		PI	1.6V power rail for the internal 1.15V core LDO
87	PMU_CAP		A	Connect a capacitor between this pin and AVDD_3V3_BUCK to maintain PMU stability
88	AVDD_3V3_BUCK		PI	3.3V power rail for internal 1.6V buck DC-DC converter
89	AVDD_3V3_BUCK		PI	3.3V power rail for internal 1.6V buck DC-DC converter
90	VOUT_1V6		PO	Output from internal 1.6V buck converter
91	VOUT_1V6		PO	Output from internal 1.6V buck converter
92	AVSS_3V3_BUCK		P	Ground for internal 1.6V buck converter
93	AVSS_3V3_BUCK		P	Ground for internal 1.6V buck converter
94	DEBUG_RXD		DI	Reserved for Azure Sphere debug
95	DEBUG_TXD		DO	Reserved for Azure Sphere debug
96	DEBUG_RTS		DO	Reserved for Azure Sphere debug
97	DEBUG_CTS		DI	Reserved for Azure Sphere debug
98	SWD_DIO		DIO	ARM SWD for Cortex CM4F debug

3.1 Pinout (continued)

Pin #	Pin Name	Major Functions	Type	Description
99	SWD_CLK		DI	ARM SWD for Cortex CM4F debug
100	SWO		DO	ARM SWO for Cortex CM4F debug
101	GPIO56	GPIO56/TX0	DIO	GPIO multiplexed with I2S 0
102	GPIO57	GPIO57/MCLK0	DIO	GPIO multiplexed with I2S 0
103	GPIO58	GPIO58/FS0	DIO	GPIO multiplexed with I2S 0
104	GPIO59	GPIO59/RX0	DIO	GPIO multiplexed with I2S 0
105	GPIO60	GPIO60/BCLK0	DIO	GPIO multiplexed with I2S 0
106	DVDD_1V15		PI	1.15V power rail
107	DVDD_3V3		PI	3.3V power rail
108	GPIO61	GPIO61/TX1	DIO	GPIO multiplexed with I2S 1
109	GPIO62	GPIO62/MCLK1	DIO	GPIO multiplexed with I2S 1
110	GPIO63	GPIO63/FS1	DIO	GPIO multiplexed with I2S 1
111	GPIO64	GPIO64/RX1	DIO	GPIO multiplexed with I2S 1
112	GPIO65	GPIO65/BCLK1	DIO	GPIO multiplexed with I2S 1
113	GPIO66	GPIO66/SCLK3/TXD3	DIO	GPIO multiplexed with ISU 3 functions
114	GPIO67	GPIO67/MOSI3/RTS3/ SCL3	DIO	GPIO multiplexed with ISU 3 functions
115	GPIO68	GPIO68/MISO3/RXD3/ SDA3	DIO	GPIO multiplexed with ISU 3 functions
116	GPIO69	GPIO69/CSA3/CTS3	DIO	GPIO multiplexed with ISU 3 functions
117	GPIO70	GPIO70/CSB3	DIO	GPIO multiplexed with ISU 3 functions
118	DVDD_3V3		PI	3.3V power rail
119	GPIO71	GPIO71/SCLK4/TXD4	DIO	GPIO multiplexed with ISU 4 functions
120	GPIO72	GPIO72/MOSI4/RTS4/ SCL4	DIO	GPIO multiplexed with ISU 4 functions
121	DVDD_1V15		PI	1.15V power rail
122	GPIO73	GPIO73/MISO4/RXD4/ SDA4	DIO	GPIO multiplexed with ISU 4 functions
123	GPIO74	GPIO74/CSA4/CTS4	DIO	GPIO multiplexed with ISU 4 functions
124	GPIO75	GPIO75/CSB4	DIO	GPIO multiplexed with ISU 4 functions
125	SYSRST_N		DI	System reset, active low
126	DVDD_1V15		PI	1.15V power rail
127	SERVICE_TXD		DO	Azure Sphere service port
128	SERVICE_RTS		DO	Azure Sphere service port
129	SERVICE_RXD		DI	Azure Sphere service port
130	SERVICE_CTS		DI	Azure Sphere service port
131	RESERVED			
132	DVDD_1V15		PI	1.15V power rail
133	DVDD_3V3		PI	3.3V power rail
134	RECOVERY_RXD		DI	Azure Sphere recovery port

3.1 Pinout (continued)

Pin #	Pin Name	Major Functions	Type	Description
135	RECOVERY_TXD		DO	Azure Sphere recovery port
136	RECOVERY_RTS		DO	Azure Sphere recovery port
137	RECOVERY_CTS		DI	Azure Sphere recovery port
138	IO0_GPIO85	IO0_GPIO85/IO0_RXD	DI	Dedicated GPIO multiplexed with UART for I/O CM4F 0
139	IO0_GPIO86	IO0_GPIO86/IO0_TXD	DO	Dedicated GPIO multiplexed with UART for I/O CM4F 0
140	IO0_GPIO87	IO0_GPIO87/IO0_RTS	DO	Dedicated GPIO multiplexed with UART for I/O CM4F 0
141	IO0_GPIO88	IO0_GPIO88/IO0_CTS	DI	Dedicated GPIO multiplexed with UART for I/O CM4F 0
142	IO1_GPIO89	IO1_GPIO89/IO1_RXD	DI	Dedicated GPIO multiplexed with UART for I/O CM4F 1
143	IO1_GPIO90	IO1_GPIO90/IO1_TXD	DO	Dedicated GPIO multiplexed with UART for I/O CM4F 1
144	DVDD_3V3		PI	3.3V power rail
145	IO1_GPIO91	IO1_GPIO91/IO1_RTS	DO	Dedicated GPIO multiplexed with UART for I/O CM4F 1
146	IO1_GPIO92	IO1_GPIO92/IO1_CTS	DI	Dedicated GPIO multiplexed with UART for I/O CM4F 1
147	RESERVED			
148	TEST		DI	Must be tied low at power on for normal operation
149	WF_G_RF_AUXIN		RF	2.4GHz Wi-Fi receive diversity port
150	NC			
151	AVDD_3V3_WF_G_PA		PI	3.3V power rail for 2.4GHz Wi-Fi power amplifier
152	NC			
153	WF_G_RF_ION		RF	2.4GHz Wi-Fi antenna port (differential)
154	WF_G_RF_ION		RF	2.4GHz Wi-Fi antenna port (differential)
155	WF_G_RF_IOP		RF	2.4GHz Wi-Fi antenna port (differential)
156	WF_G_RF_IOP		RF	2.4GHz Wi-Fi antenna port (differential)
157	NC			
158	AVDD_3V3_WF_G_TX		PI	3.3V power rail for 2.4GHz Wi-Fi transmit
159	WF_A_RF_AUXIN		RF	5GHz Wi-Fi receive diversity port
160	AVDD_3V3_WF_A_TX		PI	3.3V power rail for 5GHz Wi-Fi transmit
161	NC			
162	WF_A_RFIO		RF	5GHz Wi-Fi antenna port (unbalanced)
163	WF_A_RFIO		RF	5GHz Wi-Fi antenna port (unbalanced)
164	GND		P	Ground
165	EPAD		P	Ground

3.2 Ordering information

Part number	Total flash	Flash configuration
MT3620AN	16MB	2x 8MB dual channel quad SPI

4. Wi-Fi Radio Characteristics

4.1 Wi-Fi 2.4GHz Band RF Receiver Specifications

The specification in table below is measured at the antenna port, which includes the front-end loss.

Parameter	Description	Performance				
		Min	Typical		Max	Unit
			Main	Aux		
Frequency range	Center channel frequency	2412			2484	MHz
RX sensitivity	DBPSF, 1 Mbps DSSS	-	-94.6	-97.1	-90.0	dBm
	DQPSF, 2 Mbps DSSS	-	-91.6	-94.1	-87.0	dBm
	DQPSF, 5.5 Mbps CCK	-	-89.6	-92.1	-85.0	dBm
	DQPSF, 11 Mbps CCK	-	-86.6	-89.1	-82.0	dBm
	BPSK rate 1/2, 6 Mbps OFDM	-	-91.6	-94.1	-87.0	dBm
	BPSK rate 3/4, 9 Mbps OFDM	-	-89.3	-91.8	-86.0	dBm
	QPSK rate 1/2, 12 Mbps OFDM	-	-88.5	-91.0	-84.0	dBm
	QPSK rate 3/4, 18 Mbps OFDM	-	-86.1	-88.6	-82.0	dBm
	16QAM rate 1/2, 24 Mbps OFDM	-	-82.8	-85.3	-81.0	dBm
	16QAM rate 3/4, 36 Mbps OFDM	-	-79.4	-81.9	-78.0	dBm
	64QAM rate 1/2, 48 Mbps OFDM	-	-75.2	-77.7	-73.0	dBm
	64QAM rate 3/4, 54 Mbps OFDM	-	-73.9	-76.4	-71.0	dBm
RX sensitivity BW=20MHz Mixed mode 800ns guard interval Non-STBC	MCS 0, BPSK rate 1/2	-	-90.9	-93.4	-87.0	dBm
	MCS 1, QPSK rate 1/2	-	-87.7	-90.2	-86.0	dBm
	MCS 2, QPSK rate 3/4	-	-85.3	-87.8	-84.0	dBm
	MCS 3, 16QAM rate 1/2	-	-82.3	-84.8	-81.0	dBm
	MCS 4, 16QAM rate 3/4	-	-78.8	-81.3	-77.0	dBm
	MCS 5, 64QAM rate 2/3	-	-74.4	-76.9	-74.0	dBm
	MCS 6, 64QAM rate 3/4	-	-73.0	-75.5	-71.0	dBm
	MCS 7, 64QAM rate 5/6	-	-71.8	-74.3	-69.0	dBm
Maximum receive level	1 Mbps DSSS	-20	-10		-	dBm
	11 Mbps CCK	-20	-10		-	dBm
	6 Mbps OFDM	-20	-10		-	dBm
	54 Mbps OFDM	-20	-10		-	dBm
	HT20 MCS0	-20	-10		-	dBm
	HT20 MCS7	-20	-20		-	dBm

4.1 Wi-Fi 2.4GHz Band RF Receiver Specifications (continued)

Parameter	Description	Performance				
		Min	Typical		Max	Unit
			Main	Aux		
Receive adjacent channel rejection	BPSK rate 1/2, 6 Mbps OFDM	16	34		-	dBm
	BPSK rate 3/4, 9 Mbps OFDM	15	31		-	dBm
	QPSK rate 1/2, 12 Mbps OFDM	13	30		-	dBm
	QPSK rate 3/4, 18 Mbps OFDM	11	27		-	dBm
	16QAM rate 1/2, 24 Mbps OFDM	8	25		-	dBm
	16QAM rate 3/4, 36 Mbps OFDM	4	23		-	dBm
	64QAM rate 1/2, 48 Mbps OFDM	0	22		-	dBm
	64QAM rate 3/4, 54 Mbps OFDM	-1	22		-	dBm
	MCS 0, BPSK rate 1/2	16	33		-	dBm
	MCS 1, QPSK rate 1/2	13	29		-	dBm
	MCS 2, QPSK rate 3/4	11	26		-	dBm
	MCS 3, 16QAM rate 1/2	8	24		-	dBm
	MCS 4, 16QAM rate 3/4	4	20		-	dBm
	MCS 5, 64QAM rate 2/3	0	18		-	dBm
	MCS 6, 64QAM rate 3/4	-1	17		-	dBm
	MCS 7, 64QAM rate 5/6	-2	15		-	dBm
Receiver residual PER	All rates, -50dBm input power	-	-		0.005	%

4.2 Wi-Fi 2.4GHz Band RF Transmitter Specifications

Parameter	Description	Performance			
		Min	Typical	Max	Unit
Frequency range	Center channel frequency	2412	-	2484	MHz
Output power with spectral mask and EVM compliance	1 Mbps DSSS	-	16[1]	-	dBm
	11 Mbps CCK	-	16[1]	-	dBm
	6 Mbps OFDM	-	16[1]	-	dBm
	54 Mbps OFDM	-	16[1]	-	dBm
	HT20 MCS 0	-	16[1]	-	dBm
	HT20 MCS 7	-	16[1]	-	dBm
Output power with spectral mask and EVM compliance (at -40°C and 85°C)	1 Mbps DSSS	-	15[1]	-	dBm
	11 Mbps CCK	-	15[1]	-	dBm
	6 Mbps OFDM	-	15[1]	-	dBm
	54 Mbps OFDM	-	15[1]	-	dBm
	HT20 MCS 0	-	15[1]	-	dBm
	HT20 MCS 7	-	15[1]	-	dBm

4.2 Wi-Fi 2.4GHz Band RF Transmitter Specifications (continued)

Parameter	Description	Performance			
		Min	Typical	Max	Unit
TX EVM	1 Mbps DSSS	-	-	-10	dB
	11 Mbps CCK	-	-	-10	dB
	6 Mbps OFDM	-	-	-5	dB
	54 Mbps OFDM	-	-	-25	dB
	HT20 MCS 0	-	-	-5	dB
	HT20 MCS 7	-	-	-28	dB
Output power variation[2]	TSSI closed-loop control across all temperature range and channels and VSWR ≤ 1.5:1.	-1.5	-	1.5	dB
Carrier suppression		-	-	-30	dBc
Harmonic output power	2nd Harmonic	-	-45	-43	dBm/MHz
	3nd Harmonic	-	-45	-43	dBm/MHz

4.3 Wi-Fi 5GHz Band RF Receiver Specifications

The specification in table below is measured at the antenna port, which includes the front-end loss.

Parameter	Description	Performance				
		Min	Typical		Max	Unit
			Main	Aux		
Frequency range	Center channel frequency	5180			5825	MHz
RX sensitivity	BPSK rate 1/2, 6 Mbps OFDM	-	-90.0	-91.5	-86.0	dBm
	BPSK rate 3/4, 9 Mbps OFDM	-	-87.7	-89.2	-85.0	dBm
	QPSK rate 1/2, 12 Mbps OFDM	-	-87.0	-88.5	-83.0	dBm
	QPSK rate 3/4, 18 Mbps OFDM	-	-84.5	-86.0	-81.0	dBm
	16QAM rate 1/2, 24 Mbps OFDM	-	-81.3	-82.8	-75.0	dBm
	16QAM rate 3/4, 36 Mbps OFDM	-	-78.0	-79.5	-72.0	dBm
	64QAM rate 1/2, 48 Mbps OFDM	-	-73.6	-75.1	-70.0	dBm
	64QAM rate 3/4, 54 Mbps OFDM	-	-72.2	-73.7	-68.0	dBm
RX sensitivity	MCS 0, BPSK rate 1/2	-	-89.3	-90.8	-86.0	dBm
BW=20MHz HT	MCS 1, QPSK rate 1/2	-	-86.3	-87.8	-84.0	dBm
Mixed mode	MCS 2, QPSK rate 3/4	-	-83.8	-85.3	-82.0	dBm
800ns guard interval	MCS 3, 16QAM rate 1/2	-	-80.8	-82.3	-76.0	dBm
non-STBC	MCS 4, 16QAM rate 3/4	-	-77.3	-78.8	-74.0	dBm
	MCS 5, 64QAM rate 2/3	-	-72.8	-74.3	-72.0	dBm
	MCS 6, 64QAM rate 3/4	-	-71.4	-72.9	-70.0	dBm
	MCS 7, 64QAM rate 5/6	-	-70.2	-71.7	-66.0	dBm

4.3 Wi-Fi 5GHz Band RF Receiver Specifications (continued)

Parameter	Description	Performance				
		Min	Typical		Max	Unit
			Main	Aux		
Maximum receive level	6 Mbps OFDM	-30	-10		-	dBm
	54 Mbps OFDM	-30	-20		-	dBm
	MCS0	-30	-15		-	dBm
	MCS7	-30	-20		-	dBm
Receive adjacent channel rejection	BPSK rate 1/2, 6 Mbps OFDM	16	24		-	dBm
	BPSK rate 3/4, 9 Mbps OFDM	15	23		-	dBm
	QPSK rate 1/2, 12 Mbps OFDM	13	21		-	dBm
	QPSK rate 3/4, 18 Mbps OFDM	11	19		-	dBm
	16QAM rate 1/2, 24 Mbps OFDM	8	15		-	dBm
	16QAM rate 3/4, 36 Mbps OFDM	4	10		-	dBm
	64QAM rate 1/2, 48 Mbps OFDM	0	5		-	dBm
	64QAM rate 3/4, 54 Mbps OFDM	-1	3		-	dBm
	MCS 0, BPSK rate 1/2	16	24		-	dBm
	MCS 1, QPSK rate 1/2	13	21		-	dBm
	MCS 2, QPSK rate 3/4	11	19		-	dBm
	MCS 3, 16QAM rate 1/2	8	16		-	dBm
	MCS 4, 16QAM rate 3/4	4	12		-	dBm
	MCS 5, 64QAM rate 2/3	0	7		-	dBm
	MCS 6, 64QAM rate 3/4	-1	5		-	dBm
	MCS 7, 64QAM rate 5/6	-2	3		-	dBm
Receiver residual PER	All rates, -50dBm input power	-	-		0.005	%

4.4 Wi-Fi 5GHz Band RF Transmitter Specifications

The specification in table below is measured at the antenna port, which includes the front-end loss.

Parameter	Description	Performance			
		Min	Typical	Max	Unit
Frequency range	Center channel frequency	5180	-	5825	MHz
Output power with spectral mask and EVM compliance	6 Mbps OFDM	-	14[1]	-	dBm
	54 Mbps OFDM	-	14[1]	-	dBm
	HT20 MCS 0	-	14[1]	-	dBm
	HT20 MCS 7	-	14[1]	-	dBm

4.4 Wi-Fi 5GHz Band RF Transmitter Specifications (continued)

Parameter	Description	Performance			
		Min	Typical	Max	Unit
Output power with spectral mask and EVM compliance (at -40°C and 85°C)	6 Mbps OFDM	-	13(1)	-	dBm
	54 Mbps OFDM	-	13(1)	-	dBm
	HT20 MCS 0	-	13(1)	-	dBm
	HT20 MCS 7	-	13(1)	-	dBm
TX EVM	6 Mbps OFDM	-	-	-5	dB
	54 Mbps OFDM	-	-	-25	dB
	HT20 MCS 0	-	-	-5	dB
	HT20 MCS 7	-	-	-28	dB
Output power variation(2)	TSSI closed-loop control across all temperature range and channels and VSWR≤1.5:1.	-1.5	-	1.5	dB
Carrier suppression		-	-	-30	dBc
Harmonic output power	2nd Harmonic	-	-45	-43	dBm/MHz
	3nd Harmonic	-	-45	-43	dBm/MHz

4.5 Wi-Fi RF Receiver Blocking Specifications

The specification in table below is measured at the antenna port, which includes the front-end loss.

Parameter	Description	Performance			
		Min	Typical	Max	Unit
Receiver in-band blocking(1) CW and BT interferers	2.4 GHz CW and BT interfering signal @ ±20MHz offset	-47	-	-	dBm
	2.4 GHz CW and BT interfering signal @ ±25MHz offset	-40	-	-	dBm
	5 GHz CW interfering signal @ ±20MHz offset	-35	-	-	dBm
Receiver out-band blocking(1) CW interferer	25 ≤ f < 2300 MHz	-28	-	-	dBm
	2300 ≤ f < 2395 MHz	-40	-	-	dBm
	2483.5 < f ≤ 2583.5 MHz	-45	-	-	dBm
Receiver out-band blocking(1) CDMA, GSM, DCS and PCS interferers(2)	CDMA UL: 824 – 849 MHz	-20	-	-	dBm
	CDMA DL: 869 – 894 MHz	-10	-	-	dBm
	GSM UL: 880 – 915 MHz	-10	-	-	dBm
	GSM DL: 925 – 960 MHz	-10	-	-	dBm
	DCS UL: 1710 – 1785 MHz	-13	-	-	dBm
	DCS DL: 1805 – 1880 MHz	-20	-	-	dBm
	PCS UL: 1850 – 1910 MHz	-20	-	-	dBm
	PCS DL: 1930 – 1990 MHz	-20	-	-	dBm
Receiver out-band blocking(1) WiFi interferers	5G receiver only, interfering signal: 2400 < f ≤ 2483.5 MHz	-20	-	-	dBm
	2G receiver only, interfering signal: 5125 < f ≤ 5850 MHz	-20	-	-	dBm

5. Electrical Characteristics

5.1 Absolute Maximum Rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.63	V
T_{STG}	Storage Temperature	-40 to +125	°C
V_{ESD}	ESD protection (human body model)	2000	V

5.2 Recommended Operating Range

Symbol	Rating	Min	Typical	Max	Unit
VDD33	3.3V supply	2.97	3.3	3.63	V
AVDD_3V3_RTC	RTC supply when using internal ring oscillator	2.5	3.3	3.63	V
	RTC supply when using crystal oscillator	2.0	3.3	3.63	V
$T_{AMBIENT}$	Ambient Temperature	-40	-	85	°C

5.3 DC Characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IL}	Input Low Voltage	LVTTL	-0.28	0.8	V
V_{IH}	Input High Voltage		2.0	3.63	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 4 to 16 mA	-0.28	0.4	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 4 to 16 mA	2.4	VDD33+0.33	V
R_{PU}	Input Pull-Up Resistance	PU=high, PD=low	40	190	kΩ
R_{PD}	Input Pull-Down Resistance	PU=low, PD=high	40	190	kΩ

5.4 Current consumption

****All data preliminary****

Power mode	Description	Details		Typical current consumption	Hardware wake-up latency
		Subsystem	Power state		
RTC mode	Only RTC domain is on. Memory is not retained, requires a cold boot to resume.	Pluton CM4 subsystem	Off	0.01mA or 0.02mA (*1)	24ms (crystal and PLL lock, PMU time
		CA7 subsystem	Off		
		CM4F I/O subsystems	Off		
		Wi-Fi subsystem	Off		
		Buses/peripherals	Off		
Worst-case power consumption, no Wi-Fi	All subsystems apart from Wi-Fi running at full speed	Pluton CM4 subsystem	On	220mA Worst case 380mA (*2)	N/A, 650us WiFi subsystem resume latency
		CA7 subsystem	On		
		IO 0/1 CM4 subsystems	On		
		Wi-Fi subsystem	Light sleep		
		Buses/peripherals (*3)	On		
Worst-case power consumption with Wi-Fi (*2)	All subsystems running at full speed, Wi-Fi very active	Pluton CM4 subsystem	On	520mA (*4) Worst case 750mA (*2)	N/A
		CA7 subsystem	On		
		IO 0/1 CM4 subsystems	On		
		Wi-Fi subsystem	On		
		Buses/peripherals (*3)	On		
		RF (A or G Band)	On		
		Flash (*5)	On		

Note *1: 0.01mA/0.02mA with/without external 3.3v source PMIC control switch respectively. See section 3.2.2 for more details.

Note *2: The current values are measured under typical case (TT silicon and 25C/1.15V) and the TDP (maximum thermal design power) includes simulation worst case condition (TT/125C/1.15V/MC99, MC99 is PTPX power simulation library).

Note *3: It depends on how busy the peripherals are and how they are configured.

Note *4: This data is based on 100% Wi-Fi transmission on the 5GHz band at 14dBm.

Note *5: Depends on I/O loading and flash power consumption.

5.5 Crystal Oscillator

The table below lists the requirement for the main crystal.

Parameter	Value
Frequency	When using I2S audio function: 26 or 52 MHz When not using I2S: 20, 26, 40, 52MHz.
Frequency stability	±10 ppm @ 25°C
Aging	±3 ppm/year

5.6 ADC Characteristics

The table below lists the requirement for the main crystal.

Symbol	Parameter	Min	Typical	Max	Unit
N	Resolution	-	12	-	bit
FC	Clock Rate	-	2	-	MHz
FS	Sampling Rate @ N-Bit (1)	-	2	-	MSPS
TS	Sample period	-	0.5	-	µS
VPP	Input Swing (4)	-	-	1.8	V
VIN	Input voltage (4)	0	-	1.8	V
SC	Sampling capacitance	-	4	-	pF
RIN	Input Impedance:				
	Unselected channel	400M	-	-	Ω
	Selected channel	-	10K	-	
	Dither waveform type	-	Sawtooth	-	
	RMS noise added at input (3)	0.2	0.3	0.4	LSB
	Dither step size (programmable)	0	4	4	LSB
Navg	Number of samples averaged in hardware (programmable) (5)	1	32	64	
Tdither	Dither period (level, programmable) (6)	1	16	16	TS (7)
	Dither magnitude	0	64	64	LSB
DNL	Differential nonlinearity without dithering and averaging	-	± 1	± 2	LSB
INL	Integral nonlinearity without dithering and averaging	-	± 2	± 4	LSB
DNLdither+ average	Differential nonlinearity with dithering and averaging	-	± 0.5	± 1	LSB
INLdither+ average	Integral nonlinearity with dithering and averaging	-	-	± 2	LSB
OE	Offset error	-	-	± 10	mV
FSE	Full swing error	-	-	± 50	mV
SNR	Signal-to-noise ratio (2)	60	63	66	dB
	Current consumption	-	-	400	µA
	Power-down current	-	-	1	µA

Note 1: Given that FS=2MHz.

Note 2: At 1kHz input frequency.

Note 3: Programmable by changing comparator tail current.

Note 4: 1.77V when dithering is on.

Note 5: Programmable number 1,2,4,8,16,32,64.

Note 6: Programmable number 1,2,4,8,16. The number of averaging should be equal or larger than the number of dithering level.

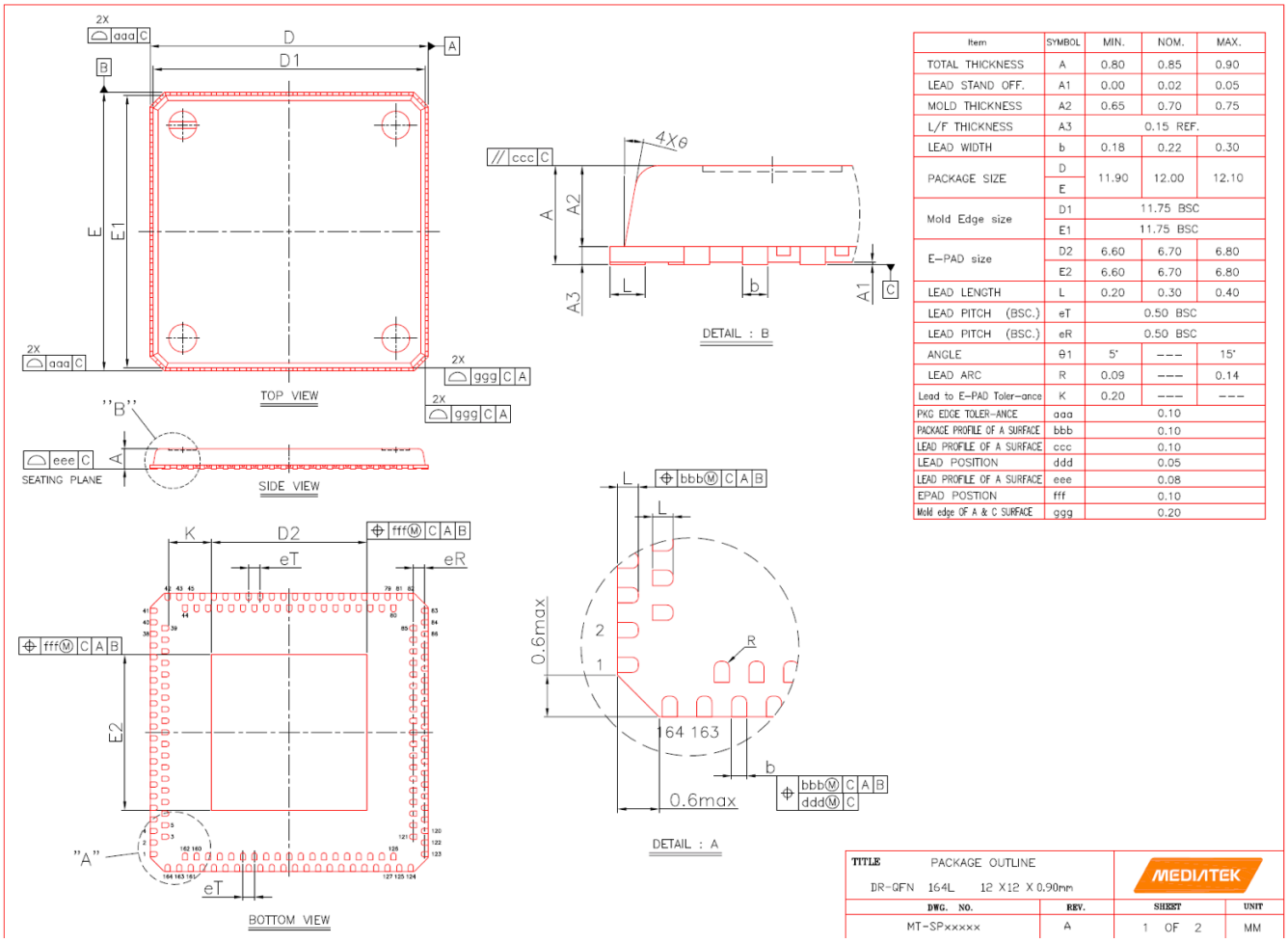
Note 7: TS = time of sampling period, i.e. 0.5us.

6. Packaging and Thermal Information

6.1 Package Drawing

MT3620 is packaged as a 164-pin 12mm x 12mm DR-QFN with a 6.7mm x 6.7mm central e-pad. The package diagram is shown below.

Figure 2.Package outline drawing



Item	SYMBOL	MIN.	NOM.	MAX.
TOTAL THICKNESS	A	0.80	0.85	0.90
LEAD STAND OFF.	A1	0.00	0.02	0.05
MOLD THICKNESS	A2	0.65	0.70	0.75
L/F THICKNESS	A3		0.15 REF.	
LEAD WIDTH	b	0.18	0.22	0.30
PACKAGE SIZE	D	11.90	12.00	12.10
	E			
Mold Edge size	D1		11.75 BSC	
	E1		11.75 BSC	
E-PAD size	D2	6.60	6.70	6.80
	E2	6.60	6.70	6.80
LEAD LENGTH	L	0.20	0.30	0.40
LEAD PITCH (BSC.)	eT		0.50 BSC	
LEAD PITCH (BSC.)	eR		0.50 BSC	
ANGLE	θ1	5°	---	15°
LEAD ARC	R	0.09	---	0.14
Lead to E-PAD Toler-ance	K	0.20	---	---
PKG EDGE TOLER-ANCE	aaa		0.10	
PACKAGE PROFILE OF A SURFACE	bbb		0.10	
LEAD PROFILE OF A SURFACE	ccc		0.10	
LEAD POSITION	ddd		0.05	
LEAD PROFILE OF A SURFACE	eee		0.08	
EPAD POSTION	fff		0.10	
Mold edge OF A & C SURFACE	ggg		0.20	

6.2 Top Mark

Figure 3. Top Mark

→ MTK part number
→ YYWW = date code, XXXX = MediaTek internal code
→ XXXXXXXXXXXX = main die lot number
→ XXXXXXXXXXXX = first flash die lot number
→ XXXXXXXXXXXX = second flash die lot number
→ Supplier information, XXXX = assembly house

6.3 Thermal Characteristics

Θ_{JC} assumes that all the heat is dissipated through the top of the package, while Jt assumes that the heat is dissipated through the top, sides, and the bottom of the package. Thus it's suggested to use Jt to estimate the junction temperature.

Symbol	Description	Performance	
		Typical	Unit
T_J	Maximum junction temperature (plastic package)	125	°C
Θ_{JA}	Junction to ambient temperature thermal resistance[1]	40	°C/W
Θ_{Jc}	Junction to case temperature thermal resistance	17.07	°C/W
Ψ_{Jt}	Junction to the package thermal resistance[2]	12.56	°C/W

Note:
[1] JEDEC 51-9 system FR4 PCB size: 101.5mm x 114.3mm
[2] 10.4mm x 10.4mm BGA package