

DESCRIPTION

The MP62071 Power Distribution Switch features internal current limiting to prevent damage to host devices due to faulty load conditions. The MP62071 operates from a 3.3V or 5V nominal input voltage and includes a 90mΩ Power MOSFET to handle up to 0.8A continuous load with a 1.25A typical current limit. The MP62071 has built-in protection for both over current and increased thermal stress. For over-current protection (OCP), the device will limit the current by going into a constant current mode.

When continuous output overload condition exceeds power dissipation of the package, the thermal protection will shut the part off. The device will recover once the device temperature reduces to approx 120°C.

The MP62071 is available in 8-PIN MSOP8E and SOIC8E package with exposed pad.

FEATURES

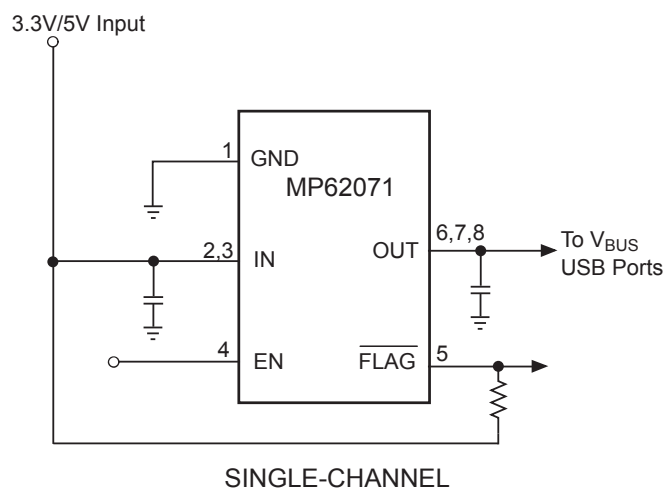
- 0.8A Continuous Current
- Accurate Current Limit
- 2.7V to 5.5V Supply Range
- 140uA Quiescent Current
- 90mΩ MOSFET
- Thermal-Shutdown Protection
- Under-Voltage Lockout
- 8ms FLAG Deglitch Time
- No FLAG Glitch During Power Up
- Reverse Current Blocking
- MSOP8E and SOIC8E package
- UL Recognized: E322138

APPLICATIONS

- Notebook PC
- Set-top-box
- Telecom and Network Systems
- PC Card Hot Swap
- USB Power Distribution

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TYPICAL APPLICATION



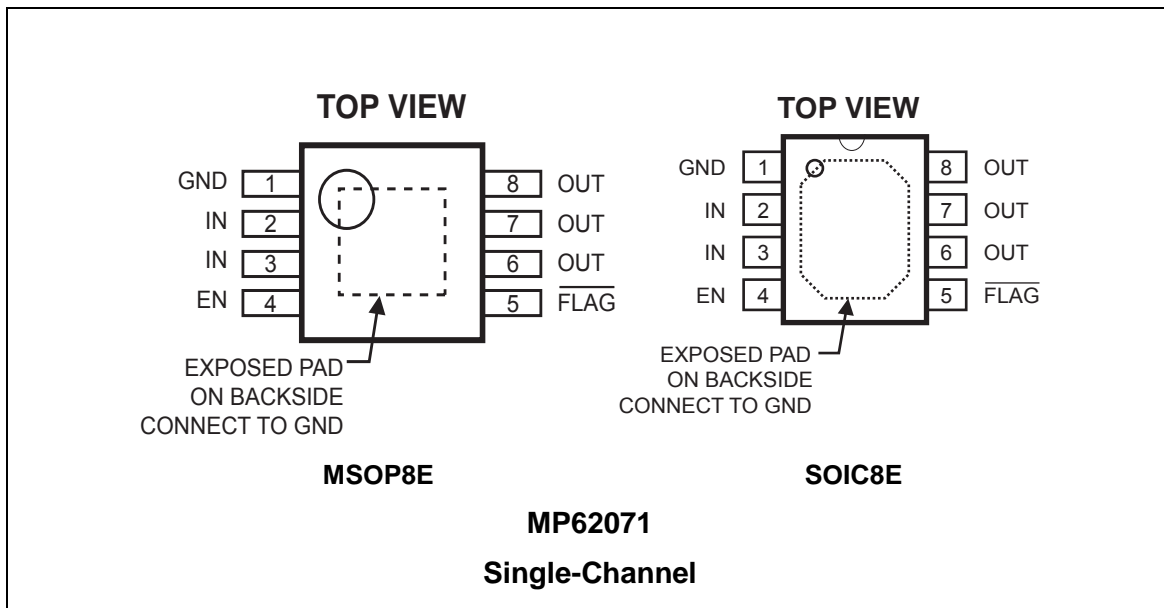
UL Recognized Component

ORDERING INFORMATION

Part Number *	Enable	Switch	Maximum Continuous Load Current	Typical Short-Circuit Current @ T _A =25°C	Package	Temperature
MP62071DH	Active High	Single	0.8A	1.25A	MSOP8E	-40°C to +85°C
MP62071DN	Active High	Single	0.8A	1.25A	SOIC8E	-40°C to +85°C

* For Tape & Reel, add suffix -Z (eg. MP62071DN-Z);
 For RoHS Compliant Packaging, add suffix -LF(eg. MP62071DN-LF-Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS ⁽¹⁾

IN.....	-0.3V to +6V
ON, FLAG, OUT to GND.....	-0.3V to +6V
Continuous Power Dissipation (T _A = +25°C) ⁽²⁾	
MSOP8E.....	2.3W
SOIC8E	2.5W
Junction Temperature.....	150°C
Lead Temperature	260°C
Storage Temperature.....	-65°C to +150°C
Operating Temperature.....	-40°C to +85°C

Thermal Resistance ⁽³⁾	θ_{JA}	θ_{JC}
MSOP8E	55	12... °C/W
SOIC8E	50	10... °C/W

Notes:

- Exceeding these ratings may damage the device.
- The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA} , and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D(MAX)=(T_J(MAX)-T_A)/ θ_{JA} . Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
- Measured on JESD51-7, 4-layer PCB..

ELECTRICAL CHARACTERISTICS ⁽⁴⁾

$V_{IN}=5V$, $T_A=+25^{\circ}C$, unless otherwise noted.

Parameter	Condition	Min	Typ	Max	Units
IN Voltage Range		2.7		5.5	V
Supply Current	EN=High, $I_{OUT}=0$		140	160	μA
Shutdown Current	Device Disable, $V_{OUT}=\text{float}$, $V_{IN}=5.5V$		1		μA
Off Switch Leakage	Device Disable, $V_{IN}=5.5V$		1		μA
Current Limit		1000	1250	1500	mA
Trip Current	Current Ramp (slew rate $\leq 100A/s$) on Output		1.45	1.9	A
Under-voltage Lockout	Rising Edge	1.95		2.65	V
Under-voltage Hysteresis			250		mV
FET On Resistance	$I_{OUT}=100mA$ and $-40^{\circ}C < T_A < 85^{\circ}C$		90	130	m Ω
EN Input Logic High Voltage		2			V
EN Input Logic Low Voltage				0.8	V
FLAG Output Logic Low Voltage	$I_{SINK}=5mA$			0.4	V
FLAG Output High Leakage Current	$V_{IN}=V_{FLAG}=5.5V$			1	μA
Thermal Shutdown			140		$^{\circ}C$
Thermal Shutdown Hysteresis			20		$^{\circ}C$
V_{OUT} Rising Time, T_r ⁽⁵⁾	$V_{IN}=5.5V$, $C_L=1\mu F$, $R_L=5\Omega$		0.9		ms
	$V_{IN}=2.7V$, $C_L=1\mu F$, $R_L=5\Omega$		1.7		ms
V_{OUT} Falling Time, T_f ⁽⁵⁾	$V_{IN}=5.5V$, $C_L=1\mu F$, $R_L=5\Omega$			0.5	ms
	$V_{IN}=2.7V$, $C_L=1\mu F$, $R_L=5\Omega$			0.5	ms
Turn On Time, T_{on} ⁽⁶⁾	$C_L=100\mu F$, $R_L=5\Omega$			3	ms
Turn Off Time, T_{off} ⁽⁶⁾	$C_L=100\mu F$, $R_L=5\Omega$			10	ms
FLAG Deglitch Time		4	8	15	ms
EN Input Leakage			1		μA
Reverse Leakage Current	OUT=5.5V, IN=GND		0.2		μA

NOTE:

- 4) Production test at $+25^{\circ}C$. Specifications over the temperature range are guaranteed by design and characterization.
 5) Measured from 10% to 90%.
 6) Measured from (50%) EN signal to (90%) output signal.

PIN FUNCTIONS

MSOP8E SOIC8E	Name	Description
1	GND	Ground.
2, 3	IN	Input Voltage. Accepts 2.7V to 5.5V input.
4	EN	Active High.
5	$\overline{\text{FLAG}}$	IN-to-OUT Over-current, active-low output flag. Open-Drain.
6, 7, 8	OUT	IN-to-OUT Power-Distribution Output (for all 3 output pins).

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = +25^\circ\text{C}$, unless otherwise noted.

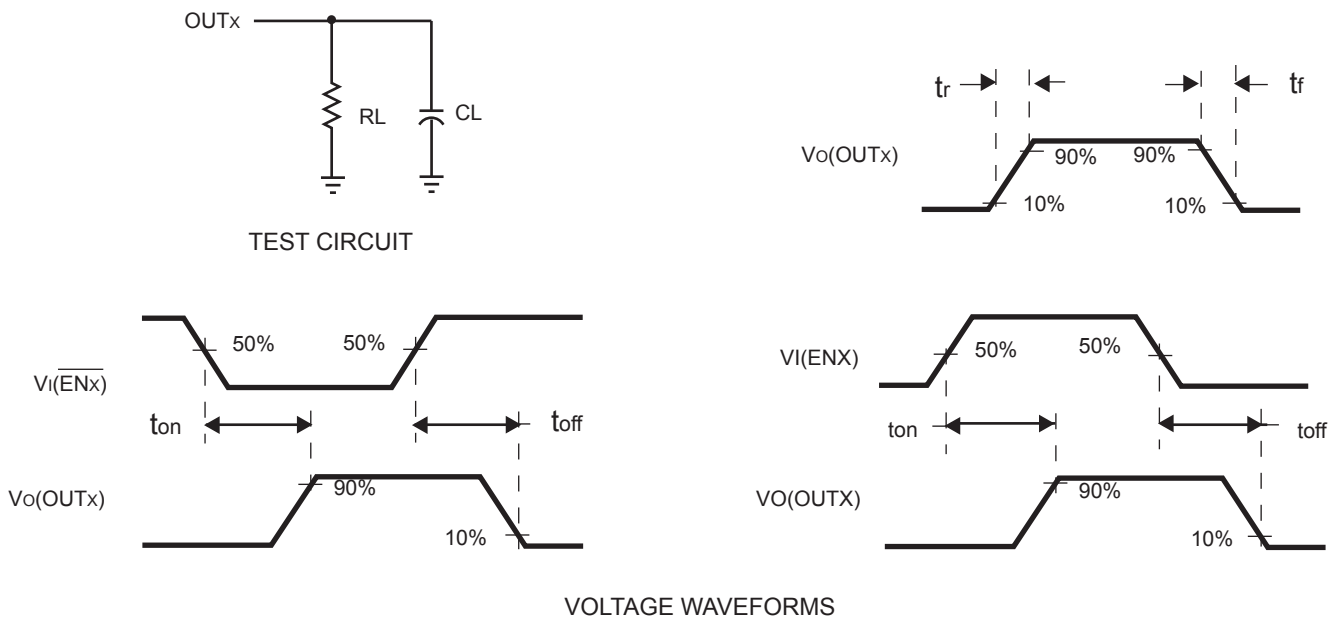


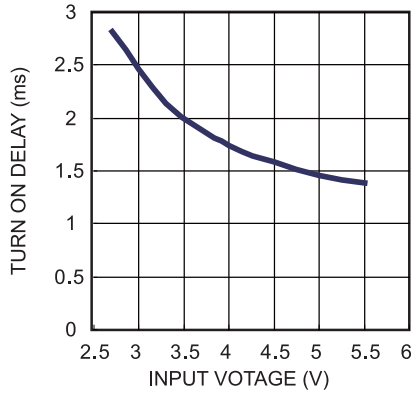
Figure 1—Test Circuit and Voltage Waveforms

TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = +25^\circ\text{C}$, $V_{IN}=5\text{V}$, $V_{EN}=5\text{V}$, $C_L=2.2\mu\text{F}$, unless otherwise noted.

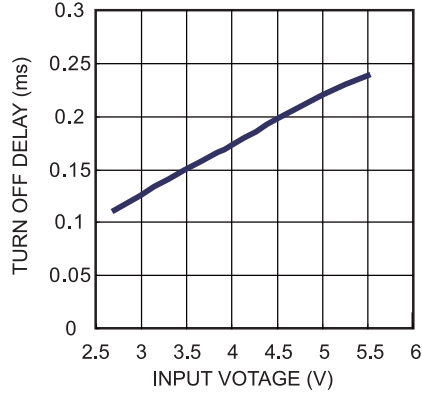
Turn on Delay vs. Input Voltage

$R_L=6.3\Omega$

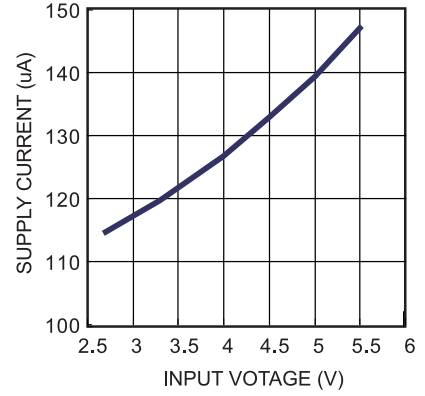


Turn off Delay vs. Input Voltage

$R_L=6.3\Omega$

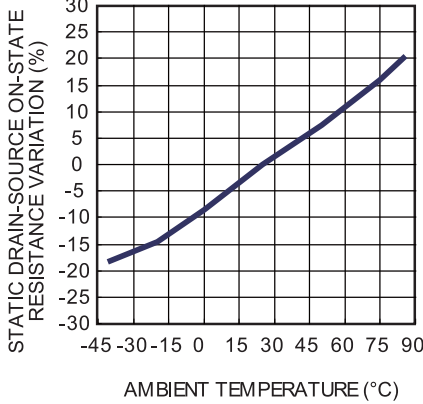


Supply Current, Output Enabled vs. Input Voltage



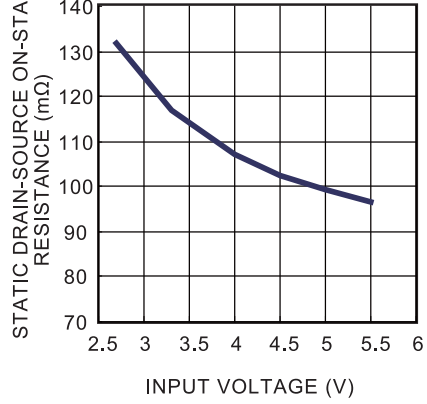
Static Drain-Source On-State Resistance Variation vs. Ambient Temperature

$I_O=0.1\text{A}$

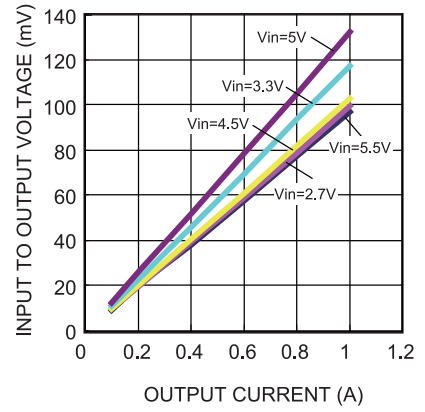


Static Drain-Source On-State Resistance vs. Input Voltage

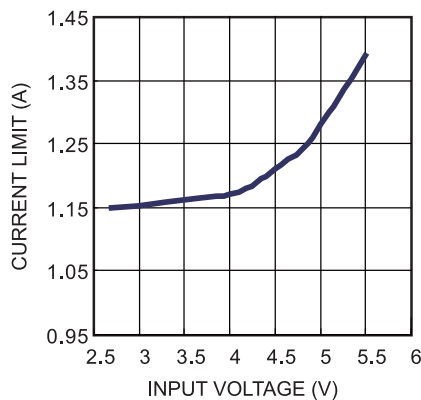
$I_{OUT}=0.8\text{A}$



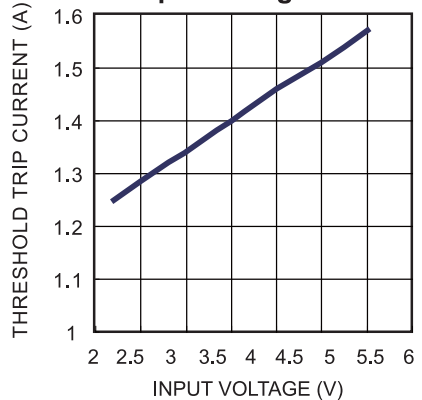
Input to Output Voltage vs. Load Current



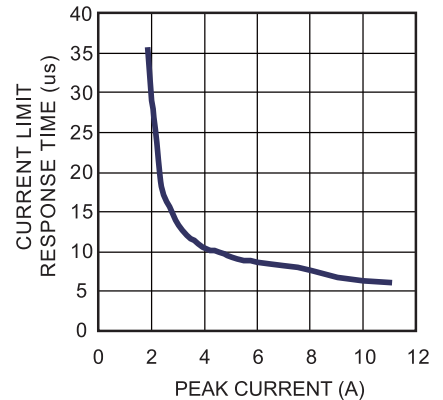
Current Limit vs. Input Voltage



Threshold Trip Current vs. Input Voltage



Current Limit Response Time vs. Peak Current

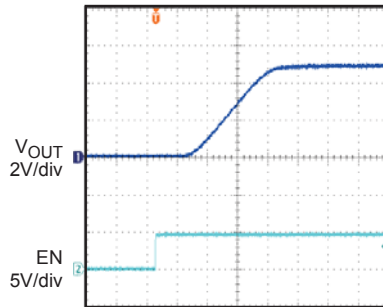


TYPICAL PERFORMANCE CHARACTERISTICS

$T_A = +25^\circ\text{C}$, $V_{IN}=5\text{V}$, $V_{EN}=5\text{V}$, $C_L=2.2\mu\text{F}$, unless otherwise noted. (continued)

Turn On Delay and Rise Time with 0.22 μF Load

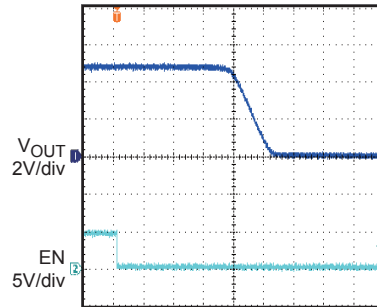
$C_L=0.22\mu\text{F}$



400us/div

Turn Off Delay and Fall Time with 0.22 μF Load

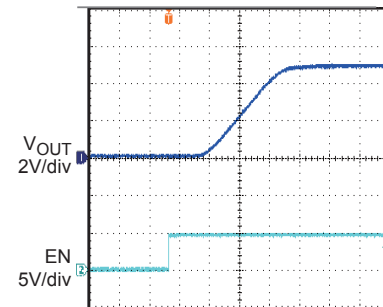
$C_L=0.22\mu\text{F}$



40us/div

Turn on Delay and Rise Time with 2.2 μF Load

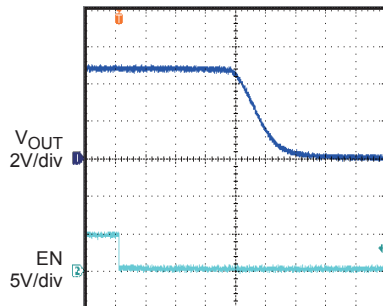
$R_L=6.3\Omega$, $C_L=2.2\mu\text{F}$



400us/div

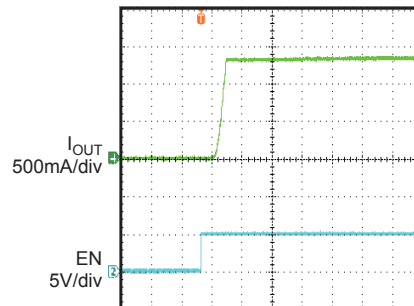
Turn off Delay and Fall Time with 2.2 μF Load

$R_L=6.3\Omega$, $C_L=2.2\mu\text{F}$



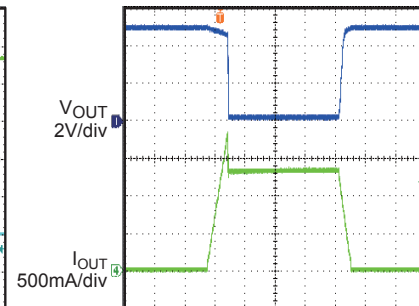
40us/div

Short Circuit Current, Device Enabled into Short



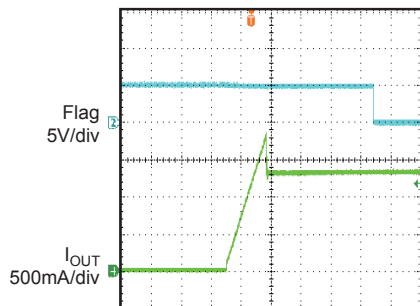
1ms/div

Threshold Trip Current with Ramped Load on Enabled Device



4ms/div

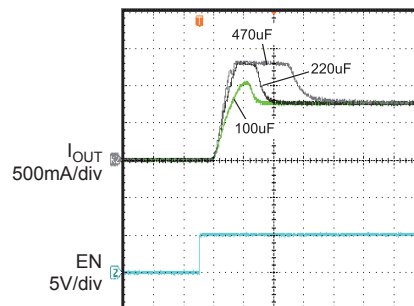
Ramped Load on Enabled Device



2ms/div

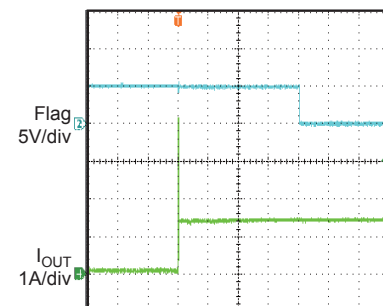
Inrush Current with Different Load Capacitance

$R_L=6.3\Omega$



1ms/div

1 Ω Load connected to Enabled Device



2ms/div

FUNCTION BLOCK DIAGRAM

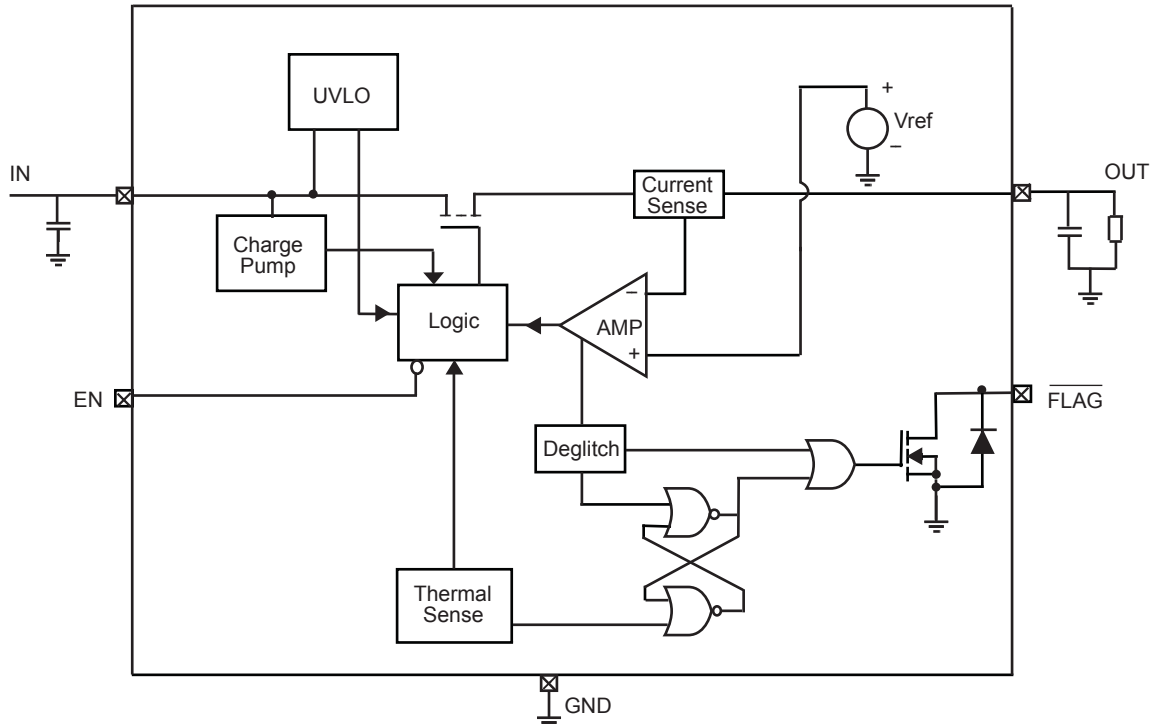


Figure2—Functional Block Diagram

DETAILED DESCRIPTION

Over Current

When the load exceeds trip current (minimum threshold current triggering constant-current mode) or a short is present, MP62071 switches into to a constant-current mode (current limit value). MP62071 will be shutdown only if the over current condition stays long enough to trigger thermal protection.

Trigger over current protection for different overload conditions occurring in applications:

- 1) The output has been shorted or overloaded before the device is enabled or input applied. MP62071 detects the short or overload and immediately switches into a constant-current mode.
- 2) A short or an overload occurs after the device is enabled. After the current-limit circuit has been tripped (reached the trip current threshold), the device switches into constant-current mode. However, high current may flow for a short period of time before the current-limit circuit can react.
- 3) Output current has been gradually increased beyond the recommended operating current. The load current rises until the trip current threshold is reached or until the thermal limit of the device is exceeded. MP62071 is capable of delivering current up to the trip current threshold without damaging the device. Once the trip threshold has been reached, the device switches into its constant-current mode.

Flag Response

The FLAG pin is an open drain configuration. This FAULT will report a fail mode after 8ms deglitch timeout. This is used to ensure that no false fault signals are reported. This internal deglitch circuit eliminates the need for extend components. The FLAG pin is not deglitched during over temperature or voltage lockout.

Thermal Protection

The purpose of thermal protection is to prevent damage in the IC by allowing excessive current to flow and heating the junction. The die temperature is internally monitored until the thermal limit is reached. Once this temperature is reached, the switch will turn off and allow the chip to cool. The switch has a built-in hysteresis.

Under-voltage Lockout (UVLO)

This circuit is used to monitor the input voltage to ensure that the MP62071 is operating correctly.

This UVLO circuit also ensures that there is no operation until the input voltage reaches the minimum spec.

Enable

The logic pin disables the switch to reduce overall supply current. Once the EN pin reaches Logic HIGH, the MP62071 is enabled.

APPLICATION INFORMATION

Power-Supply Considerations

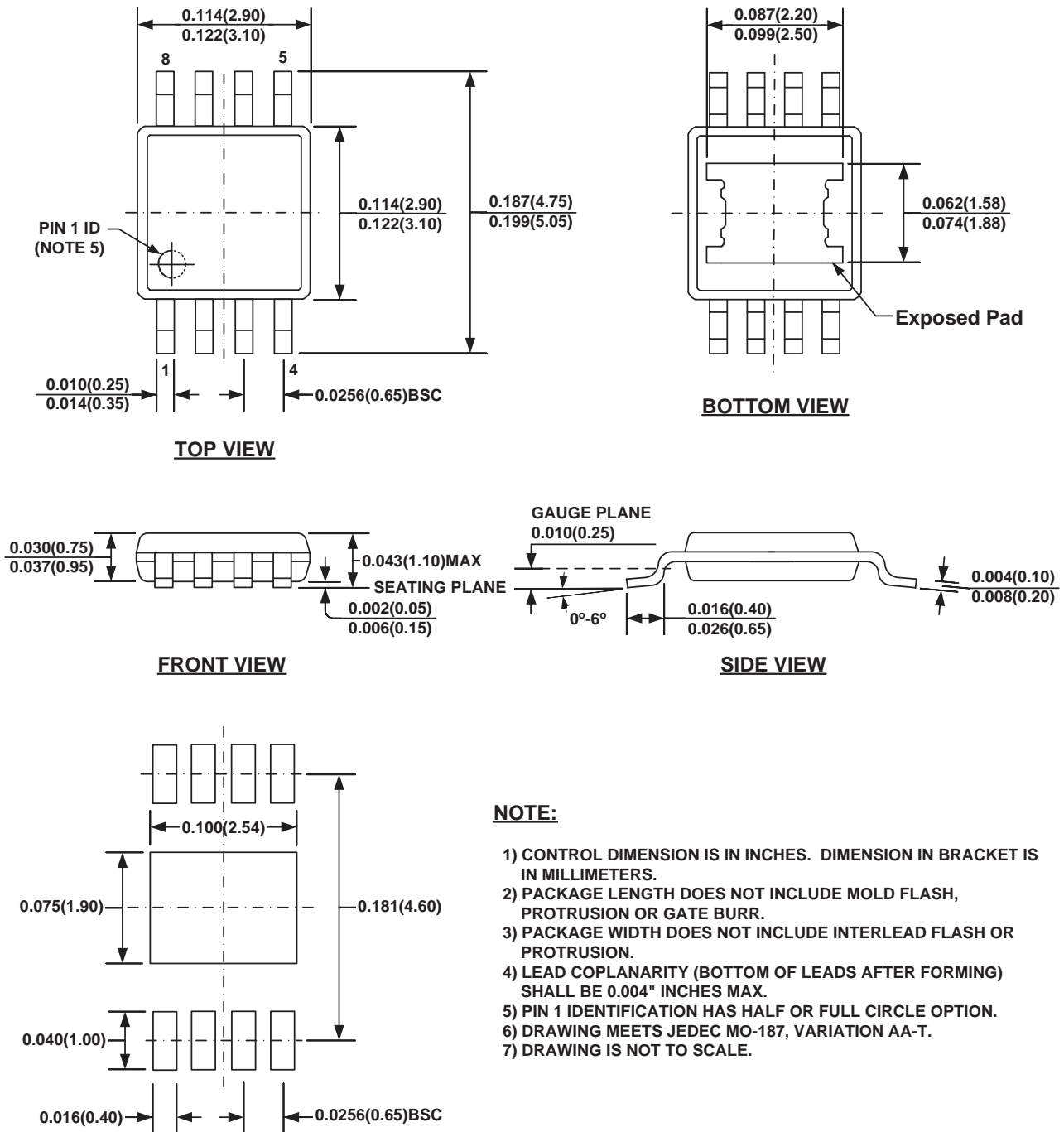
Over 10 μ F capacitor between IN and GND is recommended.

This precaution reduces power-supply transients that may cause ringing on the input and improves the immunity of the device to short-circuit transients.

In order to achieve smaller output load transient ripple, placing a high-value electrolytic capacitor on the output pin(s) is recommended when the load is heavy.

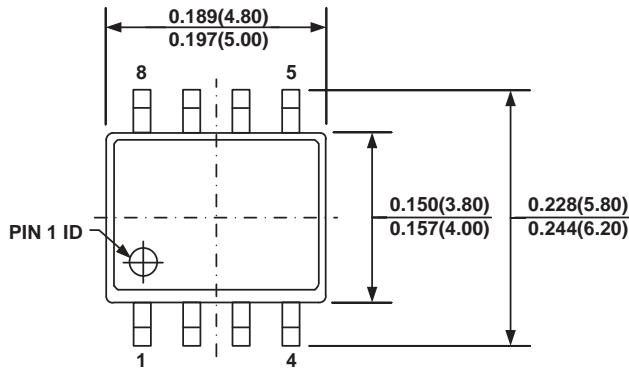
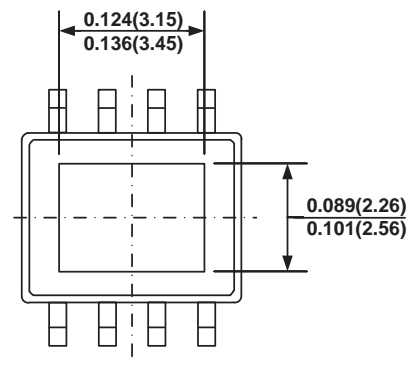
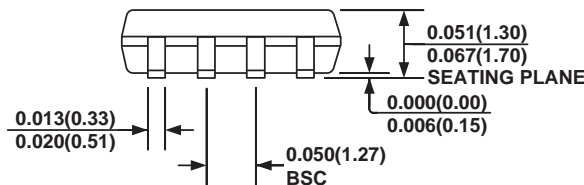
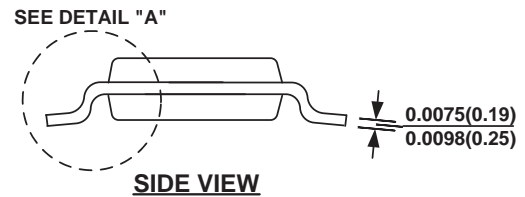
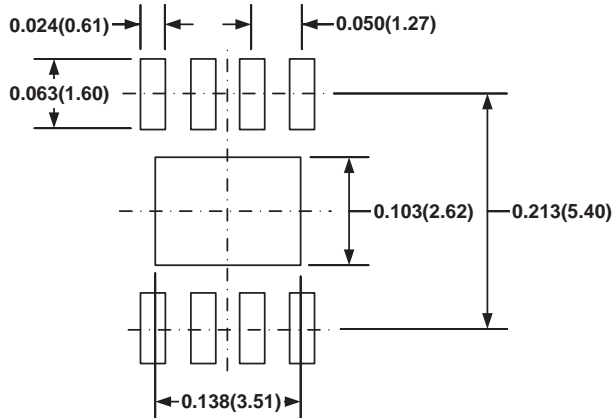
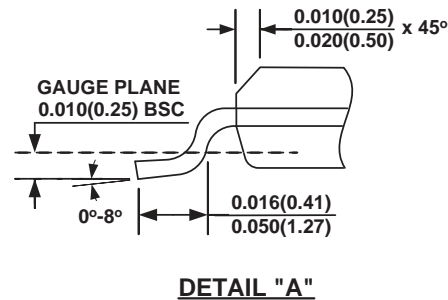
PACKAGE INFORMATION

MSOP8E (EXPOSED PAD)



NOTE:

- 1) CONTROL DIMENSION IS IN INCHES. DIMENSION IN BRACKET IS IN MILLIMETERS.
- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) PIN 1 IDENTIFICATION HAS HALF OR FULL CIRCLE OPTION.
- 6) DRAWING MEETS JEDEC MO-187, VARIATION AA-T.
- 7) DRAWING IS NOT TO SCALE.

SOIC8E (EXPOSED PAD)

TOP VIEW

BOTTOM VIEW

FRONT VIEW

SIDE VIEW

RECOMMENDED LAND PATTERN

DETAIL "A"
NOTE:

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- 2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
- 3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS.
- 4) LEAD COPLANARITY (BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.004" INCHES MAX.
- 5) DRAWING CONFORMS TO JEDEC MS-012, VARIATION BA.
- 6) DRAWING IS NOT TO SCALE.

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