

Features

- Supports up to 10 W Power
- Low Insertion Loss: 0.5 dB up to 2.7 GHz
- High Isolation: 23 dB up to 2.7 GHz
- RoHS* Compliant

Description

A broadband medium power switch element in a 1.9 x 1.1 mm DFN package. This device is electrical series and thermal direct to ground (EST2G). This device is designed for wireless infrastructure applications and test instruments. It is also suited for other applications from 100 MHz up to 10 GHz.



(2012)
Plastic Molded DFN

Electrical Specifications: $T_C = +25^\circ\text{C}$ (unless otherwise specified)

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Breakdown Voltage (V_{BR})	$I_R = 10 \mu\text{A}$	V	100	—	—
Lifetime (t)	$I_F = 10 \text{ mA}$, $I_R = 6 \text{ mA}$, 10% / 90%	ns	—	50	—
I-Region (w)	I-Layer	μm	—	8	—
Series Resistance (R_S)	$I_F = 100 \text{ mA}$	Ω	—	2	—
Junction Capacitance (C_J)	$V_R = -10 \text{ V}$, 1 MHz	pF	—	0.04	—
Insertion Loss (I_L)	$I_F = 50 \text{ mA}$, 2.3 ~ 2.7 GHz $I_F = 50 \text{ mA}$, <8 GHz	dB	—	0.40 0.75	0.6 1.0
Input Return Loss (IR_L)	$I_F = 50 \text{ mA}$, 2.3 ~ 2.7 GHz $I_F = 50 \text{ mA}$, <8 GHz	dB	20 12	25 15	—
Isolation (I_{SO})	$V_R = -10 \text{ mA}$, 2.3 ~ 2.7 GHz $V_R = -10 \text{ mA}$, <8 GHz	dB	20 11	23 14	—

* Restrictions on Hazardous Substances, European Union Directive 2011/65/EU.

Absolute Maximum Ratings^{1,2}

Parameter	Absolute Maximum
Breakdown Voltage (V_R)	100 V
Forward Current (I_F)	100 mA
Thermal Resistance (θ_{JC})	130°C/W
Junction Temperature (T_J)	175°C
Storage Temperature (T_{STG})	-65°C to +150°C
Mounting Temperature (T_{MTG})	+260°C per JEDEC STD-J-20C

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- MACOM does not recommend sustained operation near these survivability limits.

Handling Procedures

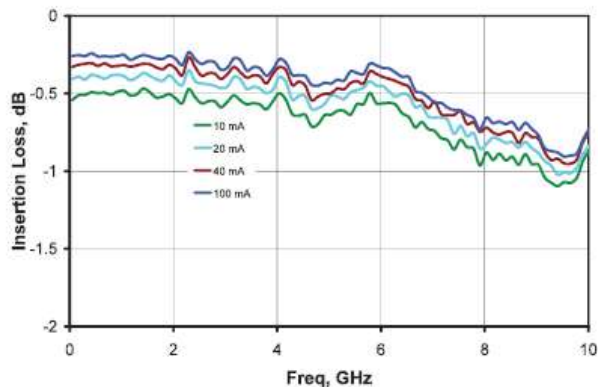
Please observe the following precautions to avoid damage:

Static Sensitivity

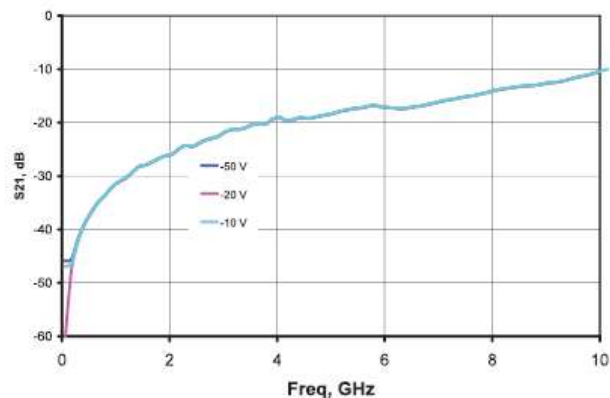
These electronic devices are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these Class 0 (HBM) devices.

Typical Performance Curves: $T_A = 25^\circ\text{C}$, $Z_O = 50 \Omega$, Small Signal

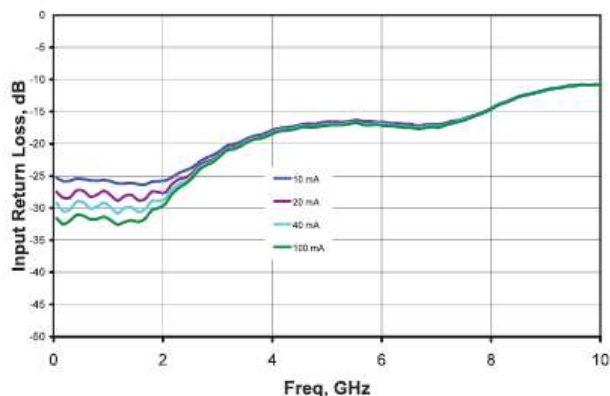
Insertion Loss



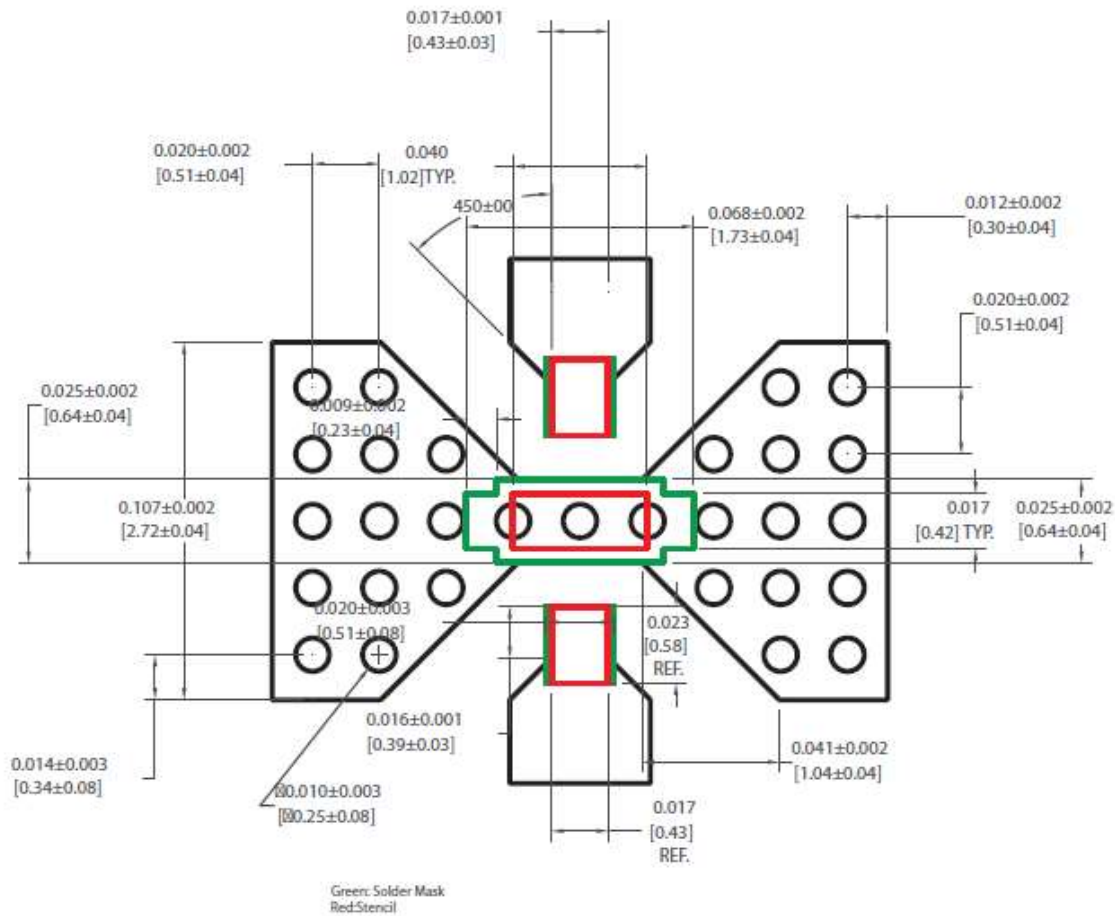
Isolation



Input Return Loss

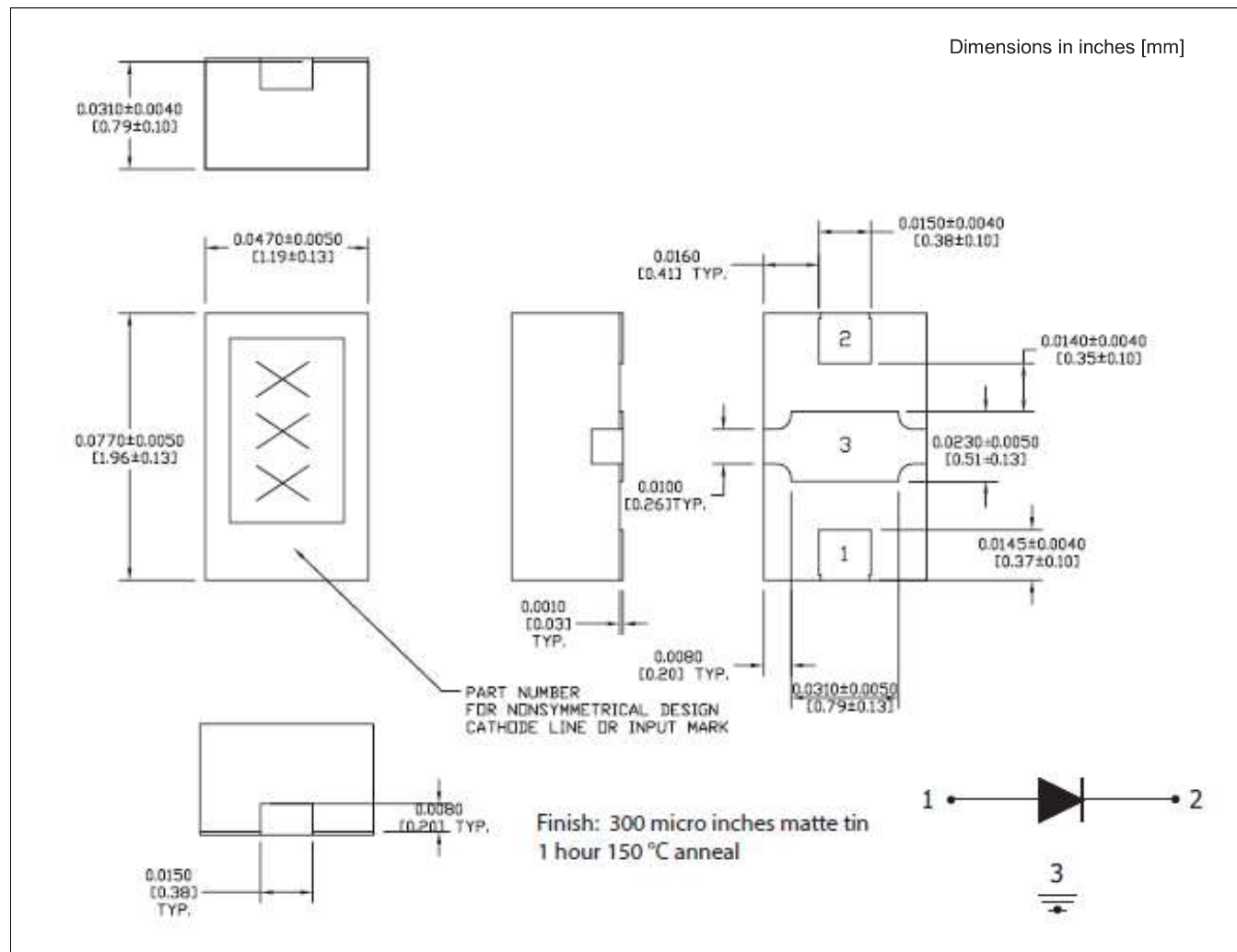


Printed Circuit Board Layout (Soldering Footprint)^{3,4,5,6}

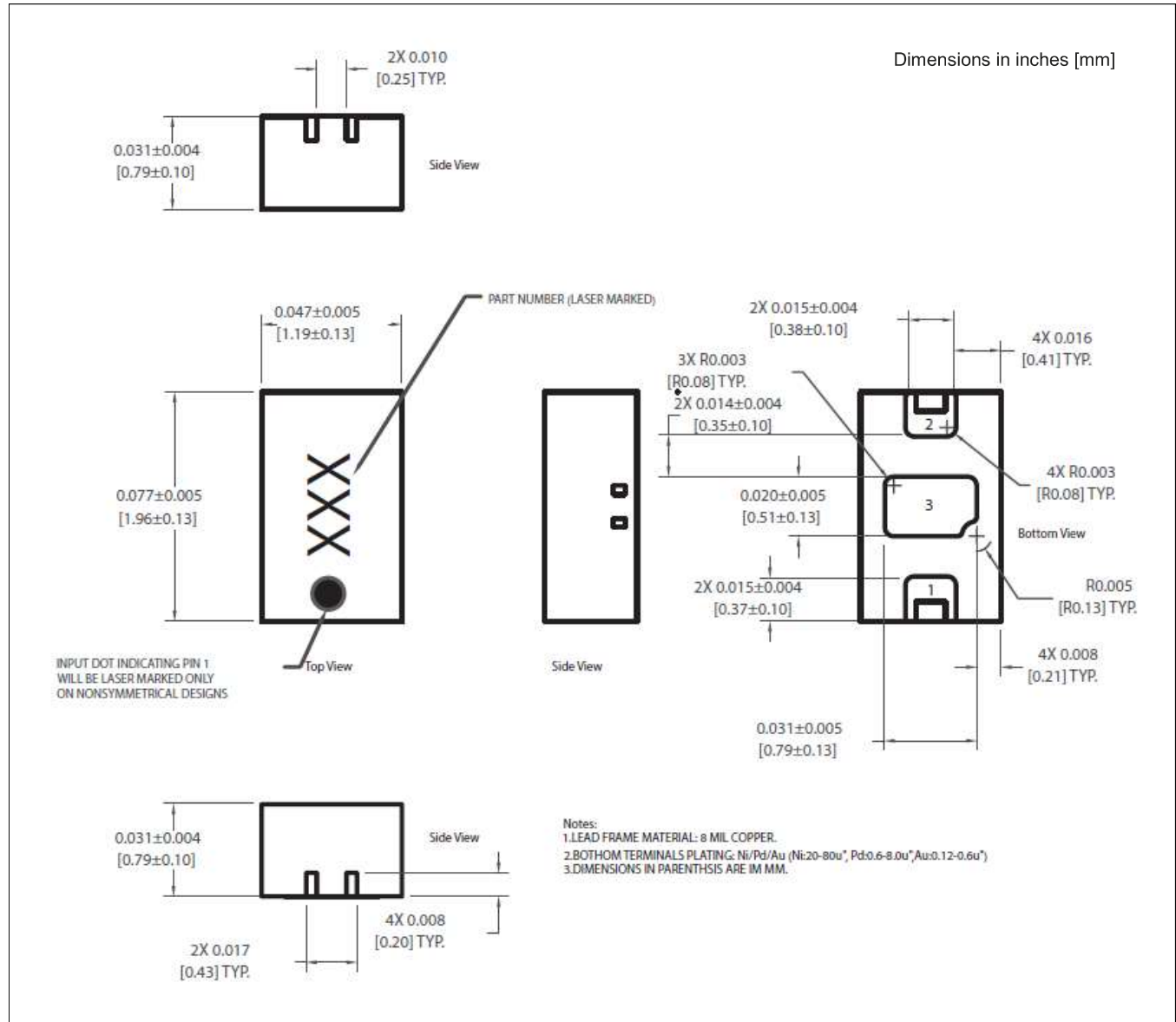


3. Unless otherwise specified: Tolerance ± 0.10 mm
4. If possible, use copper filled vias underneath pin 3 for better thermals; otherwise, use vias that are plated through, filled and plated over.
5. Solder mask should provide a 60 μ m clearance between copper pad and soldermask. Rounded package pads should have matching rounded solder mask openings.
6. Use circles or squares for thermal land stencil such that there is only 50% to 80% solder paste coverage

2012-0 Package Outline Before DC: 1528:



2012-1 Package Outline After DC: 1528:



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