

3-Channel 3-Level High-Speed Ultrasound Driver IC

Features

- Advanced CMOS Technology
- $\pm 4.5\text{V}$ to 12.5V Power Supply Voltage
- 2A Output Source and Sink Current
- 6.5 ns Rise and Fall Time with 1 nF Load
- 10 ns Propagation Delay
- ± 2 ns Matched Delay Times
- 12 Matched Channels
- 1.8V to 3.3V CMOS Logic Interface
- Smart Logic Threshold
- Low-Inductance Package

Applications

- Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Metal Flaw Detection
- Non-destructive Testing (NDT)

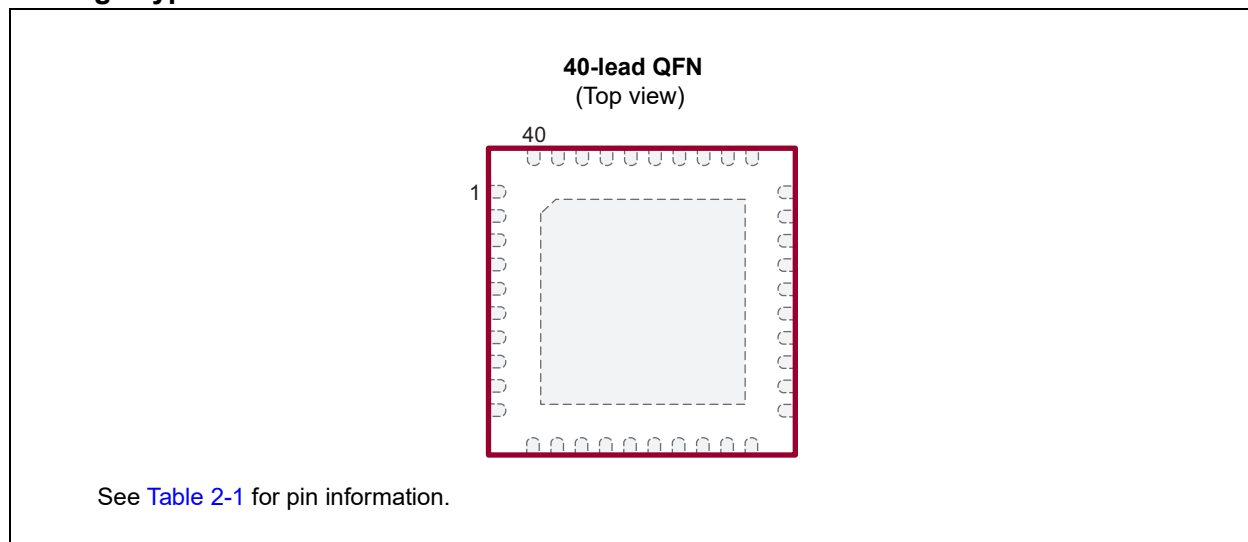
General Description

The MD1716, paired with Microchip's TC8020, forms a 3-channel 3-level high-voltage high-speed transmit pulser chip set. The chip set is designed for medical ultrasound imaging applications but can also be used for metal flaw detection, NDT, and piezoelectric transducer drivers.

The MD1716 is a 3-channel logic controller circuit with 12 low-impedance MOSFET gate drivers. There are three sets of control logic inputs—one for Channel A, one for Channel B, and one for Channel C. Each channel consists of two pairs of MOSFET gate drivers. These drivers are designed to match the drive requirements of Microchip's TC8020.

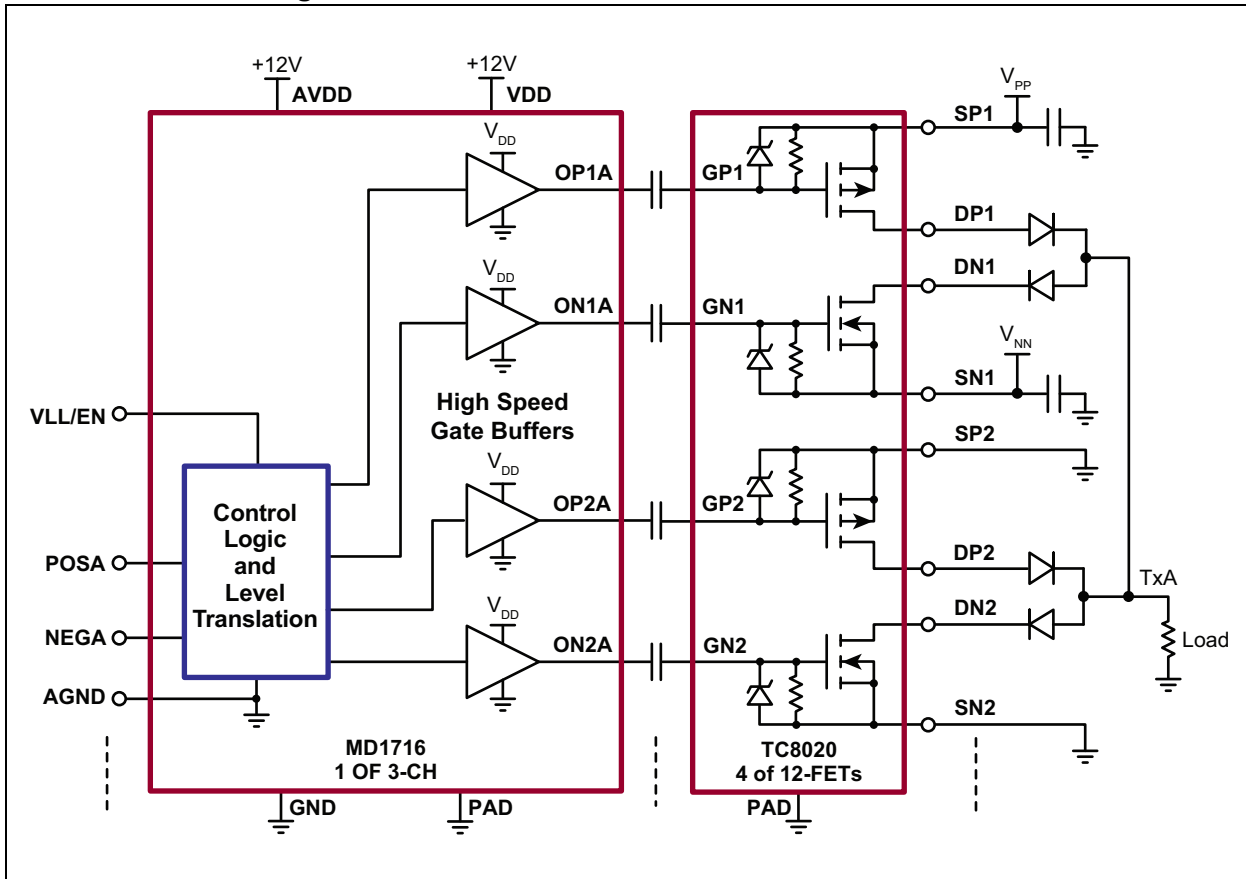
The TC8020 is the high-voltage output stage of the pulser with six pairs of MOSFETs. Each pair consists of a P-channel and an N-channel MOSFET. They are designed to have the same impedance and can provide typical peak currents of $\pm 3.5\text{A}$.

Package Type

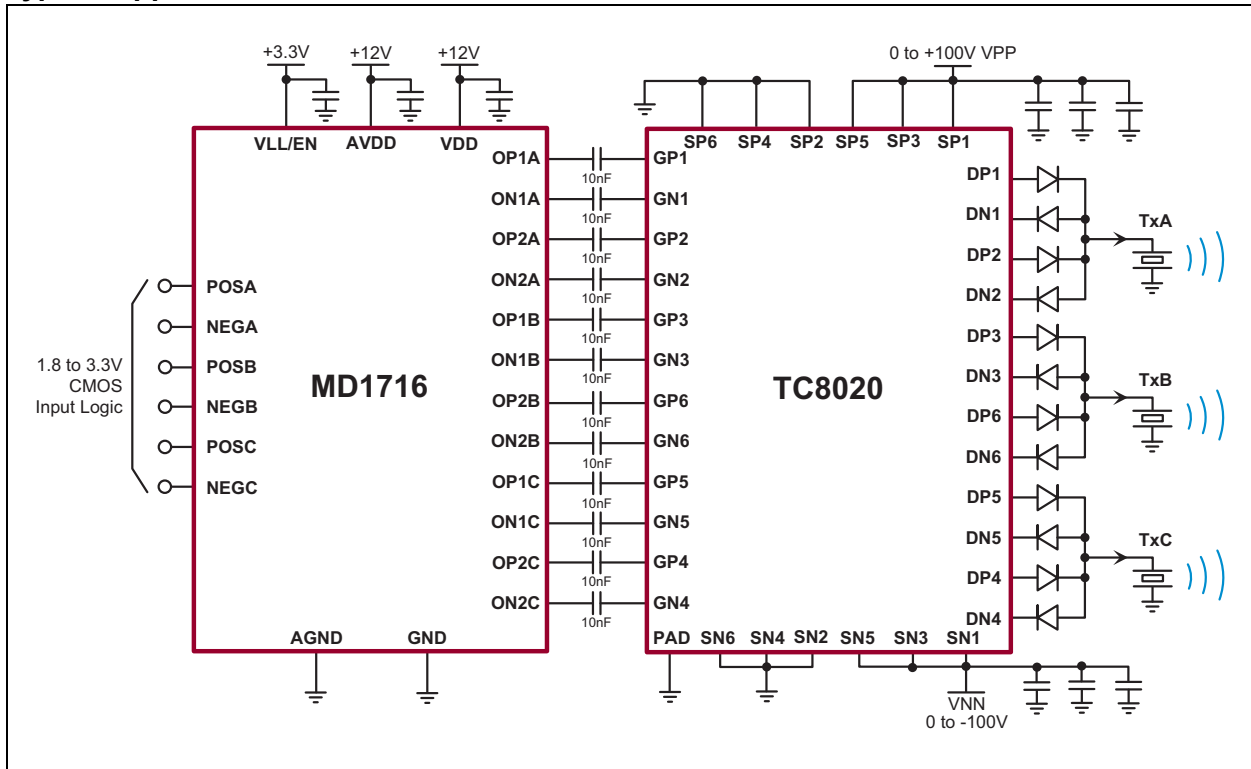


MD1716

Functional Block Diagram



Typical Application Circuit



MD1716

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings†

| | |
|---|-----------------|
| GND and AGND, Ground | 0V |
| Logic Input Pin, V_{LL} | -0.5V to +5.5V |
| Positive Gate Drive Supply, AV_{DD} , V_{DD1} , and V_{DD2} | -0.5V to +14.5V |
| Operating Junction Temperature, T_J | 0°C to +125°C |
| Storage Temperature, T_S | -65°C to +150°C |
| Power Dissipation: | |
| 40-lead QFN (Note 1) | 1.3W |

† **Notice:** Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note 1: 1 oz. four-layer 3 inches x 4 inches PCB

OPERATING SUPPLY VOLTAGES AND CURRENTS

Electrical Specifications for Operating Supply Currents: Over operating conditions unless otherwise specified.

$V_{LL} = 3.3V$, $AV_{DD} = V_{DD} = +12V$, and $T_A = 25^\circ C$

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|------------------------------|--------------|------|------|------|---------|---|
| Logic Supply | V_{LL} | 1.8 | 3.3 | 3.6 | V | |
| Positive Analog Supply | AV_{DD} | 4.75 | — | 12.9 | V | $AV_{DD} \geq V_{DD}$ |
| Positive Gate Drive Supply | V_{DD} | 4.75 | — | 12.9 | V | |
| Logic Reference Current | I_{VLL} | — | 10 | — | μA | $V_{LL} = 3.3V$ |
| AV_{DD} Power-Down Current | I_{AVDDQ} | — | 400 | — | μA | EN = 0, all inputs low |
| V_{DD} Power-Down Current | I_{VDDQ} | — | 50 | 100 | μA | |
| AV_{DD} Power-Up Current | I_{AVDDEN} | — | 2 | 3 | mA | EN = 1, all inputs low |
| V_{DD} Power-Up Current | I_{VDDEN} | — | 0.7 | 1 | mA | |
| AV_{DD} CW 5 MHz Current | I_{AVDDCW} | — | 10 | — | mA | All channels on at 5 MHz, no load, $V_{DD} = 5V$ |
| V_{DD} CW 5 MHz Current | I_{VDDCW} | — | 33 | — | mA | |

DC ELECTRICAL CHARACTERISTICS

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions | |
|--|-----------|--------------|------|----------|------|-------------------------------------|------------------------------|
| P-CHANNEL AND N-CHANNEL GATE DRIVER OUTPUTS | | | | | | | |
| Output Sink Resistance | P-Channel | R_{SINK} | — | — | 6 | Ω | $I_{SINK} = 100\text{ mA}$ |
| | N-Channel | | — | 3 | 6 | Ω | |
| Output Source Resistance | P-Channel | R_{SOURCE} | — | — | 6 | Ω | $I_{SOURCE} = 100\text{ mA}$ |
| | N-Channel | | — | 4 | 6 | Ω | |
| Peak Output Sink Current | P-Channel | I_{SINK} | 1.7 | 2 | — | A | |
| | N-Channel | | 1.7 | 2 | — | A | |
| Peak Output Source Current | P-Channel | I_{SOURCE} | 1.7 | 2 | — | A | |
| | N-Channel | | 1.7 | 2 | — | A | |
| LOGIC INPUTS | | | | | | | |
| Chip Disable Low Voltage | V_{ENL} | 0 | — | 0.3 | V | V_{LL}/EN is a dual function pin. | |
| Input Logic High Voltage | V_{IH} | $0.8 V_{LL}$ | — | V_{LL} | V | | |

DC ELECTRICAL CHARACTERISTICS (CONTINUED)

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|--------------------------|----------|------|------|--------------|---------|------------|
| Input Logic Low Voltage | V_{IL} | 0 | — | $0.2 V_{LL}$ | V | |
| Input Logic High Current | I_{IH} | — | — | 1 | μA | |
| Input Logic Low Current | I_{IL} | -1 | — | — | μA | |

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Over operating conditions unless otherwise specified. $V_{LL} = 3.3V$, $AV_{DD} = V_{DD} = +12V$, and $T_A = 25^\circ C$

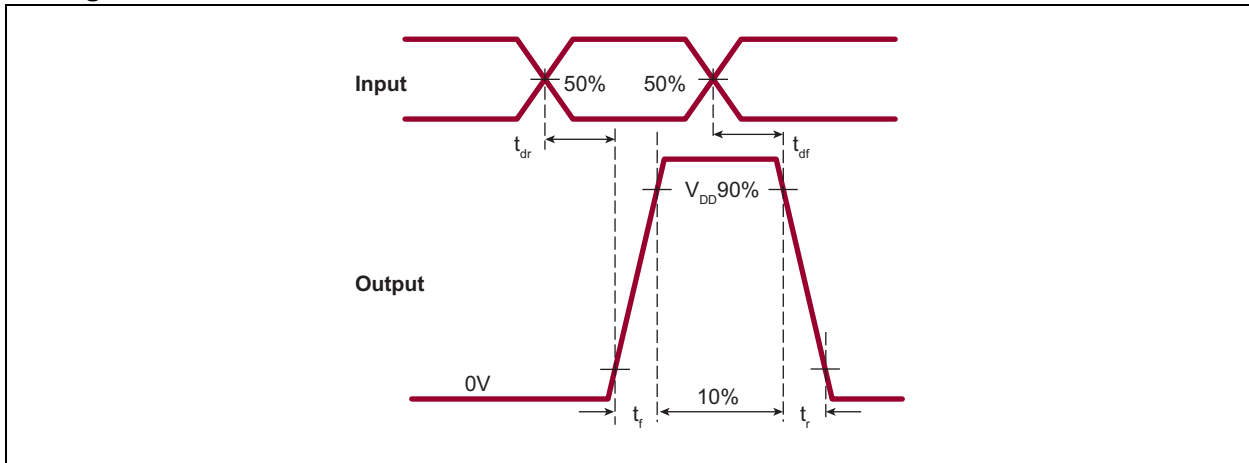
| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|-----------------------------|---------------------|------|---------|------|---------|--|
| Input Rise and Fall Time | t_{irf} | — | — | 10 | ns | Logic input edge speed requirement |
| Output Rise Time | t_r | — | 6.5 | — | ns | 1 nF load, input signal rise/fall time 2 ns (See Timing Waveforms.) |
| Output Fall Time | t_f | — | 6.5 | — | ns | |
| Output Rise Delay | t_{dr} | — | 10 | — | ns | 1 nF load, input signal rise/fall time 2 ns (See Timing Waveforms.) |
| Output Fall Delay | t_{df} | — | 10 | — | ns | |
| Rise and Fall Time Matching | $ t_r - t_f $ | — | 1 | — | — | For each channel |
| Propagation Delay Matching | $ t_{dr} - t_{df} $ | — | 1 | — | — | |
| Delay Time Matching | t_{dm} | — | ± 2 | — | ns | Channel to channel and device to device |
| Output Jitter | Δt_j | — | 20 | — | ps | $V_{DD} = 10V$ |
| IC Enable Time | t_{EN_ON} | — | — | 50 | μs | |
| IC Disable Time | t_{EN_OFF} | — | — | 2 | μs | |

TEMPERATURE SPECIFICATIONS

| Parameter | Sym. | Min. | Typ. | Max. | Unit | Conditions |
|-----------------------------------|---------------|------|------|------|--------------|------------|
| TEMPERATURE RANGE | | | | | | |
| Operating Junction Temperature | T_J | 0 | — | +125 | $^\circ C$ | |
| Storage Temperature | T_S | -65 | — | +150 | $^\circ C$ | |
| PACKAGE THERMAL RESISTANCE | | | | | | |
| 40-lead QFN | θ_{JA} | — | 24 | — | $^\circ C/W$ | |

MD1716

Timing Waveforms



2.0 PIN DESCRIPTION

The details on the pins of MD1716 are listed in [Table 2-1](#). See [Package Type](#) for the location of pins.

TABLE 2-1: PIN FUNCTION TABLE

| Pin Number | Pin Name | Description |
|------------|----------|--|
| 1 | POSA | POS input logic control for Channel A. See Table 3-1 for details. |
| 2 | NEGA | NEG input logic control for Channel A. See Table 3-1 for details. |
| 3 | POSB | POS input logic control for Channel B. See Table 3-2 for details. |
| 4 | VLL/EN | Logic high reference voltage and chip enable input |
| 5 | AVDD | Positive supply voltage of analog circuitry. AVDD should have the same or higher potential than the VDD. |
| 6 | AGND | Digital ground and connection of IC substrate |
| 7 | AGND | Digital ground and connection of IC substrate |
| 8 | NEGB | NEG input logic control for Channel B. See Table 3-2 for details. |
| 9 | POSC | POS input logic control for Channel C. See Table 3-3 for details. |
| 10 | NEGC | NEG input logic control for Channel C. See Table 3-3 for details. |
| 11 | VDD | Positive supply voltage of the gate drivers for the output stage in Channel A, Channel B, and Channel C |
| 12 | OP2C | Damping P-channel gate driver for Channel C |
| 13 | VDD | Positive supply voltage of the gate drivers for the output stage in Channel A, Channel B, and Channel C |
| 14 | GND | Power ground |
| 15 | OP1C | High-voltage output P-channel gate driver for Channel C |
| 16 | VDD | Positive supply voltage of the gate drivers for the output stage in Channel A, Channel B, and Channel C |
| 17 | ON2C | Damping N-channel gate driver for Channel C |
| 18 | GND | Power ground |
| 19 | VDD | Positive supply voltage of the gate drivers for the output stage in Channel A, Channel B, and Channel C |
| 20 | ON1C | High-voltage output N-channel gate driver for Channel C |
| 21 | GND | Power ground |
| 22 | ON2B | Damping N-channel gate driver for Channel B |
| 23 | GND | Power ground |
| 24 | OP2B | Damping P-channel gate driver for Channel B |
| 25 | VDD | Positive supply voltage of the gate drivers for the output stage in Channel A, Channel B, and Channel C |
| 26 | GND | Power ground |
| 27 | OP1B | High-voltage output P-channel gate driver for Channel B |
| 28 | VDD | Positive supply voltage of the gate drivers for the output stage in Channel A, Channel B, and Channel C |
| 29 | GND | Power ground |
| 30 | ON1B | High-voltage output N-channel gate driver for Channel B |

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TABLE 2-1: PIN FUNCTION TABLE (CONTINUED)

| Pin Number | Pin Name | Description |
|------------|-------------|---|
| 31 | ON2A | Damping N-channel gate driver for Channel A |
| 32 | VDD | Positive supply voltage of the gate drivers for the output stage in Channel A, Channel B, and Channel C |
| 33 | GND | Power ground |
| 34 | ON1A | High-voltage output N-channel gate driver for Channel A |
| 35 | VDD | Positive supply voltage of the gate drivers for the output stage in Channel A, Channel B, and Channel C |
| 36 | OP2A | Damping P-channel gate driver for Channel A |
| 37 | GND | Power ground |
| 38 | VDD | Positive supply voltage of the gate drivers for the output stage in Channel A, Channel B, and Channel C |
| 39 | OP1A | High-voltage output P-channel gate driver for Channel A |
| 40 | VDD | Positive supply voltage of the gate drivers for the output stage in Channel A, Channel B, and Channel C |
| Center Pad | Thermal pad | IC substrate. It must connect to GND externally. |

3.0 FUNCTIONAL DESCRIPTION

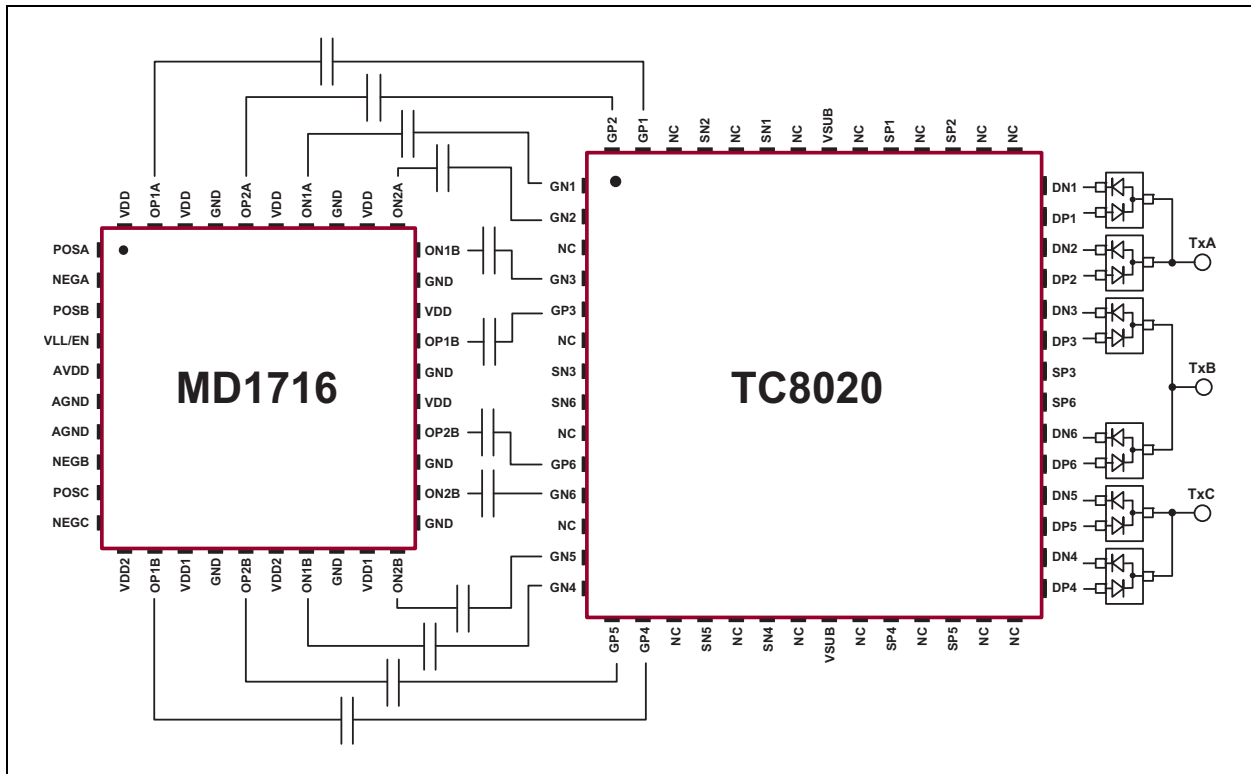


FIGURE 3-1: Circuit Pin Layout.

TABLE 3-1: TRUTH FUNCTION TABLE FOR CHANNEL A

| EN | Logic Inputs A | | SP1 to DP1 | SN1 to DN1 | SP2 to DP2 | SN2 to DN2 |
|----|----------------|------|------------|------------|------------|------------|
| | POSA | NEGA | | | | |
| 1 | 0 | 0 | OFF | OFF | ON | ON |
| 1 | 0 | 1 | OFF | ON | OFF | OFF |
| 1 | 1 | 0 | ON | OFF | OFF | OFF |
| 1 | 1 | 1 | OFF | OFF | OFF | OFF |

TABLE 3-2: TRUTH FUNCTION TABLE FOR CHANNEL B

| EN | Logic Inputs B | | SP3 to DP3 | SN3 to DN3 | SP6 to DP6 | SN6 to DN6 |
|----|----------------|------|------------|------------|------------|------------|
| | POSB | NEGB | | | | |
| 1 | 0 | 0 | OFF | OFF | ON | ON |
| 1 | 0 | 1 | OFF | ON | OFF | OFF |
| 1 | 1 | 0 | ON | OFF | OFF | OFF |
| 1 | 1 | 1 | OFF | OFF | OFF | OFF |

MD1716

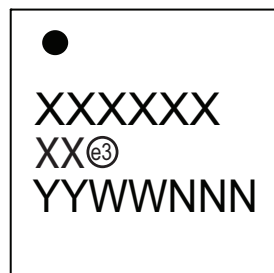
TABLE 3-3: TRUTH FUNCTION TABLE FOR CHANNEL B

| EN | Logic Inputs C | | SP5 to DP5 | SN5 to DN5 | SP4 to DP4 | SN4 to DN4 |
|-----|----------------|------|--|------------------|------------------|------------------|
| | POSC | NEGC | | | | |
| 1 | 0 | 0 | OFF | OFF | ON | ON |
| 1 | 0 | 1 | OFF | ON | OFF | OFF |
| 1 | 1 | 0 | ON | OFF | OFF | OFF |
| 1 | 1 | 1 | OFF | OFF | OFF | OFF |
| 0 | X | X | OFF | OFF | OFF | OFF |
| 0→1 | 0 | 0 | EN transitions from low to high or high to low should occur at all logic inputs low. | | | |
| 1→0 | 0 | 0 | | | | |

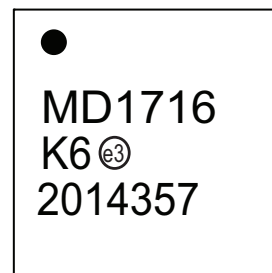
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

40-lead QFN



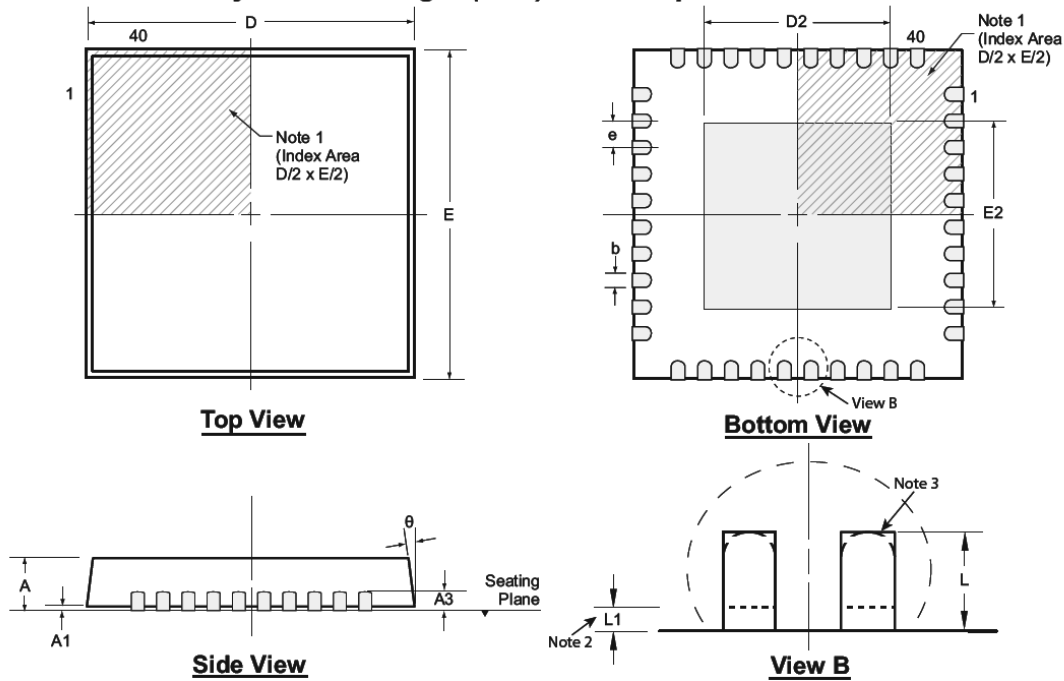
Example



| | | |
|----------------|--|--|
| Legend: | XX...X | Product Code or Customer-specific information |
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | ⓔ3 | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator (ⓔ3) can be found on the outer packaging for this package. |
| Note: | In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo. | |

MD1716

40-Lead QFN Package Outline (K6) 6.00x6.00mm body, 1.00mm height (max), 0.50mm pitch



Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier, an embedded metal marker, or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

| Symbol | A | A1 | A3 | b | D | D2 | E | E2 | e | L | L1 | θ° | |
|----------------|-----|------|------|----------|------|-------|------|-------|------|----------|-------------------|----------------|----|
| Dimension (mm) | MIN | 0.80 | 0.00 | 0.20 REF | 0.18 | 5.85* | 1.05 | 5.85* | 1.05 | 0.50 BSC | 0.30 [†] | 0.00 | 0 |
| | NOM | 0.90 | 0.02 | | 0.25 | 6.00 | - | 6.00 | - | | 0.40 [†] | - | - |
| | MAX | 1.00 | 0.05 | | 0.30 | 6.15* | 4.45 | 6.15* | 4.45 | | 0.50 [†] | 0.15 | 14 |

JEDEC Registration MO-220, Variation VJJD-6, Issue K, June 2006.

* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

APPENDIX A: REVISION HISTORY

Revision A (October 2020)

- Converted Supertex Doc# DSFP-MD1716 to Microchip DS20005924A
- Changed the package marking format
- Removed the 40-lead VQFN K6 M935 media type
- Made minor text changes throughout the document

MD1716

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| <u>PART NO.</u> | <u>XX</u> | - | <u>X</u> | - | <u>X</u> |
|-----------------|-----------------|---|---|---|------------|
| Device | Package Options | | Environmental | | Media Type |
| Device: | MD1716 | = | 3-Channel 3-Level High-Speed Ultrasound Driver IC | | |
| Package: | K6 | = | 40-lead VQFN | | |
| Environmental: | G | = | Lead (Pb)-free/RoHS-compliant Package | | |
| Media Types: | (blank) | = | 490/Tray for a K6 Package | | |

Example:

a) MD1716K6-G: 3-Channel 3-Level High-Speed Ultrasound Driver IC, 40-lead VQFN, 490/Tray

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