FUJITSU SEMICONDUCTOR
DATA SHEET

DS501-00054-1v0-E

Memory FRAM

8 M (512 K × 16) Bit

MB85R8M2T

■ DESCRIPTIONS

The MB85R8M2T is an FRAM (Ferroelectric Random Access Memory) chip consisting of 524,288 words × 16 bits of nonvolatile memory cells fabricated using ferroelectric process and silicon gate CMOS process technologies.

The MB85R8M2T is able to retain data without using a back-up battery, as is needed for SRAM.

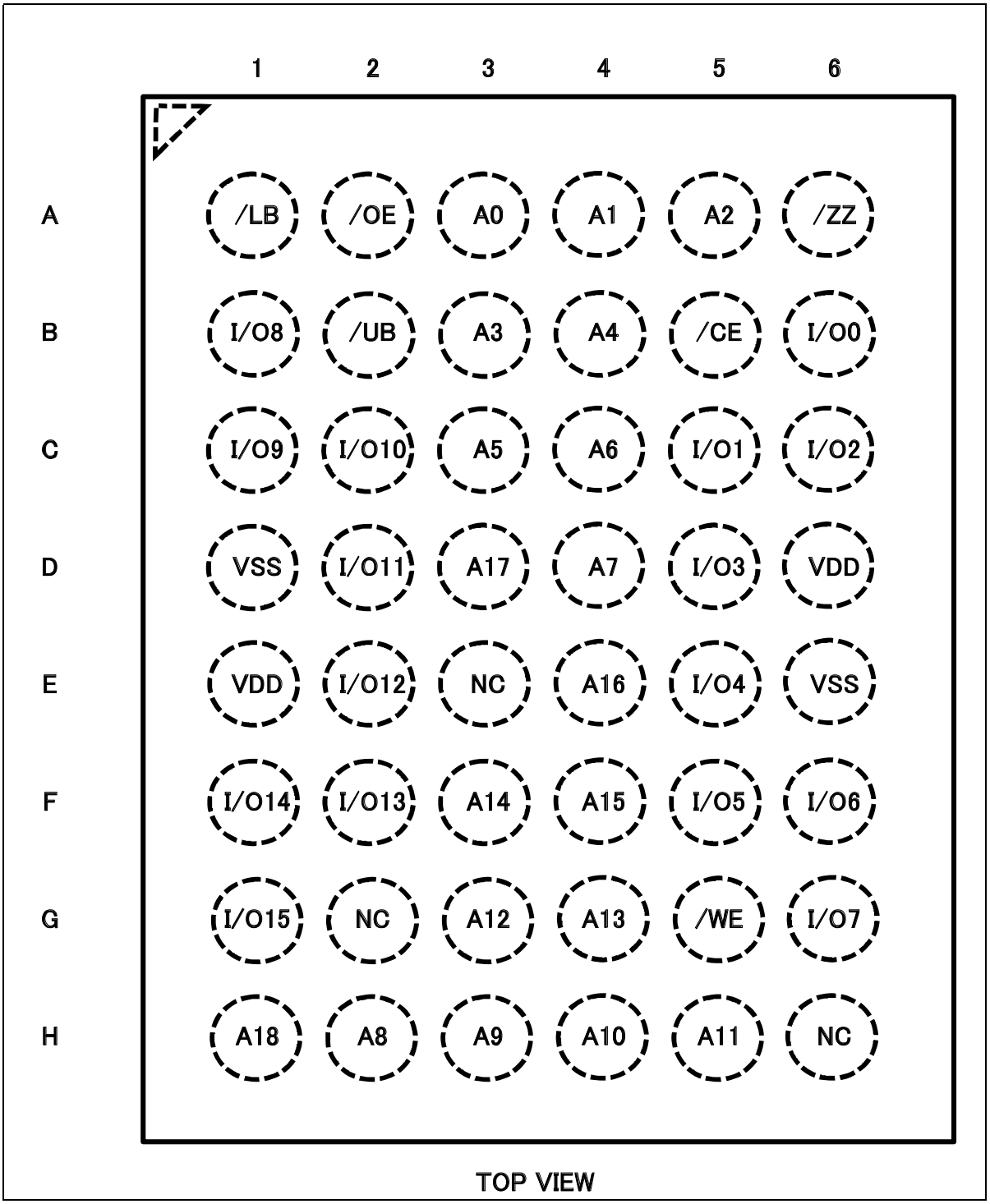
The memory cells used in the MB85R8M2T can be used for 10^{13} read/write operations, which is a significant improvement over the number of read and write operations supported by Flash memory and E2PROM. The MB85R8M2T uses a pseudo-SRAM interface.

■ FEATURES

• Bit configuration	: 524,288 words × 16 bits
• Read/write endurance	: 10^{13} times / 16 bits
• Data retention	: 10 years (+ 85 °C), 95 years (+ 55 °C), over 200 years (+ 35 °C)
• Operating power supply voltage	: 1.8 V to 3.6 V
• Low power operation	: Operating power supply current 20 mA (Max) Standby current 300 μA (Max) Sleep current 40 μA (Max)
• Operation ambient temperature range	: − 40 °C to + 85 °C
• Package	: 48-pin plastic FBGA (BGA-48P-M24) RoHS compliant

2018.05

■ PIN ASSIGNMENTS

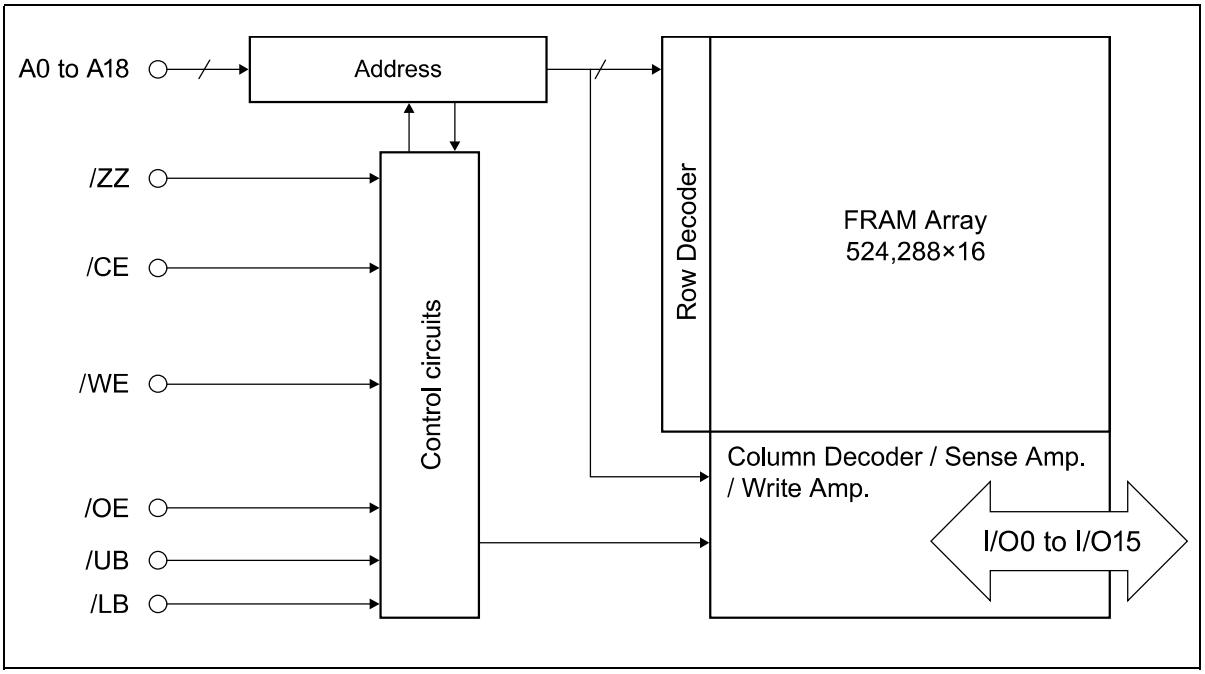


■ PIN DESCRIPTIONS

Pin Number	Pin Name	Functional Description
A3,A4,A5,B3,B4,C3, C4,D4,H2,H3,H4,H5, G3,G4,F3,F4,E4,D3, H1	A0 to A18	Address Input pins Select 524,288 words in FRAM memory array by 19 Address Input pins. When these address inputs are changed during /CE equals to “L” level, reading operation of data selected in the address after transition will start.
B6,C5,C6,D5,E5,F5, F6,G6,B1,C1,C2,D2 E2,F2,F1,G1	I/O0 to I/O15	Data Input/Output pins These are 16 bits bidirectional pins for reading and writing.
B5	/CE	Chip Enable Input pin In case the /CE equals to “L” level and /ZZ equals to “H” level, device is activated and enables to start memory access. In writing operation, input data from I/O pins are latched at the rising edge of /CE and written to FRAM memory array.
G5	/WE	Write Enable Input pin Writing operation starts at the falling edge of /WE. Input data from I/O pins are latched at the rising edge of /WE and written to FRAM memory array.
A2	/OE	Output Enable Input pin When the /OE is “L” level, valid data are output to data bus. When the /OE is “H” level, all I/O pins become high impedance (High-Z) state.
A6	/ZZ	Sleep Mode Input pin When the /ZZ becomes to “L” level, device transits to the Sleep Mode. During reading and writing operation, /ZZ pin shall be hold “H” level.
A1,B2	/LB, /UB	Lower/Upper byte Control Input pins In case /LB or /UB equals to “L” level, it enables reading/writing operation of I/O0 to I/O7 or I/O8 to I/O15 respectively. In case /LB and /UB equal to “H” level, all I/O pins become High-Z state.
D6,E1	VDD	Supply Voltage pins Connect all two pins to the power supply.
D1,E6	VSS	Ground pins Connect all two pins to ground.

Note: Please refer to the timing diagram for functional description of each pin.

■ BLOCK DIAGRAM



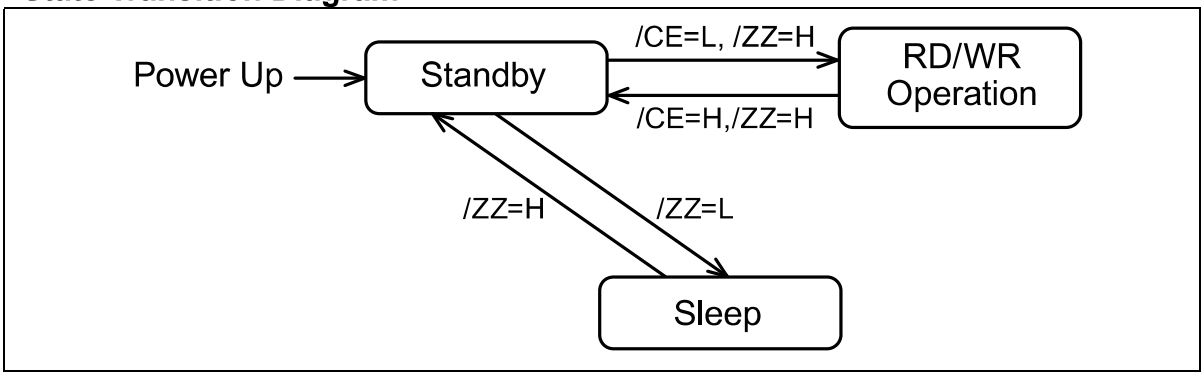
■ FUNCTIONAL TRUTH TABLE

Operation Mode	/CE	/WE	/OE	A0 to A17	/ZZ
Sleep	×	×	×	×	L
Standby	H	×	×	×	H
Read	↓	H	L	H or L	H
Address Access Read	L	H	L	↑ or ↓	H
Write(/CE Control)*1	↓	L	×	H or L	H
Write(/WE Control)*1*2	L	↓	×	H or L	H
Address Access Write*1*3	L	↓	×	↑ or ↓	H
Pre-charge	↑	×	×	×	H

Note: H= “H” level, L= “L” level, ↑= Rising edge, ↓= Falling edge, ×= H, L, ↓ or ↑

*1: In writing cycle, input data is latched at early rising edge of /CE or /WE.
*2: In writing sequence of /WE control, there exists time with data output of reading cycle at the falling edge of /CE.
*3: In writing sequence of Address Access Write, there exists time with data output of reading cycle at the address transition.

■ State Transition Diagram



■ FUNCTIONAL TRUTH TABLE OF BYTE CONTROL

Operation Mode	/WE	/OE	/LB	/UB	I/O0 to I/O7	I/O8 to I/O15
Read(Without Output)	H	H	×	×	Hi-Z	Hi-Z
	H	×	H	H	Hi-Z	Hi-Z
Read(I/O8 to I/O15)	H	L	H	L	Hi-Z	Output
Read(I/O0 to I/O7)			L	H	Output	Hi-Z
Read(I/O0 to I/O15)			L	L	Output	Output
Write(I/O8 to I/O15)	↑	×	H	L	×	Input
Write(I/O0 to I/O7)			L	H	Input	×
Write(I/O0 to I/O15)			L	L	Input	Input

Note: H= “H” level, L= “L” level, ↑= Rising edge, ↓= Falling edge, ×= H, L, ↓ or ↑
Hi-Z= High Impedance

In case the byte reading or writing are not selected, /LB and /UB pins shall be connected to GND pin.
In case the byte writing, while /CE=L, please don’t switch /LB and /UB.

■ ABABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating		Unit
		Min	Max	
Power Supply Voltage*	V_{DD}	− 0.5	+ 4.0	V
Input Pin Voltage*	V_{IN}	− 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Output Pin Voltage*	V_{OUT}	− 0.5	V_{DD} + 0.5 (≤ 4.0)	V
Operation Ambient Temperature	T_A	− 40	+ 85	°C
Storage Temperature	Tstg	− 55	+ 125	°C

* : All voltages are referenced to VSS (ground 0 V).

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

■ RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Power Supply Voltage*1	V_{DD}	1.8	3.3	3.6	V
Operation Ambient Temperature*2	T_A	− 40	—	+ 85	°C

*1: All voltages are referenced to VSS (ground 0 V).

*2: Ambient temperature when only this device is working. Please consider it to be the almost same as the package surface temperature.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

■ ELECTRICAL CHARACTERISTICS

1. DC Characteristics

(within recommended operating conditions)

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Leakage Current	$\|I_{LI}\|$	V_{IN} = 0V to V_{DD}	—	—	5	µA
Output Leakage Current	$\|I_{LO}\|$	V_{OUT} = 0V to V_{DD} /CE = V_{IH} or /OE = V_{IH}	—	—	5	µA
Operating Power Supply Current*1	I_{DD}	/CE = 0.2 V, I_{out} = 0 mA	—	15	20	mA
Standby Current	I_{SB}	/ZZ ≥ V_{DD} − 0.2V /CE, /WE, /OE ≥ V_{DD} − 0.2V /LB, /UB ≥ V_{DD} − 0.2V Others ≥ V_{DD} − 0.2V or ≤ 0.2V	—	60	300	µA
Sleep Current	I_{ZZ}	/ZZ = V_{SS} /CE, /WE, /OE ≥ V_{DD} − 0.2V /LB, /UB ≥ V_{DD} − 0.2V Others ≥ V_{DD} − 0.2V or ≤ 0.2V	—	10	40	µA
High Level Input Voltage	V_{IH}	V_{DD} = 1.8V to 3.6V	V_{DD} × 0.8	—	V_{DD} + 0.3	V
Low Level Input Voltage	V_{IL}	V_{DD} = 1.8V to 3.6V	− 0.3	—	V_{DD} × 0.17	V
High Level Output Voltage	V_{OH1}	V_{DD} = 2.7V to 3.6V I_{OH} = − 1.0mA	V_{DD} × 0.8	—	—	V
	V_{OH2}	V_{DD} = 1.8V to 2.7V I_{OH} = − 100µA	V_{DD} − 0.2	—	—	
Low Level Output Voltage	V_{OL1}	V_{DD} = 2.7V to 3.6V I_{OL} = 2.0mA	—	—	0.4	V
	V_{OL2}	V_{DD} = 1.8V to 2.7V I_{OL} = 150µA	—	—	0.2	

*1: During the measurement of I_{DD}, all Address and I/O were taken to only change once per active cycle.
Iout : output current

2. AC Characteristics

▪ AC Test Conditions

Power Supply Voltage	: 1.8 V to 3.6 V
Operation Ambient Temperature	: − 40 °C to + 85 °C
Input Voltage Amplitude	: 0 V / V_{DD}
Input Rising Time	: 3 ns
Input Falling Time	: 3 ns
Input Evaluation Level	: $V_{DD}/2$
Output Evaluation Level	: $V_{DD}/2$
Output Load Capacitance	: 30 pF

(1) Read Cycle

Parameter	Symbol	Value (V_{DD}=1.8V to 2.7V)		Value (V_{DD}=2.7V to 3.6V)		Unit
		Min	Max	Min	Max	
Read Cycle time	t_{RC}	185	—	150	—	ns
/CE Access Time	t_{CE}	—	95	—	75	ns
Address Access Time	t_{AA}	—	185	—	150	ns
/CE Output Data Hold time	t_{OH}	0	—	0	—	ns
Address Access Output Data Hold time	t_{OAH}	20	—	20	—	ns
/CE Active Time	t_{CA}	95	—	75	—	ns
Pre-charge Time	t_{PC}	90	—	75	—	ns
/LB, /UB Access Time	t_{BA}	—	35	—	20	ns
Address Setup Time	t_{AS}	5	—	5	—	ns
Address Hold Time	t_{AH}	95	—	75	—	ns
/CE↑ to Address Transition time*1	t_{CAH}	5	—	5	—	ns
/OE Access Time	t_{OE}	—	35	—	20	ns
/CE Output Floating Time*1	t_{HZ}	—	10	—	10	ns
/OE Output Floating Time	t_{OHZ}	—	10	—	10	ns
/LB, /UB Output Floating Time	t_{BHZ}	—	10	—	10	ns
Address Transition Time*1	t_{AX}	—	15	—	15	ns

*1: Same parameters with the Write cycle.

(2) Write Cycle

Parameter	Symbol	Value (V_{DD}=1.8V to 2.7V)		Value (V_{DD}=2.7V to 3.6V)		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	185	—	150	—	ns
/CE Active Time	t_{CA}	95	—	75	—	ns
/CE↓ to /WE↑ Time	t_{CW}	95	—	75	—	ns
Pre-charge Time	t_{PC}	90	—	75	—	ns
Write Pulse Width	t_{WP}	20	—	20	—	ns
Address Setup Time	t_{AS}	5	—	5	—	ns
Address Hold Time	t_{AH}	95	—	75	—	ns
/CE↑ to Address Transition time	t_{CAH}	5	—	5	—	ns
/WE↓ to /CE↑ Time	t_{WLC}	20	—	20	—	ns
Address Transition to /WE↑ Time	t_{AWH}	185	—	150	—	ns
/WE↑ to Address Transition Time	t_{WHA}	0	—	0	—	ns
/LB, /UB Setup Time	t_{BS}	2	—	2	—	ns
/LB, /UB Hold Time	t_{BH}	0	—	0	—	ns
Data Setup Time	t_{DS}	10	—	10	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
/WE Output Floating Time	t_{WZ}	—	10	—	10	ns
/WE Output Access Time*1	t_{WX}	10	—	10	—	ns
Write Setup Time*1	t_{WS}	0	—	0	—	ns
Write Hold Time*1	t_{WH}	0	—	0	—	ns

*1: Writing operation applies “Write Cycle Timing 1” or “Write Cycle Timing 2” by the relation of /CE and /WE timing. The values of t_{WX}, t_{WS} and t_{WH} are defined by these operations. The conditions of t_{WS} and t_{WH} are not checked at shipping test.

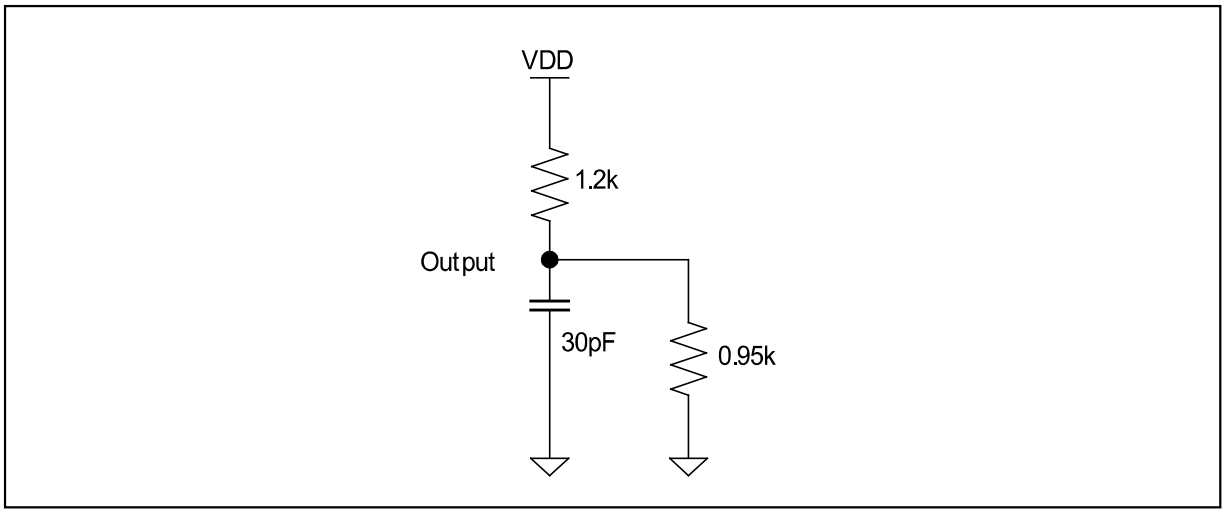
(3) Power ON/OFF Sequence and Sleep Mode Cycle

Parameter	Symbol	Value		Unit
		Min	Max	
/CE level hold time for Power ON	t_{PU}	450	—	µs
/CE level hold time for Power OFF	t_{PD}	85	—	ns
Power supply rising time	t_{VR}	50	—	µs/V
Power supply falling time	t_{VF}	100	—	µs/V
/ZZ active time	t_{ZZL}	1	—	µs
Sleep mode enable time	t_{ZZEN}	—	0	µs
/CE level hold time for Sleep mode release	t_{ZZEX}	450	—	µs

3. Pin Capacitance

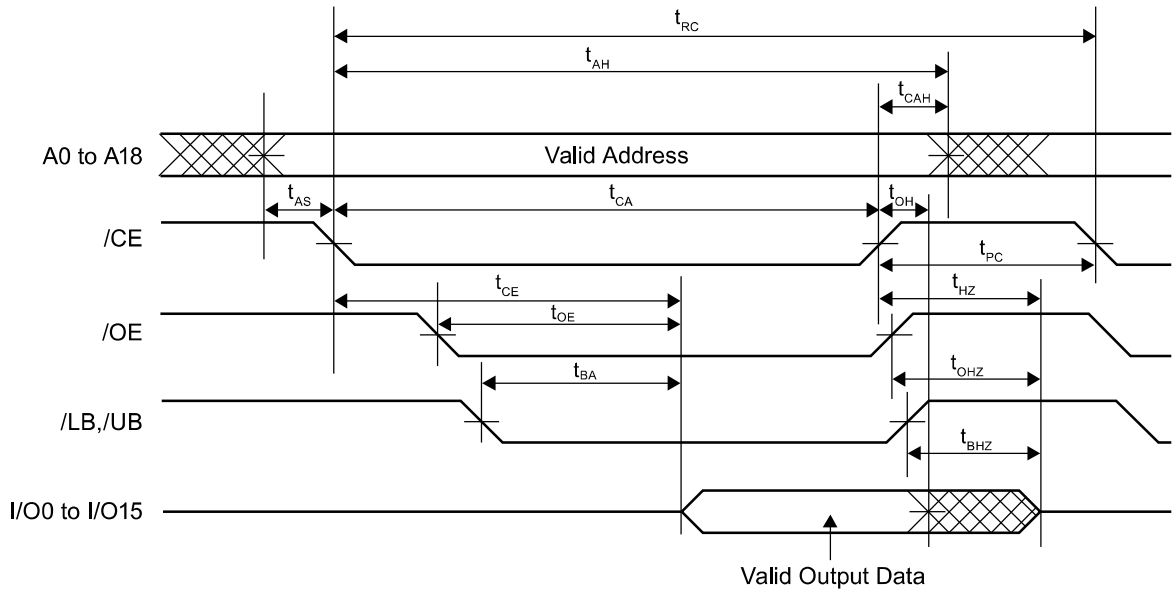
Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Input Capacitance	C_{IN}	V_{DD} = 3.3 V, f = 1 MHz, T_A = + 25 °C	—	—	9	pF
Input/Output Capacitance (I/O pin)	$C_{I/O}$		—	—	9	pF
/ZZ Pin Input Capacitance	C_{ZZ}		—	—	9	pF

■ AC Test Load Circuit



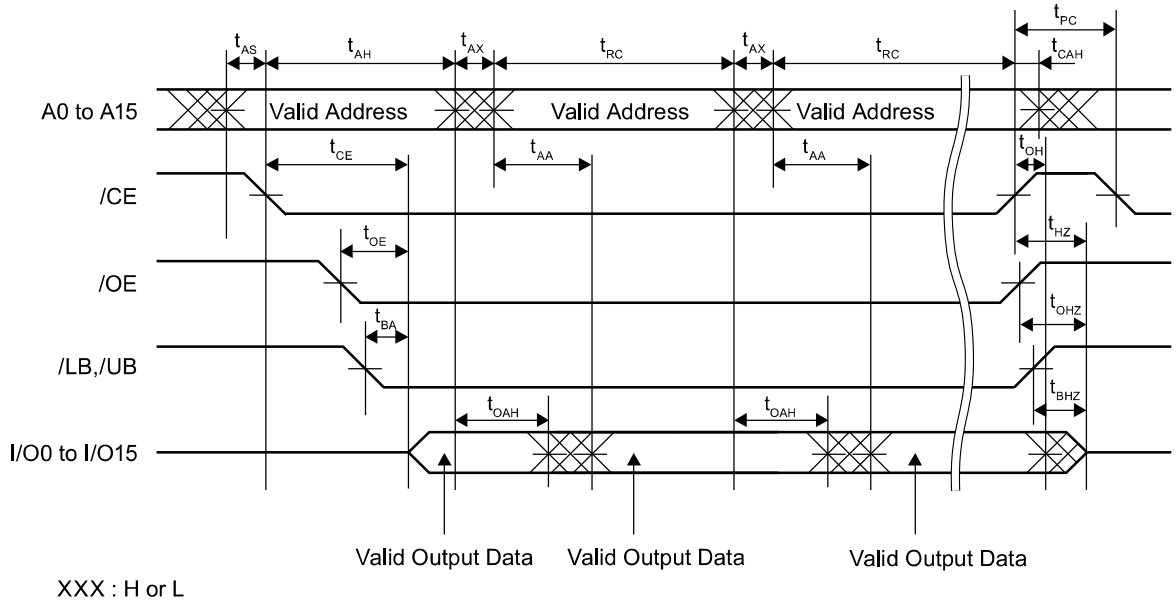
■ TIMING DIAGRAMS

1. Read Cycle Timing 1 (/CE Control)



XXX : H or L

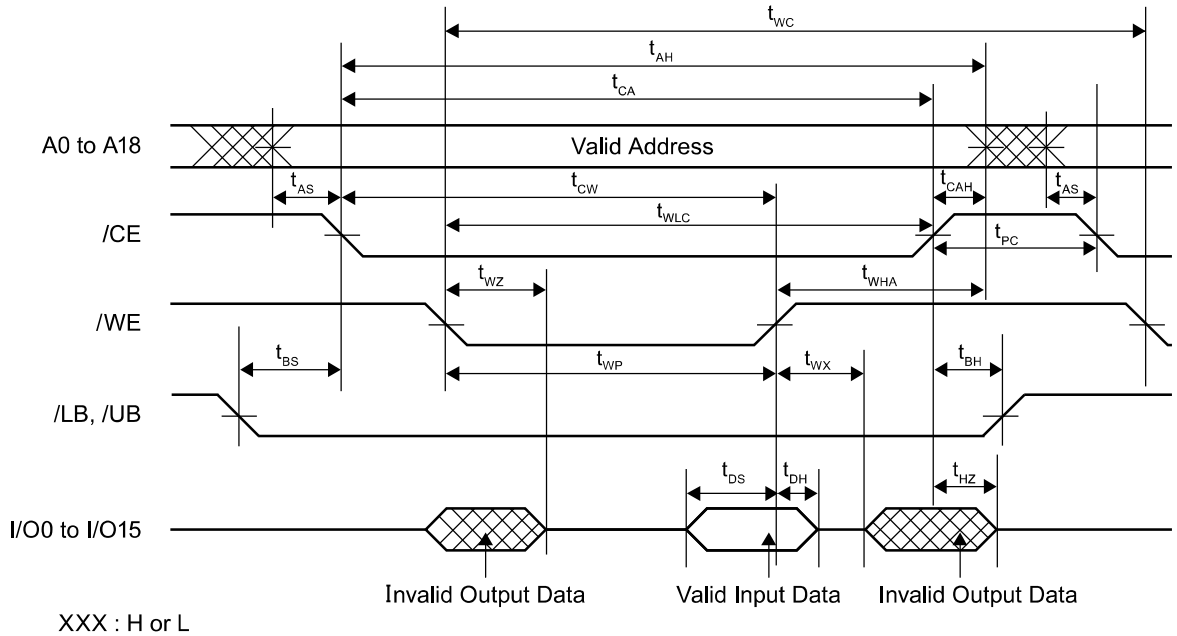
2. Read Cycle Timing 2 (Address Access)



XXX : H or L

* : Address access is possible between A0 to A15. In this case, A16 to A18 request to be fixed “H or L”.

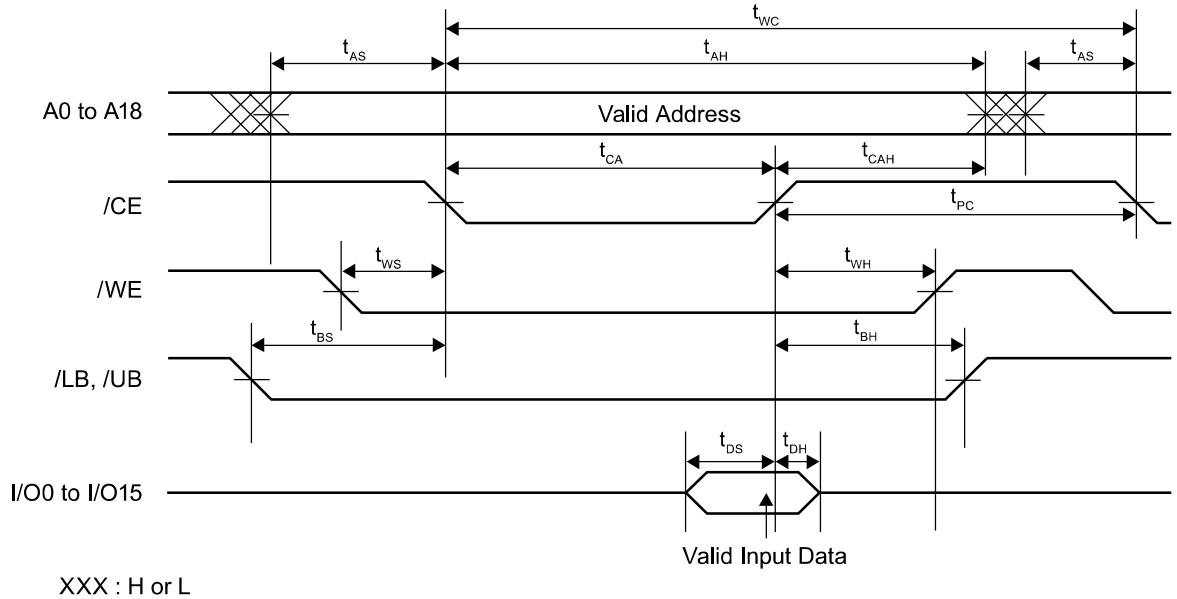
3. Write Cycle Timing 1 (/WE Control)



XXX : H or L

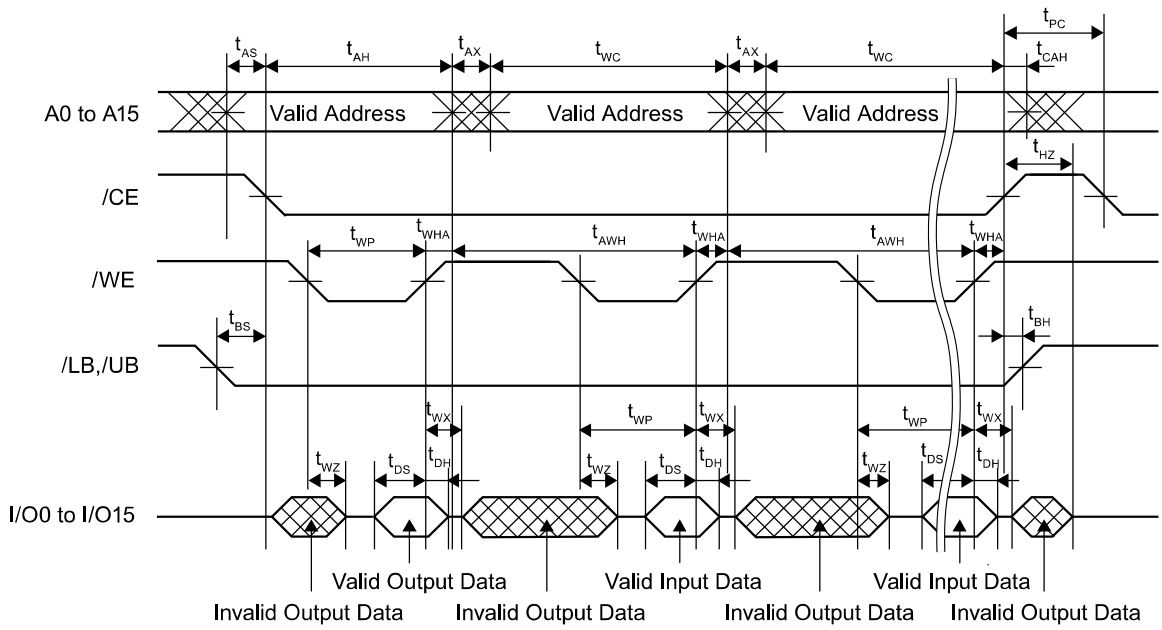
* : In case the /OE is “L” level, invalid data are output to data bus.
* : In case the /OE is “L” level, any bus conflict of input and output data shall not occur.

4. Write Cycle Timing 2 (/CE Control)



XXX : H or L

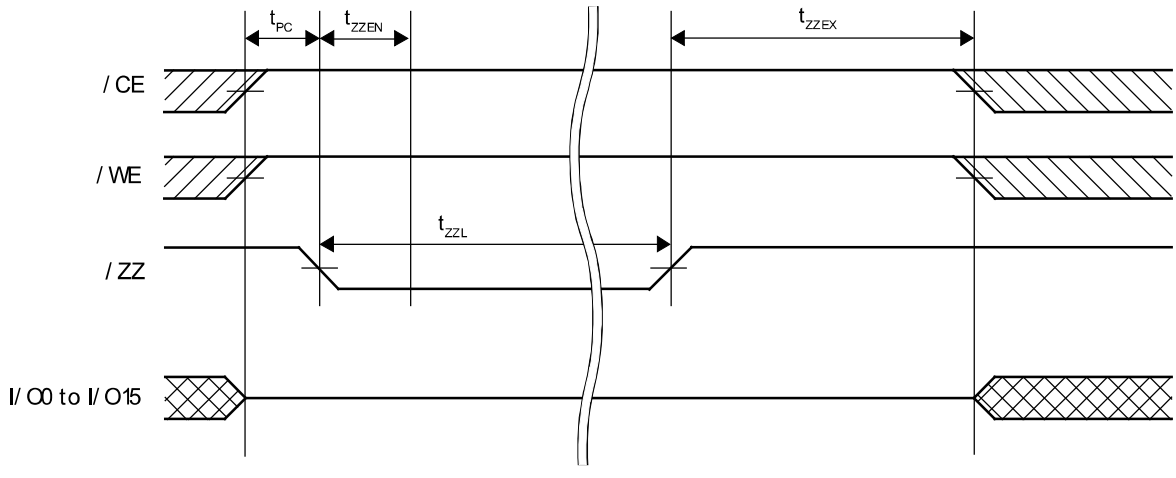
5. Write Cycle Timing 3 (Address Access and /WE Control)



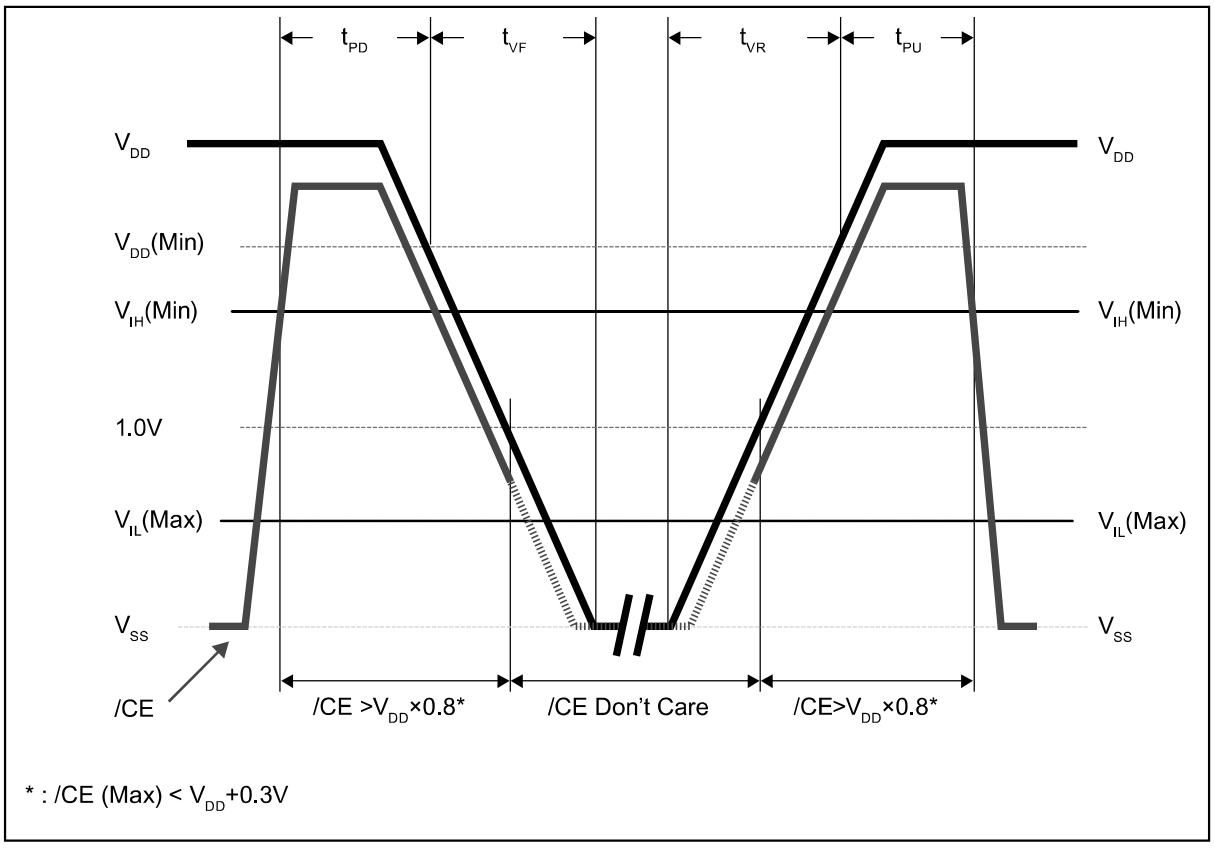
XXX : H or L

* : In case the /OE is “L” level, invalid data are output to data bus.
* : In case the /OE is “L” level, any bus conflict of input and output data shall not occur.
* : Address access is possible between A0 to A15. In this case, A16 to A18 requires to be fixed “H or L”.

6. Sleep Mode Timing



■ POWER ON/OFF SEQUENCE



* : /CE (Max) < V_{DD}+0.3V

■ FRAM CHARACTERISTICS

Item	Min	Max	Unit	Parameter
Read/Write Endurance*1	10^{13}	—	Times/16 bits	Operation Ambient Temperature T_A = + 85 °C
Data Retention*2	10	—	Years	Operation Ambient Temperature T_A = + 85 °C
	95	—		Operation Ambient Temperature T_A = + 55 °C
	≥ 200	—		Operation Ambient Temperature T_A = + 35 °C

*1: Total number of reading and writing defines the minimum value of endurance, as an FRAM memory operates with destructive readout mechanism.

*2: Minimum values define retention time of the first reading/writing data right after shipment, and these values are calculated by qualification results.

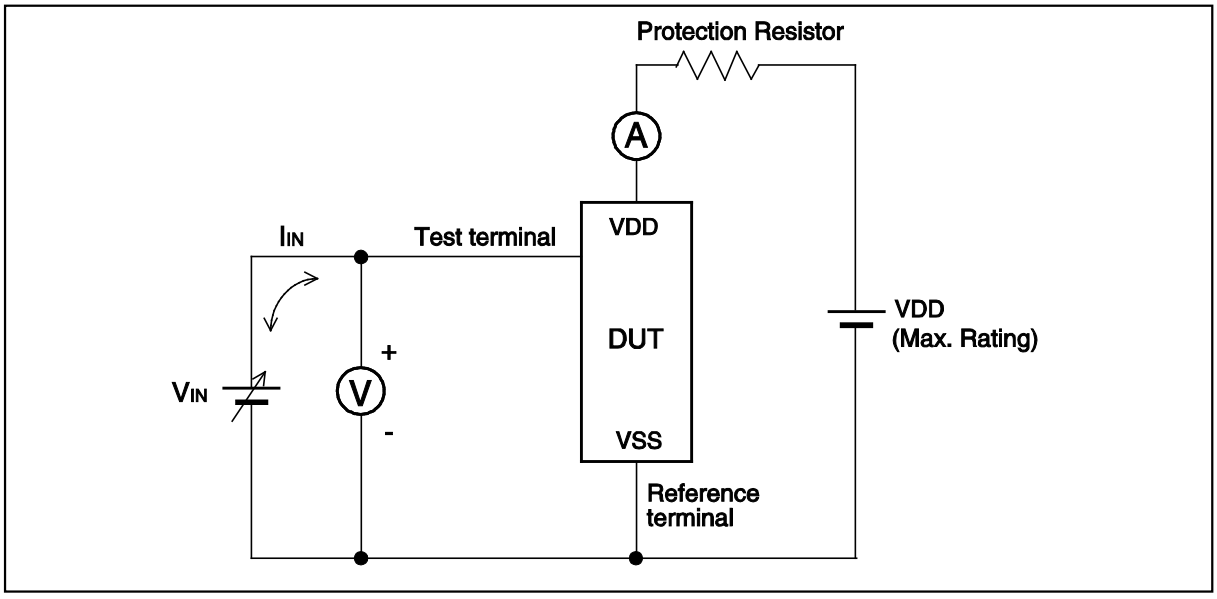
■ NOTE ON USE

- We recommend programming of the device after reflow. Data written before reflow cannot be guaranteed.

■ ESD AND LATCH-UP

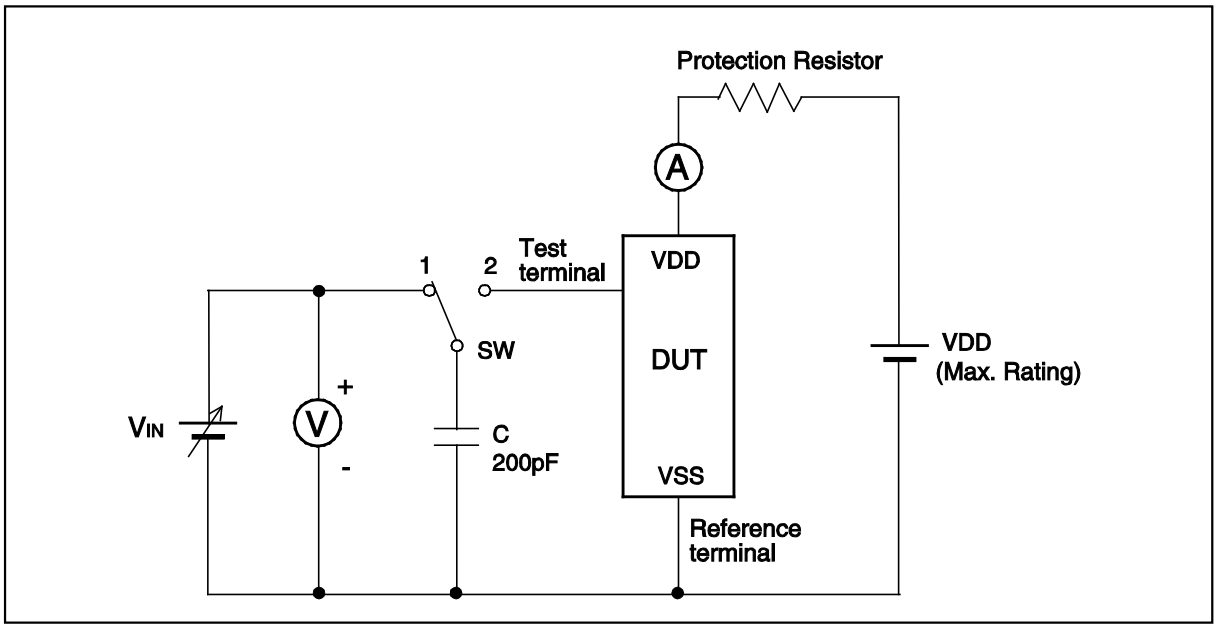
Test	DUT	Value
ESD HBM (Human Body Model) JESD22-A114 compliant	MB85R8M2TPBS-M-JAE1	≥ |2000 V|
ESD MM (Machine Model) JESD22-A115 compliant		≥ |200 V|
ESD CDM (Charged Device Model) JESD22-C101 compliant		—
Latch-Up (I-test) JESD78 compliant		—
Latch-Up (V_{supply} overvoltage test) JESD78 compliant		—
Latch-Up (Current Method) Proprietary method		—
Latch-Up (C-V Method) Proprietary method		≥ |200 V|

・Current method of Latch-Up Resistance Test



Note: The voltage VIN is increased gradually and the current I_{IN} of 300 mA at maximum shall flow.
Confirm the latch up does not occur under $I_{IN} = \pm 300$ mA.
In case the specific requirement is specified for I/O and I_{IN} cannot be 300 mA, the voltage shall be increased to the level that meets the specific requirement.

▪ **C-V method of Latch-Up Resistance Test**



Note: Charge voltage alternately switching 1 and 2 approximately 2 sec intervals. This switching process is considered as one cycle.
Repeat this process 5 times. However, if the latch-up condition occurs before completing 5times, this test must be stopped immediately.

■ REFLOW CONDITIONS AND FLOOR LIFE

[JEDEC MSL] : Moisture Sensitivity Level 3 (ISP/JEDEC J-STD-020D)

■ CURRENT STATUS ON CONTAINED RESTRICTED SUBSTANCES

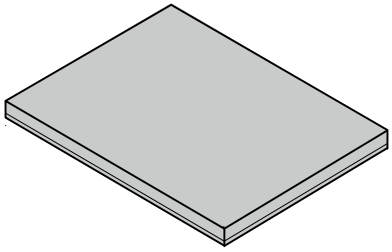
This product complies with the regulations of REACH Regulations, EU RoHS Directive and China RoHS.

■ ORDERING INFORMATION

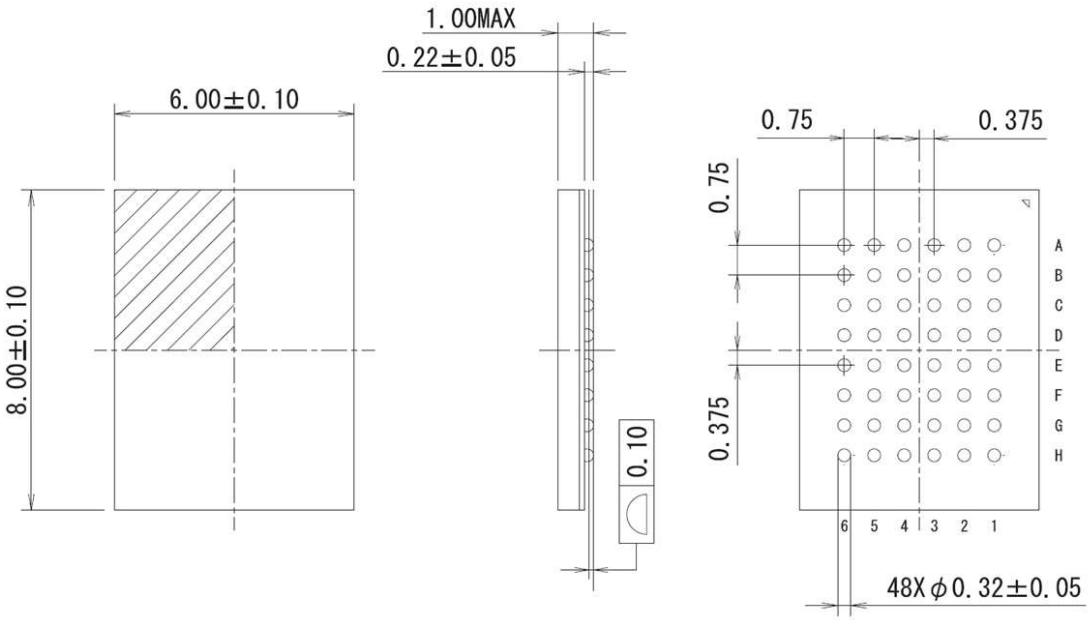
Part Number	Package	Shipping form	Minimum shipping quantity
MB85R8M2TPBS-M-JAE1	48-pin plastic FBGA (BGA-48P-M24)	Tray	—*

*: Please contact our sales office about minimum shipping quantity.

■ PACKAGE DIMENSIONS

48-pin plastic BGA		
	Lead pitch	0.75 mm
	Package width × package length	8.00mm × 6.00 mm
	Lead shape	Soldering ball
	Sealing method	Plastic Mold
	Mounting height	1.22mm Max.
	Weight	0.08g
(BGA- 48P-M24)		

48-pin-plastic BGA
(BGA-48P-M24)



Dimensions in mm.

■ MARKING

[MB85R8M2TPBS-M-JAE1]

[BGA-48P-M24]

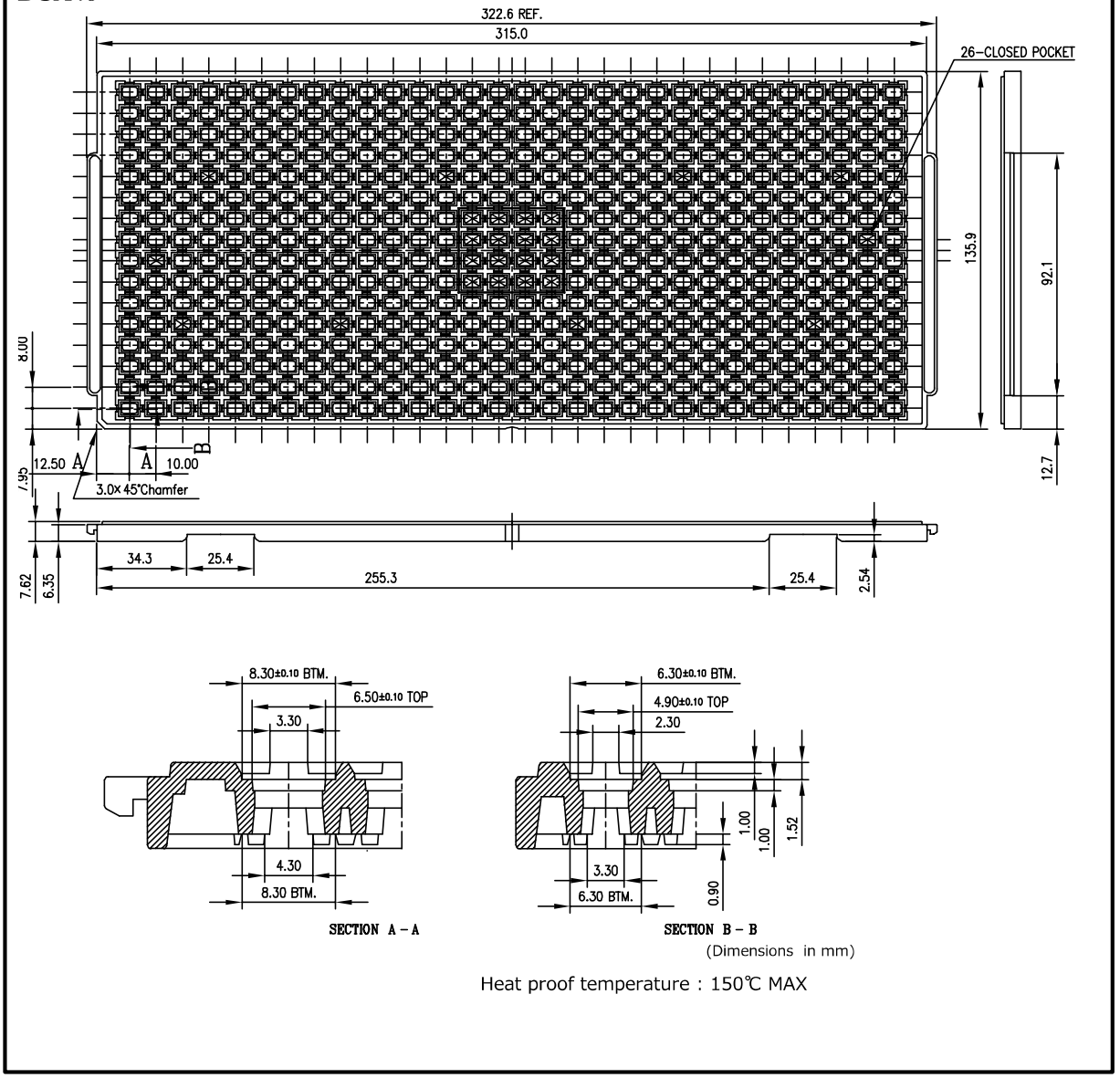
■ PACKING

1. Tray

1.1 Tray dimensions

PKG code	Maximum storage capacity		
	pcs/tray	pcs/inner box	pcs/outer box
BGA-48P-M24	480	4800 (10trays)	19200 (4 inner boxes, Max)

BGA48

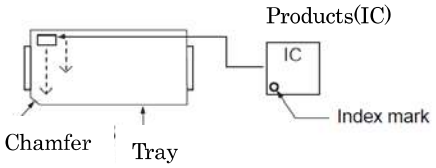


(Dimensions in mm)

Heat proof temperature : 150℃ MAX

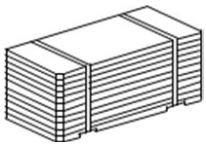
1.2 TRAY Dry Packing Specifications

(1) Pack ICs in the tray

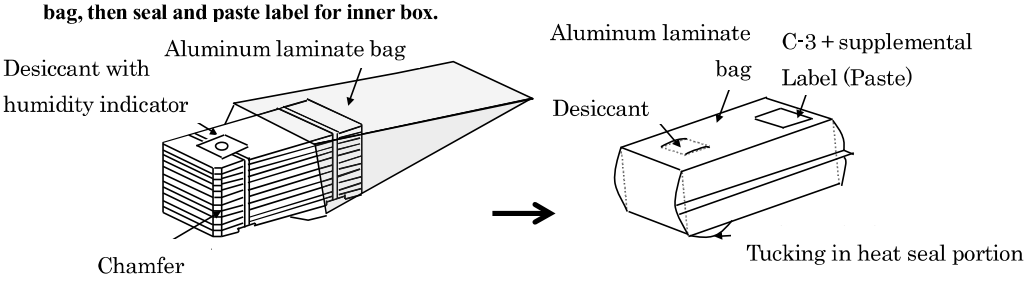


(2) Stack trays in designated number, put the lid(empty tray), bundle with bands.

* Gaps between trays are uniform.
* Chamfers direction are the same.
* Bands are around cut-out portion of trays.

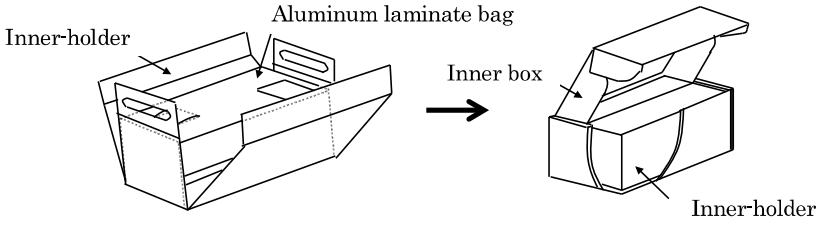


(3) Put desiccant(with humidity indicator:20g) on the bundled trays, vacuum pack in aluminum laminate bag, then seal and paste label for inner box.



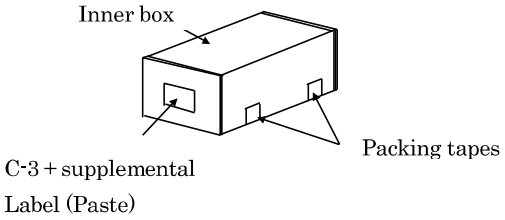
(4) Put the aluminum laminate in inner-holder, store in inner box.

* It is allowed to put inner-holder in inner box then put aluminum laminate in the inner-holder.



(5) Close the lids of the inner box, paste one label for inner box.

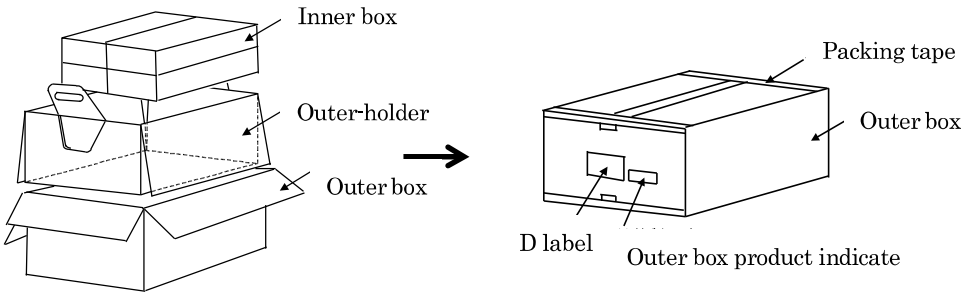
Close the inner box with packing tapes on two portions,



(6) Store in outer box

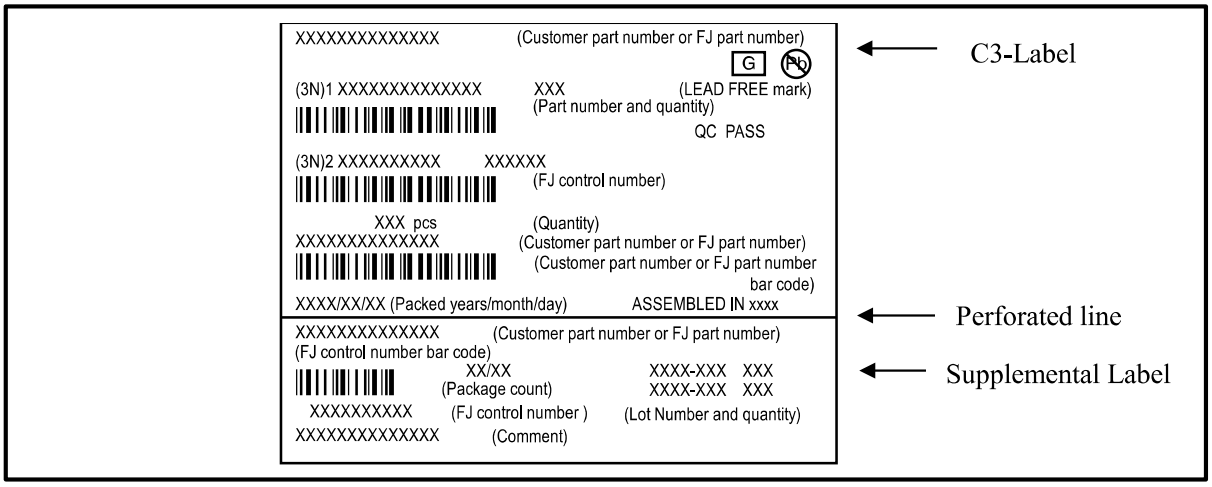
Put outer-holder in outer box, store inner box(es) maximum four.

Outer box is sealed with packing tape (H-paste), paste outer box product indicate on the designated portion.

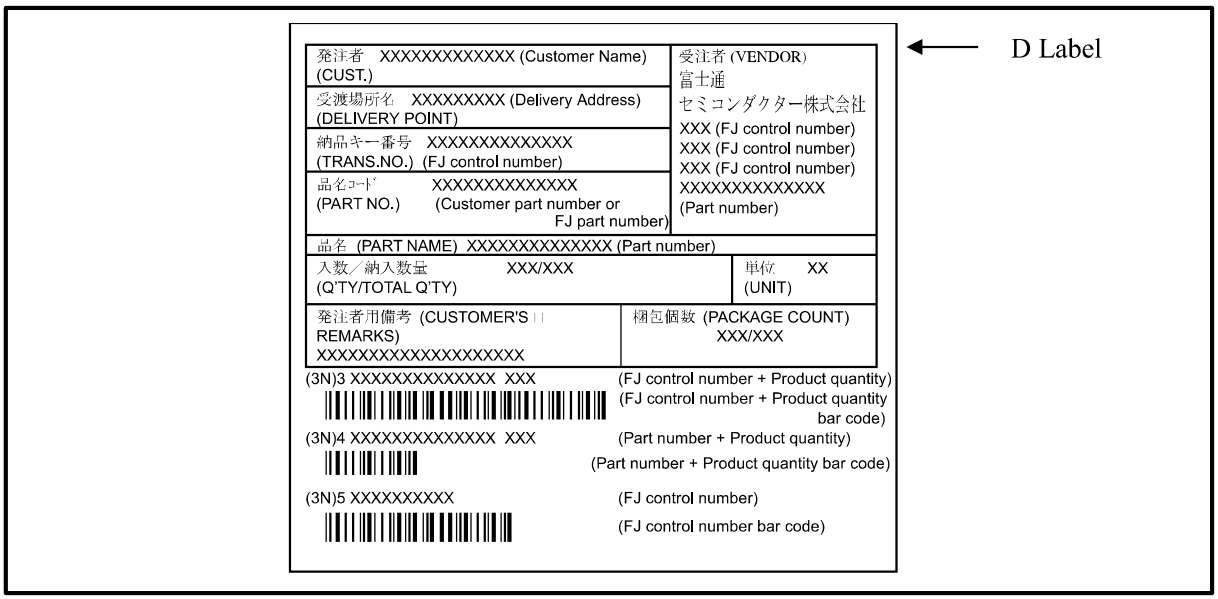


1.3 Product label indicators

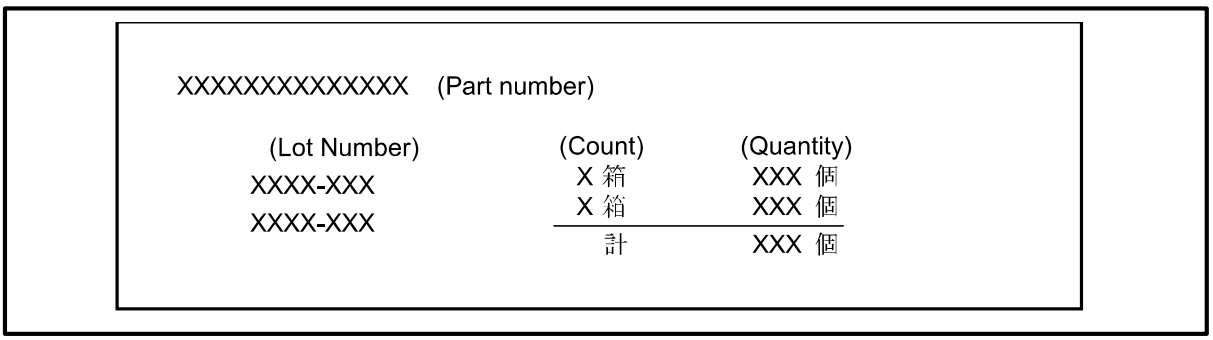
Label I: Label on Inner box/Moisture Barrier Bag/ (It sticks it on the reel for the emboss taping)
[C-3 Label (50mm x 100mm) Supplemental Label (20mm x 100mm)]



Label II-A: Label on Outer box [D Label] (100mm x 100mm)



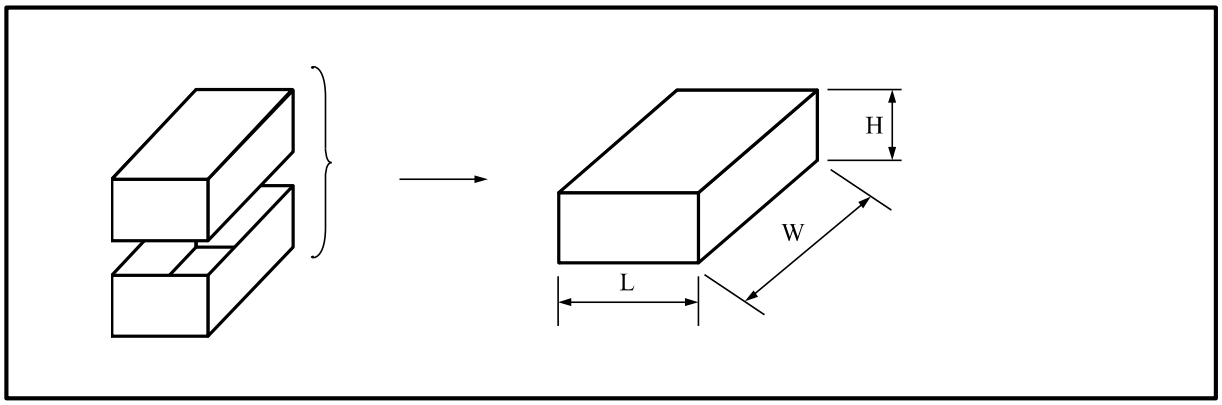
Label II-B: Outer boxes product indicate



Note: Depending on shipment state, "Label II-A" and "Label II-B" on the external boxes might not be printed.

1.4 Dimensions for container

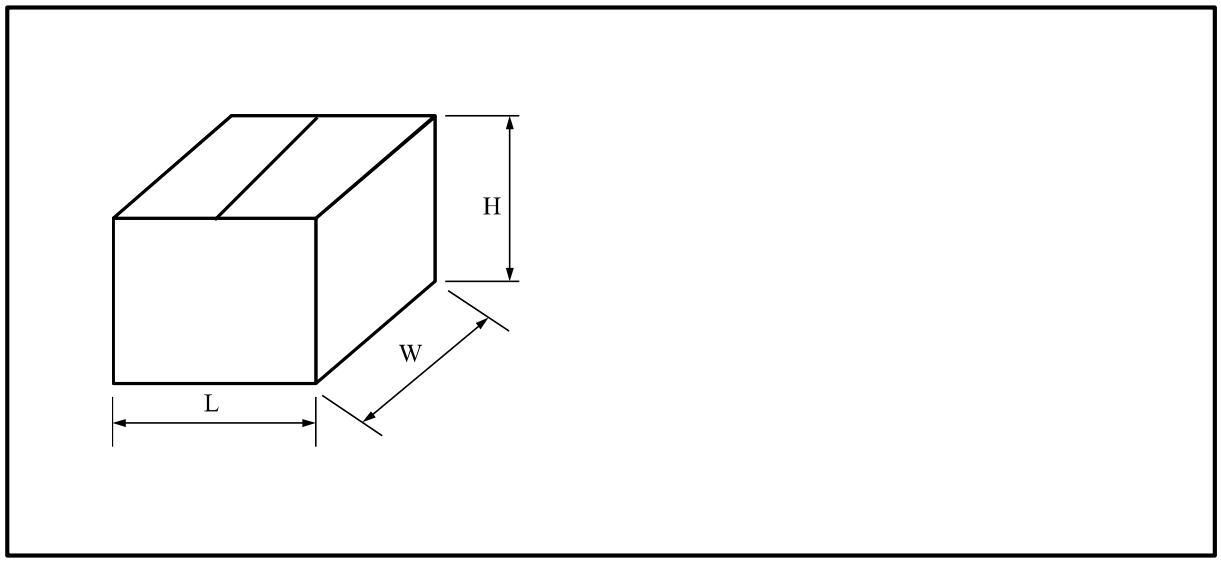
(1) Dimensions for inner box



L	W	H
162	360	90

(Dimensions in mm)

(2) Dimensions for outer box



L	W	H
375	410	225

(Dimensions in mm)

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