13-3087; Rev 0; 1/04

EVALUATION KIT AVAILABLE

Low-Cost, High-Reliability, 0.5V to 3.3V ORing MOSFET Controllers

General Description

Critical loads often employ parallel-connected power supplies with redundancy to enhance system reliability. The MAX8555/MAX8555A are highly integrated, inexpensive MOSFET controllers that provide isolation and redundant power capability in high-reliability systems. The MAX8555/MAX8555A are used in 0.5V to 3.3V systems, and have an internal charge pump to drive the gates of the N-channel pass elements to (V_{CS+} + 5V).

During startup, the MAX8555/MAX8555A monitor the voltage drop across the external MOSFETs. Once V_{CS+} approaches or exceeds the bus voltage (V_{CS-}), the MOSFETs are turned on. The MAX8555/MAX8555A feature a dual-purpose TIMER input. A single external resistor from TIMER to ground sets the turn-on speed of the external MOSFETs. Optionally, the TIMER input can be used as a logic enable input. Once the external MOSFET is turned on, these controllers monitor the load, protecting the bus against overvoltage, undervoltage, and reverse-current fault conditions. The MAX8555 is available with a 40mV reverse-current threshold, while the MAX8555A is available with a 20mV reverse-current threshold.

Overvoltage and undervoltage fault thresholds are adjustable and can be disabled. The current-limit trip points are set by the external MOSFETs' $R_{DS(ON)}$, reducing component count. An open-drain, logic-low fault output indicates if an overvoltage, undervoltage, or reverse-current fault occurs. The MAX8555 and the MAX8555A can shut down in response to a reverse-current fault condition as quickly as 200ns.

Both devices come in space-saving 10-pin µMAX or TDFN packages and are specified over the extended -40°C to +85°C temperature range.

Applications

Point-of-Load Supplies

Power-Supply Modules

Servers

Telecom Power Supplies

Rectifiers

Redundant Power Supplies in High-Availability Systems

Typical Operating Circuit appears at end of data sheet.

Features

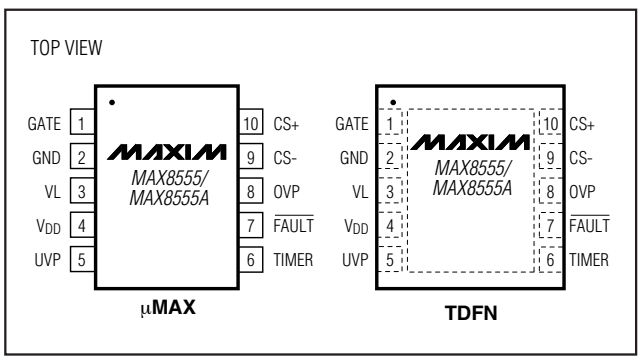
- **Simple, Integrated, and Inexpensive MOSFET Controllers**
- **ORing FET Drive for 0.5V to 3.3V**
- **Eliminate ORing Diode Power Dissipation**
- **Provide N+1 Redundant Supply Capability for Highly Reliable Systems**
- **Isolate Failed Short-Circuit Supply from Output BUS**
- **Respond to Reverse Short-Circuit Current in 200ns**
- **Adjustable Blank Time**
- **Programmable Soft-Start**
- **Logic Enable Input**
- **Adjustable Overvoltage and Undervoltage Trip Points**
- **Fault-Indicator Output**
- **Space-Saving Packages**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX8555ETB	-40°C to 85°C	10 TDFN 3mm x 3mm*	ACC
MAX8555EUB	-40°C to 85°C	10 µMAX	8555EUB
MAX8555AETB	-40°C to 85°C	10 TDFN 3mm x 3mm*	ADD
MAX8555AEUB	-40°C to 85°C	10 µMAX	8555AEUB

**Exposed paddle*

Pin Configurations



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ABSOLUTE MAXIMUM RATINGS

GATE to GND .....-0.3V to +12V
FAULT, VL to GND .....-0.3V to +6V
OVP, UVP, TIMER, CS+, CS- to GND .....-0.3V to +(V_{VL} + 0.3V)
V_{DD} to GND.....(V_{VL} - 0.3V) to +18V
Continuous Power Dissipation (T_A = +70°C)
10-Pin µMAX (derate 5.6mW/°C above +70°C) 444mW
10-Pin TDFN (derate 24.4mW/°C above +70°C) 1951mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 12V, V_{CS-} = 1.4V, V_{CS+} = 1.5V, R_{TIMER} = 25kΩ, V_{UVP} = 1V, V_{OVP} = 0.25V, R_{FAULT} = 50kΩ, C_{VDD} = C_{GATE} = C_{VL} = 0.01µF, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} SUPPLY						
V_{DD} Input Voltage	V_{TIMER} = 2.5V	VL unconnected	8.00		13.25	V
		VL = V_{DD}	3.0		5.5	
V_{DD} Supply Current	VL unconnected, V_{TIMER} = 2.5V, V_{DD} = 13.25V			2.0	3.3	mA
	V_{DD} = V_{VL} = 5V, V_{TIMER} = 2.5V			0.04	0.2	
V_{DD} Shutdown Current	V_{TIMER} = 0V, V_{DD} = 13.25V				3.0	mA
V_{DD} Overvoltage Internal Threshold	Rising threshold		14.0	14.4	15.0	V
	Falling threshold		13.3	13.8	14.5	
VL SUPPLY						
VL Input Voltage	V_{DD} = V_{VL}		3.0		5.5	V
VL Supply Current	V_{DD} = V_{VL} = 5V, V_{TIMER} = 2.5V			1.8	3.0	mA
VL Current in Shutdown Mode	TIMER = GND, V_{DD} = V_{VL} = 5V			1.6	3.0	mA
VL Output Voltage	V_{DD} = 8V to 13.25V, I_{VL} = 0A		3.80	4.1	4.45	V
VL Undervoltage Lockout	VL = V_{DD}, rising threshold		2.78	2.82	2.90	V
	VL = V_{DD}, falling threshold		2.68	2.75	2.82	
CS INPUTS						
CS+, CS- Input Current	V_{TIMER} = 2.5V, V_{CS} = 3.0V			5.2		µA
Offset Input Current (CS+, CS-)	V_{CS} = 3.0V, Figure 4		-250		+250	nA
CS+/CS- Input Range	(Note 1)		0.5		V_{VL} - 0.5	V
CS Isolation	V_{CS+} = +3V, V_{CS-} = 0V, I_{CS-}			-0.5		µA
	V_{CS-} = +3V, V_{CS+} = 0V, I_{CS+}			-0.5		
CHARGE-PUMP VOLTAGE						
GATE Voltage, V_{GATE}	Measured from GATE to CS+	V_{DD} = 8V to 13.25V	5.0	5.25	5.5	V
		V_{DD} = V_{VL} = 5V				
Charge-Pump Switching Frequency	R_{TIMER} = 20kΩ			187		kHz
	R_{TIMER} = 125kΩ			450		
	R_{TIMER} = open			500		
	V_{TIMER} = 1.5V			550		

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 12V, V_{CS-} = 1.4V, V_{CS+} = 1.5V, R_{TIMER} = 25kΩ, V_{UVP} = 1V, V_{OVP} = 0.25V, R_{FAULT} = 50kΩ, C_{VDD} = C_{GATE} = C_{VL} = 0.01µF, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TIMER						
TIMER Voltage			1.22	1.25	1.28	V
TIMER Maximum Source Current	V_{TIMER} = 1.0V		85	100	115	µA
TIMER High Input Current	V_{TIMER} = 1.5V			10	15	µA
TIMER Maximum Frequency Select Voltage Input Range	(Note 1)		1.5		V_{VL}	V
TIMER Logic High, V_{IH}	Charge pump enabled		1.0			V
TIMER Logic Low, V_{IL}	Charge pump disabled				0.5	V
FAULT						
Fault Output Low Voltage	$I_{\overline{FAULT}}$ = 10mA				0.2	V
Fault Sink Current	$V_{\overline{FAULT}}$ = 0.4V		15			mA
Fault Leakage Current	$V_{\overline{FAULT}}$ = 5.5V, T_A = +25°C				1	µA
GATE						
Gate-On Threshold	Measured from CS- to CS+	MAX8555	80	100	120	mV
		MAX8555A	35	50	65	
Gate-Drive Current	V_{GATE} = V_{CS+} = 2.5V	R_{TIMER} = open	17	25	33	µA
		R_{TIMER} = 25kΩ	8	12	16	
	V_{GATE} = V_{CS+} = 2.5V, V_{DD} = V_{VL} = 3V	R_{TIMER} = open		15		
		R_{TIMER} = 25kΩ		7.5		
	V_{GATE} = V_{CS+} = 2.5V, V_{DD} = V_{VL} = 5V	R_{TIMER} = open		30		
		R_{TIMER} = 25kΩ		15		
Gate Shutdown Delay	(Note 2)	V_{TIMER} falling		100	200	ns
		I_{REV} fault		60	150	
Gate Discharge Current	V_{GATE} = V_{CS+}= +5V			1000		mA
GATE Fall Time	Gate voltage fall from $\overline{FAULT}$ to V_{GATE} = V_{CS+}, R1 = 2Ω, Figure 3 or Figure 4			0.2		µs
CURRENT SENSE						
Reverse-Current Threshold	Measured from CS- to CS+	MAX8555	34	40	46	mV
		MAX8555A	16	20	24	
Startup I_{REV} Blank Time	TIMER = unconnected			4.1		ms
Forward-Current Threshold	Measured from CS+ to CS-		6	10	14	mV

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ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 12V, V_{CS-} = 1.4V, V_{CS+} = 1.5V, R_{TIMER} = 25kΩ, V_{UVP} = 1V, V_{OVP} = 0.25V, R_{FAULT} = 50kΩ, C_{VDD} = C_{GATE} = C_{VL} = 0.01µF, **T_A = 0°C to +85°C**, unless otherwise noted.)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
OVERVOLTAGE PROTECTION					
OVP Fault Threshold, V_{OVP}	OVP rising	0.49	0.5	0.51	V
	OVP falling		0.4		
OVP Bias Current	T_A = +25°C			0.1	µA
	T_A = +85°C		0.021		
UNDERVOLTAGE PROTECTION					
UVP Fault Threshold, V_{UVP}	UVP rising	0.488	0.5	0.512	V
	UVP falling		0.4		
UVP Bias Current	T_A = +25°C			0.1	µA
	T_A = +85°C		0.003		

ELECTRICAL CHARACTERISTICS

(V_{DD} = 12V, V_{CS-} = 1.4V, V_{CS+} = 1.5V, R_{TIMER} = 25kΩ, V_{UVP} = 1V, V_{OVP} = 0.25V, R_{FAULT} = 50kΩ, C_{VDD} = C_{GATE} = C_{VL} = 0.01µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{DD} SUPPLY						
V_{DD} Input Voltage	V_{TIMER} = 2.5V	VL unconnected	8.00		13.25	V
		VL = V_{DD}	3.0		5.5	
V_{DD} Supply Current	VL unconnected, V_{TIMER} = 2.5V, V_{DD} = 13.25V				3.3	mA
	V_{DD} = V_{VL} = 5V, V_{TIMER} = 2.5V				0.2	
V_{DD} Shutdown Current	V_{TIMER} = 0V, V_{DD} = 13.25V				3.0	mA
V_{DD} Overvoltage Internal Threshold	Rising threshold		14.0		15.0	V
	Falling threshold		13.3		14.5	
VL SUPPLY						
VL Input Voltage	V_{DD} = V_{VL}		3.0		5.5	V
VL Supply Current	V_{DD} = V_{VL} = 5V, V_{TIMER} = 2.5V				3.0	mA
VL Current in Shutdown Mode	TIMER = GND, V_{DD} = V_{VL}= 5V				3.0	mA
VL Output Voltage	V_{DD} = 8V to 13.25V, I_{VL} = 0A		3.80		4.45	V
VL Undervoltage Lockout	VL = V_{DD}, rising threshold		2.78		2.90	V
	VL = V_{DD}, falling threshold		2.68		2.82	
CS INPUTS						
Offset Input Current (CS+, CS-)	V_{CS} = 3.0V, Figure 4		-250		+250	nA
CS+/CS- Input Range	(Note 1)		0.5		V_{VL} - 0.5	V
CHARGE-PUMP VOLTAGE						
GATE Voltage, V_{GATE}	Measured from GATE to CS+	V_{DD} = 8V to 13.25V	5.0		5.5	V
		V_{DD} = V_{VL} = 5V				

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 12V, V_{CS-} = 1.4V, V_{CS+} = 1.5V, R_{TIMER} = 25kΩ, V_{UVP} = 1V, V_{OVP} = 0.25V, R_{FAULT} = 50kΩ, C_{VDD} = C_{GATE} = C_{VL} = 0.01µF, **T_A = -40°C to +85°C**, unless otherwise noted.) (Note 3)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
TIMER						
TIMER Voltage			1.22		1.28	V
TIMER Maximum Source Current	V_{TIMER} = 1.0V		85		115	µA
TIMER High Input Current	V_{TIMER} = 1.5V				15	µA
TIMER Maximum Frequency Select Voltage Input Range	(Note 1)		1.5		V_{VL}	V
TIMER Logic High, V_{IH}	Charge pump enabled		1.1			V
TIMER Logic Low, V_{IL}	Charge pump disabled				0.5	V
FAULT						
Fault Output Low Voltage	$I_{\overline{FAULT}}$ = 10mA				0.2	V
Fault Sink Current	$V_{\overline{FAULT}}$ = 0.4V		15			mA
GATE						
Gate-On Threshold	Measured from CS- to CS+	MAX8555	80		120	mV
		MAX8555A	35		65	
Gate-Drive Current	V_{GATE} = V_{CS+} = 2.5V	R_{TIMER} = open	17		33	µA
		R_{TIMER} = 25kΩ	8		16	
Gate Shutdown Delay		V_{TIMER} falling			200	ns
		I_{REV} fault			150	
CURRENT SENSE						
Reverse-Current Threshold	Measured from CS- to CS+	MAX8555	34		46	mV
		MAX8555A	16		24	
Forward-Current Threshold	Measured from CS+ to CS-		6		14	mV
OVERVOLTAGE PROTECTION						
OVP Fault Threshold, V_{OVP}	OVP rising		0.49		0.51	V
UNDERVOLTAGE PROTECTION						
UVP Fault Threshold, V_{UVP}	UVP rising		0.488		0.512	V

Note 1: Guaranteed by design. Not production tested.

Note 2: Gate shutdown delay is measured from reverse-current fault to the start of gate-voltage falling or from TIMER to the start of gate-voltage falling.

Note 3: Specifications to -40°C are guaranteed by design and not production tested.

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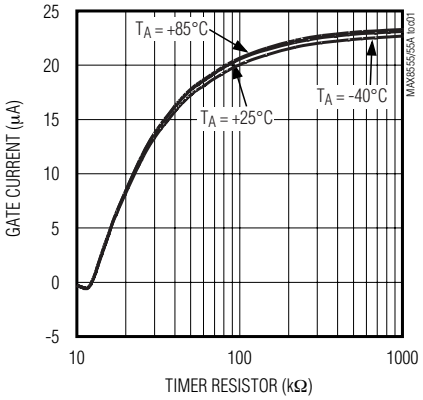
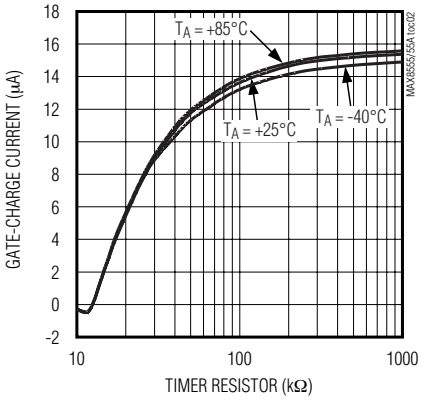
Typical Operating Characteristics

(V_{DD} = 12V, V_{CS+} = 1.5V, R_{TIMER} = 25kΩ, V_{UVP} = 1V, V_{OVP} = 0.4V, R_{FAULT} = 50kΩ to output bus, C_{VDD} = C_{GATE} = C_{VL} = 0.01µF, T_A = +25°C, R1 = 2Ω in Figure 3, MAX8555A, unless otherwise noted.)

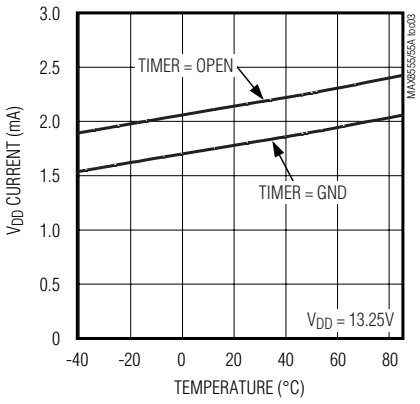
GATE-CHARGE CURRENT vs. TIMER RESISTOR (V_{DD} = 12V)



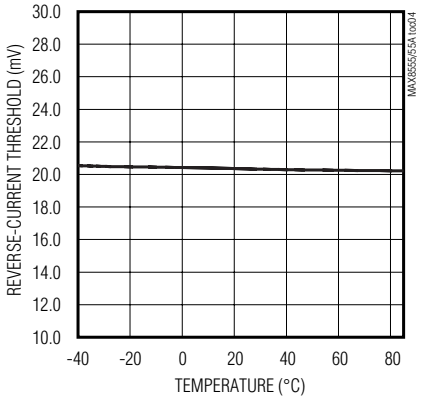
GATE-CHARGE CURRENT vs. TIMER RESISTOR (V_{DD} = V_{VL} = 3V)



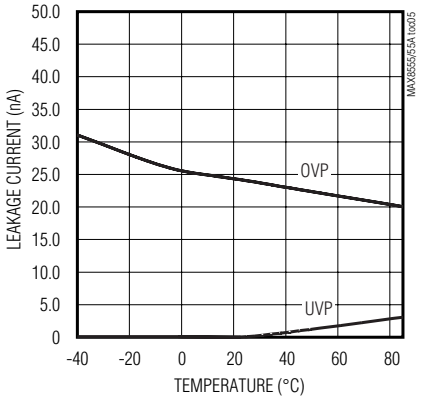
V_{DD} CURRENT vs. TEMPERATURE



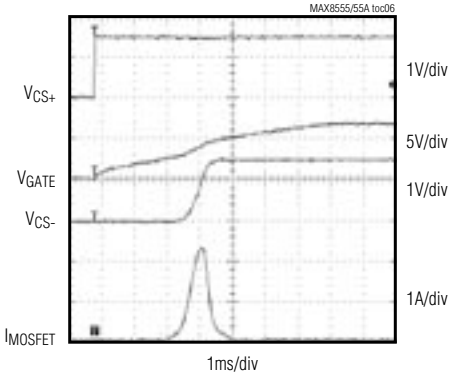
REVERSE-CURRENT THRESHOLD vs. TEMPERATURE



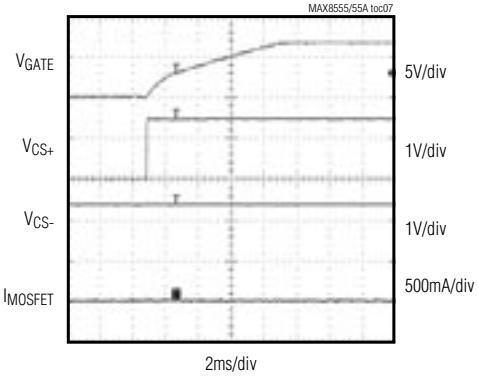
OVP AND UVP LEAKAGE CURRENT vs. TEMPERATURE



POWER-UP WAVEFORMS BUS VOLTAGE HIGH IMPEDANCE



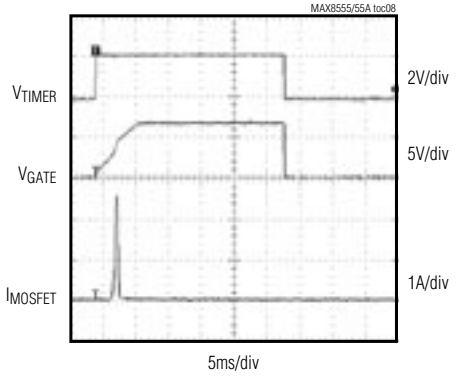
POWER-UP WAVEFORMS BUS VOLTAGE IS LIVE



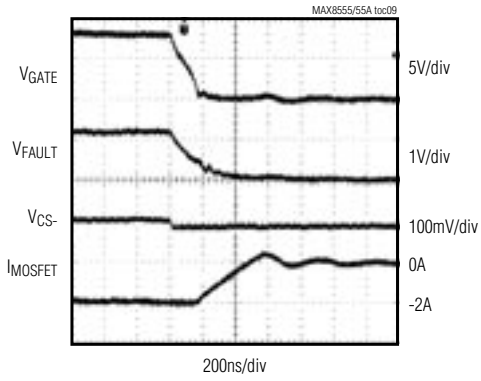
Typical Operating Characteristics (continued)

(V_{DD} = 12V, V_{CS+} = 1.5V, R_{TIMER} = 25kΩ, V_{UVP} = 1V, V_{OVP} = 0.4V, R_{FAULT} = 50kΩ to output bus, C_{VDD} = C_{GATE} = C_{VL} = 0.01µF, T_A = +25°C, R1 = 2Ω in Figure 3, MAX8555A, unless otherwise noted.)

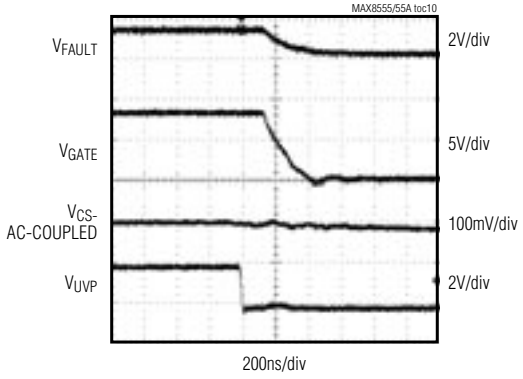
POWER-UP AND DOWN WAVEFORMS USING TIMER



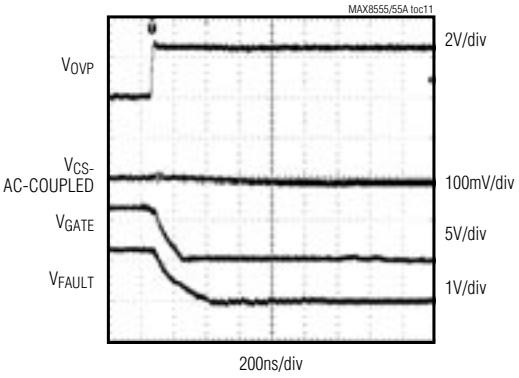
REVERSE-CURRENT SHUTDOWN WAVEFORMS



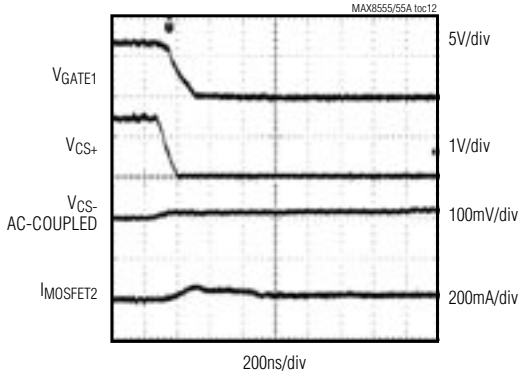
UVP SHUTDOWN WAVEFORMS



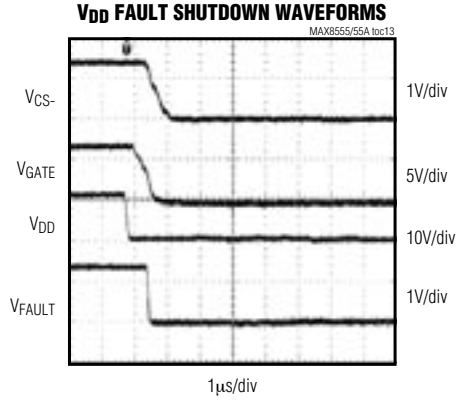
OVP SHUTDOWN WAVEFORMS



POWER-SUPPLY OUTPUT SHORT-CIRCUIT SHUTDOWN WAVEFORMS



V_{DD} FAULT SHUTDOWN WAVEFORMS



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Pin Description

PIN	NAME	FUNCTION
1	GATE	Gate-Drive Output. Nominal GATE load is a 0.01µF capacitor to ground. Gate is discharged to GND in shutdown.
2	GND	Ground
3	VL	Low-Voltage Optional Input Power. Leave disconnected when V_{DD} = 8V to 13.25V, or connect V_{DD} to VL when V_{DD} = 3V to 5.5V. Bypass VL to GND with a 0.01µF capacitor.
4	V_{DD}	Power-Supply Input. Connect to an 8V to 13.25V supply or connect to VL when using a 3V to 5.5V supply. Bypass V_{DD} with a 0.01µF capacitor to ground.
5	UVP	Undervoltage-Protection Input. Connect UVP to the center of a resistor-divider from CS+ to GND. Connect UVP to VL to disable the undervoltage protection.
6	TIMER	Timer Input. Connect a resistor from TIMER to GND to select the charge-pump operating frequency. Drive TIMER low (< 0.5V) to disable the gate drive. Drive TIMER high (above 1.5V) for charge-pump operation at 550kHz.
7	$\overline{FAULT}$	Open-Drain Fault Output. $\overline{FAULT}$ is high impedance during normal operation and is pulled to GND when a fault condition occurs. Connect a pullup resistor of 10kΩ or higher value (50kΩ typ) to a voltage rail of 5.5V or lower.
8	OVP	Overvoltage-Protection Input. Connect OVP to the center of a resistor-divider from the output bus to GND. Connect OVP to GND to disable the overvoltage protection.
9	CS-	Current-Sensing Input. Connect CS- to the positive side of the system bus. Bypass with a 1000pF capacitor to GND.
10	CS+	Current-Sensing Input. Connect CS+ to the positive side of the input power. Bypass with a 1000pF capacitor to GND.

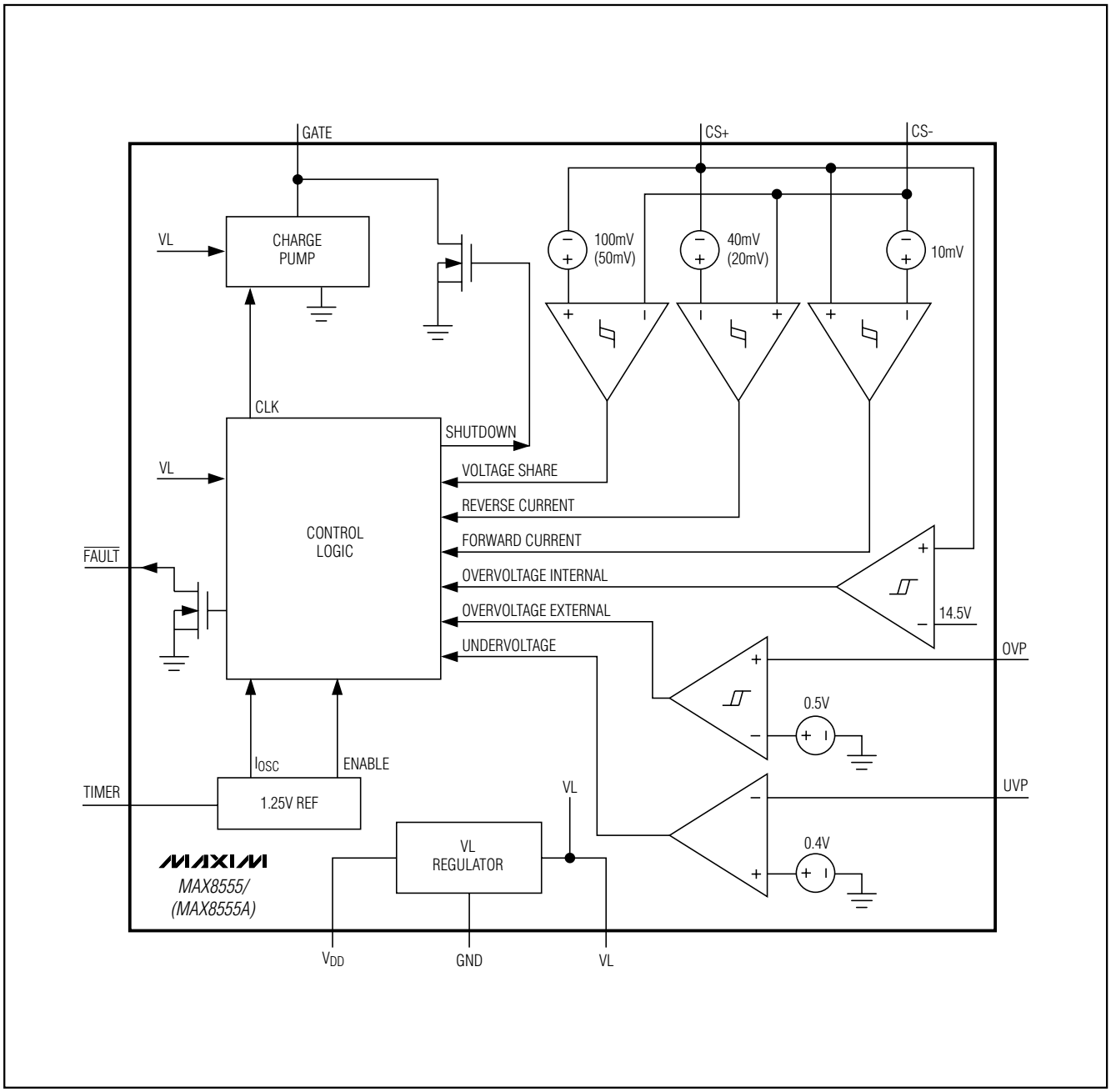
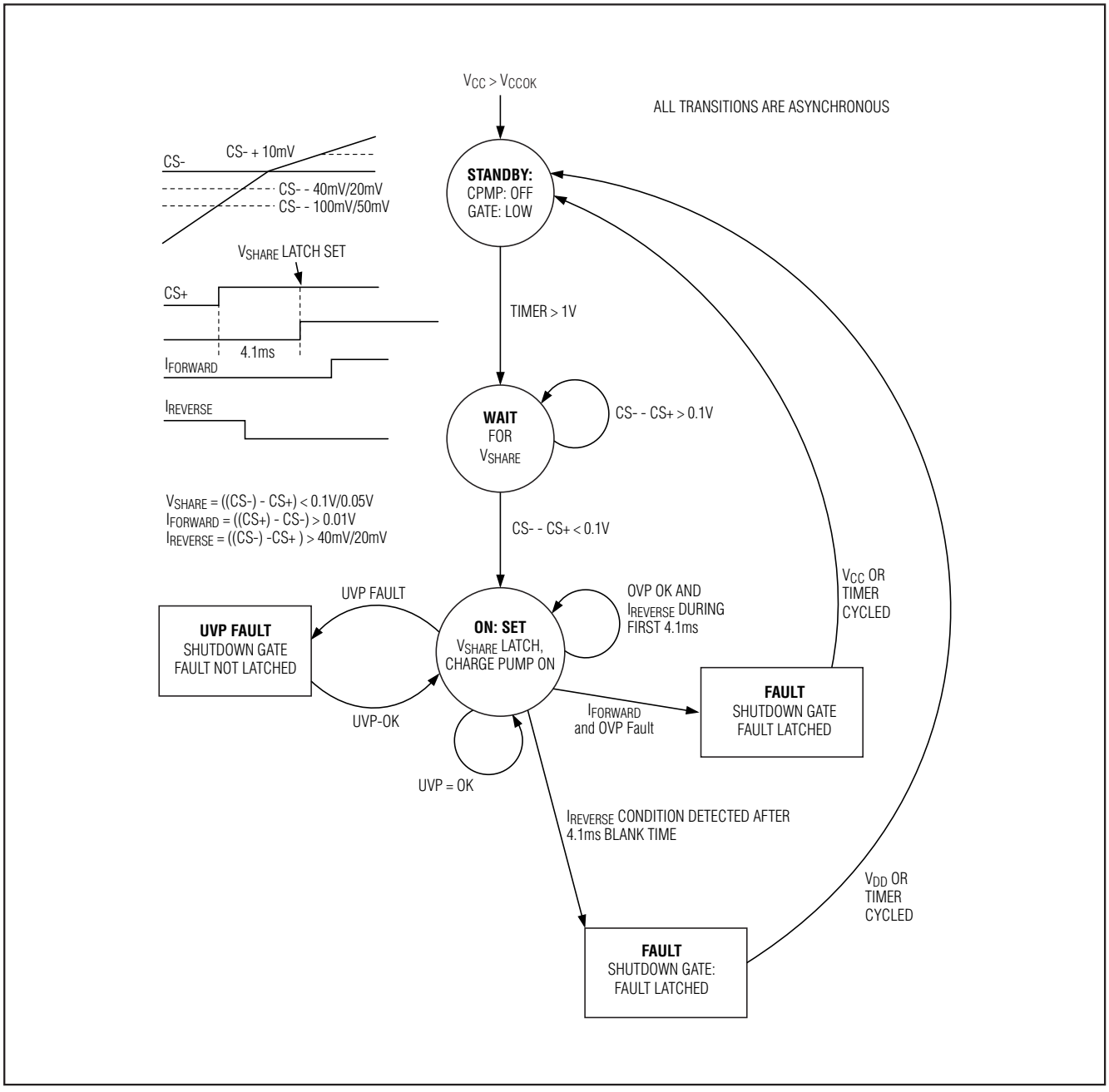


Figure 1. MAX8555/MAX8555A Functional Diagram

Low-Cost, High-Reliability, 0.5V to 3.3V ORing MOSFET Controllers

State Diagram



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General Description

Critical loads often employ parallel-connected power supplies with redundancy to enhance system reliability. The MAX8555/MAX8555A are highly integrated, inexpensive MOSFET controllers that provide isolation and redundant power capability in high-reliability systems. The MAX8555/MAX8555A are used in 0.5V to 3.3V systems, and have an internal charge pump to drive the gates of the N-channel pass elements to V_{CS+} + 5V.

During startup, the MAX8555/MAX8555A monitor the voltage drop across the external MOSFETs. Once V_{CS+} approaches or exceeds the bus voltage (V_{CS-}), the MOSFETs are turned on. The MAX8555/MAX8555A feature a dual-purpose TIMER input. A single external resistor from TIMER to ground sets the turn-on speed of the external MOSFETs. Optionally, the TIMER input can be used as a logic enable input. Once the external MOSFET is turned on, these controllers monitor the load, protecting the bus against overvoltage, undervoltage, and reverse-current fault conditions. The MAX8555 is available with a 40mV reverse-current threshold, while the MAX8555A is available with a 20mV reverse-current threshold.

Overvoltage and undervoltage fault thresholds are adjustable and can be disabled. The current-limit trip points are set by the external MOSFETs' $R_{DS(ON)}$, reducing component count. An open-drain, logic-low fault output indicates if an overvoltage, undervoltage, or reverse-current fault occurs. The MAX8555 and the MAX8555A can shut down in response to a reverse-current fault condition as quickly as 200ns.

VDD

V_{DD} is the power-supply input for the MAX8555/MAX8555A and the input to the internal preregulator. Bypass V_{DD} to GND with a 0.01µF capacitor. The input supply range for V_{DD} is 8V to 13.25V. The internal charge pump is disabled for input voltages above 14.4V (typ). For 3V to 5.5V input voltages, connect V_{DD} to VL.

VL

VL is the regulated power supply for the MAX8555/MAX8555A. The MAX8555/MAX8555A monitor VL at all times. During startup the device turns on when VL rises above VL_{OK} (2.82V typ). After V_{VL} exceeds VL_{OK} and V_{CS+} is typically greater than (V_{CS-} - 100mV), the charge pump turns on and drives GATE high, turning on the external MOSFETs. For operation from 3V to 5.5V input supplies, connect VL to V_{DD}.

TIMER

GATE is the output of the internal charge pump that drives the external MOSFETS. During startup, the voltage at GATE ramps up according to the charge-pump frequency. At 250kHz, the GATE drive current for the MAX8555/MAX8555A is 12µA. Increasing the charge-pump frequency increases the GATE drive current. To change charge-pump frequency, change the value of R_{TIMER}. See the *Selecting the TIMER Resistor* section.

CS+, CS-

The voltage drop across the external MOSFETs is measured between the CS+ and CS- inputs. CS+ connects to the positive side of the input voltage. CS- connects to the positive side of the system bus. The MAX8555/MAX8555A use the voltage drop across CS+ and CS- to determine operating mode. $I_{FORWARD}$ is defined as V_{CS+} - V_{CS-} and must be greater than 0.01V (typ) to properly detect an overvoltage fault condition. $I_{REVERSE}$ is defined as V_{CS-} - V_{CS+} and must be greater than 0.02V (MAX8555A) or 0.04V (MAX8555) (typ) for a reverse-current fault. The $I_{FORWARD}$ and $I_{REVERSE}$ thresholds can be effectively increased by placing an external divider such as R8 and R9 as shown in Figure 4. The values shown increase the thresholds by 50%. When R8 and R9 are used, also add R10 (a parallel combination of R8 and R9) to eliminate any input offset errors caused by impedance differences and input-bias-current differences.

Fault Conditions

The MAX8555/MAX8555A have an open-drain $\overline{FAULT}$ output that signals overvoltage, undervoltage, or reverse-current fault conditions. During a fault condition, $\overline{FAULT}$ is pulled to GND, the charge pump shuts down, and GATE discharges to CS- in 200ns (typ). See Table 1 for fault modes.

Undervoltage Fault

The MAX8555/MAX8555A turn off the external MOSFETs if V_{UVP} falls below the UVP threshold (0.4V). Connect UVP to the center of a resistor-divider from the input supply to GND. Once V_{UVP} rises above the UVP rising threshold (0.5V), $\overline{FAULT}$ clears and GATE is driven high. $\overline{FAULT}$ is not latched. Connect UVP to VL to disable the undervoltage-protection feature.

Overvoltage Fault

The MAX8555/MAX8555A are protected from overvoltage conditions using an adjustable overvoltage-protection input. A resistor-divider from the output bus to GND with OVP connected to the center tap sets the overvoltage threshold. When V_{OVP} exceeds the OVP threshold (0.5V) and the device is in the $I_{FORWARD}$ condition

Low-Cost, High-Reliability, 0.5V to 3.3V ORing MOSFET Controllers

Table 1. Fault Modes

FAULT MODE	CONDITIONS	GATE	$\overline{\text{FAULT}}$	LATCHING
VL UVLO	$VL < VL_{OK}$	LOW	High Impedance	NO
UVP Undervoltage Protection	$V_{UVP} < 0.4V$	LOW	LOW	NO
OVP Overvoltage Protection	$V_{OVP} > 0.5V$ $V_{CS+} > V_{CS-} + 0.01V$	LOW	LOW	YES
Reverse-Current Protection	$V_{CS+} < V_{CS-} - 0.04V$ (0.02V for MAX8555A) and GATE is on for > 2048 charge-pump cycles	LOW	LOW	YES
V_{DD} Internal Overvoltage Protection	$V_{DD} > 14.5V$	LOW	LOW	NO

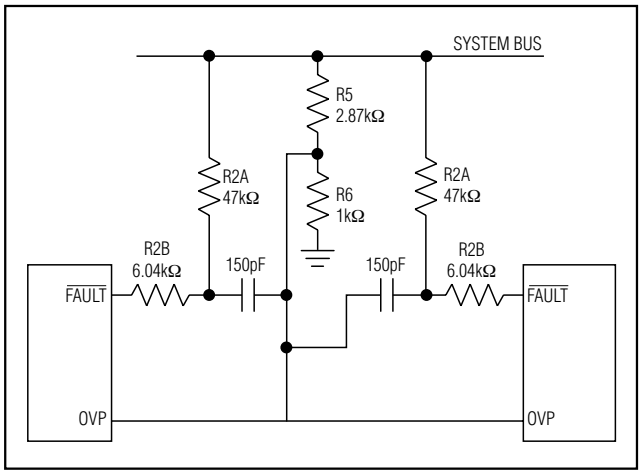


Figure 2. OVP Connection when Multiple MAX8555s Are Used

(defined as $V_{CS+} > V_{CS-} + 0.01V$), the MAX8555/MAX8555A discharge GATE to GND and $\overline{\text{FAULT}}$ is latched low. If the $I_{FORWARD}$ condition is not detected, OVP is disabled. In redundant systems, when one input supply approaches its OVP threshold, some of the other input supplies may be pulled up with it, thereby tripping those OVP comparators with a slightly lower set point. The $I_{FORWARD}$ condition for the pulled-up supplies may not be detected until the first supply is shut down. An alternate application schematic for $\overline{\text{FAULT}}$ and OVP is shown in Figure 2. The $\overline{\text{FAULT}}$ output of the first channel, which has both OVP and $I_{FORWARD}$ conditions, temporarily reduces the common OVP signal by 125mV. This ensures that only the input supply, which is causing the overvoltage condition, is turned off in a redundant power-system application. Exceeding the OVP threshold causes the MAX8555/MAX8555A to be latched off. Toggle V_{DD} or TIMER to reset the IC. Connect OVP to GND to disable the overvoltage-protection feature.

Reverse-Current Fault

The MAX8555/MAX8555A provide a reverse-current fault-protection feature that turns off the oring MOSFET when a reverse-current fault condition is detected. Once a reverse-current fault condition is detected, the MAX8555/MAX8555A discharge GATE to GND and latch $\overline{\text{FAULT}}$ low. Toggle V_{DD}, VL, or TIMER to reset the IC. The reverse-current-protection feature is blanked for 2048 charge-pump cycles at startup.

Selecting the TIMER Resistor

Connect a resistor from TIMER to GND to set the internal charge pump's frequency of operation. Determine the TIMER resistor with the following equation:

$$R_{TIMER} = \frac{1.25V}{100\mu A - \frac{f}{5kHz/\mu A}}$$

Drive TIMER above 1.5V for the maximum charge-pump frequency (550kHz). Drive TIMER below 0.5V to disable the charge pump and shut down the MAX8555/MAX8555A.

Selecting the GATE Capacitor and GATE Resistor

The charge pump uses an internal monolithic transfer capacitor to charge the external MOSFET gates. Normally, the external MOSFET's gate capacitance is sufficient to serve as a reservoir capacitor. To slow down turn-on times further, add a small capacitor between GATE and GND. Adding a small resistor between GATE and the gate of the Oring MOSFET reduces the high-frequency ringing due to gate trace inductance. However, the resistor increases the turn-off time.

Applications Information

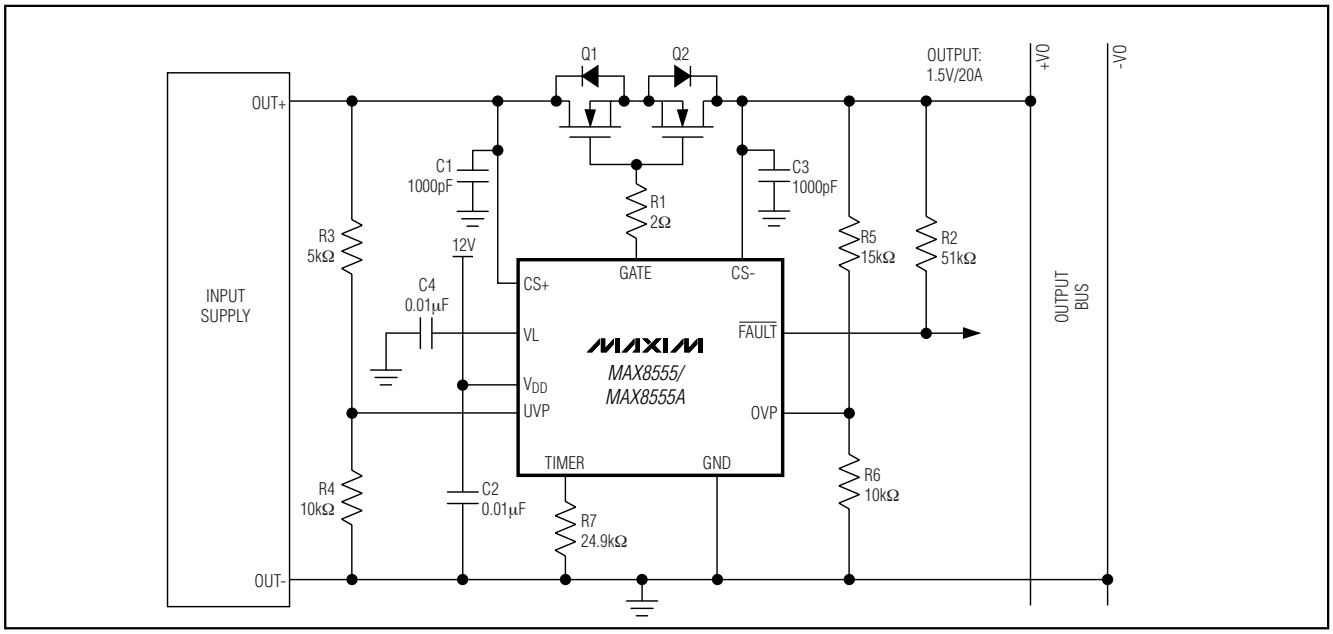


Figure 3. Application Circuit for 12V IC Supply Voltage

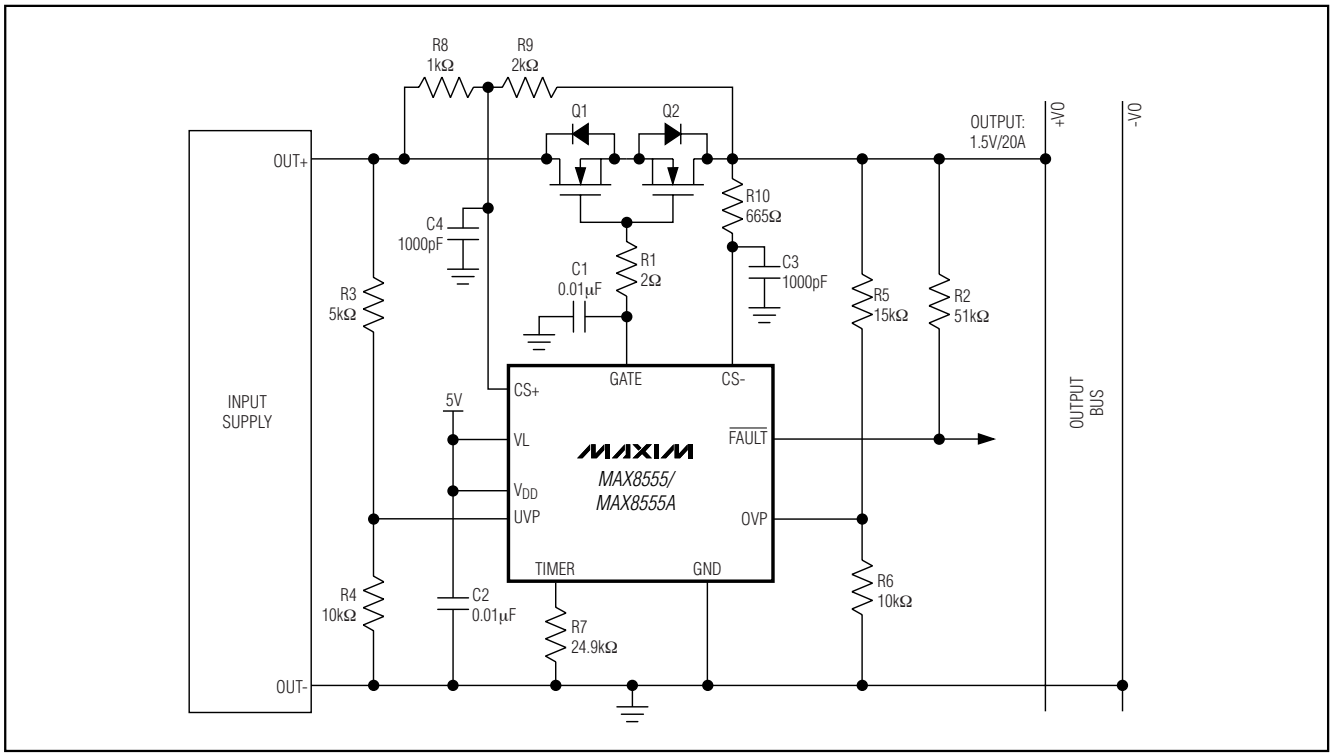


Figure 4. Application Circuit for 5V IC Supply Voltage

Low-Cost, High-Reliability, 0.5V to 3.3V ORing MOSFET Controllers

Set the UVP Fault Threshold

Use a resistor-divider from the input supply to GND with the center tap connected to UVP to set the undervoltage threshold. Use a 10kΩ resistor from UVP to GND (R4 in Figure 4) and calculate R3 as follows:

$$R_3 = R_4 \left(\frac{V_{UV}}{V_{UVP}} - 1 \right)$$

where V_{UV} is the desired undervoltage trip point and V_{UVP} is the UVP reference threshold (0.4V typ). Connect UVP to VL to disable the undervoltage-protection feature.

Set the OVP Fault Threshold

For a single-supply application, use a resistor-divider from the output bus to GND with the center tap connected to OVP to set the overvoltage threshold. Use a 10kΩ resistor from OVP to GND (R6 in Figure 4) and calculate R5 as follows:

$$R_5 = R_6 \left(\frac{V_{OV}}{V_{OVP}} - 1 \right)$$

where V_{OV} is the desired overvoltage threshold and V_{OVP} is the OVP reference threshold (0.5V typ). Connect OVP to GND to disable the overvoltage-protection feature.

For (n + 1) applications, the required circuit values are:

$$R6 = 1k\Omega$$

$$R5 = R6 \times \left[\frac{V_{OV}}{V_{OVP}} - 1 \right]$$

$$R2A = 47k\Omega$$

$$R2B = 2 \times R5$$

where the resistors are as shown in Figure 2.

MOSFET Selection

The MAX8555/MAX8555A drive N-channel MOSFETs. The most important specification of the MOSFETs is $R_{DS(ON)}$. As load current flows through the external MOSFET, V_{DS} is generated from source to drain due to the MOSFET's on-resistance, $R_{DS(ON)}$. The MAX8555/MAX8555A monitor V_{DS} of the MOSFETs at all times to determine the state of the monitored power supply. Selecting a MOSFET with a low $R_{DS(ON)}$ allows more current to flow through the MOSFETs before the MAX8555/MAX8555A detect reverse-current ($I_{REVERSE}$) and forward-current ($I_{FORWARD}$) conditions.

Using Two MOSFETs

Two MOSFETs must be used for overvoltage protection. When using two external MOSFETs, the monitored voltage equation becomes:

$$V_{DSTOTAL} = R_{DS(ON)1} \times I_{LOAD} + R_{DS(ON)2} \times I_{LOAD}$$

Using One MOSFET

A single MOSFET can be used if the overvoltage-protection function is not needed. Connect CS+ to the source of the MOSFET and CS- to the drain of the MOSFET.

Calculating GATE Current

The charge-pump output current is proportional to both oscillator frequency and V_{VL}. There is also a small internal load of approximately 6MΩ. The GATE current for a given V_{VL} and R_{TIMER} is calculated as:

$$I_{GATE} \approx \left\{ 24.12 \times \left[\frac{(V_L - 0.8)}{3.4} \right] \times \left[1 - \left[\frac{12{,}500}{R_{TIMER}} \right] \right] - 0.4 \right\} \mu A$$

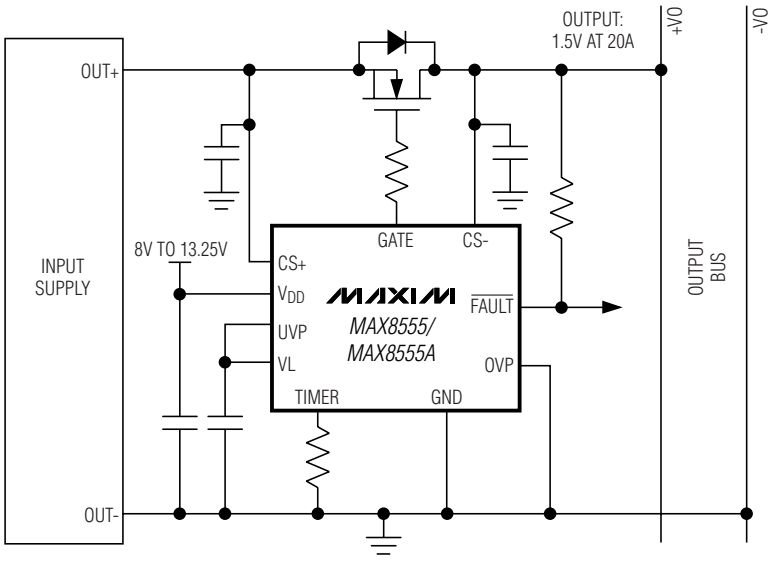
Layout Guidelines

It is important to keep all traces as short as possible and to maximize the high-current trace dimensions to reduce the effect of undesirable parasitic inductance. The MOSFET dissipates a fair amount of heat due to the high currents involved, especially during an overcurrent condition. To dissipate the heat generated by the MOSFET, make the power traces very wide with a large amount of copper area and place the MAX8555 as close as possible to the drain of the external MOSFET. A more efficient way to achieve good power dissipation on a surface-mount package is to lay out two copper pads directly under the MOSFET package on both sides of the board. Use enlarged copper mounting pads on the top side of the board. Use a ground plane to minimize impedance and inductance. In addition to the usual high-power considerations, here are three tips to prevent false faults:

1) Kelvin connect CS+ and CS- to the external MOSFET and route the two traces in parallel, as close as possible, back to the IC.
2) Bypass V_{DD} with a 0.01µF capacitor to ground and bypass CS+ and CS- with a 1000pF capacitor to ground.
3) Make the traces connected to UVP and OVP as short as possible.

Refer to the MAX8555/MAX8555A evaluation kit for an example of good PC board layout.

Typical Operating Circuit



Chip Information

TRANSISTOR COUNT: 2309

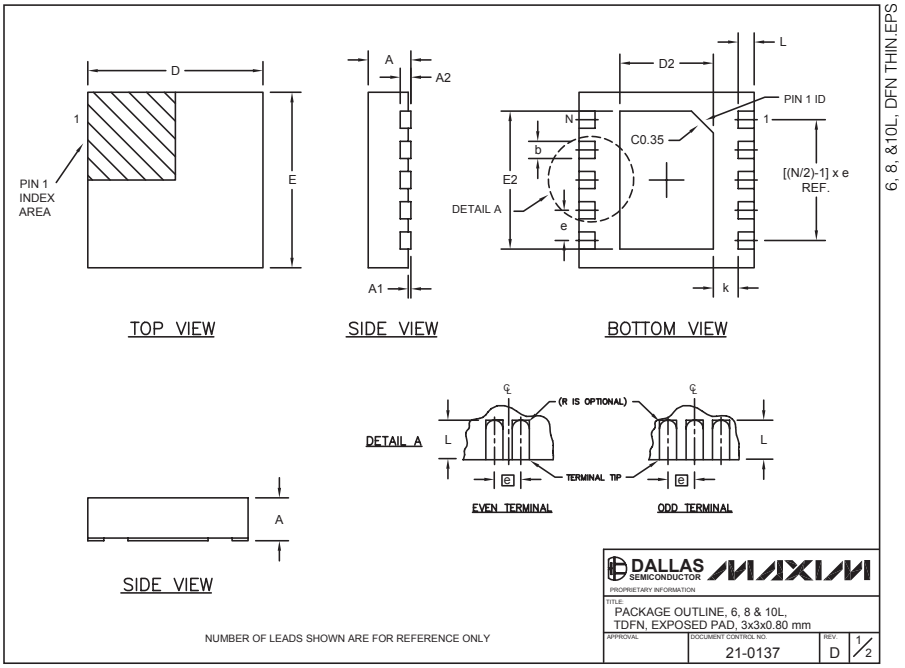
PROCESS: BiCMOS

Low-Cost, High-Reliability, 0.5V to 3.3V ORing MOSFET Controllers

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

6, 8, &10L, DFN THIN.EPS



COMMON DIMENSIONS		
SYMBOL	MIN.	MAX.
A	0.70	0.80
D	2.90	3.10
E	2.90	3.10
A1	0.00	0.05
L	0.20	0.40
k	0.25 MIN.	
A2	0.20 REF.	

PACKAGE VARIATIONS							
PKG. CODE	N	D2	E2	e	JEDEC SPEC	b	[(N/2)-1] x e
T633-1	6	1.50±0.10	2.30±0.10	0.95 BSC	MO229 / WEEA	0.40±0.05	1.90 REF
T833-1	8	1.50±0.10	2.30±0.10	0.65 BSC	MO229 / WEEC	0.30±0.05	1.95 REF
T1033-1	10	1.50±0.10	2.30±0.10	0.50 BSC	MO229 / WEED-3	0.25±0.05	2.00 REF

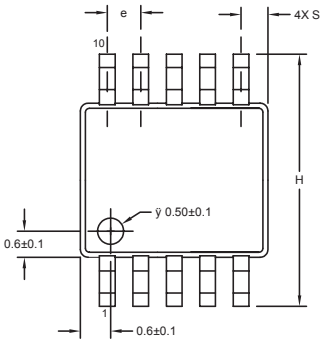
NOTES:
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY SHALL NOT EXCEED 0.08 mm.
3. WARPAGE SHALL NOT EXCEED 0.10 mm.
4. PACKAGE LENGTH/PACKAGE WIDTH ARE CONSIDERED AS SPECIAL CHARACTERISTIC(S).
5. DRAWING CONFORMS TO JEDEC MO229, EXCEPT DIMENSIONS "D2" AND "E2".
6. "N" IS THE TOTAL NUMBER OF LEADS.

DALLAS SEMICONDUCTOR MAXIM
PROPRIETARY INFORMATION
TITLE
PACKAGE OUTLINE, 6, 8 & 10L,
TDFN, EXPOSED PAD, 3x3x0.80 mm
APPROVAL
DOCUMENT CONTROL NO.
21-0137
REV.
D
2/2

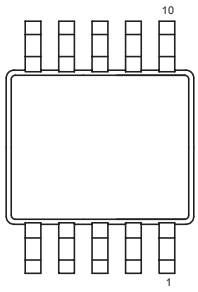
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

10LUMAX.EPS

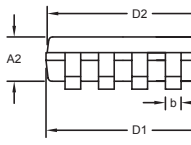


TOP VIEW

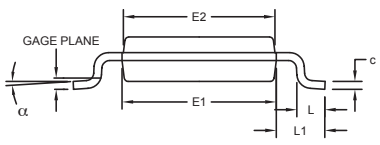


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0∞	6∞	0∞	6∞



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1