*Click **here** to ask an associate for production status of specific part numbers.*

MAX20480

Four- to Seven-Input Automotive Power-System Monitor Family

General Description

The MAX20480 is a complete ASIL-compliant SoC power-system monitor with up to seven voltage monitor inputs. Each input has programmable OV/UV thresholds of between 2.5% and 10% with ±1% accuracy. Two of the inputs have a separate remote ground-sense input and support DVS through the integrated I2C interface.

The MAX20480 contains a programmable flexible power sequence recorder (FPSR). This recorder stores power-up and power-down timestamps separately, and supports on/off and sleep/standby power sequences. The MAX20480 also contains a programmable challenge/response watchdog, which is accessible through the I2C interface, along with a configurable RESET output.

The MAX20480 improves reliability while significantly reducing system size and component count, compared to separate ICs or discrete components. The MAX20480 meets ASIL D reliability when used with a supervisory controller. The device is designed to operate over the ambient temperature range of -40°C to +125°C.

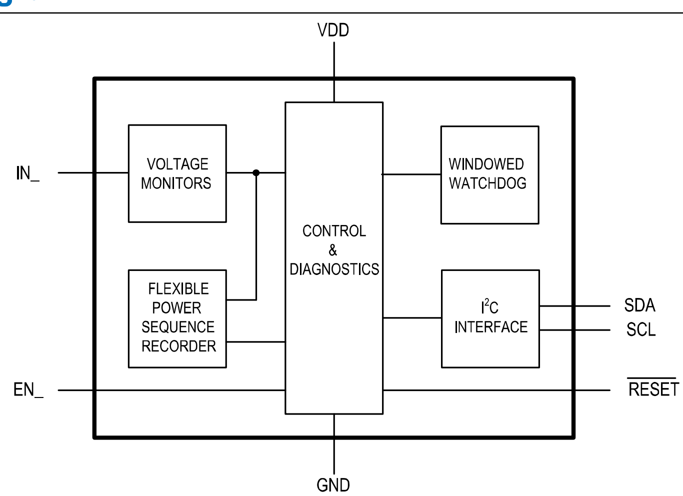
Applications

- ADAS
- Autonomous Driving Processing Systems
- Remote Sensor Modules
- Power System Supervision and MCU/SoC Monitoring

Benefits and Features

- Small Solution
  - 2.35V to 5.50V Operating Supply Voltage
  - Only One External Component Required
  - 150μA Operating Current
  - 8μA Power-Down Mode
- High Precision
  - Selectable 102.5% to 110% OV Monitors
  - Selectable 97.5% to 90% UV Monitors
  - ±1% Accuracy
  - 0.5% Step Size
  - ASIL D Compliance
- Highly Integrated
  - Five Fixed-Voltage Monitoring Inputs
  - Two Differential DVS Tracking-Voltage Monitoring Inputs with Remote-Ground Sense
  - Power-Sequencing Recording
  - Simple or Challenge/Response Windowed Watchdog
  - Fault Recording
  - CRC on I2C Interface
  - Programmable I2C Address
  - OTP Configuration with Error-Correcting Code and Reload Functionality
  - Programmable RESET Pin
- 16-Pin, Side-Wettable TQFN with Exposed Pad (3mm x 3mm)
- AEC-Q100 Qualified
- -40°C to +125°C Operating Temperature

Simplified Block Diagram



Ordering Information *appears at end of data sheet.*

19-100398; Rev 14; 11/21

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Absolute Maximum Ratings

V_{DD} to GND ... -0.3V to +6V
EN0, EN1 to GND ... -0.3V to +6V
IN1-IN5 to GND ... -0.3V to +6V
INP6-INP7 to GND ... -0.3V to +6V
INM to GND ... -0.3V to 0.3V
RESET to GND ... -0.3V to +6V
SDA, SCL to GND ... -0.3V to +6V
ADDR to GND ... -0.3V to V_{DD} + 0.3V
Continuous Power Dissipation (T_A = +70°C) ...
16-TQFN (derate 20.8mW/°C > 70°C) ... 1666.7mW
Operating Temperature ... -40ºC to +125ºC
Junction Temperature ... +150ºC
Storage Temperature Range ... -65ºC to +150ºC
Lead Temperature Range ... +300ºC

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

16-TQFN-EP

Package Code	T1633Y+5
Outline Number	21-100150
Land Pattern Number	90-100064
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction-to-Ambient (θ_{JA})	44.5°C/W
Junction-to-Case Thermal Resistance (θ_{JC})	5.9°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{DD} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted, Typical values are at T_A = 25°C under normal conditions unless otherwise noted.,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage Range	V_{DD}	Fully operational	2.35		5.5	V
		RESET output guaranteed low	1.2			
Supply Current	I_{VDD}	EN0 = high, no change of state on EN1 and not in sequence monitoring mode		150	210	µA
		EN0 = low and power-down sequence complete. All IN_ comparators turned off.		8	16	
UVLO	V_{UVLO}	V_{DD} Voltage Rising	1.85	2.05	2.25	V
		V_{DD} Voltage Falling	1.75	1.95	2.15	
Internal Oscillator	f_{OSC}		1.15	1.28	1.40	MHz
IN1-IN4						
Input Current	$I_{IN\_}$	$V_{IN\_}$ ≤ 3.3V		1	1.5	µA
Set-Point Range			0.5		3.6875	V
Set-Point Resolution		12.5mV/step		8		Bits
OV/UV Threshold Range			2.5		10	%

Electrical Characteristics (continued)

(V_{DD} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted, Typical values are at T_A = 25°C under normal conditions unless otherwise noted.,)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OV/UV Threshold Resolution		0.5%/step		4		Bits
OV/UV Threshold Accuracy		(IN1 through IN4) ≥ 1.0V. Factory-trimmed thresholds.	-1		1	%
		(IN1 through IN4) < 1.0V. Factory-trimmed thresholds.	-10		10	mV
OFF Threshold	V_{OFF}	(IN1 through IN4) voltage falling	0.23	0.25	0.27	V
		(IN1 through IN4) voltage rising	0.28	0.3	0.32	
UV Comparator Filter Time	t_{UV}	2% below threshold		5		µs
OV Comparator Filter Time	t_{OV}	2% above threshold		5		µs
IN5						
Input Current	I_{IN5}	V_{IN5} ≤ 5V		1.5	2.3	µA
Set-Point Range			0.5		5.5	V
Set-Point Resolution		20mV/step		8		Bits
OV/UV Threshold Resolution		0.5%/step		4		Bits
OV/UV Threshold Accuracy		IN5 ≥ 1.0V. Factory-trimmed thresholds.	-1		1	%
		IN5 < 1.0V. Factory-trimmed thresholds.	-10		10	mV
OFF Threshold	V_{OFF}	IN5 voltage falling	0.23	0.25	0.27	V
		IN5 voltage rising	0.28	0.3	0.32	
UV Comparator Filter Time	t_{UV}	2% below threshold		5		µs
OV Comparator Filter Time	t_{OV}	2% above threshold		5		µs
OV/UV Threshold Range			2.5		10	%
IN6P-IN7P, INM						
INM Range	V_{INM}		-0.1		0.1	V
Input Current	$I_{IN\_}$	$V_{IN\_}$ ≤ 1.8V		1.4	2.2	µA
Set-Point Range		Relative to INM	0.5		1.775	V
Set-Point Resolution		5mV/step		8		Bits
Set-Point Accuracy		(IN6P, IN7P) ≥ 1.0V	-1		1	%
		(IN6P, IN7P) < 1.0V	-10		10	mV
OFF Threshold	V_{OFF}	(IN6P, IN7P) voltage falling, relative to INM	0.23	0.25	0.27	V
		(IN6P, IN7P) voltage rising, relative to INM	0.28	0.3	0.32	
UV Comparator Filter Time	t_{UV}	2% below threshold		5		µs

Electrical Characteristics (continued)

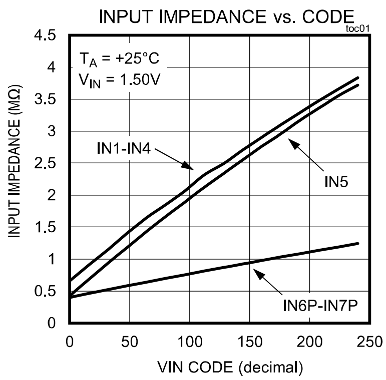
(V_{DD} = 3.3V, T_A = T_J = -40°C to +125°C, unless otherwise noted, Typical values are at T_A = 25°C under normal conditions unless otherwise noted.,)

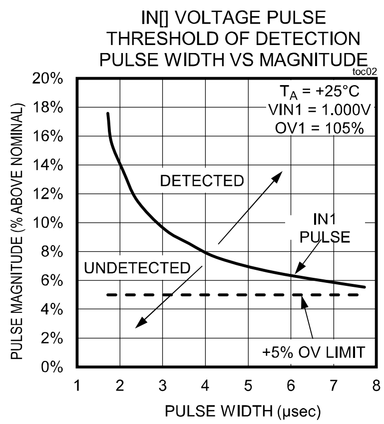
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
OV Comparator Filter Time	t_{OV}	2% above threshold		5		µs
ADDR, EN0, EN1 INPUTS						
Input High Level	V_{IH}	Input Voltage Rising	1.3			V
Input Low Level	V_{IL}	Input Voltage Falling			0.4	V
Hysteresis				0.1		V
EN0, EN1 Pulldown Resistance	R_{PD}	V_{EN0} = V_{EN1} = 3.3V	1.1	2	3	MΩ
EN0, EN1 Spike Suppression				60		ns
ADDR Input Leakage	$I_{ADDR\text{-}LKG}$	V_{ADDR} = V_{DD} = 3.3V			1	µA
DIGITAL OUTPUT ($\overline{RESET}$)						
Digital Output Low Level	V_{RL}	V_{DD} = 2.35V, I_{SINK} = 2mA			0.2	V
Digital Output Leakage	$I_{R\text{-}LKG}$	$\overline{RESET}$ = 5.0V			1	µA
Active Timeout Period	t_{HOLD}	RHLD[1:0] = 00		6		µs
		RHLD[1:0] = 01	7.2	8	8.8	ms
		RHLD[1:0] = 10	14.4	16	17.6	
		RHLD[1:0] = 11	28.8	32	35.2	
I^2C INTERFACE						
Input High Level	V_{IH}	Input Voltage Rising	1.3			V
Input Low Level	V_{IL}	Input Voltage Falling			0.4	V
Output Low	V_{OL}	I_{SINK} = 4mA			0.3	V
Input Leakage	I_{LKG}	V_{SCL} = V_{SDA} = 3.3V			1	µA
Clock Frequency	f_{SCL}				1.1	MHz
Setup Time (Repeated) START	$t_{SU:STA}$		260			ns
Hold Time (Repeated) START	$t_{HD:STA}$		260			ns
SCL Low Time	t_{LOW}		350			ns
SCL High Time	t_{HIGH}		260			ns
Data Setup Time	$t_{SU:DAT}$		150			ns
Data Hold Time	$t_{HD:DAT}$		30			ns
Setup Time for STOP Condition	$t_{SU:STO}$		260			ns
Spike Suppression				50		ns

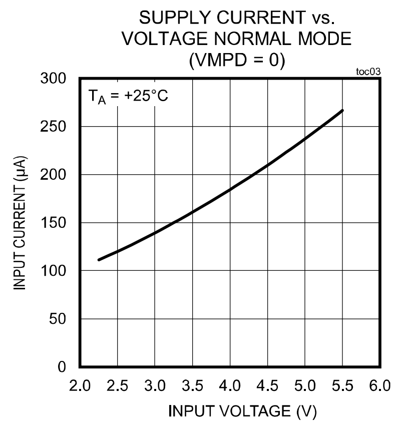
Note 1: All units are 100% production tested at +25˚C. All temperature limits are guaranteed by design.

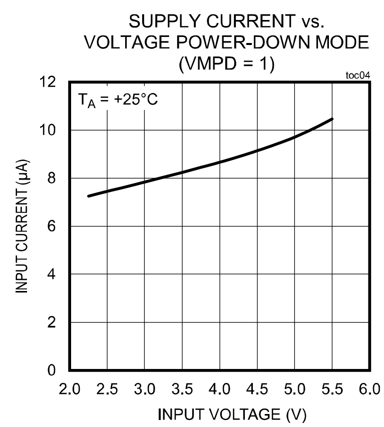
Typical Operating Characteristics

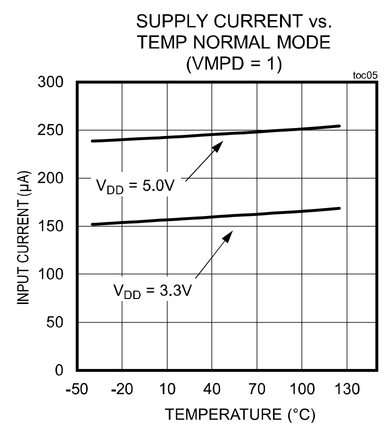
(V_{DD} = 3.3V, T_A = +25°C)

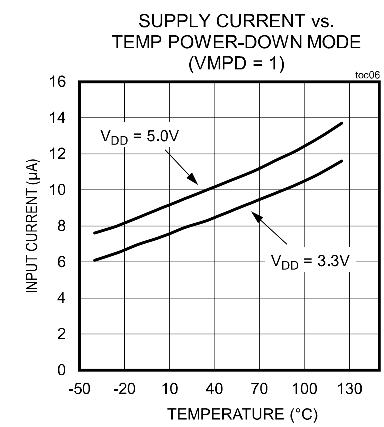


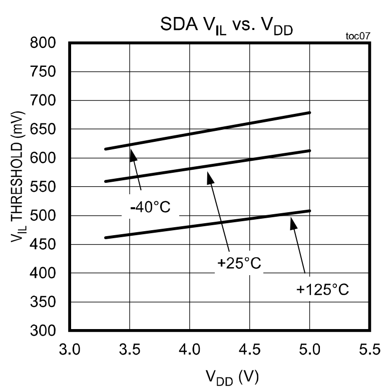


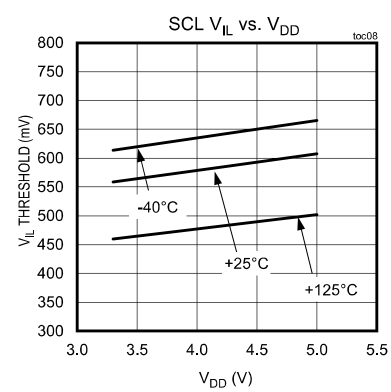


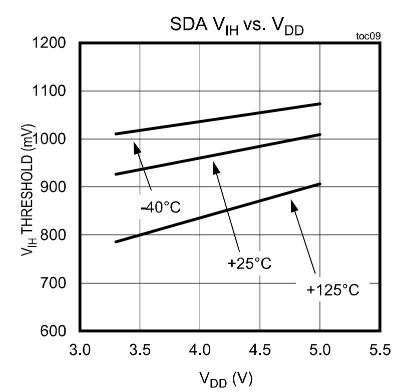






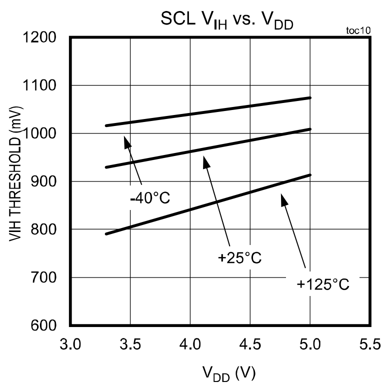


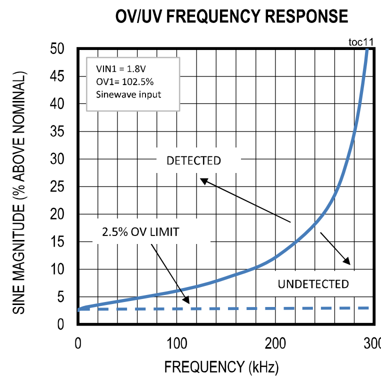




Typical Operating Characteristics (continued)

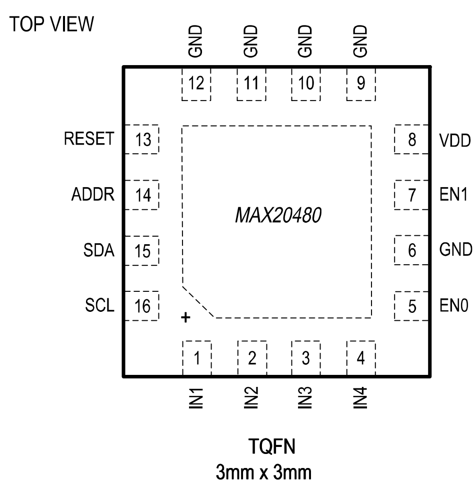
(V_{DD} = 3.3V, T_A = +25°C)



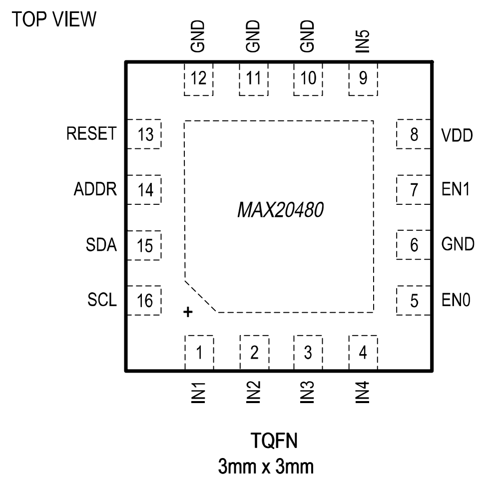


Pin Configurations

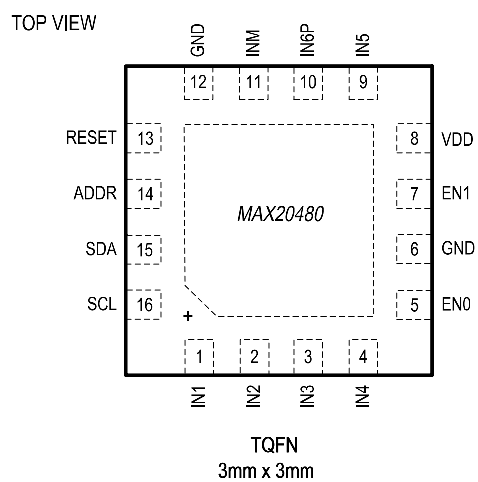
MAX20480A



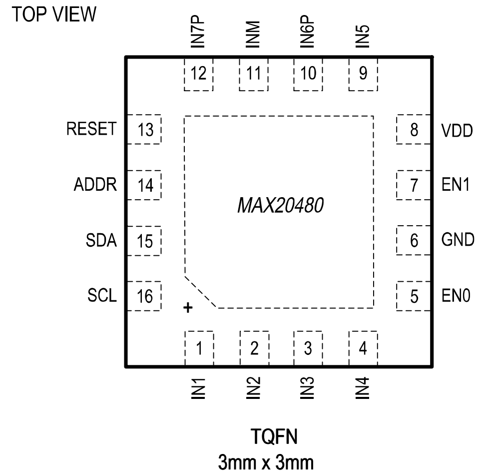
MAX20480B



MAX20480C



MAX20480D



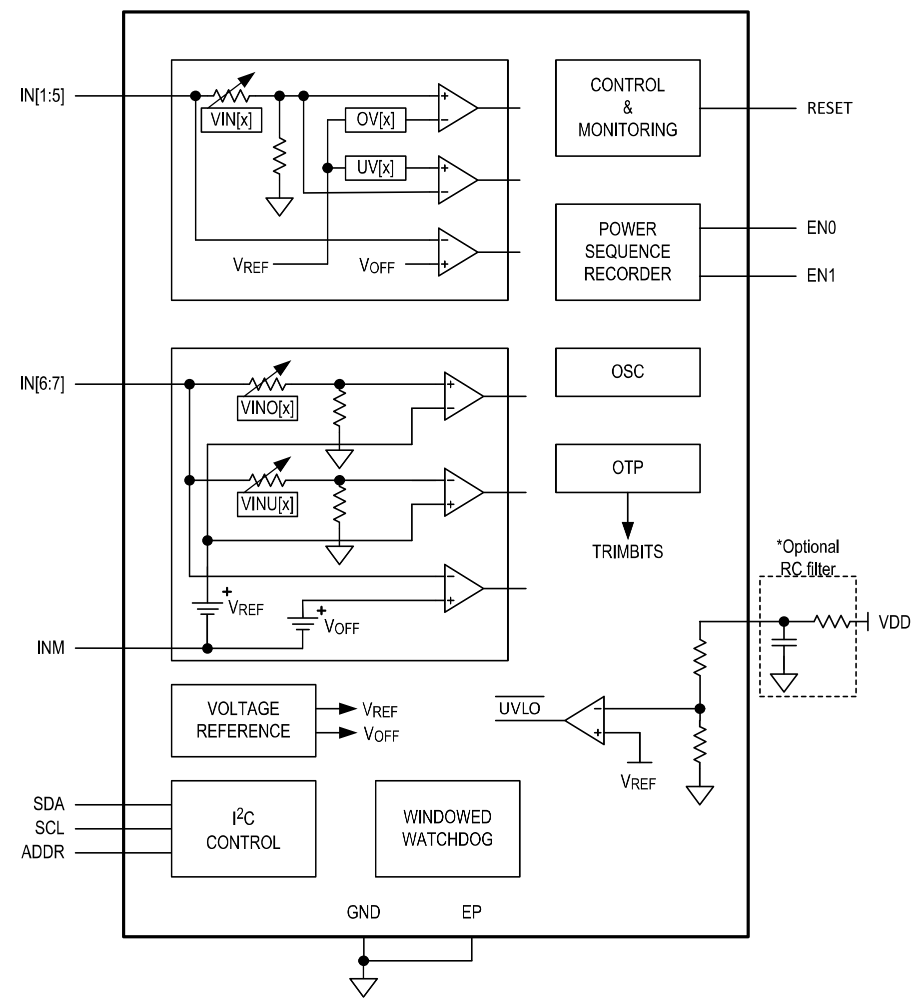
Pin Description

PIN				NAME	FUNCTION
MAX20480A	MAX20480B	MAX20480C	MAX20480D		
1	1	1	1	IN1	Input Voltage Monitor 1.
2	2	2	2	IN2	Input Voltage Monitor 2.
3	3	3	3	IN3	Input Voltage Monitor 3.
4	4	4	4	IN4	Input Voltage Monitor 4.
5	5	5	5	EN0	Enable Input 0. Raise/lower the EN0 input to indicate a transition from OFF→ON/ON→OFF, respectively, in the system.
6	6	6	6	GND	Ground. Connect all grounds together at the EP.
7	7	7	7	EN1	Enable Input 1. Raise/lower the EN1 input to indicate a transition from SLEEP→ON/ ON→SLEEP, respectively, in the system.
8	8	8	8	V_{DD}	Input Supply Voltage. Connect a 0.1µF capacitor between V_{DD} and GND and place close to the IC. For excessive VDD transients with edge rates >40mV/µs an RC filter is required on the VDD supply.
9	-	-	-	GND	Ground. Connect all grounds together at the EP.
-	9	9	9	IN5	Input Voltage Monitor 5.
10	10	-	-	GND	Ground. Connect all grounds together at the EP.
-	-	10	10	IN6P	Differential Input Voltage Monitor 6.
11	11	-	-	GND	Ground. Connect all grounds together at the EP.
-	-	11	11	INM	Common negative input for voltage monitors IN6P and IN7P.
12	12	12	–	GND	Ground. Connect all grounds together at the EP.

Pin Description (continued)

PIN				NAME	FUNCTION
MAX20480A	MAX20480B	MAX20480C	MAX20480D		
13	13	13	13	$\overline{RESET}$	$\overline{RESET}$ Output. Open-drain output that signals a status change. Can be mapped to any combination of input monitors to indicate they are within nominal operating range. Connect to logic supply with a pullup resistor.
-	-	-	12	IN7P	Differential Input Voltage Monitor 7.
14	14	14	14	ADDR	I^2C Address Select. Connect to GND or V_{DD}, with or without a 100kΩ pullup resistor, to set the I^2C address. See Table 1.
15	15	15	15	SDA	I^2C Data I/O.
16	16	16	16	SCL	I^2C Clock Input.
-	-	-	-	EP	Exposed Pad. Connect to ground. Does not serve as a substitute for a proper GND pin connection.

Functional Diagram



Detailed Description

The MAX20480 is a complete ASIL-D compliant SoC power-system monitor. It has three main subsystems with which to monitor a given application system: a 7-channel voltage monitor, a flexible power sequence recorder (FPSR), and a challenge/response windowed watchdog. It also includes an I²C interface to communicate with a supervisory controller for monitoring and diagnosis of fault conditions. To meet ASIL-D reliability specifications, there are numerous checks and redundancies in the system to maintain a high performance level, as well as configuration and diagnostics available over the I²C interface for a supervisory controller to adjust and monitor.

I²C Interface

The MAX20480 features an I²C, 2-wire serial interface consisting of a serial-data line (SDA) and a serial-clock line (SCL). SDA and SCL facilitate communication between the MAX20480 and the master at clock rates up to 1.1MHz. The master, typically a microcontroller, generates SCL and initiates data transfer on the bus. Figure 1 shows the two-wire interface timing diagram.

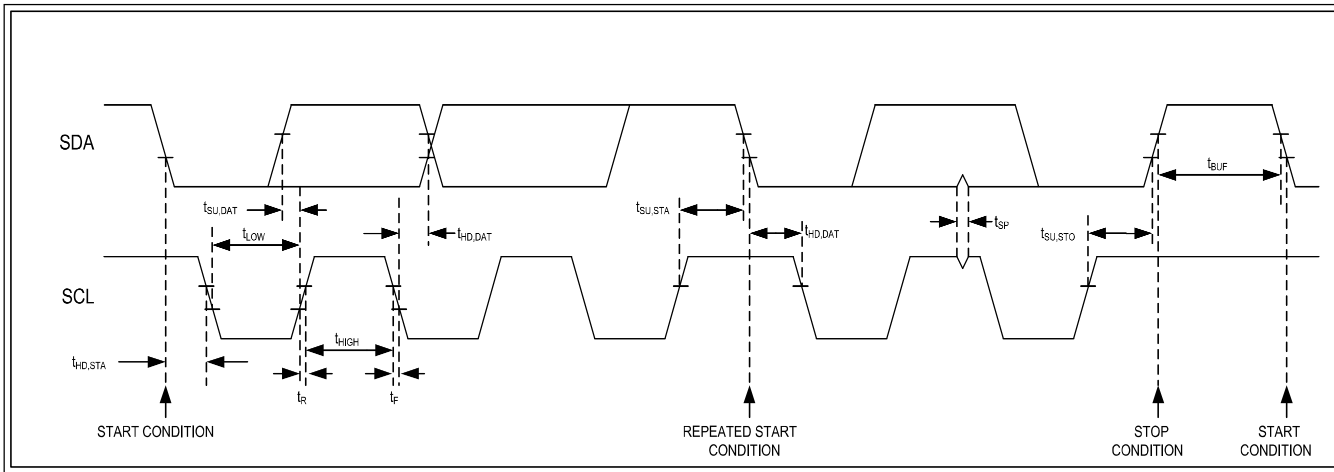


Figure 1. I²C Timing Diagram

A master device communicates to the MAX20480 by transmitting the proper address followed by the data word. Each transmit sequence is framed by a START (S) or REPEATED START (Sr) condition and a STOP (P) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse.

The MAX20480 SDA line operates as both an input and an open-drain output. A pullup resistor greater than 500Ω is required on the SDA bus. The MAX20480 SCL line operates as an input only. A pullup resistor greater than 500Ω is required on SCL if there are multiple masters on the bus, or if the master in a single-master system has an open-drain SCL output. Series resistors in line with SDA and SCL are optional. The SCL and SDA inputs suppress noise spikes to assure proper device operation, even on a noisy bus.

Bit Transfer

One data bit is transferred during each SCL cycle. The data on SDA must remain stable during the high period of the SCL pulse. Changes in SDA while SCL is high are control signals (see the *STOP and START Conditions* section). SDA and SCL idle high when the I²C bus is not busy.

STOP and START Conditions

A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA with SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high (Figure 2). A START (S) condition from the master signals the beginning of a transmission to the MAX20480. The master terminates transmission and frees the bus by issuing a STOP (P) condition. The bus remains active if a REPEATED START (Sr) condition is generated instead of a STOP condition.

Early STOP Condition

The MAX20480 recognizes a STOP condition at any point during data transmission except if the STOP condition occurs in the same high pulse as a START condition.

Clock Stretching

In general, the clock signal generation for the I^2C bus is the responsibility of the master device. The I^2C specification allows slow slave devices to alter the clock signal by holding down the clock line, a process that is typically called clock stretching. The MAX20480 does not use any form of clock stretching to hold down the clock line.

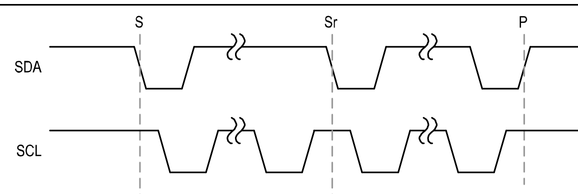


Figure 2. START, STOP, and REPEATED START Conditions

I^2C General Call Address

The MAX20480 does not implement the I^2C specification's general call address. If the MAX20480 sees the general call address (0b0000_0000), it will not issue an acknowledge.

Packet Error Checking (PEC)

In order to increase fault coverage on the I^2C interface, an optional PEC byte is supported. This follows the SMBus 3.0 implementation, which has a CRC-8 polynomial of $x8 + x^2 + x + 1$. If the PEC byte is enabled and a supervisor system attempts to read more than 2 bytes (one data and one PEC) from the IC in a single communication packet, the IC will return 0xFF for the remaining bytes read. If a master device transmits a byte and an incorrect PEC, the IC replies with a NACK and discards the attempted write.

Slave Address

The I^2C address is factory programmable from 0b0000000 to 0b1111011. The address is defined as the 7 most significant bits (MSbs) followed by the R/W bit. Set the R/W bit to 1 to configure the device to read mode. Set the R/W bit to 0 to configure the device to write mode. The address is the first byte of information sent to the device after the START condition.

Once the device is enabled, the I^2C slave address is set by the ADDR pin and internal OTP settings. The address is defined as the 7 MSbs followed by the R/W bit. Connect the ADDR pin to GND or VSUP, with or without a 100kΩ resistor in series, to set the last 2 bits of the I^2C address. The first 4 bits of the I^2C address are factory-configurable (noted by * in Table 1).

Table 1. I^2C Slave Addresses

ADDR PIN	A6*	A5*	A4*	A3*	A2	A1	A0	ADDRESS
Short to GND	0	1	1	1	0	0	0	0x38
100kΩ Pulldown to GND	0	1	1	1	0	0	1	0x39
100kΩ Pullup to VDD	0	1	1	1	0	1	0	0x3A
Short to VDD	0	1	1	1	0	1	1	0x3B

Acknowledge

The acknowledge bit (ACK) is a clocked ninth bit that the device uses to handshake receipt of each byte of data (Figure 3). The device pulls down SDA during the master-generated ninth clock pulse. The SDA line must remain stable and low during the high period of the acknowledge clock pulse. Monitoring ACK allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master can reattempt communication. Transmitting an incorrect PEC byte to the MAX20480 (when PEC is enabled) will also result in a NACK from the IC.

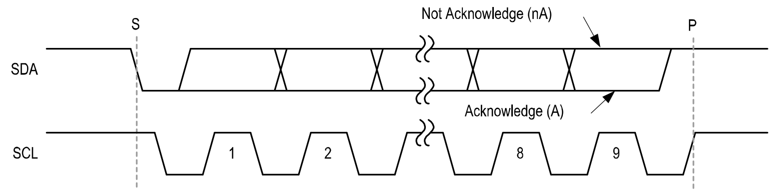


Figure 3. Acknowledge Condition

Write-Data Format

A write to the device includes transmission of a START condition, the slave address with the R/W bit set to 0, 1 byte of data to register address, 1 to 8 bytes of data to write to registers, and a STOP condition. Figure 4 illustrates the proper format for one frame. If multiple bytes are transmitted, they are written to sequential registers starting at the register address transmitted. If the register address for the write reaches the end of the valid address space, the target register pointer will stay at the last valid register. If the write starts out-of-bounds, then all the bytes written will be discarded and the IC will return a NACK for each byte transmitted.

Read-Data Format

A read from the device includes the following:

- Transmission of a START condition
- Slave address with the R/W bit set to 0
- 1 byte of data to register address
- Restart condition
- Slave address with R/W bit set to 1
- 1 to 8 bytes written by the IC
- STOP condition

Figure 4 illustrates the proper format for one frame. The master device must acknowledge each byte received, and provide a NACK at the last byte read.

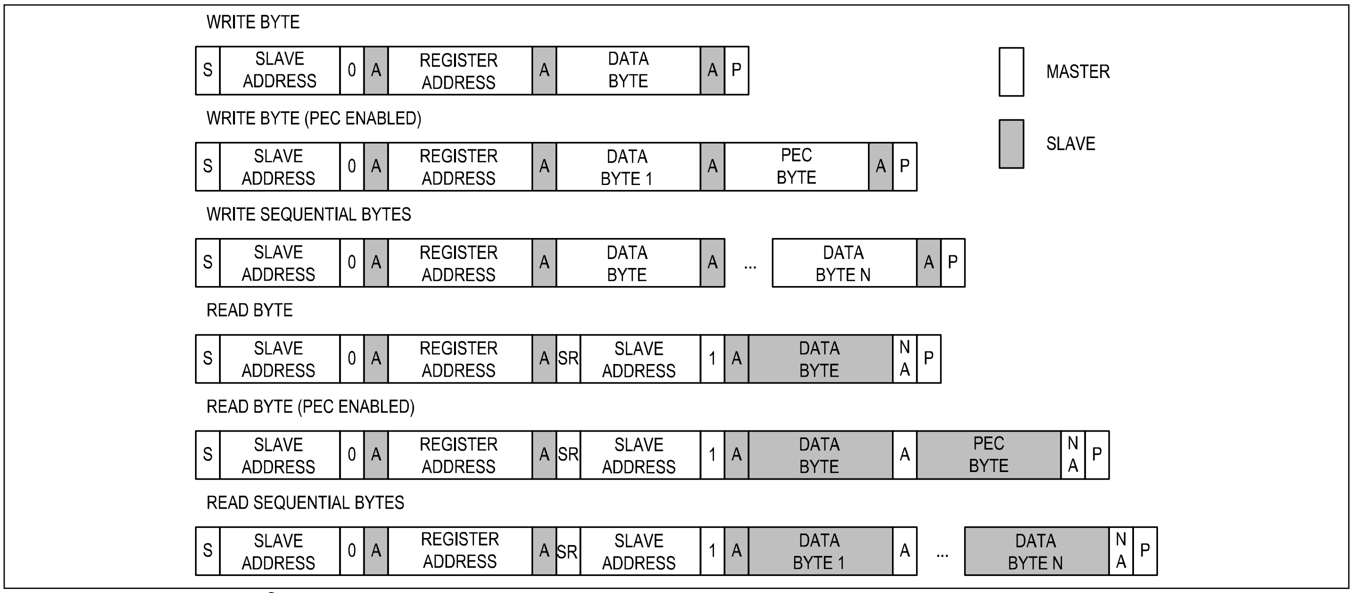


Figure 4. Data Format of I²C Interface

Voltage Monitor

The MAX20480 IC has up to seven voltage-monitor channels available for system power rails. Five of the monitors have single-ended inputs. For these channels, a nominal voltage is set first and OV/UV thresholds (as a percentage of that nominal voltage setting) are set second. The remaining two monitors have differential inputs and share a remote ground-sense pin (INM). Unlike the other monitors with a nominal voltage + %OV/UV configuration, the two differential inputs have completely independent OV and UV comparators; each comparator can be configured with a separate reference voltage.

Monitor channels IN1 through IN5 have the single-ended configuration, with OV/UV thresholds independently configurable from ±2.5% to ±10% in 0.5% steps. IN1 through IN4 have a nominal voltage set-point range of 0.50V to 3.6875V, while IN5 has an extended range of 0.50V to 5.50V. IN6P and IN7P have the differential configuration. Their OV and UV set points can range from 0.50V to 1.775V; these measurements are with respect to the voltage difference between the INxP supply and INM remote ground-sense pins. Every monitor channel also has an OFF comparator that asserts when the monitor input voltage falls below 0.25V (typ).

Modern SoCs and processors can require a large amount of supply current, which may cause small offsets in ground voltages (even when using multiple large ground planes). To account for this when using the differential channels, route the INM pin separately from ground and connect to a point near where the IN6P and IN7P lines are connected. If this feature is not necessary, the INM pin can be grounded directly at the IC.

The comparators on the voltage monitors are designed to respond quickly for applications that require rapid response to voltage fluctuations. If a slower response is desired, an RC filter can be added between the IC pin and the monitored voltage rail. If an RC filter is implemented, the value of the resistor should be kept low to avoid artificial voltage shift at the IC's pins. Because each IN_ pin draws a few microamperes of current, the filter resistor value should be 1kΩ or less.

DVS Operation

Because IN6P and IN7P have independent OV and UV monitors, it is possible to utilize the channels to monitor SoC power rails that implement dynamic voltage scaling (DVS) in response to processing demand. Prior to a DVS event, one of the OV/UV comparator voltage targets can be moved in the direction of the ramp, and then the other can be moved once the ramp has finished. This allows the system to maintain continuous voltage monitoring despite the change in supply voltage.

The other inputs (IN1 through IN5) can also have their target voltage altered, but are not meant to be adjusted while active and are therefore not well-suited to DVS operations. The recommended procedure for changing the target voltage on one of the single-ended channels (IN1 through IN5) while the system is operational is as follows:

1. Disable the channel.
2. Turn off the RESET mapping, if active.
3. Change the target voltage and OV/UV thresholds as desired.
4. Re-enable the channel.
5. Read the OV/UV/OFF registers once to clear any spurious faults.
6. Re-enable the RESET mapping.

DVS Command Sequence (Low to High):

1. Set VINO (OV set point) to high OV threshold.
2. Send DVS command to power supply.
3. Delay as needed to allow supply to reach the target.
4. Set VINU (UV set point) to the high UV threshold.

DVS Command Sequence (High to Low):

1. Set VINU (UV set point) to the low UV threshold.
2. Send DVS command to power supply.
3. Delay as needed to allow supply to reach the target.
4. Set VINO (OV set point) to the low OV threshold.

I²C DVS Timing Example (Low to High)

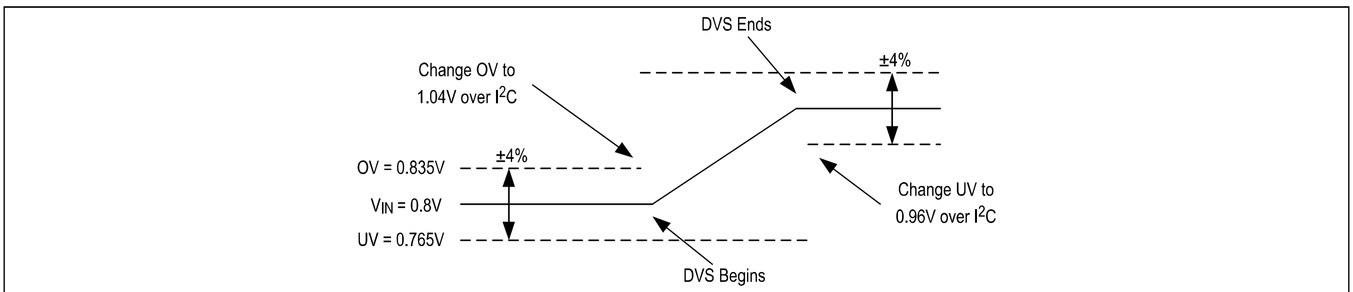


Figure 5. I²C DVS Timing Example (Low-to-High Transition)

Flexible Power Sequence Recorder

The flexible power sequence recorder allows a supervisory controller to validate the power-up and power-down sequencing of all supplies monitored by the IC. The FPSR has an adjustable clock rate (from 25µs/tick to 3200µs/tick) and records 8-bit timestamps (6.375ms to 816ms maximum window length). The FPSR is triggered by level changes on the EN pins. It always responds to EN0 transitions, and can be configured to also respond to EN1 transitions.

Power-up and power-down sequence timestamps are recorded separately. Power-up sequences are triggered by low-to-high pin transitions, and power-down sequences are triggered by high-to-low transitions. The FPSR has additional bits to communicate when it is running, signal which EN pin triggered the sequencer, and choose whether to assert RESET when done recording a sequence. A power-up timestamp is recorded for an enabled channel when the associated voltage rises above the programmed UV threshold. A power-down timestamp is recorded for an enabled channel when the associated voltage falls below the OFF threshold (0.25V falling, typ.).

Once a sequence is captured, it is retained until a flag bit is manually cleared. If another sequence (of the same type, up or down) is triggered before the flag is cleared, it is not recorded, and a separate flag bit is set to indicate this anomaly. To preserve the OTP-reload functionality (see *Applications Information*), the FPSR still runs normally even if the associated UVAL or DVAL bit is set, even though new timestamps may not be recorded. The sequencer will run until either the maximum time is reached, or all enabled voltage monitors have detected that the associated power rails have powered up or down (depending on which type of sequence is being recorded).

Windowed Watchdog and Reset Control

The IC also contains a challenge/response windowed watchdog for external SoC monitoring. The closed and open windows are independently adjustable, as well as the main watchdog clock (which can range from 200µs/tick to 12.8ms/tick). Because the watchdog is meant to supervise a processor system, it features an extended first-update window. When the IC $\overline{\text{RESET}}$ pin de-asserts, the watchdog window is immediately opened and extended to provide extra time for an SoC to finish any boot sequences before being required to update the watchdog. The specific length of the extended first-update window is also configurable.

The watchdog is refreshed through the I^2C interface. When configured as a challenge/response watchdog, there is a key-value register that must be read and used to compute the appropriate response. The IC contains a linear-feedback shift register with a polynomial of $x^8 + x^6 + x^5 + x^4 + 1$ (shift bits upwards toward MSb and insert calculated bit as new LSb). The watchdog can also be configured as a simple windowed watchdog. In this case, any value written to the WDKEY register will refresh the watchdog. For additional resilience, there is an option to lock all of the watchdog-related registers except for the key register and the lock bit itself.

The watchdog has several status bits to communicate current status and past faults. Separate flags are provided to indicate an update-too-early fault, a wrong-key fault, and a no-update-received fault. These fields are cleared when read. There is also a signal to indicate when the watchdog window is open to receive updates. The watchdog itself may be configured to assert $\overline{\text{RESET}}$ on every violation, or wait until it encounters two consecutive violations before triggering a fault. The watchdog is inactive while the $\overline{\text{RESET}}$ pin is asserted low (for any fault condition).

Sample C Code For Challenge/Response

```
// feedback polynomial: x^8 + x^6 + x^5 + x^4 + 1

unsigned char lfsr(unsigned char iKey)
{
unsigned char lfsr = iKey;
unsigned char bit = ((lfsr >> 7) ^ (lfsr >> 5) ^
(lfsr >> 4) ^ (lfsr >> 3)) & 1;
lfsr = (lfsr << 1)| bit;
return lfsr;
}
```

Watchdog Window Settings

A regular watchdog window consists of two parts: an initial (closed) window during which updates are not allowed, and a second (open) window during which updates are accepted. For a given watchdog clock rate t_{WDCLK} (set according to the WDCDIV register), the two window lengths are as follows:

$t_{CLO} = t_{WDCLK} \times 8 \times \text{WDCFG1.CLO}[3:0]$

$t_{OPN} = t_{WDCLK} \times 8 \times \text{WDCFG1.OPN}[3:0]$

If a refresh is sent to the IC during the closed window, the IC asserts a fault and re-starts the watchdog once $\overline{\text{RESET}}$ de-asserts. When the IC receives a valid refresh, it immediately transitions to a new closed window; it will not finish the existing open window. The first cycle encountered once the watchdog starts (either on power-on reset or once $\overline{\text{RESET}}$ de-asserts) is different from the typical closed/open cycle. It has no closed window, and is longer than a normal cycle. This is to allow for an SoC or MCU to run through a boot sequence that may take longer than the usual watchdog cycle. The length of the first update window is an odd multiple of the sum of the normal closed and open windows:

$t_{1UD} = (t_{OPN} + t_{CLO}) \times (1 + 2 \times \text{WDCFG2.1UD}[2:0])$

$\overline{\text{RESET}}$ Output

The device features an open-drain interrupt/reset output that asserts low when any mapped fault conditions occur. $\overline{\text{RESET}}$ remains asserted for a fixed timeout period after all triggering fault conditions are removed. The fixed timeout period can be set to 6µs, 8ms, 16ms, or 32ms. The $\overline{\text{RESET}}$ pin works as an open-drain output. To obtain a logic signal, place a pullup resistor between the $\overline{\text{RESET}}$ pin and system I/O voltage (10kΩ to 100kΩ recommended for reduced current consumption). The selection of which fault sources are mapped to the pin is fully programmable.

Enable Inputs (EN0/EN1)

The primary purpose of the EN0 and EN1 inputs is to indicate that a power-up or power-down sequence is about to occur. EN0 is normally used to indicate a transition between OFF and ON states, while EN1 is for a transition between ON and SLEEP states. This refers to system states, not device states. The device uses EN0 to manage its own power state to maintain the lowest quiescent current possible. With VMPD set to 1 and EN0 low, the device turns off all comparators to reduce quiescent current. With EN1 low, the OFF comparators on input channels that are enabled are left enabled so that the device can continue to monitor active inputs.

Comparator Power States

The voltage-monitor comparators can be individually turned on or off based on the current state of EN0 and the device settings/state. Table 2 details the conditions for the on/off state of the voltage monitor comparators.

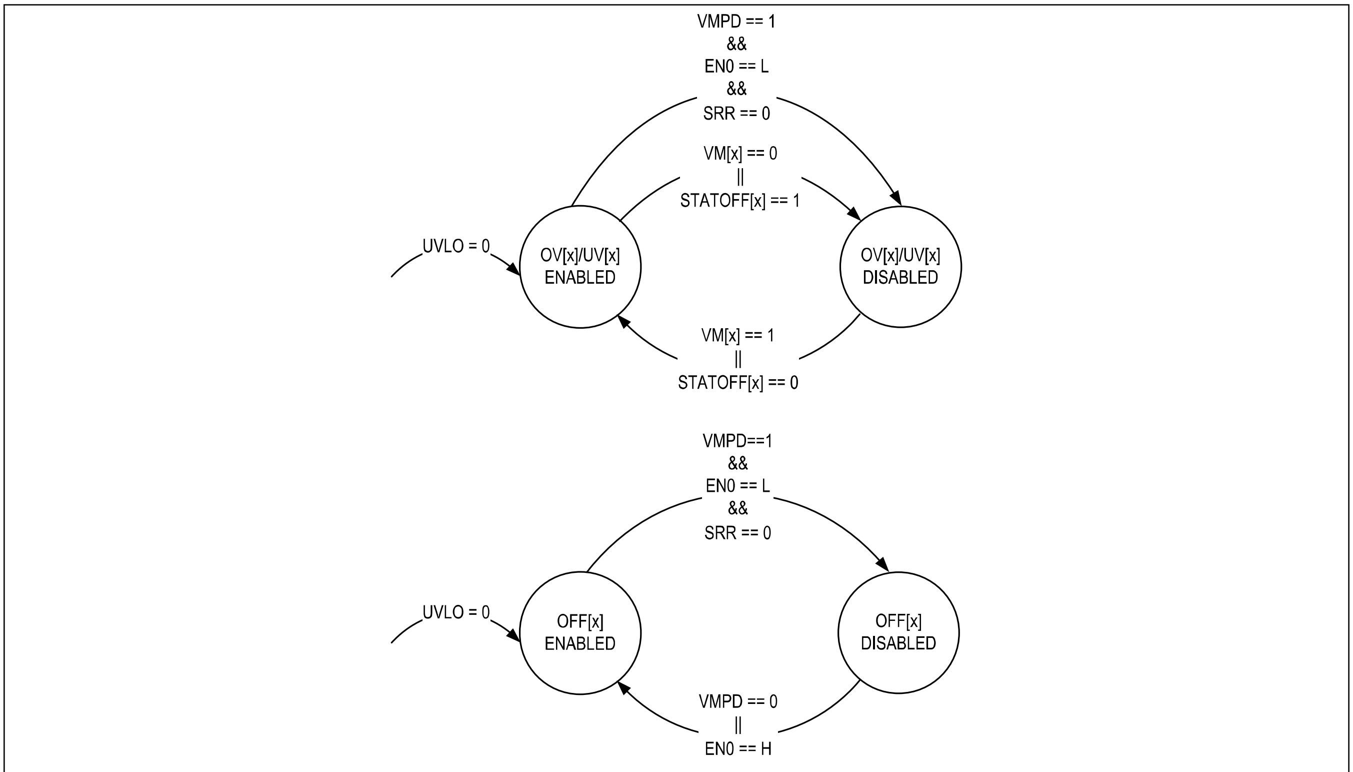


Figure 6. state diagram

Table 2. Comparator Power States

COMPARATORS	COMMENTS
OV[X]/UV[X]	OV/UV comparators for each channel will be powered on/off as needed to maintain the lowest possible quiescent current: OV[x]/UV[x] Enabled: VM[x] == 1 && ((VMPD == 0 && STATOFF[x] == 0) || (VMPD == 1 && EN0 == L && SRR == 1))
OFF[X]	OFF comparators for each channel can be powered off when EN0 is low: OFF[x] Enabled: VM[x] == 1 && (VMPD == 0 || EN0 == H || SRR == 1)

Register Map

Top Level

ADDRESS	NAME	MSB							LSB
GENERAL CONFIGURATION									
0x00	ID[7:0]	REV[3:0]				DEV[3:0]			
0x01	CONFIG1[7:0]	–	–	–	–	–	RR	MBST	PECE
0x02	CONFIG2[7:0]	CLKF	PAR	RSTF	RST	EN1	EN0	BSTO*	BSTU*
VOLTAGE MONITOR SYSTEM									
0x03	VMON[7:0]	VMPD	VM7	VM6	VM5	VM4	VM3	VM2	VM1
0x04	RSTMAP[7:0]	PARM	IN7	IN6	IN5	IN4	IN3	IN2	IN1
0x05	STATOV[7:0]	–	IN7	IN6	IN5	IN4	IN3	IN2	IN1
0x06	STATUV[7:0]	–	IN7	IN6	IN5	IN4	IN3	IN2	IN1
0x07	STATOFF[7:0]	–	IN7	IN6	IN5	IN4	IN3	IN2	IN1
0x08	VIN1[7:0]	D[7:0]							
0x09	VIN2[7:0]	D[7:0]							
0x0A	VIN3[7:0]	D[7:0]							
0x0B	VIN4[7:0]	D[7:0]							
0x0C	VIN5[7:0]	D[7:0]							
0x0D	VINO6[7:0]	D[7:0]							
0x0E	VINU6[7:0]	D[7:0]							
0x0F	VINO7[7:0]	D[7:0]							
0x10	VINU7[7:0]	D[7:0]							
0x11	OVUV1[7:0]	OV[3:0]				UV[3:0]			
0x12	OVUV2[7:0]	OV[3:0]				UV[3:0]			
0x13	OVUV3[7:0]	OV[3:0]				UV[3:0]			
0x14	OVUV4[7:0]	OV[3:0]				UV[3:0]			
0x15	OVUV5[7:0]	OV[3:0]				UV[3:0]			
FLEXIBLE POWER SEQUENCE RECORDER									
0x16	FPSSTAT1[7:0]	–	–	–	NOTRD	UEN	DEN	FPSE	SRR
0x17	FPSCFG1[7:0]	UVAL	DVAL	UVALM	DVALM	FPSEN1	FDIV[2:0]		
0x18	UTIME1[7:0]	D[7:0]							
0x19	UTIME2[7:0]	D[7:0]							
0x1A	UTIME3[7:0]	D[7:0]							
0x1B	UTIME4[7:0]	D[7:0]							
0x1C	UTIME5[7:0]	D[7:0]							
0x1D	UTIME6[7:0]	D[7:0]							
0x1E	UTIME7[7:0]	D[7:0]							
0x1F	DTIME1[7:0]	D[7:0]							
0x20	DTIME2[7:0]	D[7:0]							
0x21	DTIME3[7:0]	D[7:0]							
0x22	DTIME4[7:0]	D[7:0]							
0x23	DTIME5[7:0]	D[7:0]							

ADDRESS	NAME	MSB							LSB
0x24	DTIME6[7:0]	D[7:0]							
0x25	DTIME7[7:0]	D[7:0]							
WATCHDOG AND RESET CONTROL									
0x26	WDSTAT[7:0]	–	–	–	–	OPEN	LFSR	WDUV	WDEXP
0x27	WDCDIV[7:0]	–	SWW	WDIV[5:0]					
0x28	WDCFG1[7:0]	CLO[3:0]				OPN[3:0]			
0x29	WDCFG2[7:0]	–	–	–	–	WDEN	1UD[2:0]		
0x2A	WDKEY[7:0]	KEY[7:0]							
0x2B	WDLOCK[7:0]	–	–	–	–	–	–	–	LOCK
0x2C	RSTCTRL[7:0]	–	–	–	–	–	MR1	RHLD[1:0]	
0x2D	CID[7:0]	CID[7:0]							

Register Details

ID (0x00)

Silicon Identification

BIT	7	6	5	4	3	2	1	0
Field	REV[3:0]				DEV[3:0]			
Reset	0x3				0x0			
Access Type	Read Only				Read Only			

BITFIELD	BITS	DESCRIPTION
REV	7:4	Revision
DEV	3:0	Device ID

CONFIG1 (0x01)

Configuration Register 1

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	RR	MBST	PECE
Reset	–	–	–	–	–	OTP	OTP	OTP
Access Type	–	–	–	–	–	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
RR	2	Reload Default OTP Configuration.	0b0: Reload when EN0 goes low and sequence recording finishes. 0b1: Also reload when RESET goes low due to watchdog violation.
MBST	1	Built-In Self-Test Mapping. When set, any comparator that fails BIST will cause the RESET pin to be asserted.	0b0: BIST for OV/UV/OFF comparators not mapped to RESET pin. 0b1: BIST for OV/UV/OFF comparators mapped to RESET pin.
PECE	0	Packet Error Checking Enable.	0b0: PEC disabled 0b1: PEC enabled

CONFIG2 (0x02)

Configuration Register 2

*The BIST is initiated once V_{DD} crosses the ULVO rising threshold, and takes approximately 60μs (typ), 72.2μs (max) to complete by setting bits [1:0] in the CONFIG2 register.

BIT	7	6	5	4	3	2	1	0
Field	CLKF	PAR	RSTF	RST	EN1	EN0	BSTO*	BSTU*
Reset								
Access Type	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
CLKF	7	Internal Oscillator Fault. Internal diagnostics will flag clock-stuck and "frequency-too-low" conditions.	0b0: Internal oscillator running properly. 0b1: Internal oscillator halted or below approximately 100kHz.
PAR	6	Parity Check Fault.	0b0: No register faults detected. 0b1: At least one R/W register has failed a parity check.
RSTF	5	$\overline{\text{RESET}}$ Fault Assertion. This internal flag asserts whenever any fault condition is detected by the IC that would cause the pin $\overline{\text{RESET}}$ to assert. Under normal conditions, this bit will always be the inverse of the voltage signal on the $\overline{\text{RESET}}$ pin.	0b0: No fault condition detected. $\overline{\text{RESET}}$ pin should be high. 0b1: Fault condition detected. $\overline{\text{RESET}}$ pin should be low.
RST	4	$\overline{\text{RESET}}$ Output Status. The actual read-back state of the $\overline{\text{RESET}}$ pin is indicated here. This allows detection of open or shorted pin faults by a supervisor.	0b0: $\overline{\text{RESET}}$ is low. 0b1: $\overline{\text{RESET}}$ is high.
EN1	3	EN1 Input Status. The actual read-back state of the EN1 pin is indicated here. This allows detection of open or shorted pin faults by a supervisor.	0b0: EN1 is low. 0b1: EN1 is high.
EN0	2	EN0 Input Status. The actual read-back state of the EN0 pin is indicated here. This allows detection of open or shorted pin faults by a supervisor.	0b0: EN0 is low. 0b1: EN0 is high.
BSTO*	1	Built-In Self-Test Status. The BIST for the OV comparators verify that they are operational.	0b0: BISTs for OV comparators passed successfully. 0b1: One or more of the OV comparators failed its BIST.
BSTU*	0	Built-In Self-Test Status. The BIST for the UV comparators verify that they are operational.	0b0: BISTs for UV and OFF comparators passed successfully. 0b1: One or more of the UV or OFF comparators failed its BIST.

VMON (0x03)

Voltage Monitor Enable

BIT	7	6	5	4	3	2	1	0
Field	VMPD	VM7	VM6	VM5	VM4	VM3	VM2	VM1
Reset	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
VMPD	7	Voltage Monitor Power-Down Enable. When set and EN0 is low and the power-down sequence recorder is complete, all comparators turn off to greatly reduce IC power consumption. All comparators turn on at the rising edge of EN0. See Table 2 for specific conditions.	0b0: All OFF comparators are enabled at all times. OV/UV comparators are enabled as needed. 0b1: All comparators power down with EN0 low and power-down sequence recording finished..
VM7	6	Voltage Monitor Enable. When set, the channel's OV/UV monitors are enabled.	0b0: OV/UV monitors disabled. 0b1: OV/UV monitors enabled.
VM6	5	Voltage Monitor Enable. When set, the channel's OV/UV monitors are enabled.	0b0: OV/UV monitors disabled. 0b1: OV/UV monitors enabled.
VM5	4	Voltage Monitor Enable. When set, the channel's OV/UV monitors are enabled.	0b0: OV/UV monitors disabled. 0b1: OV/UV monitors enabled.
VM4	3	Voltage Monitor Enable. When set, the channel's OV/UV monitors are enabled.	0b0: OV/UV monitors disabled. 0b1: OV/UV monitors enabled.
VM3	2	Voltage Monitor Enable. When set, the channel's OV/UV monitors are enabled.	0b0: OV/UV monitors disabled. 0b1: OV/UV monitors enabled.
VM2	1	Voltage Monitor Enable. When set, the channel's OV/UV monitors are enabled.	0b0: OV/UV monitors disabled. 0b1: OV/UV monitors enabled.
VM1	0	Voltage Monitor Enable. When set, the channel's OV/UV monitors are enabled.	0b0: OV/UV monitors disabled. 0b1: OV/UV monitors enabled.

RSTMAP (0x4)

Interrupt Mapping

BIT	7	6	5	4	3	2	1	0
Field	PARM	IN7	IN6	IN5	IN4	IN3	IN2	IN1
Reset	OTP	OTP	OTP	OTP	OTP	OTP	OTP	OTP
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
PARM	7	Parity $\overline{RESET}$ Mapping. Defines whether a parity check failure asserts the $\overline{RESET}$ pin.	0b0: Parity faults are not mapped to the $\overline{RESET}$ pin. 0b1: Any parity fault causes the $\overline{RESET}$ pin to be asserted.
IN7	6	$\overline{RESET}$ Mapping. Defines whether OV/UV assertions cause the $\overline{RESET}$ pin to trigger.	0b0: OV/UV faults are not mapped to the $\overline{RESET}$ pin. 0b1: OV/UV faults are mapped to the $\overline{RESET}$ pin.
IN6	5	$\overline{RESET}$ Mapping. Defines whether OV/UV assertions cause the $\overline{RESET}$ pin to trigger.	0b0: OV/UV faults are not mapped to the $\overline{RESET}$ pin. 0b1: OV/UV faults are mapped to the $\overline{RESET}$ pin.
IN5	4	$\overline{RESET}$ Mapping. Defines whether OV/UV assertions cause the $\overline{RESET}$ pin to trigger.	0b0: OV/UV faults are not mapped to the $\overline{RESET}$ pin. 0b1: OV/UV faults are mapped to the $\overline{RESET}$ pin.

BITFIELD	BITS	DESCRIPTION	DECODE
IN4	3	RESET Mapping. Defines whether OV/UV assertions cause the RESET pin to trigger.	0b0: OV/UV faults are not mapped to the RESET pin. 0b1: OV/UV faults are mapped to the RESET pin.
IN3	2	RESET Mapping. Defines whether OV/UV assertions cause the RESET pin to trigger.	0b0: OV/UV faults are not mapped to the RESET pin. 0b1: OV/UV faults are mapped to the RESET pin.
IN2	1	RESET Mapping. Defines whether OV/UV assertions cause the RESET pin to trigger.	0b0: OV/UV faults are not mapped to the RESET pin. 0b1: OV/UV faults are mapped to the RESET pin.
IN1	0	RESET Mapping. Defines whether OV/UV assertions cause the RESET pin to trigger.	0b0: OV/UV faults are not mapped to the RESET pin. 0b1: OV/UV faults are mapped to the RESET pin.

STATOV (0x5)

Voltage Monitor OV Comparator Statuses

BIT	7	6	5	4	3	2	1	0
Field	–	IN7	IN6	IN5	IN4	IN3	IN2	IN1
Reset	–							
Access Type	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
IN7	6	OV Comparator Status.	0b0: IN voltage is below OV threshold. 0b1: IN voltage is above OV threshold.
IN6	5	OV Comparator Status.	0b0: IN voltage is below OV threshold. 0b1: IN voltage is above OV threshold.
IN5	4	OV Comparator Status.	0b0: IN voltage is below OV threshold. 0b1: IN voltage is above OV threshold.
IN4	3	OV Comparator Status.	0b0: IN voltage is below OV threshold. 0b1: IN voltage is above OV threshold.
IN3	2	OV Comparator Status.	0b0: IN voltage is below OV threshold. 0b1: IN voltage is above OV threshold.
IN2	1	OV Comparator Status.	0b0: IN voltage is below OV threshold. 0b1: IN voltage is above OV threshold.
IN1	0	OV Comparator Status.	0b0: IN voltage is below OV threshold. 0b1: IN voltage is above OV threshold.

STATUV (0x6)

Voltage Monitor UV Comparator Statuses

BIT	7	6	5	4	3	2	1	0
Field	–	IN7	IN6	IN5	IN4	IN3	IN2	IN1
Reset	–							
Access Type	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
IN7	6	UV Comparator Status.	0b0: IN voltage is above UV threshold. 0b1: IN voltage is below UV threshold.

BITFIELD	BITS	DESCRIPTION	DECODE
IN6	5	UV Comparator Status.	0b0: IN voltage is above UV threshold. 0b1: IN voltage is below UV threshold.
IN5	4	UV Comparator Status.	0b0: IN voltage is above UV threshold. 0b1: IN voltage is below UV threshold.
IN4	3	UV Comparator Status.	0b0: IN voltage is above UV threshold. 0b1: IN voltage is below UV threshold.
IN3	2	UV Comparator Status.	0b0: IN voltage is above UV threshold. 0b1: IN voltage is below UV threshold.
IN2	1	UV Comparator Status.	0b0: IN voltage is above UV threshold. 0b1: IN voltage is below UV threshold.
IN1	0	UV Comparator Status.	0b0: IN voltage is above UV threshold. 0b1: IN voltage is below UV threshold.

STATOFF (0x7)

Voltage Monitor OFF Comparator Statuses - Not Latched

BIT	7	6	5	4	3	2	1	0
Field	–	IN7	IN6	IN5	IN4	IN3	IN2	IN1
Reset	–							
Access Type	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
IN7	6	OFF Comparator Status.	0b0: IN voltage is above OFF threshold. 0b1: IN voltage is below OFF threshold.
IN6	5	OFF Comparator Status.	0b0: IN voltage is above OFF threshold. 0b1: IN voltage is below OFF threshold.
IN5	4	OFF Comparator Status.	0b0: IN voltage is above OFF threshold. 0b1: IN voltage is below OFF threshold.
IN4	3	OFF Comparator Status.	0b0: IN voltage is above OFF threshold. 0b1: IN voltage is below OFF threshold.
IN3	2	OFF Comparator Status.	0b0: IN voltage is above OFF threshold. 0b1: IN voltage is below OFF threshold.
IN2	1	OFF Comparator Status.	0b0: IN voltage is above OFF threshold. 0b1: IN voltage is below OFF threshold.
IN1	0	OFF Comparator Status.	0b0: IN voltage is above OFF threshold. 0b1: IN voltage is below OFF threshold.

VIN1 (0x8)

IN1 Nominal Voltage Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	Nominal Rail Voltage	V_{NOM} = 500mV + 12.5mV x D[7:0] (0.5V to 3.6875V)

VIN2 (0x9)

IN2 Nominal Voltage Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	Nominal Rail Voltage	V_{NOM} = 500mV + 12.5mV x D[7:0] (0.5V to 3.6875V)

VIN3 (0xA)

IN3 Nominal Voltage Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	Nominal Rail Voltage	V_{NOM} = 500mV + 12.5mV x D[7:0] (0.5V to 3.6875V)

VIN4 (0xB)

IN4 Nominal Voltage Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	Nominal Rail Voltage	V_{NOM} = 500mV + 12.5mV x D[7:0] (0.5V to 3.6875V)

VIN5 (0xC)

IN5 Nominal Voltage Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	Nominal Rail Voltage	V_{NOM} = 500mV + 20mV x D[7:0] (0.5V to 5.6V)

VINO6 (0xD)

IN6 Overvoltage Threshold Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	OV Threshold	V_{OV6} = 500mV + 5mV x D[7:0] (0.5V to 1.775V)

VINU6 (0xE)

IN6 Undervoltage Threshold Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	UV Threshold	V_{UV6} = 500mV + 5mV x D[7:0] (0.5V to 1.775V)

VINO7 (0xF)

IN7 Overvoltage Threshold Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	OV Threshold	V_{OV7} = 500mV + 5mV x D[7:0] (0.5V to 1.775V)

VINU7 (0x10)

IN7 Undervoltage Threshold Set Point

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset	OTP							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	UV Threshold	V_{UV7} = 500mV + 5mV x D[7:0] (0.5V to 1.775V)

OVUV1 (0x11)

IN1 Overvoltage and Undervoltage Thresholds

BIT	7	6	5	4	3	2	1	0
Field	OV[3:0]				UV[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
OV	7:4	IN1 Overvoltage Threshold	OV (%) = 102.5% + 0.5% x OV[3:0]
UV	3:0	IN1 Undervoltage Threshold	UV (%) = 97.5% - 0.5% x UV[3:0]

OVUV2 (0x12)

IN2 Overvoltage and Undervoltage Thresholds

BIT	7	6	5	4	3	2	1	0
Field	OV[3:0]				UV[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
OV	7:4	IN2 Overvoltage Threshold	OV (%) = 102.5% + 0.5% x OV[3:0]
UV	3:0	IN2 Undervoltage Threshold	UV (%) = 97.5% - 0.5% x UV[3:0]

OVUV3 (0x13)

IN3 Overvoltage and Undervoltage Thresholds

BIT	7	6	5	4	3	2	1	0
Field	OV[3:0]				UV[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
OV	7:4	IN3 Overvoltage Threshold	OV (%) = 102.5% + 0.5% x OV[3:0]
UV	3:0	IN3 Undervoltage Threshold	UV (%) = 97.5% - 0.5% x UV[3:0]

OVUV4 (0x14)

IN4 Overvoltage and Undervoltage Thresholds

BIT	7	6	5	4	3	2	1	0
Field	OV[3:0]				UV[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
OV	7:4	IN4 Overvoltage Threshold	OV (%) = 102.5% + 0.5% x OV[3:0]
UV	3:0	IN4 Undervoltage Threshold	UV (%) = 97.5% - 0.5% x UV[3:0]

OVUV5 (0x15)

IN5 Overvoltage and Undervoltage Thresholds

BIT	7	6	5	4	3	2	1	0
Field	OV[3:0]				UV[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
OV	7:4	IN5 Overvoltage Threshold	OV (%) = 102.5% + 0.5% x OV[3:0]
UV	3:0	IN5 Undervoltage Threshold	UV (%) = 97.5% - 0.5% x UV[3:0]

FPSSTAT1 (0x16)

Flexible Power Sequence Recorder Status

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	NOTRD	UEN	DEN	FPSE	SRR
Reset	–	–	–					0x0
Access Type	–	–	–	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
NOTRD	4	FPSR Data Not Read. Indicates that the UVAL and/or DVAL bits were not cleared before last power-up/power-down event.	0b0: Sequencer running normally. 0b1: The sequencer encountered two power-up/power-down triggers before the UVAL and/or DVAL bits were cleared.
UEN	3	Power-Up Source. This is the source of the UTIME_ timestamps recorded.	0b0: EN0 low-to-high transition triggered the FPSR to record timestamps in UTIME_ registers. 0b1: EN1 low-to-high transition triggered the FPSR to record timestamps in UTIME_ registers.
DEN	2	Power-Down Source. This is the source of the DTIME_ timestamps recorded.	0b0: EN0 high-to-low transition triggered the FPSR to record timestamps in DTIME_ register. 0b1: EN1 high-to-low transition triggered the FPSR to record timestamps in DTIME_ registers.
FPSE	1	Flexible Power Sequence Recorder Enable	0b0: FPSR is disabled. 0b1: FPSR is enabled.
SRR	0	Sequence Recorder Running	0b0: Sequence recorder not running. 0b1: Sequence recorder is actively recording a power-up or power-down sequence.

FPSCFG1 (0x17)

Flexible Power Sequence Recorder Configuration

BIT	7	6	5	4	3	2	1	0
Field	UVAL	DVAL	UVALM	DVALM	FPSEN1	FDIV[2:0]		
Reset	OTP		OTP	OTP	OTP	OTP		
Access Type	Write 0 to Clear, Read	Write 0 to Clear, Read	Write, Read	Write, Read	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
UVAL	7	Power-Up Sequence Validation. This bit is set when the FPSR records a power-up sequence, and must be cleared before a new power-up sequence can be recorded. This is typically done after the UTIME register contents are read.	0b0: Power-up sequence capture is not completed. 0b1: Power-up sequence captured. FPSR inhibited from recording a new power-up sequence.
DVAL	6	Power-Down Sequence Validation. This bit is set when the FPSR records a power-down sequence, and must be cleared before a new power-down sequence can be recorded. This is typically done after the DTIME register contents are read.	0b0: Power-down sequence capture is not completed. 0b1: Power-down sequence captured. FPSR inhibited from recording a new power-up sequence.
UVALM	5	Power-Up Sequence Validation Interrupt Mask.	0b0: The completion of a power-up sequence recording will generate an interrupt, pulling $\overline{\text{RESET}}$ low. 0b1: No interrupt is generated when a power-up sequence recording finishes.
DVALM	4	Power-Down Sequence Validation Interrupt Mask.	0b0: The completion of a power-down sequence recording generates an interrupt, pulling $\overline{\text{RESET}}$ low. 0b1: No interrupt is generated when a power-down sequence recording finishes.
FPSEN1	3	FPS Timer Start on EN1 Transition.	0b0: EN1 pin is masked and will not start FPSR timer (transitions on EN1 will be ignored). Only EN0 transitions will trigger FPSR. 0b1: Both EN0 and EN1 rising/falling transitions will start the FPSR timer. A rising transition will start a power-up sequence recording and a falling transition will start a power-down sequence recording.
FDIV	2:0	FPS Clock Divider. The main oscillator is divided by 32, and the resulting signal is sent to the FPS subsystem. This field controls how the signal is further divided before being used by the FPS.	0b000: 25µs/tick, 6.375ms total recording time 0b001: 50µs/tick, 12.75ms total recording time 0b010: 100µs/tick, 25.5ms total recording time 0b011: 200µs/tick, 51ms total recording time 0b100: 400µs/tick, 102ms total recording time 0b101: 800µs/tick, 204ms total recording time 0b110: 1600µs/tick, 408ms total recording time 0b111: 3200µs/tick, 816ms total recording time

UTIME1 (0x18)

Power-Up Timestamp for IN1

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	This gives the time at which the input rose above the UV threshold.	0b0: Input voltage never rose above UV threshold Else: time = (D[7:0] - 1) x 25µs x $2^{FDIV[2:0]}$

UTIME2 (0x19)

Power-Up Timestamp for IN2

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	This gives the time at which the input rose above the UV threshold.	0b0: Input voltage never rose above UV threshold Else: time = (D[7:0] - 1) x 25μs x $2^{FDIV[2:0]}$

UTIME3 (0x1A)

Power-Up Timestamp for IN3

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	This gives the time at which the input rose above the UV threshold.	0b0: Input voltage never rose above UV threshold Else: time = (D[7:0] - 1) x 25μs x $2^{FDIV[2:0]}$

UTIME4 (0x1B)

Power-Up Timestamp for IN4

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	This gives the time at which the input rose above the UV threshold.	0b0: Input voltage never rose above UV threshold Else: time = (D[7:0] - 1) x 25μs x $2^{FDIV[2:0]}$

UTIME5 (0x1C)

Power-Up Timestamp for IN5

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	This gives the time at which the input rose above the UV threshold.	0b0: Input voltage never rose above UV threshold Else: time = (D[7:0] - 1) x 25μs x $2^{FDIV[2:0]}$

UTIME6 (0x1D)

Power-Up Timestamp for IN6

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	This gives the time at which the input rose above the UV threshold.	0b0: Input voltage never rose above UV threshold Else: time = (D[7:0] - 1) x 25µs x $2^{FDIV[2:0]}$

UTIME7 (0x1E)

Power-Up Timestamp for IN7

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	This gives the time at which the input rose above the UV threshold.	0b0: Input voltage never rose above UV threshold Else: time = (D[7:0] - 1) x 25µs x $2^{FDIV[2:0]}$

DTIME1 (0x1F)

Power-Down Timestamp for IN1

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	This gives the time at which the input fell below the OFF threshold.	0b0: Input voltage never rose above UV threshold Else: time = (D[7:0] - 1) x 25µs x $2^{FDIV[2:0]}$

DTIME2 (0x20)

Power-Down Timestamp for IN2

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	This gives the time at which the input fell below the OFF threshold.	0b0: Input voltage never rose above UV threshold Else: time = (D[7:0] - 1) x 25µs x $2^{FDIV[2:0]}$

DTIME3 (0x21)

Power-Down Timestamp for IN3

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	This gives the time at which the input fell below the OFF threshold.	0b0: Input voltage never rose above UV threshold Else: time = (D[7:0] - 1) x 25µs x $2^{FDIV[2:0]}$

DTIME4 (0x22)

Power-Down Timestamp for IN4

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	This gives the time at which the input fell below the OFF threshold.	0b0: Input voltage never rose above UV threshold Else: time = (D[7:0] - 1) x 25µs x $2^{FDIV[2:0]}$

DTIME5 (0x23)

Power-Down Timestamp for IN5

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	This gives the time at which the input fell below the OFF threshold.	0b0: Input voltage never rose above UV threshold Else: time = (D[7:0] - 1) x 25µs x $2^{FDIV[2:0]}$

DTIME6 (0x24)

Power-Down Timestamp for IN6

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	This gives the time at which the input fell below the OFF threshold.	0b0: Input voltage never rose above UV threshold Else: time = (D[7:0] - 1) x 25µs x $2^{FDIV[2:0]}$

DTIME7 (0x25)

Power-Down Timestamp for IN7

BIT	7	6	5	4	3	2	1	0
Field	D[7:0]							
Reset								
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
D	7:0	This gives the time at which the input fell below the OFF threshold.	0b0: Input voltage never rose above UV threshold Else: time = (D[7:0] - 1) x 25µs x $2^{FDIV[2:0]}$

WDSTAT (0x26)

Watchdog Status

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	OPEN	LFSR	WDUV	WDEXP
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Read Only	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
OPEN	3	Watchdog Window Open.	0b0: Watchdog updates not accepted. 0b1: Updates refresh the watchdog.
LFSR	2	LFSR Write Mismatch	0b0: LFSR key matches 0b1: LFSR key mismatch
WDUV	1	Watchdog Update Violation.	0b0: No timing violation detected. 0b1: Watchdog updated too early.
WDEXP	0	Watchdog Window Expired.	0b0: No timing violation detected. 0b1: Watchdog open-window time expired before being refreshed.

WDCDIV (0x27)

Watchdog Mode and Clock Divider

BIT	7	6	5	4	3	2	1	0
Field	–	SWW	WDIV[5:0]					
Reset	–	OTP	OTP					
Access Type	–	Write, Read	Write, Read					

BITFIELD	BITS	DESCRIPTION	DECODE
SWW	6	Simple Windowed Watchdog Enable. The watchdog can operate in challenge/response mode (in which a specific key value must be written to WDKEY) or in simple mode (in which any write to WDKEY will update the watchdog).	0b0: Challenge/response watchdog mode 0b1: Simple windowed watchdog mode
WDIV	5:0	Watchdog Clock Divider. The main oscillator is divided by 32 and supplied to the watchdog subsystem. This field controls further dividing of the clock.	t_{WDCLK} = (WDIV[5:0] + 1) x 25µs x 8

WDCFG1 (0x28)

Watchdog Configuration Register 1

BIT	7	6	5	4	3	2	1	0
Field	CLO[3:0]				OPN[3:0]			
Reset	OTP				OTP			
Access Type	Write, Read				Write, Read			

BITFIELD	BITS	DESCRIPTION	DECODE
CLO	7:4	Watchdog Closed Window. Sets the length of the first portion of a watchdog period, where updates are rejected.	t_{CLO} = (CLO[3:0] + 1) x 8 x t_{WDCLK}
OPN	3:0	Watchdog Open Window. Sets the length of the second portion of a watchdog period, where updates are accepted.	t_{OPN} = (OPN[3:0] + 1) x 8 x t_{WDCLK}

WDCFG2 (0x29)

Watchdog Configuration Register 2

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	WDEN	1UD[2:0]		
Reset	–	–	–	–	OTP	OTP		
Access Type	–	–	–	–	Write, Read	Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
WDEN	3	Watchdog Enable.	0b0: Watchdog disabled 0b1: Watchdog enabled
1UD	2:0	First Update Extension. Sets the length of the first open window after $\overline{RESET}$ deassertion.	t_{1OPN} = (t_{CLO} + t_{OPN}) x (1UD[2:0] x 2 + 1)

WDKEY (0x2A)

Watchdog Key Register

BIT	7	6	5	4	3	2	1	0
Field	KEY[7:0]							
Reset	0x55							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION	DECODE
KEY	7:0	Contains the current key value, which must be used to compute the next key value in the sequence for challenge/response mode. Write key value to register to refresh.	LFSR polynomial: $x^8 + x^6 + x^5 + x^4 + 1$. Calculate new bit, shift existing bits upwards toward MSb, insert calculated bit as new LSb.

WDLOCK (0x2B)

Watchdog Lock

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	LOCK
Reset	–	–	–	–	–	–	–	OTP
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
LOCK	0	Watchdog Lock Bit.	0b0: All watchdog-related registers can be written to. 0b1: All writes to watchdog-related registers are ignored except for WDKEY and WDLOCK.

RSTCTRL (0x2C)

RESET Control

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	MR1	RHLD[1:0]	
Reset	–	–	–	–	–	OTP	OTP	
Access Type	–	–	–	–	–	Write, Read	Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
MR1	2	Watchdog Violation Count for RESET Assertion. This determines whether the RESET pin is asserted on any single watchdog violation, or after two consecutive violations.	0b0: RESET asserts after any watchdog violation. 0b1: RESET asserts only after two consecutive violations. Valid updates will reset the violation counter if one violation has been encountered.
RHLD	1:0	RESET Hold/Active Timeout Time. This is the amount of time that the RESET pin remains low after the removal of any event that would cause the RESET pin to assert low.	0b00: 0ms (6µs typ, used for interrupt-style functionality) 0b01: 8ms 0b10: 16ms 0b11: 32ms

CID (0x2D)

Chip Identification

BIT	7	6	5	4	3	2	1	0
Field	CID[7:0]							
Reset	OTP							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION	DECODE
CID	7:0	A unique chip identification code to help determine which device is being queried.	Set at factory

Applications Information

Diagnostics

The MAX20480 is ASIL D compliant when combined with a supervisor for monitoring and control over the IC. Individual fault indicators are available (see register CONFIG2) for parity-check failure, clock fault, EN and $\overline{RESET}$ pin readbacks, and BIST results. Internal OTP configuration information is protected by an automatic single-error-correcting coding scheme. Individual voltage-monitor comparators provide their statuses through the STATOV/UV/OFF registers. The FPSR relates sequencing status, triggers, and faults through the FPSSTAT1 and FPSCFG1 registers. The watchdog has individual fault flags to determine which type of error was encountered. To prevent the IC from being misconfigured by an I^2C master device, which could cause a permanent fault, the IC features an OTP reload mechanism. Every time the EN0 pin transitions from high to low, the IC reloads all the registers with the information stored in the OTP after the FPSR finishes recording the power-down sequence. The data stored in the sequencer's UTIME and DTIME registers are not affected by this reload. There is also a configuration bit that, when set, causes the registers to reload from OTP whenever a watchdog fault is asserted. The OTP reload time after a high-to-low transition on EN0 or after a watchdog violation takes approximately 1µs.

For full safety-related information, contact Analog Devices.

Table 3. Diagnostics

FAULT	DIAGNOSTIC COVERAGE
Short to GND/V_{DD} on IN_ pins	OV/UV comparators assert depending on voltage.
Open on IN_ pins	UV/OFF comparators assert.
Short to GND on V_{DD} pin	Loss of I^2C communications.
Open on V_{DD} pin	Loss of I^2C communications.
Open/short to GND EN0/EN1 pins	Sequencing will not be detected. This is detectable by reading the EN0/EN1 state through the I^2C and by the loss of sequencing information in the status register.
Open/short on SDA/ SCL	No I^2C communications. Communication attempts will result in a NACK response. Watchdog will violate due to inability to update the watchdog.
Open GND pin	$\overline{RESET}$ can still assert down to one body diode above system ground. Persistent UV conditions will occur if any voltage monitors are active.
Short to V_{DD} on RESET	Test at power-on can verify that $\overline{RESET}$ pins are low.
Open on RESET pin	Can be detected by reading the state of the $\overline{RESET}$ pin through I^2C. If the $\overline{RESET}$ pin should be high, but is low (due to 2µA pulldown current), the pin is open. Also detectable if a power-on watchdog test is performed.
Internal watchdog block failure	Can be detected through host-induced test.

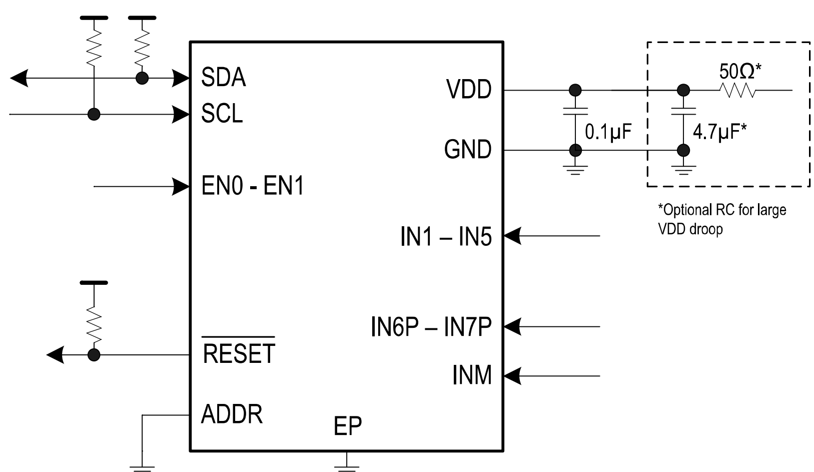
Table 4. ASIL Safety Diagnostics

DESCRIPTION	FAULT TO BE DETECTED	FAULT REACTION STATE
OV Comparator Diagnostics for Channels 1–5	OV comparator stuck high/low	$\overline{RESET}$ pin asserted, I^2C register flag set
UV Comparator Diagnostics for Channels 1–5	UV comparator stuck high/low	$\overline{RESET}$ pin asserted, I^2C register flag set
OFF Comparator Diagnostics for Channels 1–5	V_{OFF} comparator stuck high/low	$\overline{RESET}$ pin asserted, I^2C register flag set
OV Comparator Diagnostics for Channel 6/7	OV comparator stuck high/low	$\overline{RESET}$ pin asserted, I^2C register flag set

Table 4. ASIL Safety Diagnostics (continued)

UV Comparator Diagnostics for Channels 6/7	UV comparator stuck high/low	$\overline{\text{RESET}}$ pin asserted, I^{2}C register flag set
OFF Comparator Diagnostics for Channels 6/7	V_{OFF} comparator stuck high/low	$\overline{\text{RESET}}$ pin asserted, I^{2}C register flag set
$\overline{\text{RESET}}$ Output	Communicate all faults to supervisory systems	$\overline{\text{RESET}}$ pin asserted
OV Comparator for Channels 1–5	Voltage rail too high	$\overline{\text{RESET}}$ pin asserted, I^{2}C register flag set
UV Comparator for Channels 1–5	Voltage rail too low	$\overline{\text{RESET}}$ pin asserted, I^{2}C register flag set
V_{OFF} Comparator for Channels 1–5	Voltage rail shut down	$\overline{\text{RESET}}$ pin asserted, I^{2}C register flag set
OV Comparator for Channels 6/7	Voltage rail too high	$\overline{\text{RESET}}$ pin asserted, I^{2}C register flag set
UV Comparator for Channels 6/7	Voltage rail too low	$\overline{\text{RESET}}$ pin asserted, I^{2}C register flag set
V_{OFF} Comparator for Channels 6/7	Voltage rail shut down	$\overline{\text{RESET}}$ pin asserted, I^{2}C register flag set
Functionality Check of System Clock	Clock stuck high/low; frequency too low	$\overline{\text{RESET}}$ pin asserted
Parity for I^{2}C Registers	Erroneous bit flip in active register data	$\overline{\text{RESET}}$ pin asserted
Dual UVLO	IC supply voltage too low	$\overline{\text{RESET}}$ pin asserted, I^{2}C comm lost

Typical Application Circuit



Ordering Information

PART	CID	SLAVE ID	CH1 (V)	CH2 (V)	CH3 (V)	CH4 (V)	CH5 (V)	CH6 OV (V)	CH6 UV (V)	CH7 OV (V)	CH7 UV (V)
MAX20480BATEA/VY+*	0x10	0x48	3.3	1.8	1.8	1.8	5.0	-	-	-	-
MAX20480BATEB/VY+	0x39	0x48	3.3	1.25	2.5	2.5	5.0	-	-	-	-
MAX20480BATEC/VY+	0x40	0x48	1.8	3.3	1.2	0.9	1.1	-	-	-	-
MAX20480BATED/VY+*	0x52	0x28	1.5	1.05	1.8	0.9	3.3	-	-	-	-
MAX20480DATEA/VY+	0x0F	0x38	3.3	1.8	1.2	3.3	1.8	1.26	1.14	1.15	0.6
MAX20480DATEB/VY+	0x0B	0x48	1.8	1.8	1.8	1.8	3.3	1.15	0.6	1.15	0.6
MAX20480DATEC/VY+	0x0C	0x58	3.3	3.3	3.3	3.3	3.3	1.15	0.6	1.15	0.6
MAX20480DATED/VY+	0x0D	0x28	0.8	1.0	1.1	1.2	3.3	1.15	1.05	0.65	0.58
MAX20480DATEE/VY+	0x0E	0x38	1.8	1.0	1.8	1.8	3.3	1.2	0.6	1.5	1.1
MAX20480DATEF/VY+*	0x09	0x58	3.4	3.4	3.4	3.4	2.3	1.165	0.6	1.165	0.6
MAX20480DATEG/VY+*	0x0A	0x28	0.8125	1.1025	1.125	1.225	3.38	1.165	1.06	0.65	0.58
MAX20480DATEI/VY+*	0x01	0x38	1.0	1.1	1.8	2.5	3.3	0.84	0.79	0.85	0.8
MAX20480DATEJ/VY+	0x11	0x48	0.6	0.6	1.2	0.85	3.3	0.89	0.81	0.89	0.81
MAX20480DATEW/VY+	0x30	0x38	1.8	0.9375	1.35	2.5	1.8	1.0	0.5	1.5	1.1

For variants with different options, contact the factory.

/V Denotes an automotive qualified part.

Y Denotes a side-wettable package.

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

**Future product—contact factory for availability.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	9/18	Initial release	—
1	10/18	Added future product status to the following products in *Ordering Information:* ● MAX20480DATEA/VY+* ● MAX20480DATEC/VY+* ● MAX20480DATED/VY+* ● MAX20480DATEE/VY+*	42
2	10/18	Removed future product status from the following products in *Ordering Information:* ● MAX20480DATEA/VY+* ● MAX20480DATEC/VY+* ● MAX20480DATED/VY+* ● MAX20480DATEE/VY+*	42
3	11/18	Corrected base I^2C address of MAX20480DATEA/VY+ to 0x38 in *Ordering Information*	42
4	2/19	Added MAX20480BATEA/VY+* to *Ordering Information*	42
5	5/19	Updated *Package Information*	3
6	7/19	Updated Register Map, *Applications Information*, and *Ordering Information*	20, 21, 40, 42
7	9/19	Updated Typical Operating Characteristics, ID (0x00), and *Ordering Information*	8, 21, 43
8	12/19	Updated Typical Operating Characteristics, Functional Diagram, Watchdog Window Settings, CONFIG2 (0x02), and added Figure 6 and Table 4	8, 12, 18, 22, 41
9	9/20	Updated *Ordering Information* to remove future-product notation from MAX20480DATEJ/ VY+	40
10	1/21	Updated *Pin Descriptions*, *Functional Diagrams*, Register Map, and *Ordering Information*	10, 12, 26, 40
11	5/21	Updated *Typical Operating Characteristics*, *Functional Diagrams*, and *Ordering Information*	12, 16, 25
12	8/21	Updated *Ordering Information*	25
13	10/21	Updated *Ordering Information*	22
14	11/21	Added Register Map and *Applications Information* Section	22-38, 39-40

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