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4.5V to 60V, 3A Current-Limiter with OV, UV and Reverse Protection

MAX17613A/MAX17613B/ MAX17613C

General Description

The Olympus series of ICs is the industry's smallest and most robust integrated system protection solution. The MAX17613A/MAX17613B/MAX17613C adjustable overvoltage and overcurrent protection devices are ideal to protect systems against positive and negative input voltage faults up to +60V and -65V, and feature low 130mΩ (typ) R_{ON} FETs.

The adjustable input overvoltage protection range is 5.5V to 60V and the adjustable input undervoltage protection range is 4.5V to 59V. The input overvoltage-lockout (OVLO) and undervoltage-lockout (UVLO) thresholds are set using external resistors. Additionally, the devices offer an internal input undervoltage threshold at 4.2V (typ).

The devices feature programmable current-limit protection up to 3A; hence, controlling the inrush current at startup while charging large capacitors at the output. The current-limit threshold is programmed by connecting a resistor from the SETI pin to GND. When the device current reaches the programmed threshold, the device prevents further increases in current by modulating the FET resistance. The devices can be programmed to behave in three different ways under current-limit condition: autoretry, continuous, or latchoff modes. The voltage appearing on the SETI pin is proportional to the instantaneous current flowing through the device and can be read by an ADC. The devices offer a programmable startup blanking time that enables charging the large capacitors connected at the output.

MAX17613A and MAX17613C block current flowing in the reverse direction (i.e., from OUT to IN) whereas MAX17613B allows current flow in the reverse direction. The devices feature thermal shutdown protection against excessive power dissipation.

The devices are available in a small, 20-pin (4mm x 4mm) TQFN-EP package and operate over the -40°C to +125°C extended temperature range.

Ordering Information appears at end of data sheet.

Benefits and Features

- **Robust Protection Reduces System Downtime**
  - Wide Input-Supply Range of +4.5V to +60V
  - Hot Plug-in Tolerant without TVS up to 35V Input Supply
  - Negative Input Tolerance up to -65V
  - Low R_{ON} 130mΩ (typ)
  - Reverse Current-Blocking Protection
  - Thermal Overload Protection
  - Programmable Startup Blanking Time
  - Extended -40°C to +125°C Temperature Range
  - MAX17613A Enables OV, UV, and Reverse Voltage Protection
  - MAX17613B Enables OV and UV Protection
  - MAX17613C Enables Reverse Voltage Protection
- **Flexible Design Options Enable Reuse and Less Requalification**
  - Adjustable OVLO and UVLO Thresholds
  - Programmable Forward Current Limit: 0.15A to 3A with ±3.5% Accuracy
  - Accuracy Over Full Temperature Range
  - Programmable Overcurrent Fault Response: Autoretry, Continuous, and Latchoff Modes
  - Smooth Current Transitions
- **Saves Board Space and Reduces External BOM Count**
  - 20-Pin, 4mm x 4mm, TQFN-EP Package
  - Integrated FETs
- **UL 2367 Recognized, File No. E211395**
- **IEC 62368-1 Certified**

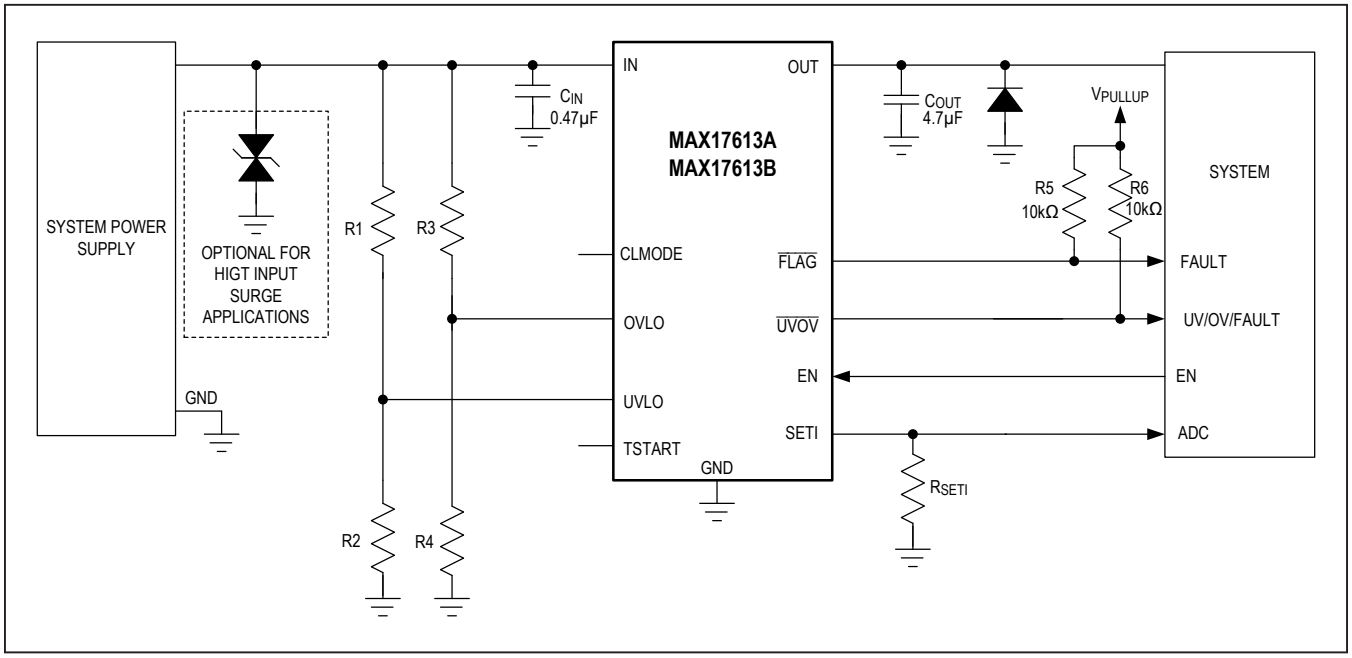
Applications

- Sensor Systems
- Condition Monitoring
- Factory Sensors
- Process Instrumentation
- Weighing and Batching Systems
- Industrial Applications such as PLC, Control Network Modules, Battery-Operated Modules

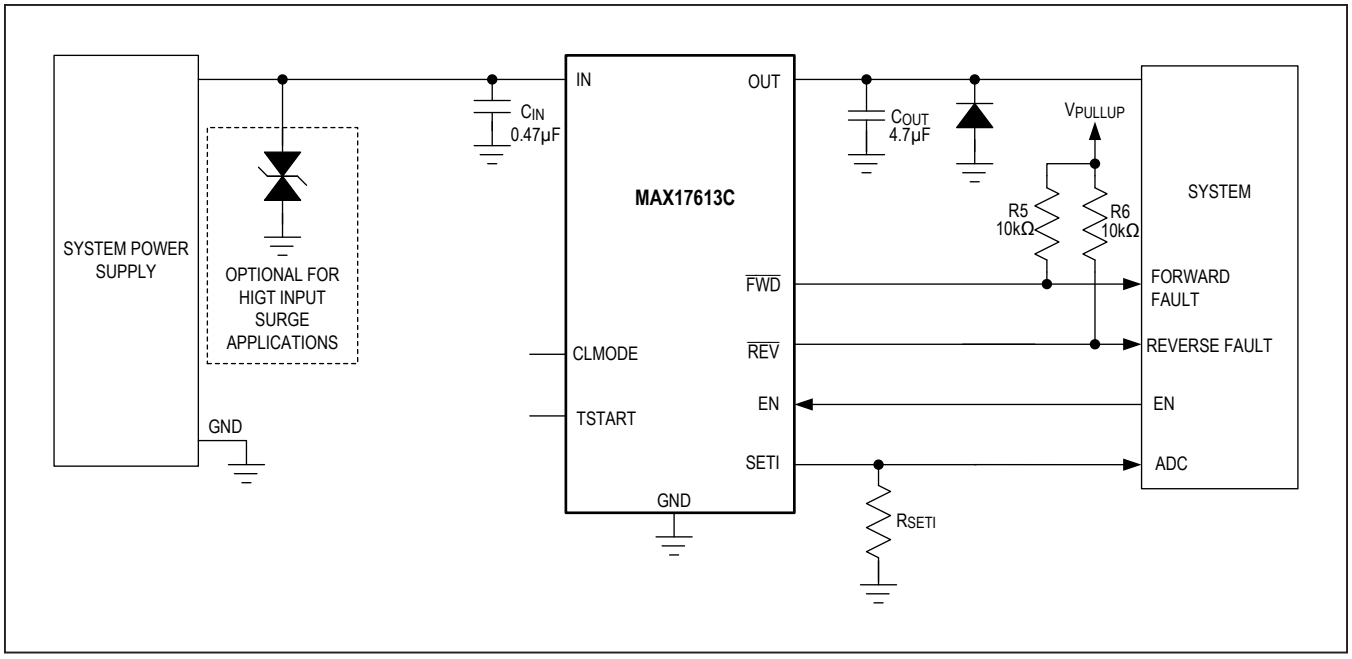
19-100414; Rev 1; 11/21

Typical Operating Circuit

MAX17613A and MAX17613B



MAX17613C



Absolute Maximum Ratings

IN to GND (MAX17613A and MAX17613C).....-65V to +65V
IN to GND (MAX17613B).....-0.3V to +65V
IN to OUT (MAX17613A and MAX17613C).....-65V to +65V
IN to OUT (MAX17613B).....-0.3V to +65V
OUT to GND .....-0.3V to +65V
UVLO, OVLO to GND
(MAX17613A and MAX17613B).....-0.3V to (max (V_{IN},V_{OUT})+0.3V)
EN, CLMODE, TSTART to GND .....-0.3V to +6V
$\overline{UVOV}$, $\overline{FLAG}$ to GND
(MAX17613A and MAX17613B).....-0.3V to +6.0V
$\overline{FWD}$, $\overline{REV}$ to GND (MAX17613C).....-0.3V to +6V
IN Current (DC).....3.3A
SETI to GND (Note1).....-0.3V to +1.6V
Continuous Power Dissipation
(T_A = +70°C, derate 30.3mW/°C above +70°C).....2424.2mW
Extended Operating Temperature Range
(Note 2).....-40°C to +125°C
Junction Temperature Range.....-40°C to +150°C
Storage Temperature Range.....-65°C to +150°C
Lead Temperature (Soldering, 10s).....+300°C

Note 1: The SETI pin is internally clamped. Forcing more than 5mA current into the pin can damage the device.
Note 2: Junction temperature greater than +125ºC degrades operating life times.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 20 TQFN	
Package Code	T2044+4C
Outline Number	**21-100172**
Land Pattern Number	**90-0409**
THERMAL RESISTANCE, FOUR-LAYER BOARD:	
Junction to Ambient (θ_{JA})	33ºC/W
Junction to Case (θ_{JC})	2ºC/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{IN} = +4.5 to +60V, T_A = -40°C to +125°C unless otherwise noted. Typical values are at V_{IN} = +24V, T_A = +25°C, R_{SETI} = 1.5kΩ.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Voltage Range	V_{IN}		4.5		60	V
Shutdown Input Current	I_{SHDN}	V_{EN} = 0V		28	66	µA
Shutdown Output Current	I_{OFF}	V_{EN} = 0V, V_{OUT} = 0V (V_{IN} = 60V)	-2			µA
Reverse Input Current	I_{IN_RVS}	V_{IN} = -60V, V_{OUT} = 0V	-85	-50		µA
Supply Current	I_{IN}	V_{IN} = 24V		0.88	1.2	mA
Internal Undervoltage Trip Level	$V_{UVLOINT}$	V_{IN} rising	3.84	4.20	4.50	V
		V_{IN} falling	3.37	3.48	3.83	
UVLO Rising Threshold	V_{UVLOR}	MAX17613A and MAX17613B	1.47	1.50	1.53	V
UVLO Falling Threshold	V_{UVLOF}	MAX17613A and MAX17613B	1.42	1.45	1.48	V
OVLO Rising Threshold	V_{OVLOR}	MAX17613A and MAX17613B	1.47	1.50	1.53	V
OVLO Falling Threshold	V_{OVLOF}	MAX17613A and MAX17613B	1.42	1.45	1.48	V

Electrical Characteristics (continued)

(V_{IN} = +4.5 to +60V, T_A = -40°C to +125°C unless otherwise noted. Typical values are at V_{IN} = +24V, T_A = +25°C, R_{SETI} = 1.5kΩ.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
UVLO, OVLO Leakage Current	I_{LEAK}	V_{UVLO} = V_{OVLO} = 0V to 2V.	MAX17613A and MAX17613B	-100		+100	nA
OVLO Adjustment Range		MAX17613A and MAX17613B (Note 4)		5.5		60	V
UVLO Adjustment Range		MAX17613A and MAX17613B (Note 4)		4.5		59	V
Internal POR Rising	V_{PORR}			3.40	3.88	4.50	V
Internal POR Falling	V_{PORF}			3.00	3.80	4.30	V
INTERNAL FETs							
Internal FETs On-Resistance	R_{ON}	I_{LOAD} = 100mA,V_{IN} > 8V, T_J = 25°C			130	155	mΩ
		I_{LOAD} = 100mA,V_{IN} > 8V, T_J = 85°C				200	
		I_{LOAD} = 100mA,V_{IN} > 8V, -40°C ≤ T_J ≤ 125°C				230	
Current-Limit Adjustment Range	I_{LIM}	(Note 5)		0.15		3	A
Current-Limit Accuracy		0.15A ≤ I_{LIM} ≤ 3A		-3.5		+3.5	%
$\overline{FLAG}$ Assertion Drop Voltage Threshold	V_{FA}	Increase (V_{IN} - V_{OUT}) drop until $\overline{FLAG}$ asserts, V_{IN} = 24V (MAX17613A and MAX17613B)		400	500	600	mV
$\overline{FWD}$ Assertion Drop Voltage Threshold	V_{FA}	Increase (V_{IN} - V_{OUT}) drop until $\overline{FWD}$ asserts, V_{IN} = 24V (MAX17613C)		400	500	600	mV
Reverse Current Blocking Slow-Threshold	V_{RIBS}	V_{OUT} - V_{IN} (MAX17613A and MAX17613C)		2	11	20	mV
Reverse Current Blocking Debounce Blanking Time	t_{DEBRIB}	MAX17613A and MAX17613C		100	140	180	µs
Reverse Current Blocking Powerup Blanking Time	t_{BLKRIB}	MAX17613A and MAX17613C		14.4	16	17.6	ms
Reverse Current Blocking Fast-Threshold	V_{RIBF}	V_{OUT} -V_{IN} (MAX17613A and MAX17613C).		70	105	140	mV
Reverse Current Blocking Fast Response Time	t_{RIB}	Time from when $I_{REVERSE}$ crosses 55A and $I_{REVERSE}$ reaches its peak. (MAX17613A and MAX17613C) (Note 6)			150	250	ns
Reverse Blocking Supply Current	I_{RBL}	Current into OUT when (V_{OUT} - V_{IN}) > 130mV (MAX17613A and MAX17613C)			0.92	1.25	mA
SETI							
R_{SETI} x I_{LIM}	V_{RI}				1.5		V
Current Mirror Output Ratio	C_{IRATIO}	0.15A ≤ I_{IN} ≤ 0.3A		2910	3000	3090	A/A
		0.3A ≤ I_{IN} ≤ 3A		2940	3000	3060	
Internal SETI Clamp		5mA into SETI		1.6		2.2	V
SETI Leakage Current		V_{SETI} = 1.6V		-0.1		+0.1	µA
LOGIC INPUT							
EN Input Logic High	V_{IH}			1.4			V
EN Input Logic Low	V_{IL}					0.4	V

Electrical Characteristics (continued)

(V_{IN} = +4.5 to +60V, T_A = -40°C to +125°C unless otherwise noted. Typical values are at V_{IN} = +24V, T_A = +25°C, R_{SETI} = 1.5kΩ.) (Note 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EN Pullup Voltage		EN pin unconnected. V_{IN} = 60V		1.4	2	V
EN Input Current		V_{EN} = 5.5V		60	95	µA
EN Pullup Current		V_{EN} = 0.4V	2.2	5.8	12	µA
CLMODE Input Logic High			2	3.8	4.9	V
CLMODE Input Logic Low			0.25	0.60	0.95	V
CLMODE Pullup Input Current			8	10	12	µA
$\overline{FLAG}$, $\overline{UVOV}$ OUTPUTs						
$\overline{FLAG}$, $\overline{UVOV}$ Output Logic Low Voltage		I_{SINK} = 1mA (MAX17613A and MAX17613B)			0.4	V
$\overline{FLAG}$, $\overline{UVOV}$ Output Leakage Current		V_{IN} = $V_{\overline{FLAG}}$ = $V_{\overline{UVOV}}$ = 5V, $\overline{FLAG}$, and $\overline{UVOV}$ deasserted (MAX17613A and MAX17613B)			1	µA
$\overline{FWD}$, $\overline{REV}$ OUTPUTs						
$\overline{FWD}$, $\overline{REV}$ Output Logic Low Voltage		I_{SINK} = 1mA (MAX17613C)			0.4	V
$\overline{FWD}$, $\overline{REV}$ Output Leakage Current		V_{IN} = $V_{\overline{FWD}}$ = $V_{\overline{REV}}$ = 5V, $\overline{FWD}$, and $\overline{REV}$ deasserted (MAX17613C)			1	µA
TSTART STARTUP						
TSTART Reference Voltage	$V_{TSTART-REF}$		1.425	1.5	1.575	V
TSTART Output Current	I_{TSTART}		4.5	5	5.5	µA
TSTART Internal Shunt Discharge Resistance	R_{TSTART}	Discharging Resistance			260	Ω
TSTART Unconnecting Check Time Interval	$t_{TSTART-UNCONNECTED}$			100		µs
TSTART default interval	$t_{TSTART-DEFAULT}$		90	100	110	ms
TIMING CHARACTERISTICS						
Switch Turn-On Time	t_{ON_SWITCH}	V_{IN} = 24V, R_{LOAD} = 1kΩ, C_{LOAD} = 0µF, R_{SETI} = 1.5kΩ		2	3.3	ms
Overvoltage Switch Turn-Off Time	t_{OFF_OVP}	From (V_{IN} going from V_{IN_OVLO} - 1V to V_{IN_OVLO} + 1V in 10ns) to (V_{OUT} = 80% of V_{IN_OVLO}); R_{LOAD} = 1kΩ (MAX17613A and MAX17613B)		0.8	1.3	µs
Overvoltage Falling Edge Debounce Time	t_{DEB_OVP}	(MAX17613A and MAX17613B)		10		µs
Overcurrent Protection Response Time	t_{OCP_RES}	I_{LIM} = 3A, C_{LOAD} = 0µF, I_{OUT} step from 1.5A to 3A. Time to regulate I_{OUT} to current limit.		100		µs

Electrical Characteristics (continued)

(V_{IN} = +4.5 to +60V, T_A = -40°C to +125°C unless otherwise noted. Typical values are at V_{IN} = +24V, T_A = +25°C, R_{SETI} = 1.5kΩ.) (Note 3)

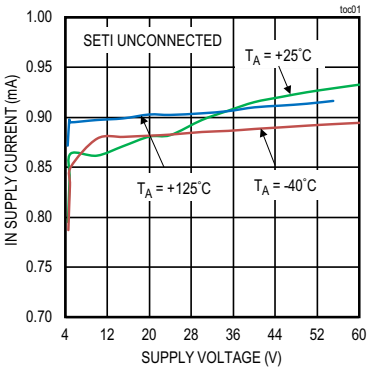
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IN Debounce Time	t_{DEB}	From (V_{IN_UVLO} < V_{IN} < V_{IN_OVLO}) and (EN = High) to V_{OUT} = 10% of V_{IN}. Elapses only at power-up.	14.4	16	17.6	ms
Current-Limit Smooth-Transition Time	t_{REF_RAMP}			60		µs
Current-Limit Blanking Time	t_{BLANK}		18	20	22	ms
Current-Limit Autoretry Time	t_{RETRY}	After blanking time from I_{OUT} > I_{LIM} to $\overline{FLAG}$ deasserted (MAX17613A and MAX17613B) (Note 7)	900	1000	1100	ms
		After blanking time from I_{OUT} > I_{LIM} to $\overline{FWD}$ deasserted (MAX17613C) (Note 7)	900	1000	1100	
THERMAL PROTECTION						
Thermal Shutdown	T_{JC_MAX}			155		°C
Thermal Shutdown Hysteresis	T_{JC_HYS}			15		°C

Note 3: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design; not production tested.
Note 4: User settable. See overvoltage/undervoltage lockout instructions.
Note 5: The current limit can be set below 150mA with a decreased accuracy.
Note 6: Guaranteed by design, not production tested.
Note 7: The ratio between autoretry time and blanking time is fixed and equal to 50.

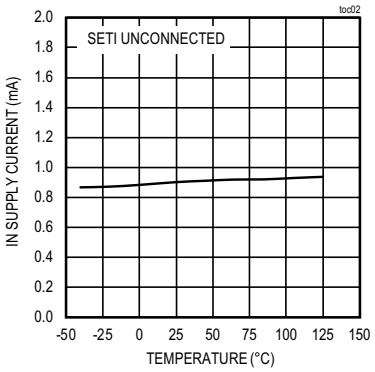
Typical Operating Characteristics

(C_{IN} = 0.47µF, C_{OUT} = 4.7µF, V_{IN} = 24V, T_A = +25°C, unless otherwise noted.)

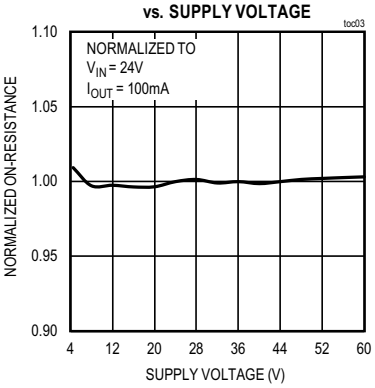
IN SUPPLY CURRENT vs. SUPPLY VOLTAGE



IN SUPPLY CURRENT vs. TEMPERATURE



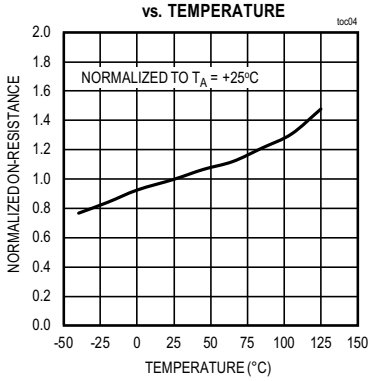
NORMALIZED ON-RESISTANCE vs. SUPPLY VOLTAGE



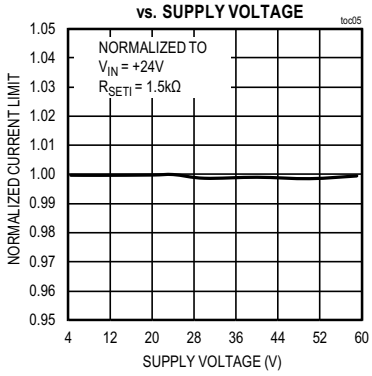
Typical Operating Characteristics (continued)

(C_{IN} = 0.47µF, C_{OUT} = 4.7µF, V_{IN} = 24V, T_A = +25°C, unless otherwise noted.)

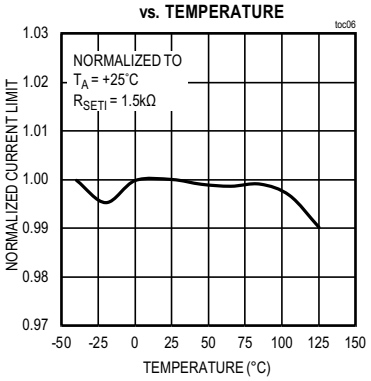
NORMALIZED ON-RESISTANCE vs. TEMPERATURE



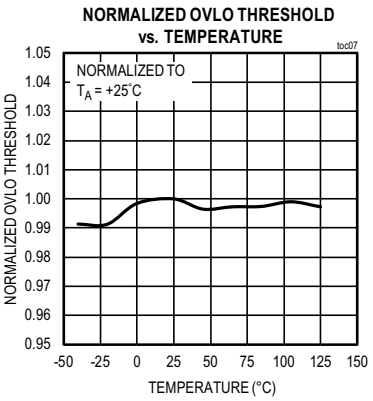
NORMALIZED CURRENT LIMIT vs. SUPPLY VOLTAGE



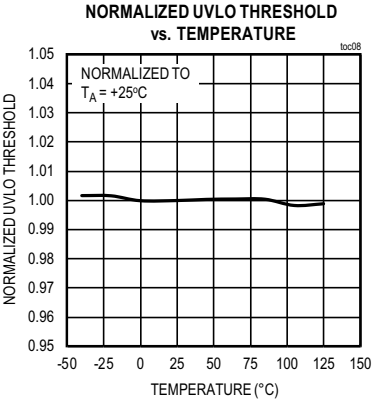
NORMALIZED CURRENT LIMIT vs. TEMPERATURE



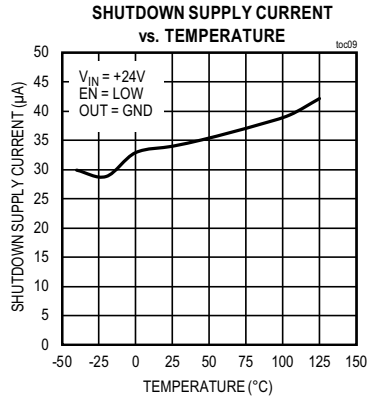
NORMALIZED OVLO THRESHOLD vs. TEMPERATURE



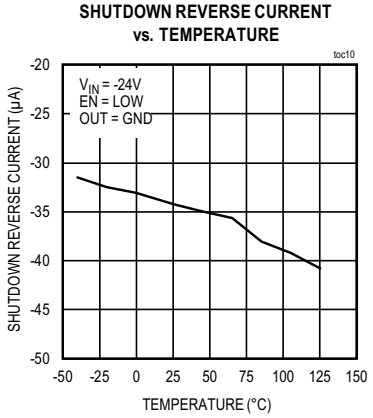
NORMALIZED UVLO THRESHOLD vs. TEMPERATURE



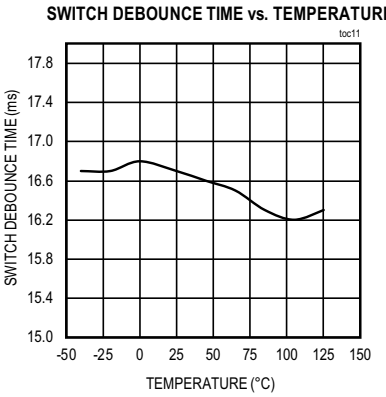
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



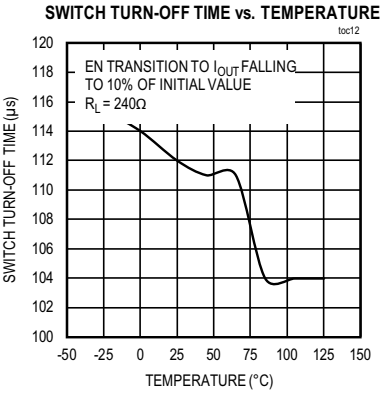
SHUTDOWN REVERSE CURRENT vs. TEMPERATURE



SWITCH DEBOUNCE TIME vs. TEMPERATURE



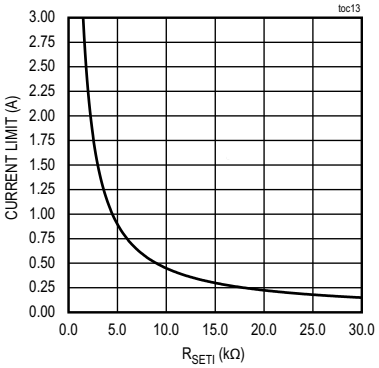
SWITCH TURN-OFF TIME vs. TEMPERATURE



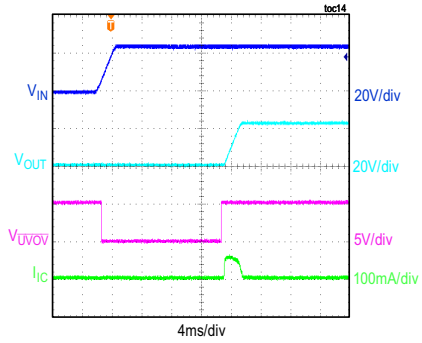
Typical Operating Characteristics (continued)

(C_{IN} = 0.47µF, C_{OUT} = 4.7µF, V_{IN} = 24V, T_A = +25°C, unless otherwise noted.)

CURRENT LIMIT vs. R_{SETI}

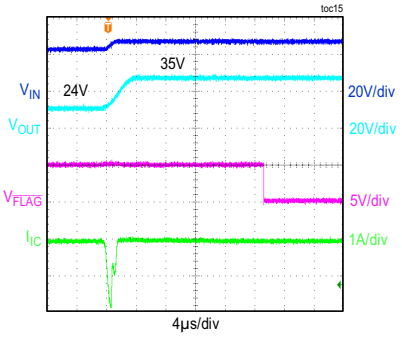


MAX17613A, POWER-UP RESPONSE

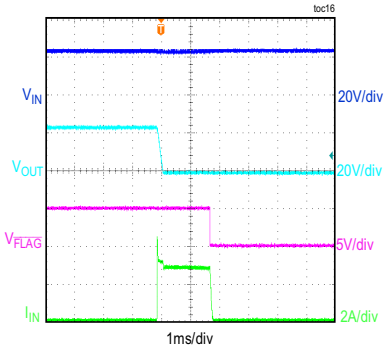


CONDITIONS: C_{OUT} = 4.7µF, I_{LIMIT} = 0.3A, MODE = AUTORETRY

REVERSE-BLOCKING RESPONSE

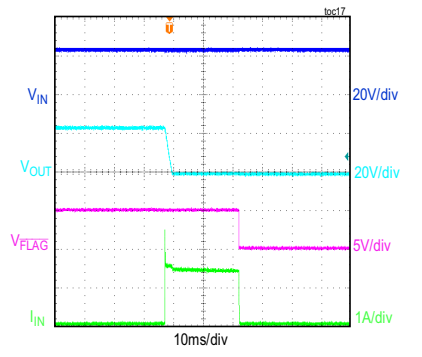


THERMAL SHUTDOWN DUE TO OUTPUT SHORT CIRCUIT



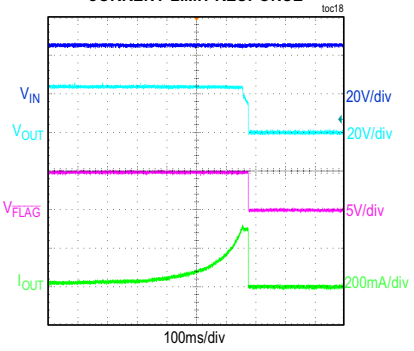
CONDITIONS: I_{LIMIT} = 3A, MODE = AUTORETRY

OUTPUT SHORT-CIRCUIT RESPONSE



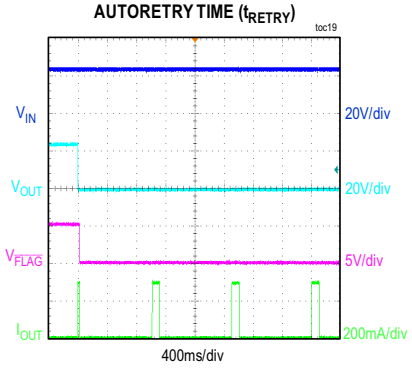
CONDITIONS: I_{LIMIT} = 1.5A, MODE = AUTORETRY

CURRENT-LIMIT RESPONSE



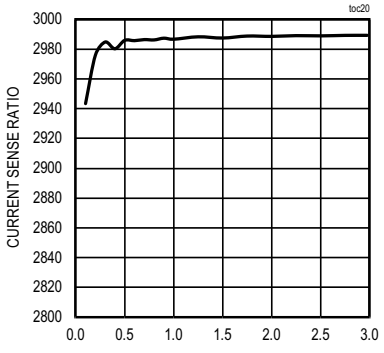
CONDITIONS: I_{LIMIT} = 1.5A, I_L = 100mA TO 1.5A
SHORT ON OUTPUT

AUTORETRY TIME (t_{RETRY})

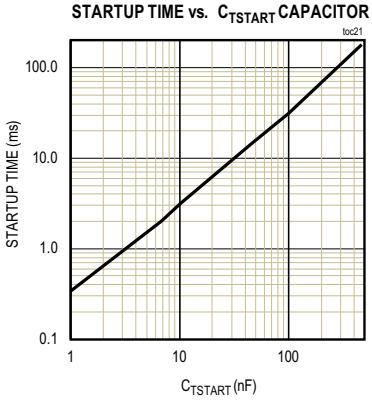


CONDITIONS: I_{LIMIT} = 0.3A, MODE = AUTORETRY

CURRENT SENSE RATIO vs. OUTPUT CURRENT



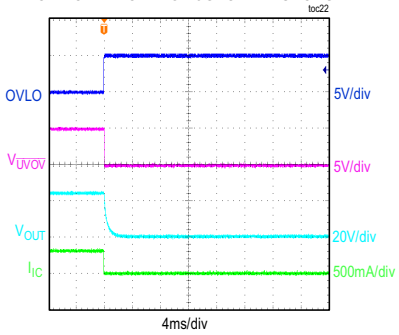
STARTUP TIME vs. C_{TSTART} CAPACITOR



Typical Operating Characteristics (continued)

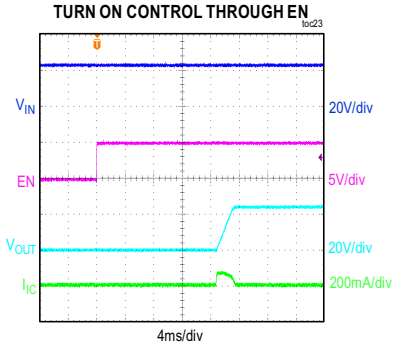
(C_{IN} = 0.47µF, C_{OUT} = 4.7µF, V_{IN} = 24V, T_A = +25°C, unless otherwise noted.)

OVP OVERVOLTAGE CUTOFF RESPONSE



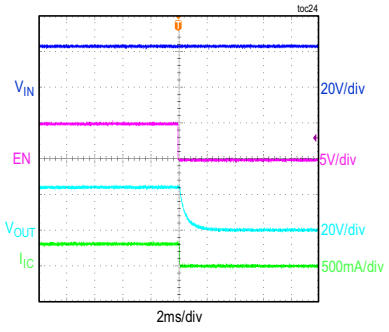
CONDITIONS: I_{LIMIT} = 3A, MODE = AUTORETRY

TURN ON CONTROL THROUGH EN

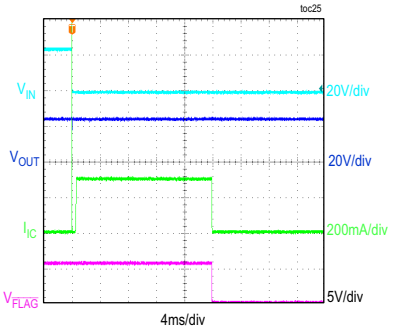


CONDITIONS: I_{LIMIT} = 0.3A, MODE: AUTORETRY

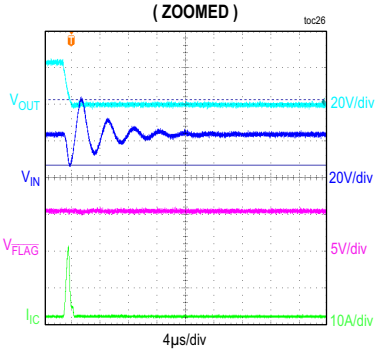
TURN-OFF CONTROL THROUGH EN



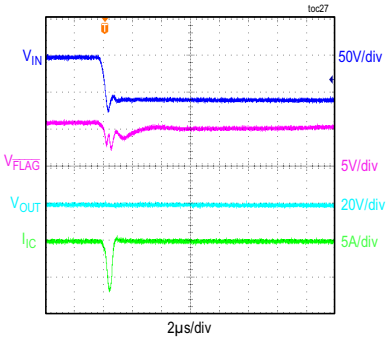
OUTPUT HARD SHORT FAST TRIP RESPONSE



OUTPUT HARD SHORT FAST TRIP RESPONSE (ZOOMED)

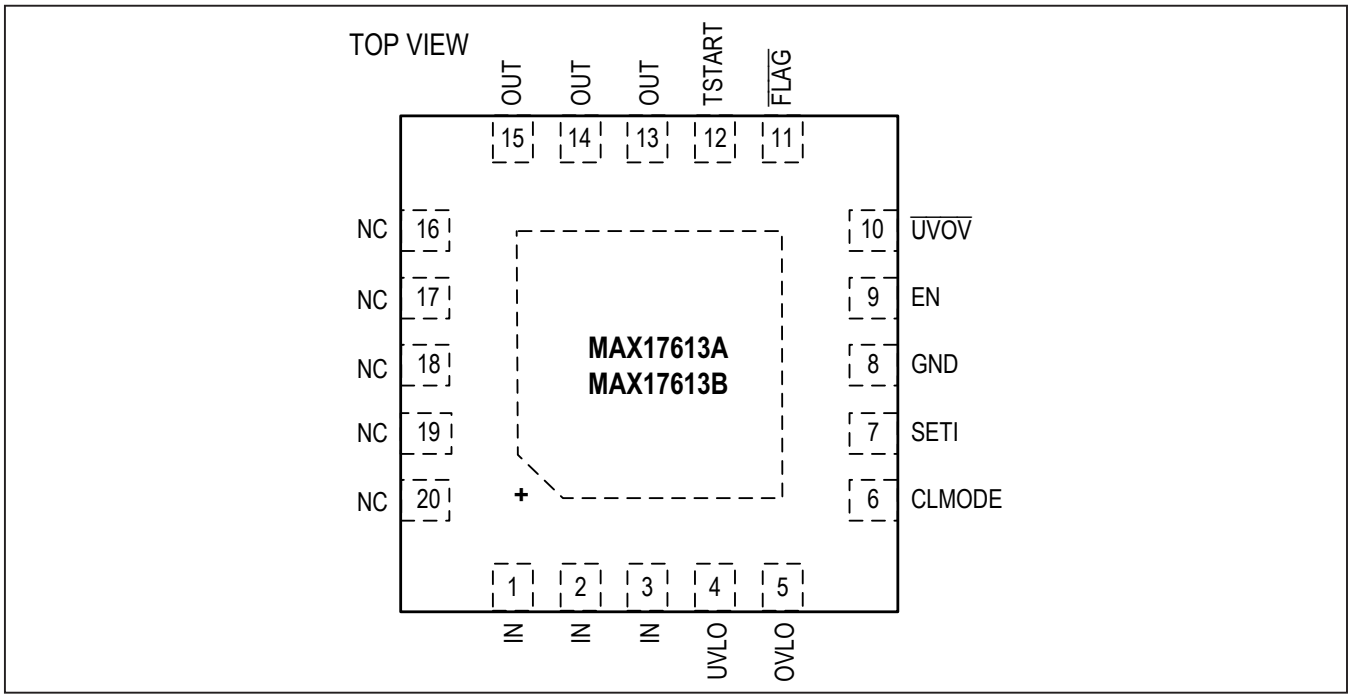


60V REVERSE INPUT SUPPLY PROTECTION RESPONSE

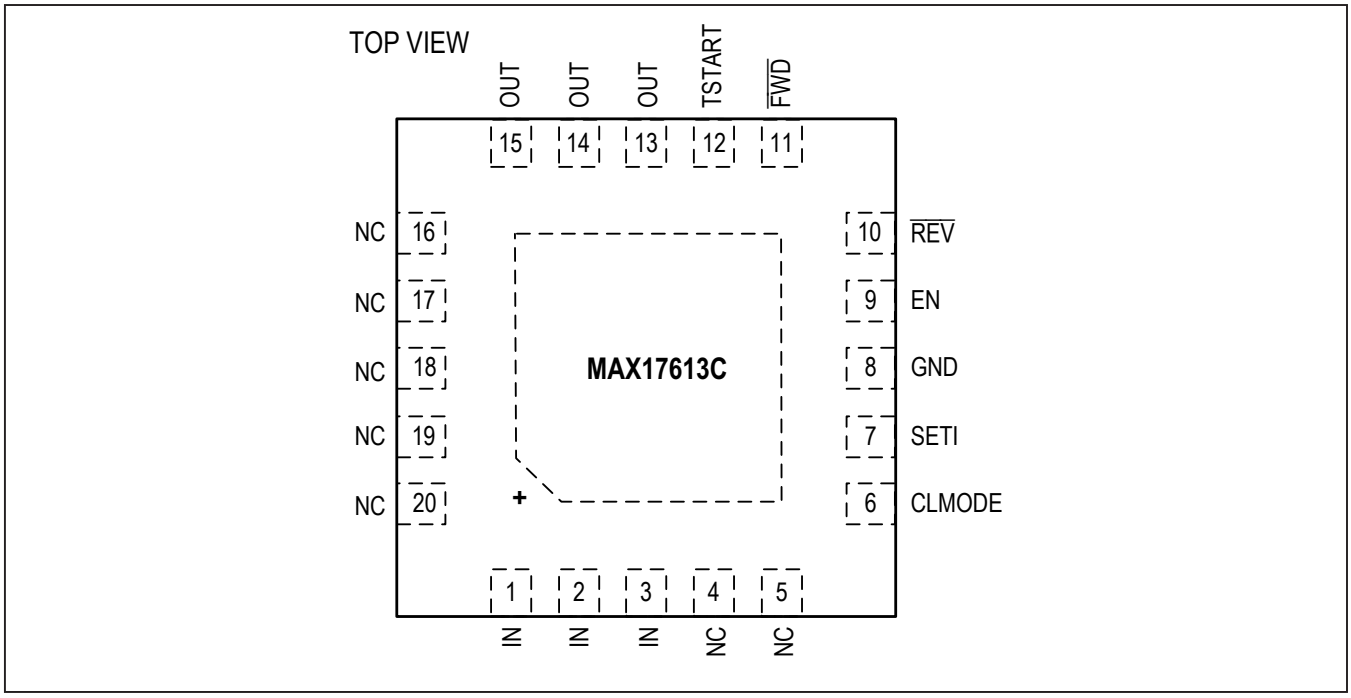


Pin Configuration

MAX17613A and MAX17613B



MAX17613C

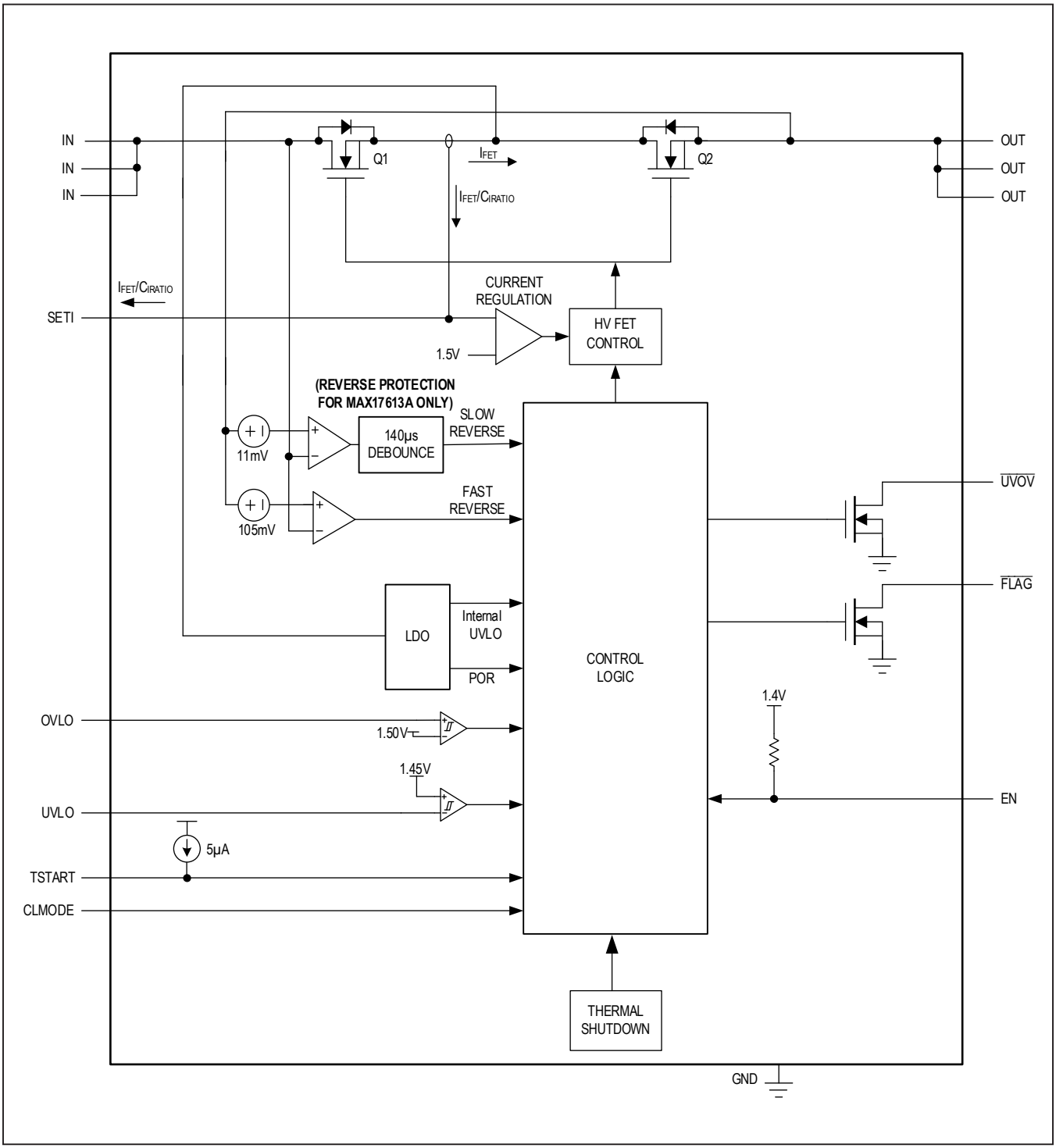


Pin Description

PIN		NAME	FUNCTION
MAX17613A, MAX17613B	MAX17613C		
1-3	1-3	IN	Input Pins. Use a low-ESR ceramic capacitor to enhance ESD protection. For Hot Plug-in applications, see the *Applications Information* section.
4	—	UVLO	UVLO Adjustment. Connect resistive potential divider from IN to GND to set the UVLO threshold.
5	—	OVLO	OVLO Adjustment. Connect resistive potential divider from IN to GND to set the OVLO threshold.
6	6	CLMODE	Current-Limit Mode Selector. Connect CLMODE to GND for Continuous mode. Connect a 150kΩ resistor between CLMODE and GND for latchoff mode. Leave CLMODE unconnected for autoretry mode.
7	7	SETI	Overcurrent-Limit Adjustment Pin and Current Monitoring Output. Connect a resistor from SETI to GND to set overcurrent limit. Do not connect more than 10pF to SETI. See the *Setting the Current-Limiting Threshold (ILIM)* section.
8	8	GND	Ground
9	9	EN	Active High Enable Input. Internally pulled up to 1.8V. Leave it unconnected for always on operation.
10	—	$\overline{UVOV}$	Open-Drain, Fault Indicator Output. $\overline{UVOV}$ goes low with any of the following • Input voltage falls below UVLO threshold. • Input voltage rises above OVLO threshold.
—	10	$\overline{REV}$	Open-Drain, Fault Indicator Output. $\overline{REV}$ goes low when reverse current is detected.
11	—	$\overline{FLAG}$	Open-Drain, Fault Indicator Output. $\overline{FLAG}$ goes low with any of the following • Overcurrent duration exceeds the blanking time. • Overcurrent duration exceeds the startup blanking time. • Reverse current is detected. • Thermal shutdown is active. • R_{SETI} is less than 1.5kΩ (max).
—	11	$\overline{FWD}$	Open-Drain, Fault Indicator Output. $\overline{FWD}$ goes low when: • Overcurrent duration exceeds the blanking time. • Overcurrent duration exceeds the startup blanking time. • Thermal shutdown is active. • R_{SETI} is less than 1.5kΩ (max).
12	12	TSTART	Startup Blanking Time Programming Input. Connect a capacitor from TSTART to GND to program the desired startup blanking time (t_{TSTART}). Leave TSTART unconnected for default startup blanking time of 100ms. See the *Programming Startup Blanking Time (TSTART)* section for more details.
13-15	13-15	OUT	Output Pins. For a long output cable or inductive load, see the *Applications Information* section.
16-20	4, 5, 16-20	NC	Not Connected
—	—	EP	Exposed Pad. Connect EP to a large GND plane with several thermal vias for best thermal performance. Refer to the MAX17613A/B/C EV kit data sheet for a reference layout design.

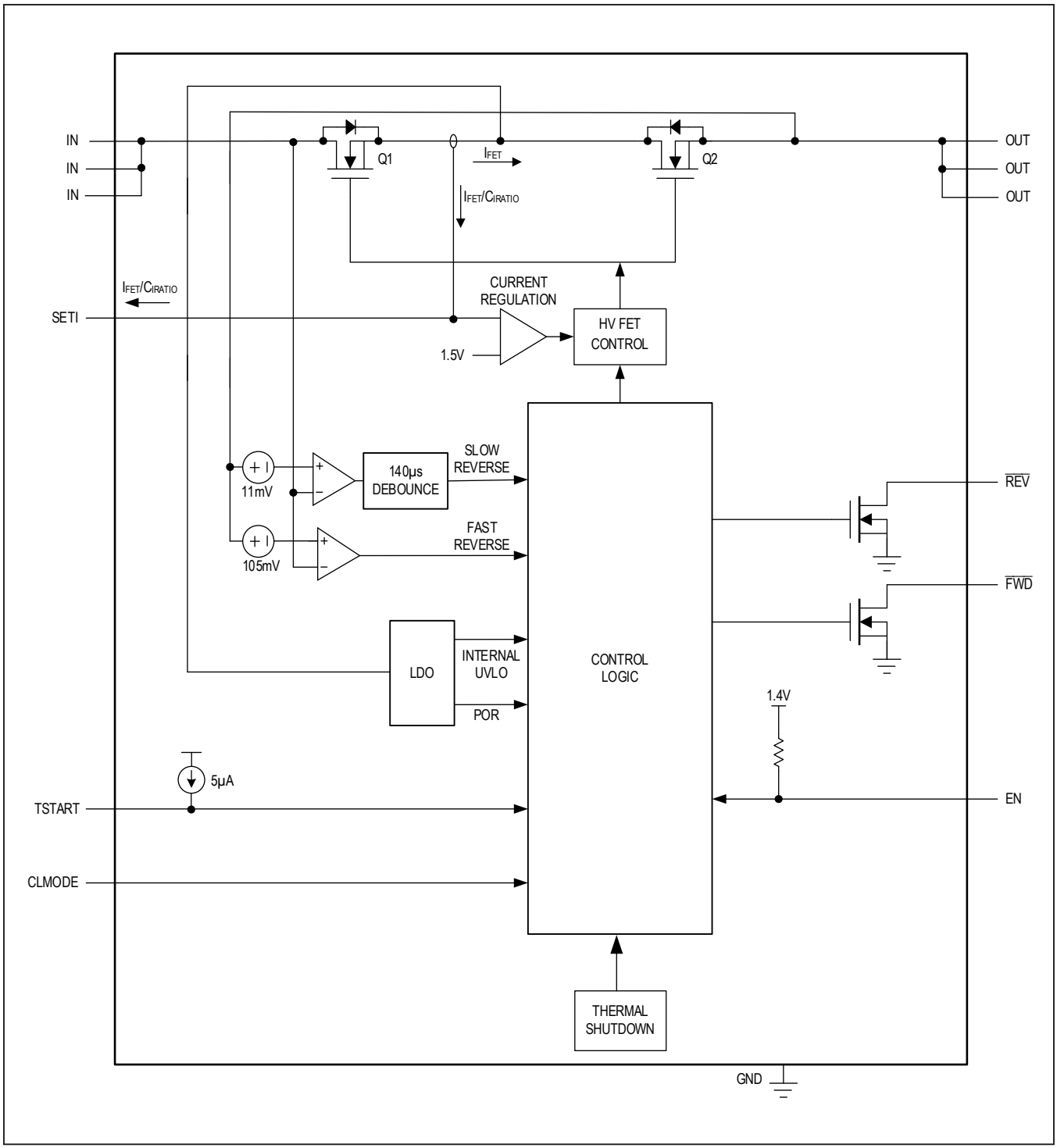
Functional Diagrams

MAX17613A and MAX17613B



Functional Diagrams (continued)

MAX17613C



Detailed Description

The MAX17613A/MAX17613B/MAX17613C overvoltage and overcurrent protection devices offer adjustable protection boundaries for systems against input positive and negative faults up to +60V and -65V, and output load current up to 3A. The devices feature two internal MOSFETs connected in series with a low cumulative R_{ON} of 130mΩ (typ). The devices block out negative input voltages completely. Input undervoltage protection can be programmed between 4.5V and 59V, while the overvoltage protection can be independently programmed between 5.5V and 60V. Additionally, the devices have an internal default undervoltage lockout set at 4.2V (typ). The devices are enabled or disabled through the EN pin by a master supervisory system; hence, offering a switch operation to turn on or turn off power delivery to connected load.

The current through the devices is limited by setting a current limit, which is programmed by a resistor connected from SETI to GND. The current limit can be programmed between 0.15A to 3A. When the device current reaches or exceeds the set current limit, the on-resistance of the internal output NFET Q2 is modulated to limit the current to set limits. The devices offer three different behavioral modes when under current-limited operations: autoretry, continuous, and latchoff modes. The SETI pin also presents a voltage with reference to GND, which under normal operation is proportional to the device current. The voltage appearing on the SETI pin can be read by an ADC on the monitoring system for recording instantaneous device current.

The devices offer status signals to indicate different operational and fault signals. MAX17613A and MAX17613B offer $\overline{FLAG}$ and $\overline{UVOV}$ signals, while MAX17613C offers $\overline{FWD}$ and $\overline{REV}$ signals. All status signal pins are open drain in nature and require external pullup resistors to appropriate system interface voltage. MAX17613A and MAX17613C block reverse current flow (from OUT to IN) while MAX17613B allows reverse current flow. All three devices offer internal thermal shutdown protection against excessive power dissipation. The devices offer a programmable startup blanking time that enables charging large capacitors at the output.

Undervoltage Lockout (UVLO)

Connect an external resistive potential divider to the UVLO pin as shown in the *Typical Operating Circuit* to adjust the UVLO threshold voltage. Use the following equation to adjust the UVLO threshold. The recommended value of R1 is 2.2MΩ.

$$V_{UVLO} = V_{UVLOR} \times \left[1 + \frac{R1}{R2}\right]$$

where V_{UVLOR} is the UVLO rising threshold and V_{UVLO} is the input supply voltage at which the device exits the UVLO condition.

When the voltage on UVLO pin rises above VUVLOR, MAX17613A and MAX17613B devices exit Undervoltage Lockout (UVLO) condition and turn ON. The devices enter UVLO condition and turns OFF when the voltage on UVLO pin falls below VUVLOF. The devices also have a 4.20V (typ) internal UVLO rising threshold. The external resistor divider based UVLO setting should not be set lower than the internal UVLO threshold. MAX17613C offers fixed internal UVLO feature only.

MAX17613A and MAX17613B have an internal power ON reset (POR) sensed at the middle of Q1 and Q2 FETs. These devices turn off the internal FETs Q1 and Q2 when the IN pin voltage is below the internal POR falling threshold of 3.48V (typ). The $\overline{UVOV}$ pin is asserted high and the SETI pin is deactivated. When the IN pin voltage rises above the internal POR rising threshold of 3.88V (typ), the $\overline{UVOV}$ pin is asserted low and the SETI pin is activated. The internal FETs Q1 and Q2 remain turned off. The devices also implement an internal UVLO sensed at the middle of Q1 and Q2 FETs. The Q1 FET is turned on when the IN voltage rises above the internal UVLO rising threshold of 4.20V (typ). The Q2 FET is turned on after 16ms from the instant IN pin voltage rises above the user defined external UVLO voltage rising threshold and the $\overline{UVOV}$ pin is asserted high.

MAX17613C also has an internal power ON reset (POR) sensed at the middle of Q1 and Q2 FETs. The device turns off the internal FETs Q1 and Q2 when the IN pin voltage is below the internal POR falling threshold of 3.48V (typ). The SETI pin is deactivated. When the IN pin voltage rises above the internal POR rising threshold of 3.88V (typ), the SETI pin is activated. The internal FETs Q1 and Q2 remain turned off. The device implements an internal UVLO sensed at the middle of Q1 and Q2 FETs. The Q1 FET is turned on when the IN pin voltage rises above the internal UVLO rising threshold of 4.20V (typ) and the Q2 FET is turned on after 16ms.

Overvoltage Lockout (OVLO)

Connect an external resistive potential divider to the OVLO pin as shown in the *Typical Operating Circuit* to adjust OVLO threshold voltage. Use the following equation to adjust OVLO threshold. The recommended value of R3 is 450kΩ–500kΩ.

$$V_{OVLO} = V_{OVLOR} \times \left[1 + \frac{R3}{R4}\right]$$

where V_{OVLOR} is the OVLO rising threshold and V_{OVLO} is the input supply voltage at which the device enters the OVLO condition.

The MAX17613C does not offer overvoltage protection feature.

The OVLO rising threshold (V_{OVLOR}) is set at 1.5V. If the voltage at the OVLO pin exceeds V_{OVLOR} for time equal to overvoltage switch turn-off time (t_{OFF_OVP}), the switch is turned off and $\overline{UVOV}$ is asserted. When the OVLO condition is removed, the device takes overvoltage falling edge debounce time (t_{DEB_OVP}) to start the switch turn-on process. The switch turns back on after switch turn-on time (t_{ON_SWITCH}) and $\overline{UVOV}$ is deasserted. Figure 1 depicts a typical behavior in overvoltage condition.

Input Debounce Protection

The device features input debounce protection. The device starts operation (turn on the internal FETs) only if the input voltage is higher than the UVLO threshold for a period greater than the debounce time (t_{DEB}). The t_{DEB} elapses only at power-up of the devices. This feature is intended for applications where the EN signal is present when the power supply ramps up. Figure 2 depicts a typical debounce timing diagram.

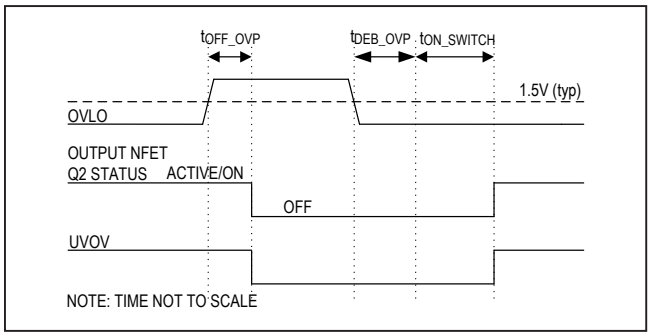


Figure 1. Overvoltage Fault Timing Diagram

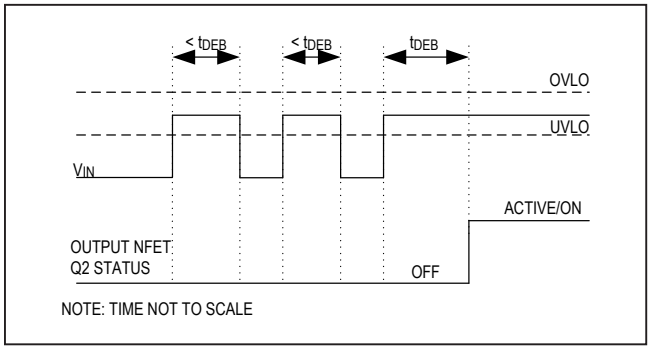


Figure 2. Debounce Timing Diagram

Enable (EN)

The device can be enabled or disabled through the EN pin by driving it above or below EN threshold voltage. Hence the device can be used to turn on or off power delivery to connected loads using the EN pin. Input debounce protection is present when the devices are turned on by driving the EN pin.

Setting the Current-Limiting Threshold (ILIM)

During overload events, the device continuously regulates the device current to the overcurrent limit I_{LIM} programmed by the resistor R_{SETI} connected at the SETI pin. The current limit can be programmed between 0.15A to 3A. Use the following equation to calculate current-limit setting resistor:

$$R_{SETI} = \frac{4500}{I_{LIM}}$$

where,

I_{LIM} is the desired current limit in mA and R_{SETI} is in kΩ.

Do not use R_{SETI} lower than 1.5kΩ. Table 1 shows current-limit thresholds for different resistor values.

When the device current reaches or exceeds the set current limit during overload, short-circuit or during startup cycle charging a large output capacitor, the on-resistance of the internal output NFET Q2 is modulated to limit the current to set limits, resulting in the output voltage droop and increased power dissipation in the device. If the device junction temperature reaches the thermal shutdown threshold T_{JC_MAX} the output NFET Q2 turns off and $\overline{FLAG}$ (or $\overline{FWD}$) is asserted. The output NFET Q2 turns back on in current-limit mode only after the junction temperature cools down by T_{JC_HYS}. The devices feature read out of the current flowing into the IN pin.

Table 1. Current-Limit Threshold vs. SETI Resistor Values

R_{SETI} (kΩ)	CURRENT LIMIT I_{LIM} (A)
30.00	0.15
15.00	0.3
4.53	1.0
2.26	2.0
1.80	2.5
1.50	3.0

A current mirror, with a ratio of C_{IRATIO}, is implemented, using a current-sense auto-zero operational amplifier. The mirrored current flows out through the SETI pin, into the external current-limit resistor. The voltage on the SETI pin provides information about IN current with the following relationship:

$$I_{IN-OUT} = \frac{3 \times V_{SETI}}{R_{SETI}}$$

If SETI is left unconnected, $V_{SETI} \geq 1.5V$. The Q2 FET is turned OFF and allows only a few µA current to flow due to internal circuitry. During startup, this causes the switches to remain off and $\overline{FLAG}$ (or $\overline{FWD}$) to assert after t_{BLANK} elapses. During Startup, if R_{SETI} is lower than 350Ω, the switches remain off and $\overline{FLAG}$ (or $\overline{FWD}$) asserts. For best damped measurement, the capacitance on the SETI pin shall be limited to 10pF.

Programming Startup Blanking Time (TSTART)

The MAX17613A/MAX17613B/MAX17613C devices offer a programmable startup blanking time (t_{TSTART}) that enables charging the large capacitors on the output during startup and when recovering from a fault condition. Connect a capacitor from TSTART to GND to program the startup blanking time (t_{TSTART}). The startup capacitor (C_{TSTART}) is charged with a constant current of 5µA during startup. t_{TSTART} is the time taken for the voltage on C_{TSTART} to reach 1.5V. If the TSTART pin is left unconnected or if the voltage on TSTART pin reaches 1.5V within 100µs ($t_{START-UNCONNECTED}$) during startup, the startup blanking time is internally set to a default value of 100ms ($t_{START-DEFAULT}$). Figure 3 depicts the startup blanking time with and without a capacitor on TSTART pin. t_{TSTART} is the time allowed for V_{OUT} to reach the designated value (V_{IN} - V_{FA}) before the devices enter fault mode. If the output voltage does not reach (V_{IN} - V_{FA}) within the programmed time (t_{TSTART}), then the $\overline{FLAG}$ (or $\overline{FWD}$) is asserted and both the MOSFETs are turned off. During t_{TSTART}, the devices operate in continuous current-limit mode only. This enables charging large capacitors on the output by only inducing a thermal shutdown and recovery process without any additional retry time delay or latch-off event. For thermal shutdown and recovery process, see *Thermal Shutdown Protection* section. When the voltage on the capacitor (C_{TSTART}) reaches 1.5V, t_{TSTART} is considered expired and the capacitor is discharged to ground.

$$t_{TSTART} = \frac{C_{TSTART}}{5\mu} \times 1.5$$

The Table 2 presents C_{TSTART} required for different t_{TSTART} durations.

For the given output capacitor, the startup capacitor (C_{TSTART}) is calculated as:

$$C_{TSTART} \geq \frac{3.33 \times C_{OUT(MAX)} \times V_{IN(MAX)}}{I_{LIM}}$$

The startup blanking time (t_{TSTART}) is related to the startup capacitor (C_{TSTART}) by the following equation:

$$t_{TSTART} = 300 \times C_{TSTART}$$

where,

C_{TSTART} is in nF,

$C_{OUT(MAX)}$ = Maximum output capacitance in µF,

$V_{IN(MAX)}$ = Maximum input voltage in V,

I_{LIM} = Programmed current limit in mA,

t_{TSTART} is in µs.

Do not connect TSTART to GND. If TSTART is connected to GND, the startup blanking time is infinite.

Current Limit Type Selection (CLMODE)

The CLMODE pin shall be used to program the overcurrent response of the device in one of the three modes. Connect a 150kΩ resistor between CLMODE and GND for latchoff current-limit mode. Connect CLMODE to GND for continuous current-limit mode. Leave the CLMODE pin unconnected for autoretry current-limit mode.

In all the three current-limit modes, if the current through the device reaches or exceeds the current-limit threshold, the device limits output current to the programmed current limit by modulating the internal output NFET Q2 on-state resistance.

Table 2. C_{TSTART} vs. t_{TSTART}

t_{TSTART} (ms)	C_{TSTART} (nF)
15	50
60	200
300	1000
100	Left open

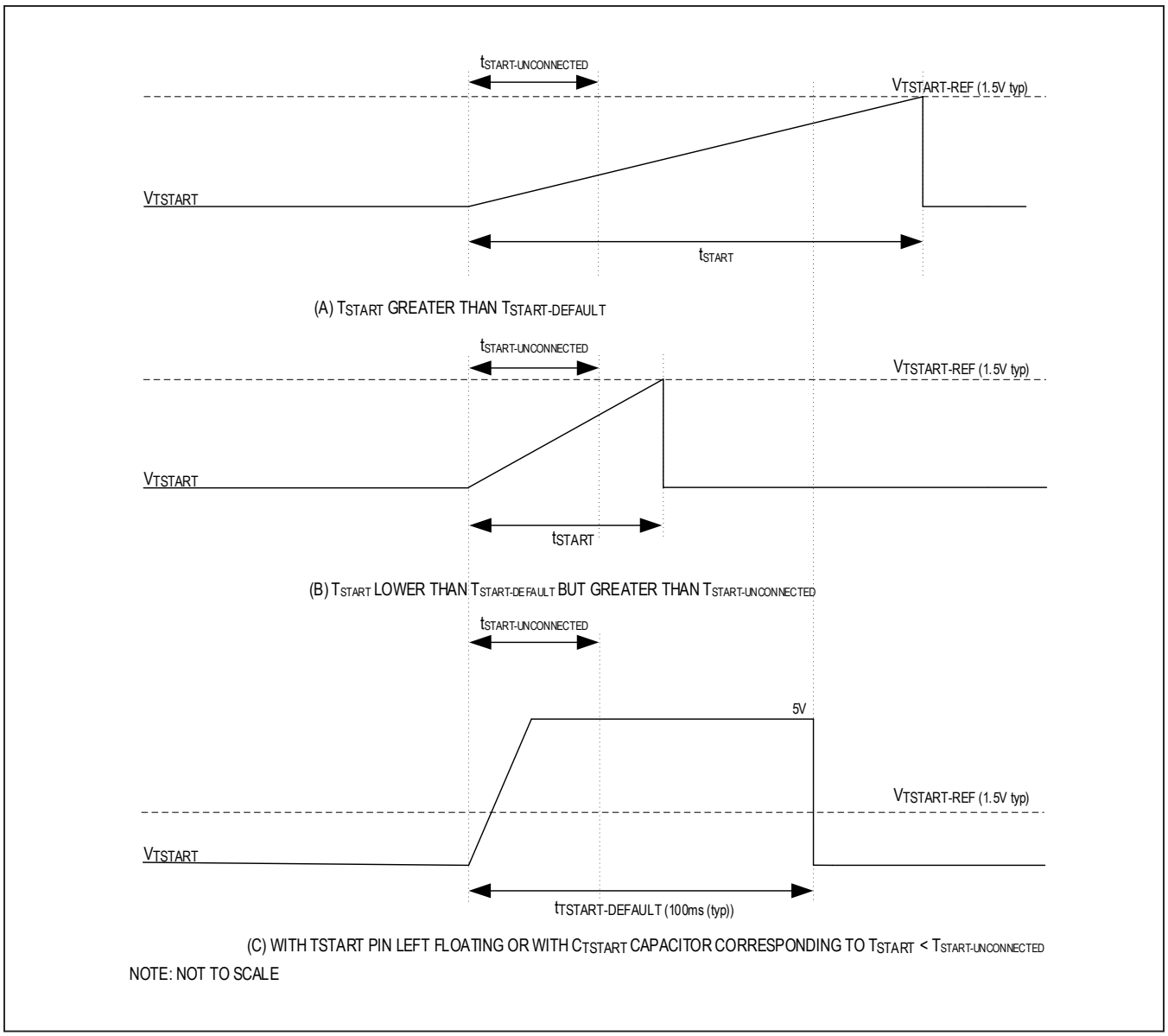


Figure 3. Startup Blanking Time Programming using C_{TSTART}

Continuous Current-Limit Mode

In continuous current-limit mode during startup, the device starts as the startup blanking time (t_{TSTART}) interval starts. The timer t_{TSTART} resets if the output voltage V_{OUT} reaches (V_{IN} - V_{FA}) within t_{TSTART} and then the normal operation continues. If the output voltage V_{OUT} does not reach (V_{IN} - V_{FA}) within t_{TSTART}, the t_{TSTART} timer resets, the $\overline{FLAG}$ (or $\overline{FWD}$) pin asserts, the output NFET Q2 is not turned off, and the operation continues. If the device enters thermal shutdown mode, the $\overline{FLAG}$ (or $\overline{FWD}$) pin asserts and the output NFET Q2 turns off and it turns back on after the junction temperature cools down by T_{JC_HYS}. The $\overline{FLAG}$ (or $\overline{FWD}$) deasserts after V_{OUT} reaches (V_{IN} - V_{FA}). Figure 4 depicts a typical startup behavior in continuous current-limit mode.

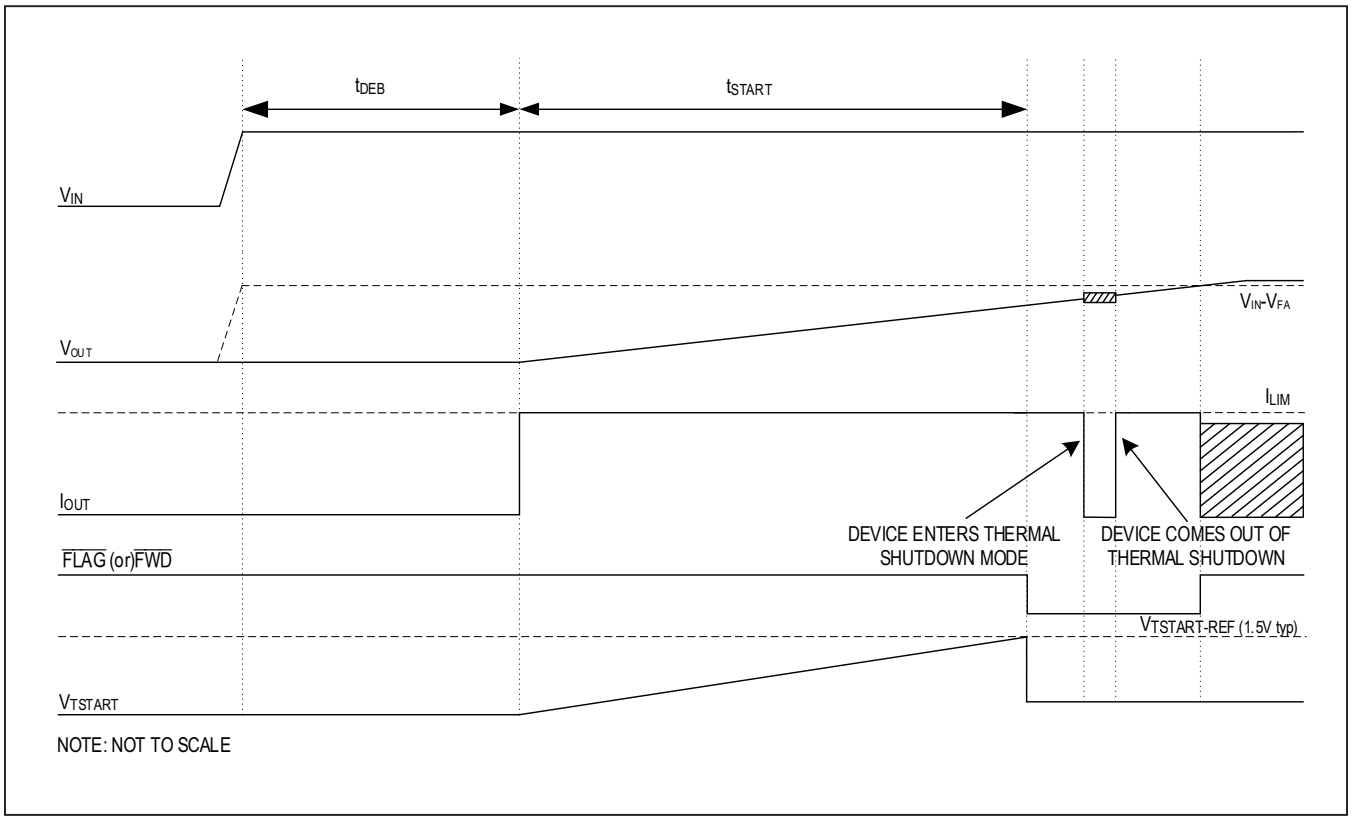


Figure 4. Startup Fault Timing Diagram in Continuous Current-Limit Mode

In continuous current-limit mode during normal operation, if the device enters an overcurrent condition the t_{BLANK} timer starts. The t_{BLANK} timer resets when the overcurrent condition resolves before the t_{BLANK} duration has elapsed and then the normal operation continues. If the overcurrent condition exists for the t_{BLANK} duration, the t_{BLANK} timer resets, the $\overline{FLAG}$ (or $\overline{FWD}$) pin asserts, the output NFET Q2 is not turned-off and the operation continues. If the device enters thermal shutdown mode, $\overline{FLAG}$ (or $\overline{FWD}$) pin asserts and the output NFET Q2 turns off and it turns back on after the junction temperature cools down by T_{JC_HYS}. $\overline{FLAG}$ (or $\overline{FWD}$) deasserts after V_{OUT} reaches (V_{IN} - V_{FA}). Figure 5 depicts a typical operating behavior in continuous current-limit mode.

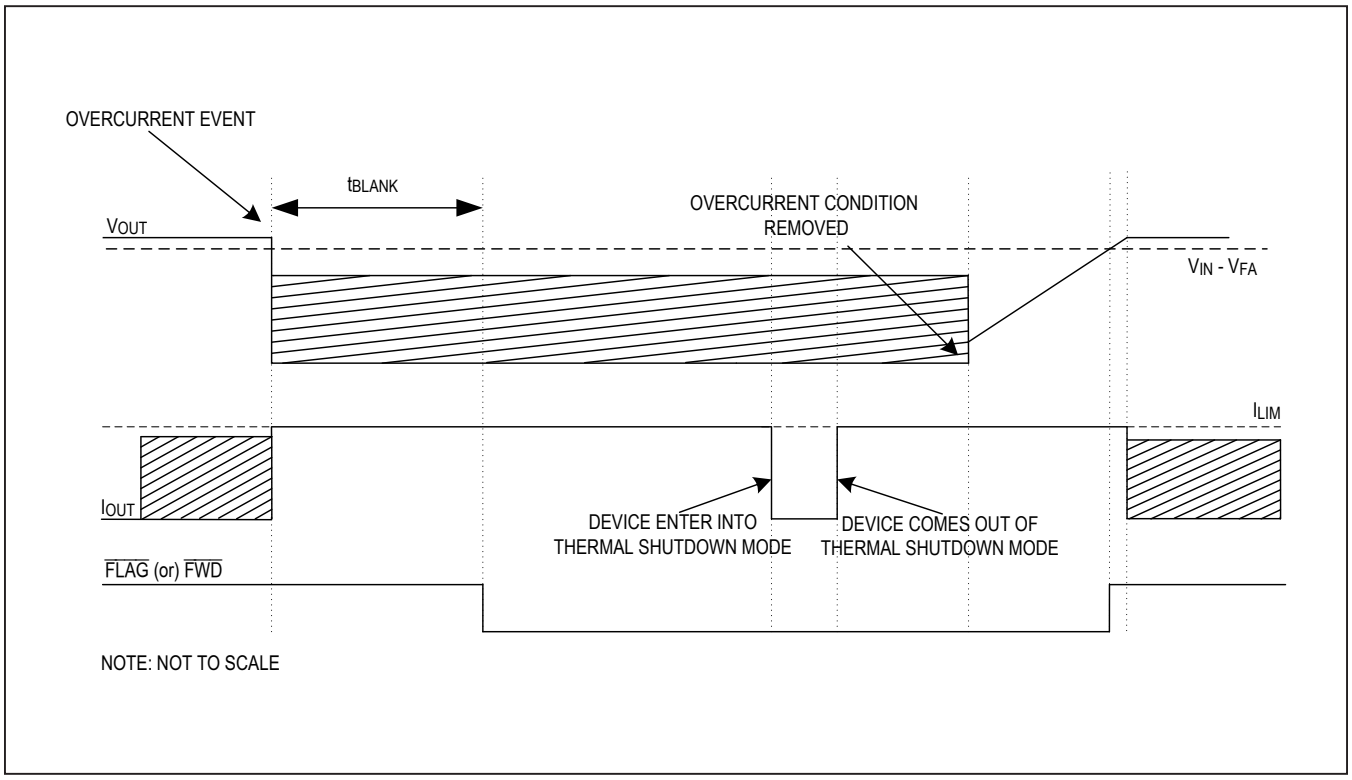


Figure 5. Overcurrent Fault Timing Diagram in Continuous Current-Limit Mode

Autoretry Current-Limit Mode

In autoretry current-limit mode during startup, the device operates in continuous current-limit mode until t_{TSTART}. The timer t_{TSTART} resets if the output voltage V_{OUT} reaches (V_{IN} - V_{FA}) within t_{TSTART} and then the normal operation continues. If the overcurrent condition is present for startup blanking time (t_{TSTART}), the output NFET Q2 is turned off, the timer t_{TSTART} resets, and the $\overline{FLAG}$ (or $\overline{FWD}$) pin asserts. A retry time delay (t_{RETRY}) starts after t_{TSTART} has elapsed and after the device comes out of thermal shutdown mode, if it was entered. During t_{RETRY} time, the output NEFT Q2 remains off. Once the t_{RETRY} time has elapsed, the device reinitiates the startup cycle again. If the overcurrent fault still exists, the autoretry startup cycle is repeated and the $\overline{FLAG}$ (or $\overline{FWD}$) pin remains asserted. If the overcurrent condition is resolved, and the output voltage (V_{OUT}) reaches (V_{IN} - V_{FA}) the output NFET Q2 stays on and the $\overline{FLAG}$ (or $\overline{FWD}$) deasserts. Figure 6 depicts a typical startup behavior in autoretry current-limit mode.

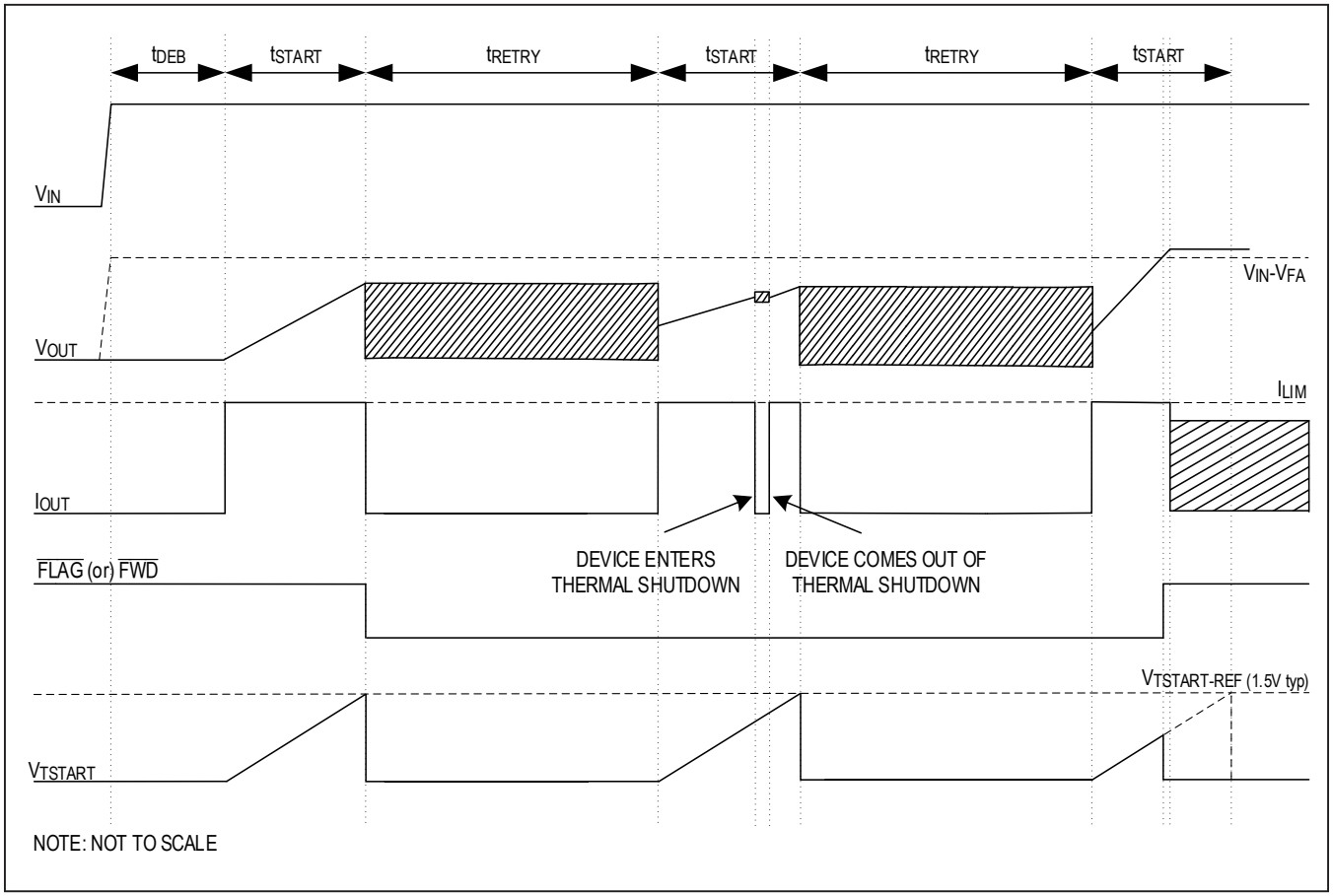


Figure 6. Startup Fault Timing Diagram in Autoretry Current-Limit Mode

In autoretry current-limit mode during normal operation, if the device enters an overcurrent condition, the t_{BLANK} timer starts. The t_{BLANK} timer resets as and when the overcurrent condition resolves before the t_{BLANK} duration has elapsed, and then the normal operation continues. If the overcurrent condition is present for t_{BLANK} duration or if the device junction temperature reaches T_{JC_MAX}, the output NFET Q2 is turned-off, the t_{BLANK} timer resets, and the $\overline{FLAG}$ (or $\overline{FWD}$) pin asserts. A retry time delay (t_{RETRY}) starts after t_{TSTART} has elapsed and after the device comes out of thermal shutdown mode, if it was entered. During the t_{RETRY} interval, the output NFET Q2 remains turned off. Once t_{RETRY} has elapsed, the device initiates the startup cycle. Figure 7 depicts a typical operating behavior in autoretry current-limit mode.

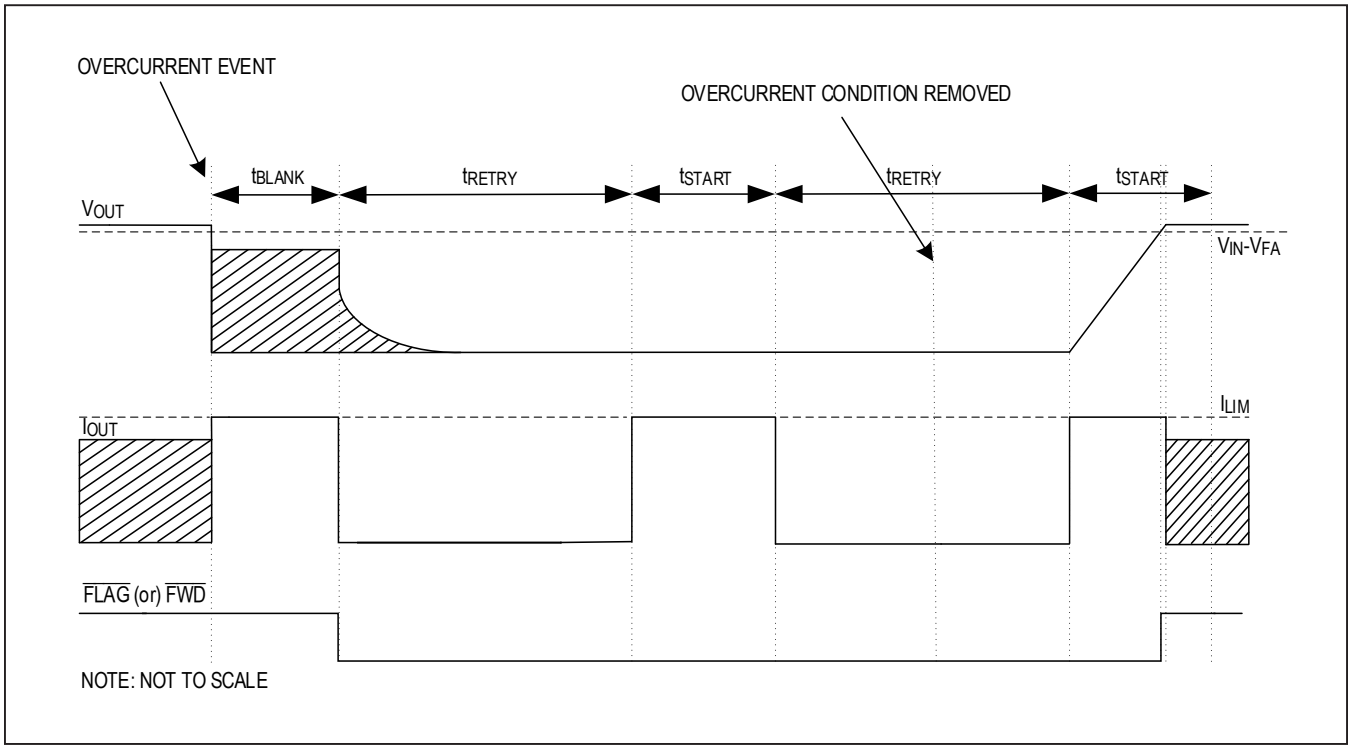


Figure 7. Overcurrent Fault Timing Diagram in Autoretry Current-Limit Mode

The autoretry feature reduces system power compared to continuous current-limit mode in case of overcurrent or short-circuit conditions. When the device is turned on for t_{TSTART} time, the supply current is held at the current limit. During t_{RETRY} time, there is no current through the switch. Thus, the average output current is much less than the programmed current limit. Calculate the average output current using the following equation:

$$I_{LOAD} = I_{LIM}\left[\frac{t_{TSTART}}{t_{TSTART} + t_{RETRY}}\right]$$

The duty cycle is dependent on t_{TSTART} time. For a current-limit threshold setting of 300mA, output voltage of 24V and output capacitance of 1000µF, the t_{TSTART} time is ~80ms. With 1000ms (typ) of t_{RETRY} time, the duty cycle is ~8%, resulting in a 92% power reduction when compared to the device being on the entire time.

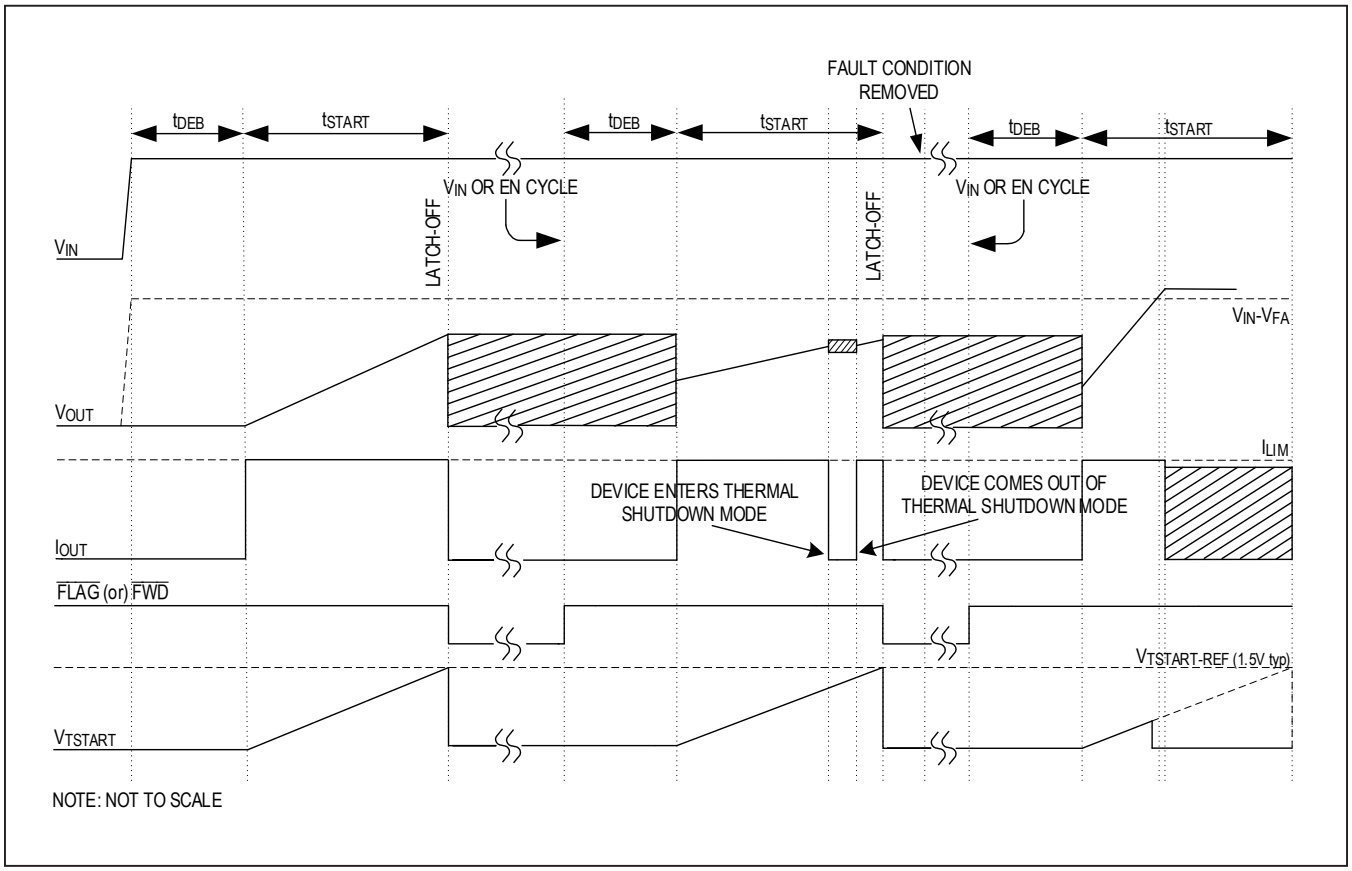


Figure 8. Startup Fault Timing Diagram in Latchoff Current-Limit Mode

Latchoff Current-Limit Mode

In latchoff current-limit mode during startup, the device operates in continuous current-limit mode until t_{TSTART}. The timer t_{TSTART} resets if the output voltage V_{OUT} reaches (V_{IN} - V_{FA}) within t_{TSTART} and then the normal operation continues. If the overcurrent condition is present for longer than startup blanking time (t_{TSTART}), the output NFET Q2 is turned off and latched, the timer t_{TSTART} resets, and the $\overline{FLAG}$ (or $\overline{FWD}$) pin asserts. To reset the device, either toggle the enable control signal (EN) or cycle the input voltage. Figure 8 depicts a typical startup behavior in latchoff current-limit mode.

In latchoff current-limit mode during normal operation, if the device enters an overcurrent condition, the t_{BLANK} timer starts. The t_{BLANK} timer resets as and when the overcurrent condition resolves before the t_{BLANK} duration has elapsed, and then the normal operation continues. If the overcurrent condition exists for the t_{BLANK} duration or if the device junction temperature reaches T_{JC_MAX}, the output NFET Q2 is turned off and latched, the t_{BLANK} timer resets, and the $\overline{FLAG}$ (or $\overline{FWD}$) pin asserts. To reset the device, either toggle enable control signal (EN) or cycle the input voltage. Figure 9 depicts a typical operating behavior in latchoff current-limit mode.

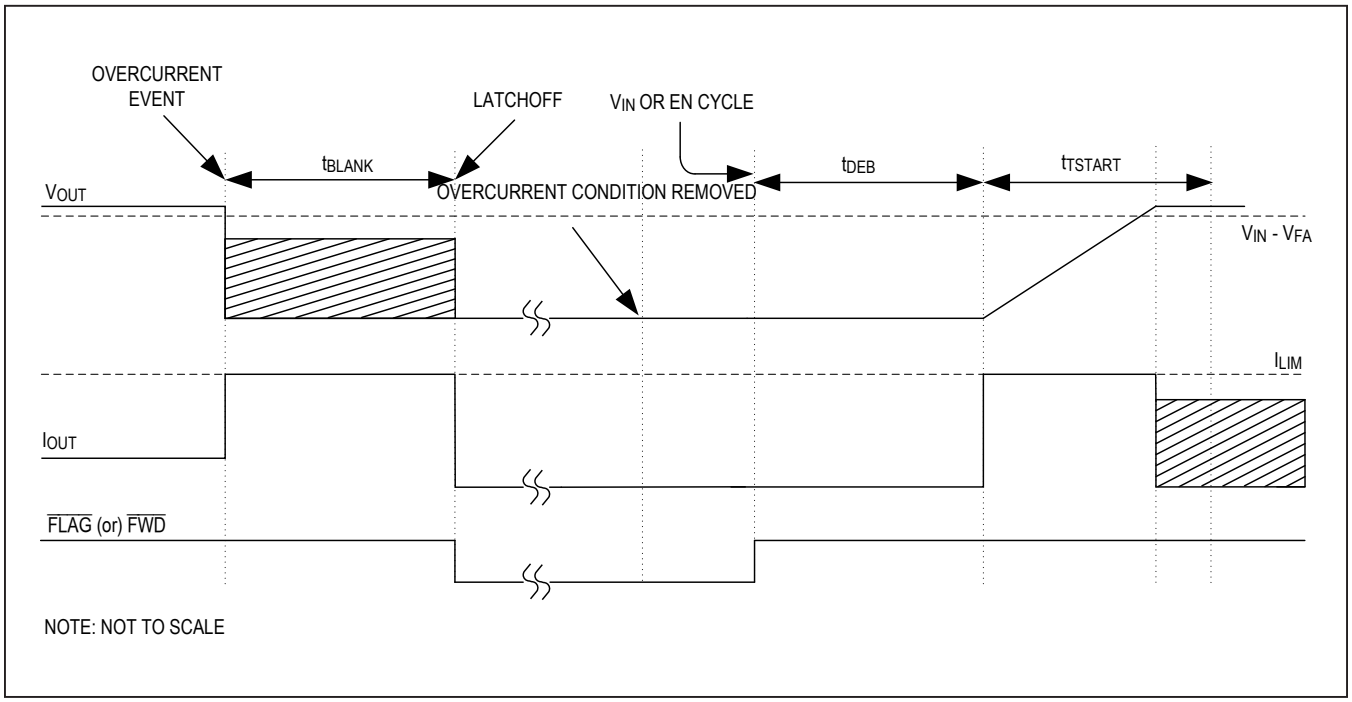


Figure 9. Overcurrent Fault Timing Diagram in Latchoff Current-Limit Mode

Short Circuit Protection

During a hard output short circuit event, the current through the device increases very rapidly. The device incorporates a fast-trip current comparator to limit the output short circuit peak current. The fast-trip current comparator turns off only the internal FET Q2 within 1µs(t_{DELAY1}), when the current through the FET exceeds I_{OCP}. The I_{OCP} is internally set to 4.5A above the set current limit. After a time delay 400µs(t_{DELAY2}), the device turns back on and limits the output current to programmed current limit and operates as described in earlier current limit mode sections. Figure 10 illustrates the behavior of the system when the current exceeds the I_{OCP} threshold.

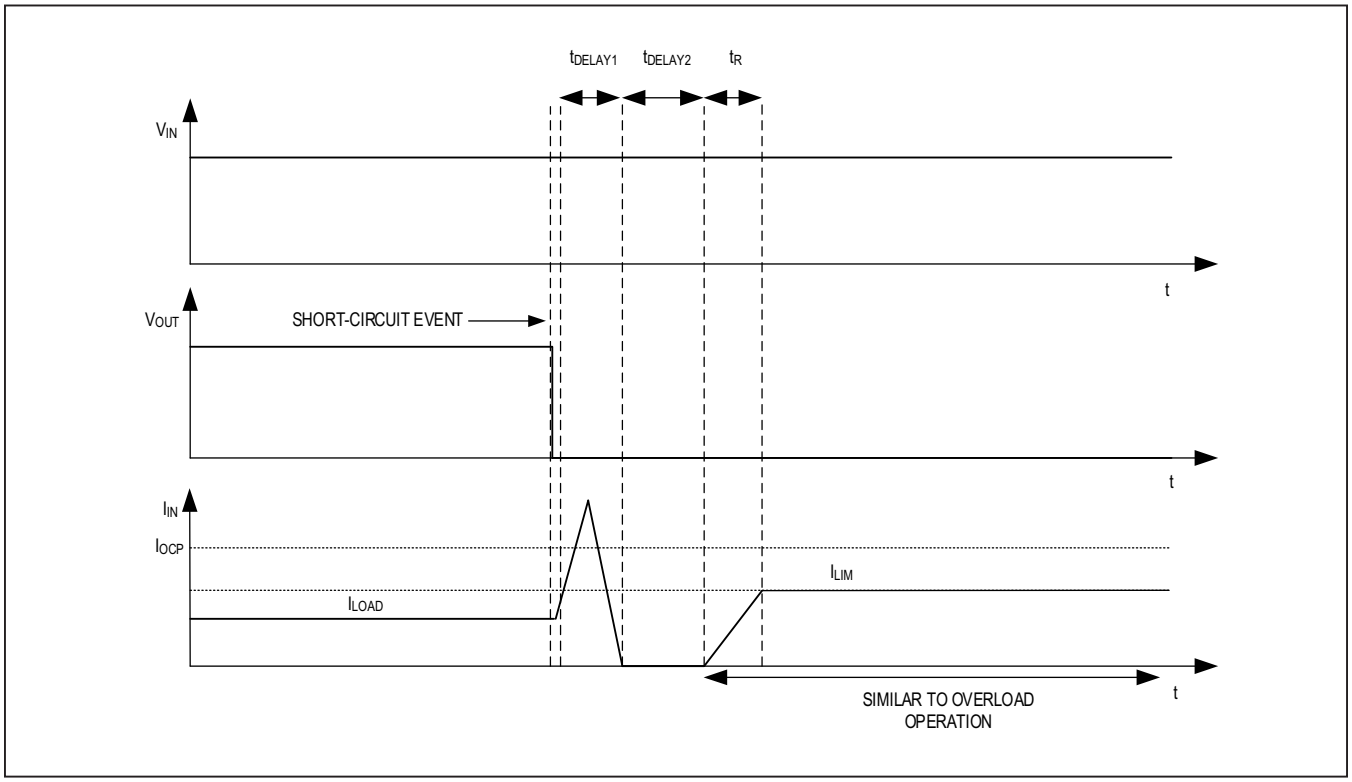


Figure 10. Fast Overcurrent Trip Timing Diagram

Reverse Current Protection

In MAX17613A and MAX17613C, the reverse current protection feature is enabled and it prevents reverse current flow from the OUT to IN pins. In MAX17613B, the reverse current protection feature is disabled, which allows reverse current flow from the OUT to IN pins. This feature is useful in applications with inductive loads.

The MAX17613A and MAX17613C devices monitor V_{IN} and V_{OUT} to provide true reverse current blocking when a reverse condition or input failure condition is detected. In both MAX17613A and MAX17613C devices, two reverse current protection features are implemented.

A slow reverse current condition is detected if (V_{IN} - V_{OUT}) < $-V_{RIBS}$ is present for reverse current blocking debounce blanking time (t_{DEBRIB}). During this condition, only the input NFET Q1 turns off and $\overline{FLAG}$ (or $\overline{REV}$) is asserted while the output NFET Q2 is kept on. During and after this time, the device monitors the voltage difference between the OUT and IN pins to determine whether the reverse current is still present. Once the reverse current condition has been removed, input NFET Q1 turns back on and the $\overline{FLAG}$ (or $\overline{REV}$) pin is deasserted. The input NFET Q1 takes ~100µs (t_{Q1_ON}) to turn on. Figure 11 depicts typical behavior in slow reverse current conditions.

A fast reverse current condition is detected if (V_{IN} - V_{OUT}) < $-V_{RIBF}$ is present for reverse current blocking fast response time (t_{RIB}). During this condition, only the input NFET Q1 turns off and $\overline{FLAG}$ (or $\overline{REV}$) is asserted while the output NFET Q2 is kept on. During and after this time, the device monitors the voltage difference between the OUT and IN pins to determine whether the reverse current is still present. Once the reverse current condition has been removed, input NFET Q1 turns back on and the $\overline{FLAG}$ (or $\overline{REV}$) pin is deasserted. The input NFET Q1 takes ~100µs (t_{Q1_ON}) to turn on. Figure 12 depicts typical behavior in fast reverse current conditions.

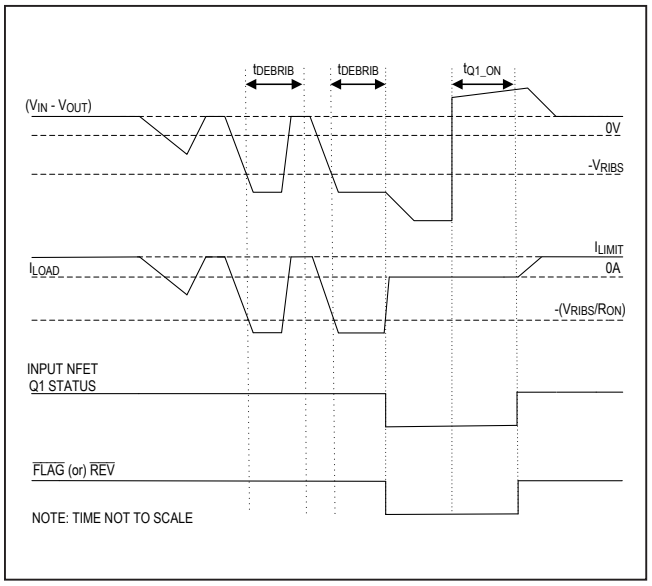


Figure 11. Slow Reverse Current Fault Timing Diagram

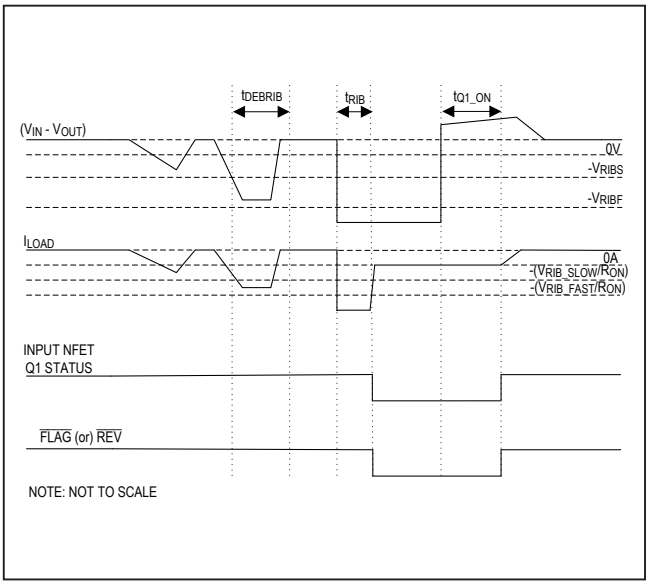


Figure 12. Fast Reverse Current Fault Timing Diagram

Fault Output

The MAX17613A and MAX17613B devices have two open-drain fault outputs, $\overline{FLAG}$ and $\overline{UVOV}$. They require external pullup resistors to a DC supply. The $\overline{FLAG}$ pin goes low when any of the following conditions occur:

- Overcurrent duration exceeds blanking time t_{BLANK}.
- Overcurrent duration exceeds startup blanking time (t_{TSTART}) during the startup cycle.
- Reverse current is detected (MAX17613A only).
- Thermal shutdown is active.
- R_{SETI} is less than 1.5kΩ (max).

The other fault output $\overline{UVOV}$ goes low when input voltage falls below the UVLO threshold or rises above the OVLO threshold. Note that the UVLO fault has a debounce time of 16ms. This fault is removed 16ms after the input voltage has crossed the UVLO threshold. This debounce also elapses only at powerup. As a consequence, the $\overline{UVOV}$ pin fault signal is always asserted at power-up for at least 16ms.

The MAX17613C device has two open-drain fault outputs, $\overline{FWD}$ and $\overline{REV}$. They require external pullup resistors to a DC supply. $\overline{FWD}$ goes low when any of the following conditions occur:

- Overcurrent duration exceeds the blanking time.
- Thermal shutdown is active.
- R_{SETI} is less than 1.5kΩ (max).

$\overline{REV}$ goes low when reverse current is detected.

Thermal Shutdown Protection

The device has the thermal shutdown feature to protect against overheating. The device turns off and the $\overline{FLAG}$ (or $\overline{FWD}$) pin asserts when the junction temperature exceeds T_{JC_MAX} (+155°C typ). The device exits thermal shutdown and resume normal operation after the junction temperature cools down by T_{JC_HYS} (15°C typ), except when in latchoff mode, the device remains latched off.

The thermal limit behaves similar to the current limit. In autoretry mode, the thermal limit works with the autoretry timer. When the device comes out of thermal limit, the part is turned on after the retry time. In latchoff mode, the device latches off until power or EN is cycled. In continuous mode, the device only disables while the temperature is over the limit. There is no blanking time for thermal protection.

Applications Information

IN Capacitor

A 0.47µF capacitor from the IN pin to GND is recommended to hold input voltage during sudden load current changes.

Hot Plug-In at the IN terminal

In many system powering applications, an input-filtering capacitor is required to lower radiated emission and enhance ESD capability. In hot plug-in applications, parasitic cable inductance along with the input capacitor causes overshoot and ringing when a live power cable is connected to the input terminal.

This effect causes the protection device to see almost twice the applied voltage. A transient voltage suppressor (TVS) is often used in industrial applications to protect the system from these conditions. A TVS that is capable of limiting surge voltage to 60V (max) should be placed close to the input terminal for enhanced protection. The tolerated slew rate at the IN pins is 100V/µs (max).

Input Hard Short to Ground

In many system applications, an input short-circuit protection is required. The MAX17613A and MAX17613C devices detect reverse current entering at the OUT pin and flowing out of the IN pin, then turns off the internal FETs. The magnitude of reverse current depends on the inductance of input circuitry and any capacitor installed near the IN pins.

The devices can be damaged in case V_{IN} goes so negative that (V_{OUT} - V_{IN}) > 60V.

OUT Capacitor

The maximum capacitive load (C_{MAX} in µF) that can be connected is a function of current-limit setting (I_{LIM} in mA), the startup time (t_{TSTART} in ms) and the input voltage. C_{MAX} is calculated using the following relationship:

$$C_{MAX} = \frac{I_{LIM} \times t_{TSTART}}{V_{IN}}$$

For example, for V_{IN} = 24V, t_{TSTART} = 60ms, and I_{LIM} = 1000mA, C_{MAX} equals 2500µF.

Output capacitor values in excess of C_{MAX} can trigger false overcurrent condition. Note that the above expression assumes no load current is drawn from the OUT pins. Any load current drawn would offset the capacitor charging current resulting in a larger charging period; hence, the possibility of a false overcurrent condition.

Hot Plug-In at the OUT terminal

In some applications, there might be a possibility of applying an external voltage at the OUT terminal of the devices with or without presence of input voltage. During these conditions, devices detect any reverse current entering at the OUT pin and flowing out of the IN pin and turn off the internal FETs. Parasitic cable inductance along with input and output capacitors cause overshoot and ringing when an external voltage is applied at the OUT terminal. This causes the protection devices to see up to twice the applied voltage, which can damage the devices. It is recommended to maintain overvoltages such that the voltages at the pins do not exceed the absolute maximum ratings. The tolerated slew rate at the OUT pins is 100V/µs (max).

Output Freewheeling Diode for Inductive Hard Short to Ground

In applications that require protection from a sudden short to ground with an inductive load or a long cable, a schottky diode between the OUT terminal and ground is recommended. This is to prevent a negative spike on the OUT due to the inductive kickback during a short-circuit event.

Layout and Thermal Dissipation

To optimize the switch response time to output short-circuit conditions, it is very important to keep all traces as short as possible to reduce the effect of undesirable parasitic inductance. Place input and output capacitors as close as possible to the device (no more than 5mm). The IN and OUT pins must be connected with wide short traces to the power bus. During normal operation, the power dissipation is small and the package temperature change is minimal.

Power dissipation under steady-state normal operation may be calculated as:

$$P_{(SS)} = (I_{OUT})^2 \times R_{ON}$$

Refer to the *Electrical Characteristics* table and *Typical Operating Characteristics* for R_{ON} values at various operating temperatures.

If the output is continuously shorted to ground at the maximum supply voltage, the switches with the autoretry option might not cause thermal shutdown detection to trip. Power dissipation in the devices operating in autoretry mode can be calculated using the following equation:

$$P_{(AVG)} = \frac{V_{IN(MAX)} \times I_{OUT(MAX)} \times \left(t_{START}\right)}{t_{START} + t_{RETRY}}$$

Attention must be given to continuous current-limit mode when the power dissipation during a fault condition can cause the device to reach the thermal shutdown threshold. Thermal vias from the exposed pad to the ground plane are highly recommended to increase system thermal capacitance while reducing the thermal resistance to ambient temperature.

ESD Protection

The devices are specified for ±15kV (HBM) typical ESD resistance on IN when IN is bypassed to ground with a 0.47µF low-ESR ceramic capacitor. No capacitor is required for ±2kV (HBM) typical ESD on IN. All the pins have a ±2kV (HBM) typical ESD protection.

Figure 13 shows the Human Body Model and Figure 14 shows the current waveform it generates when discharged into a low impedance. This model consists of a 100pF capacitor charged to the ESD voltage of interest, which is then discharged into the device through a 1.5kΩ resistor.

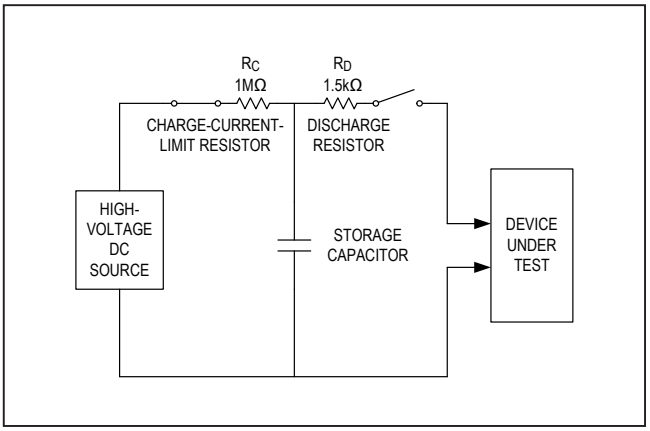


Figure 13. Human Body ESD Test Model

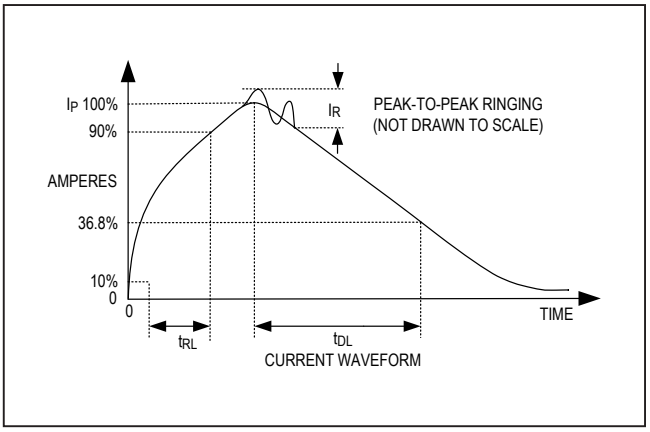


Figure 14. Human Body Current Waveform

Ordering Information

PART	TEMP RANGE	PIN PACKAGE	FEATURE DIFFERENCES
MAX17613AATP+T	-40°C to +125°C	20 TQFN-CU EP*	OV, UV, Reverse Current Protection
MAX17613BATP+T	-40°C to +125°C	20 TQFN-CU EP*	OV,UV
MAX17613CATP+T	-40°C to +125°C	20 TQFN-CU EP*	Reverse Current Protection
MAX17613AATP+	-40°C to +125°C	20 TQFN-CU EP*	OV, UV, Reverse Current Protection
MAX17613BATP+	-40°C to +125°C	20 TQFN-CU EP*	OV,UV
MAX17613CATP+	-40°C to +125°C	20 TQFN-CU EP*	Reverse Current Protection

+ Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape-and-reel.
**EP = Exposed pad.*

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/19	Initial release	—
1	11/21	Updated *General Description*, *Benefits and Features*, *Absolute Maximum Ratings*, *Electrical Characteristics* table, *Typical Operating Characteristics*, *Pin Description* table, *Functional Diagrams*, *Detailed Description*, *Figures 3-4, Figures 6-8, Applications Information and Ordering Information. Added Figure 10.*	1, 2-5, 7-23