*Click **here** to ask an associate for production status of specific part numbers.*

MAX16173

Ideal Diode Controller with Active Rectifier

General Description

The MAX16173 is an ideal diode controller that provides system protection against input transients and reverse-current conditions. The wide operating voltage range of 3V to 50V, combined with 3µA of shutdown current, make the MAX16173 ideal for automotive applications.

The MAX16173 features an integrated boost converter that is capable of driving the gate of the external n-channel power MOSFET 11V above the source during high load operation. Fast pull up and pull down current sources allow rectification of 50kHz to 250kHz AC components riding on the main supply input. A fast-acting comparator allows the MAX16173 to block reverse-current flow by shorting the gate to the source when the input is driven 10mV (typ) lower than the output. In light load applications, the MAX16173 regulates the voltage between the source and drain of the external n-channel MOSFET to 20mV(typ). For high load applications, the gate is driven high to enhance operation mode to minimize power dissipation and to increase system's power efficiency.

During normal operation, the boost converter regulates the gate voltage by monitoring the voltage across CD and DRN. When the voltage across V_{CD-DRN} drops below the 11V(typ) regulated voltage, the boost converter is enabled to maintain the regulation voltage.

The MAX16173 features a diagnostic procedure to check the health of the power MOSFET. An open-drain active-high output (FETOK) deasserts low when the power MOSFET is either open or short. A power good output (PG) asserts high after the completion of power up to indicate the good power-up condition.

The MAX16173 is available in a 3mm x 3mm, 10-pin TDFN package and operates over the automotive temperature range of -40°C to +125°C.

Applications

- Automotive Power Systems
- Network Telecom Power Systems
- RAID Systems
- Servers

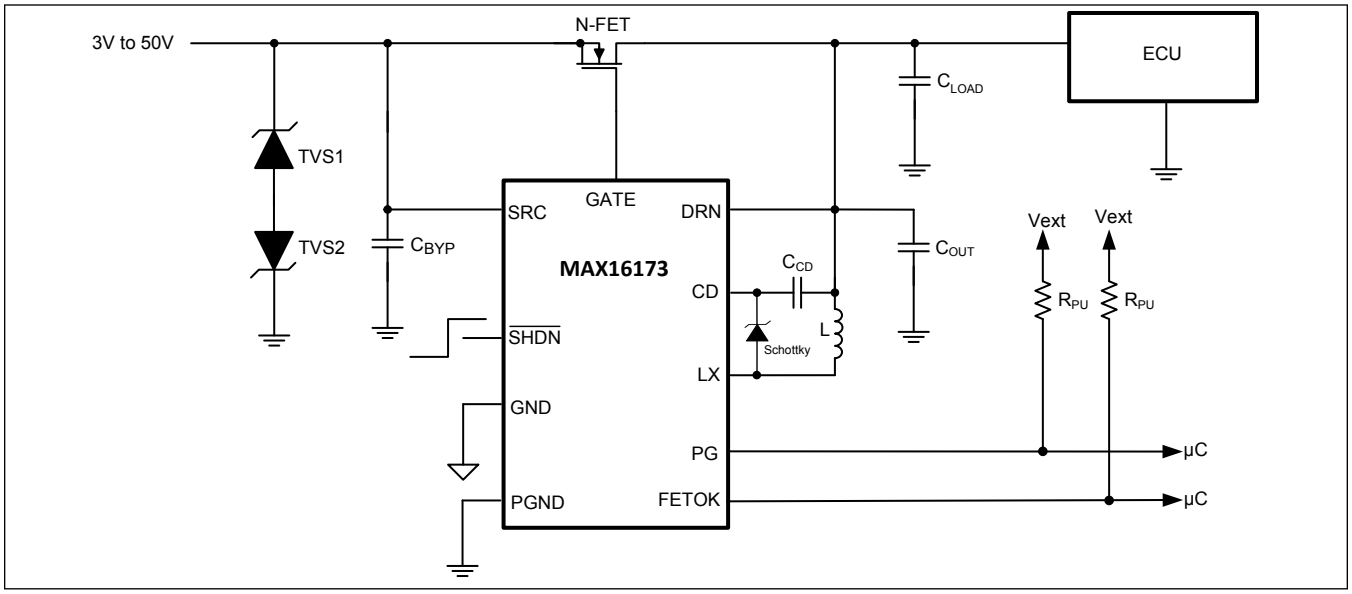
Benefits and Features

- -42V to +65V Protection Voltage Range
- 3V to 50V Operating Voltage Range
- MOSFET Diagnostic Test
- 3µA (Typ) Shutdown Current
- Active Rectifier
- Open-Drain FETOK Output
- Open-Drain Power Good Output
- -40°C to +125°C Temperature Range
- 3mm x 3mm Side Wettable TDFN

***Ordering Information** appears at end of data sheet.*

19-101198; Rev 0; 5/22

Typical Application Circuit



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Absolute Maximum Ratings

SRC, $\overline{SHDN}$ to GND ..... -42V to +65V
SRC to $\overline{SHDN}$ ..... -42V to +65V
DRN to GND ..... -0.3V to +65V
DRN to SRC ..... -65V to +70V
GATE to CD ..... -76V to +0.3V
GATE to SRC ..... -0.3V to +17V
LX to SRC ..... -65V to +66V
CD to GND ..... -0.3V to +76V
PG, FETOK to GND ..... -0.3V to +6V
Continuous Power Dissipation (Single Layer Board) (T_A = +70°C, derate 18.5mW/°C above +70°C.) 1481.5mW
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 24.4mW/°C above +70°C.) 1951.2mW

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

10 TDFN

Package Code	T1033Y+1C
Outline Number	21-100346
Land Pattern Number	90-0003
Thermal Resistance, Four Layer Board:	
Junction-to-Ambient (θ_{JA})	41C/W
Junction-to-Case Thermal Resistance (θ_{JC})	9C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics

(V_{SRC} = 12V, $C_{GATE-SRC}$ = 10nF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All specs are subject to change. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Voltage Range	V_{SRC}	Operating range	3		50	V
Minimum DRN Voltage			3			V
Input Protection Voltage Range	V_{SRC}		-42		+65	V
Start-Up Time	t_{SU}	V_{SRC} rising from 0V to 12V		10		ms
INPUT SUPPLY CURRENT						
Supply Current	I_{SRC} + I_{DRN}	V_{SRC} = 12V, V_{SHDN} = high, active controller in regulation, T_A = -40°C to +27°C		30	38	µA
		V_{SRC} = 12V, V_{SHDN} = high, active controller in regulation, T_A = -40°C to +125°C		30	62	
Shutdown Current	I_{SRC}+I_{DRN}	V_{SHDN} = Low, V_{SRC} = 12V		3	6	µA
$\overline{SHDN}$ to Gate Enable Delay	t_{EN}	$\overline{SHDN}$ (low to high) to GATE starting to go high		1.5		ms

Electrical Characteristics (continued)

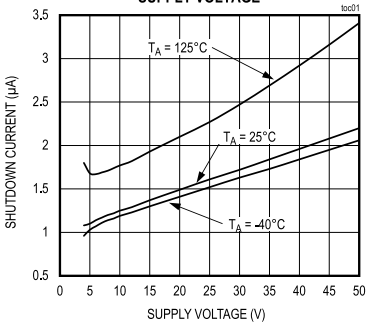
(V_{SRC} = 12V, $C_{GATE-SRC}$ = 10nF, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All specs are subject to change. (*Note 1*))

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
$\overline{SHDN}$ Logic-High Input Voltage	V_{IH}		1.5			V
$\overline{SHDN}$ Logic-Low Input Voltage	V_{IL}				0.4	V
$\overline{SHDN}$ Input Current			-120		+120	nA
GATE OUTPUT VOLTAGE						
Maximum GATE to SRC Driver Voltage	V_{GS}	V_{SD}>=30mV		11		V
SRC to DRN Regulation Voltage	V_{SD}	V_{SRC} = 12V, GATE drive is unsaturated.	10	20	30	mV
GATE Fast Pull Down Current				300		mA
GATE Fast Pull Up Current				300		mA
REVERSE CURRENT THRESHOLD						
Reverse-Current Threshold	V_{REV_TH}	Reverse current threshold is detected by the difference in voltage between DRN and SRC.	4	10	19	mV
SRC-DRN Fast Pull up Threshold			52	75	102	mV
Reverse Current Blocking Time	t_{REV}	Step (V_{SRC}- V_{DRN}) from +130mV to -70mV V_{GATE} -V_{SRC} < 1V		0.8	1.42	µs
GATE Turn-On Delay Time		Step (V_{SRC}- V_{DRN}) from -70mV to +130mV, V_{GATE} -V_{SRC} >5V		0.7	1.42	µs
Boost Output Regulation Voltage		V_{SRC} = 12V	8	11	16	V
Boost Regulator Internal FET Current Limit			75	100	135	mA
Boost Regulator Internal FET RDSON				2		Ω
FETOK, PG Leakage Current		FETOK and PG deassert	-150		+150	nA
GATE-SRC Voltage For Negative SRC		V_{SRC} = -42V		0.3		V
SRC Current For Negative SRC		V_{SRC} = -42V	-100			µA

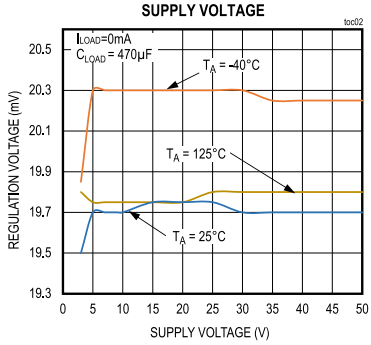
Note 1: All devices are 100% production tested at T_A = +25°C. Specifications over temperature are guaranteed by design.

Typical Operating Characteristics

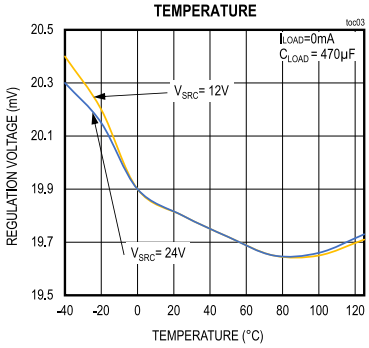
SHUTDOWN CURRENT VS SUPPLY VOLTAGE



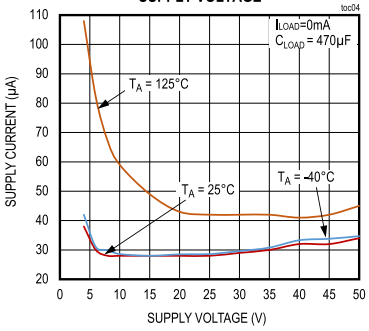
REGULATION VOLTAGE VS SUPPLY VOLTAGE



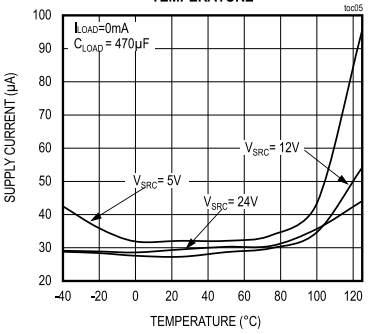
REGULATION VOLTAGE VS TEMPERATURE



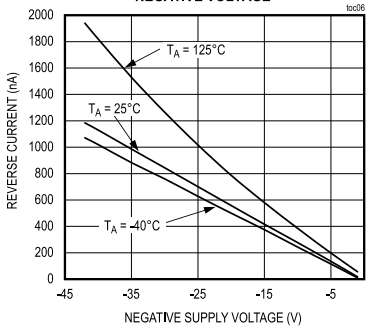
SUPPLY CURRENT VS SUPPLY VOLTAGE



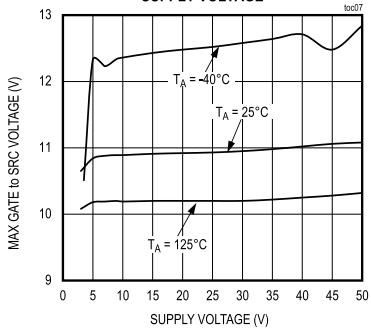
SUPPLY CURRENT VS TEMPERATURE



REVERSE CURRENT VS NEGATIVE VOLTAGE

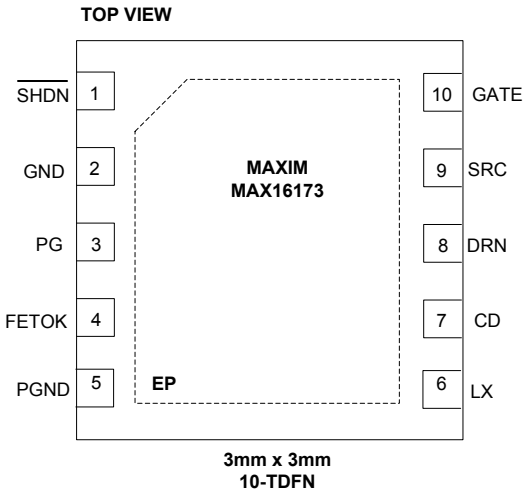


MAX GATE to SRC VOLTAGE VS SUPPLY VOLTAGE



Pin Configuration

MAX16173

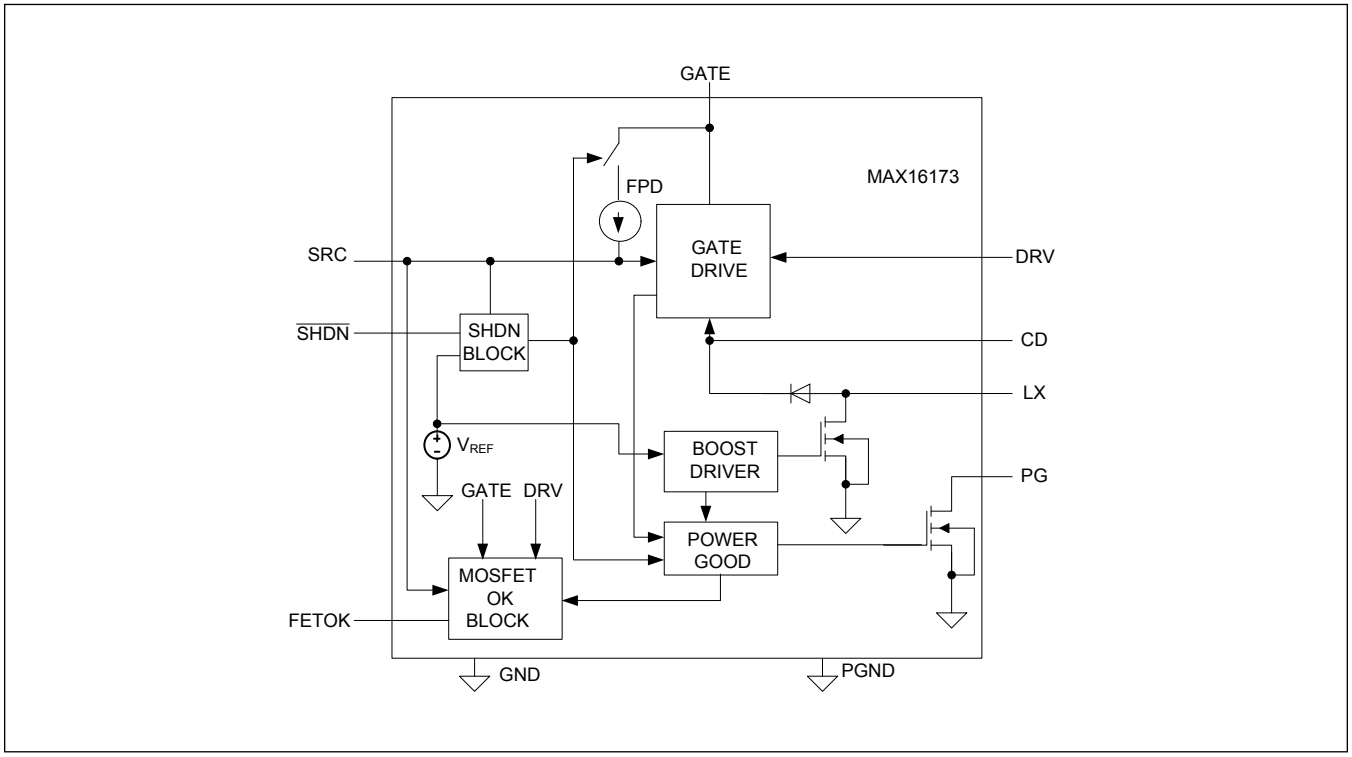


Pin Description

PIN	NAME	FUNCTION
1	$\overline{\text{SHDN}}$	Active-Low Shutdown Input. Drive $\overline{\text{SHDN}}$ low to disable the gate drive and the boost regulator. Drive $\overline{\text{SHDN}}$ high to enable the gate drive and the boost regulator.
2	GND	Ground.
3	PG	Open Drain, Active-High, Power Good Output. Requires external pullup resistor when used.
4	FETOK	Open Drain, Active-High Output. Requires external pullup resistor whether it is used or not. FETOK pulls low when the MAX16173 detects a MOSFET failure during self diagnostic test.
5	PGND	Power Ground
6	LX	Boost Converter Switching Node. Connect an inductor between DRN and LX.
7	CD	Boost Reservoir Capacitor Connection. Connect a cap between CD and DRN.
8	DRN	Drain Voltage Sense and Supply Voltage. The voltage sensed at this pin is used to control the external MOSFET gate. It also provides current to the MAX16173 internal circuitry. Connect this pin as close as possible to the drain of the external n-channel MOSFET.
9	SRC	Source Connection. Connect SRC to the source pin of the external n-channel MOSFET.
10	GATE	Gate Driver Output. Connect GATE to the gate of the external n-channel MOSFET.
-	EP	Exposed Pad. Connect EP to a contiguous ground plane. Do not use as the only ground connection in the system.

Functional Diagrams

Internal Block Diagrm



Detailed Description

Input Voltage Range

The MAX16173 operates over a wide supply voltage range of 3V to 50V while protecting itself against an input-transient range of -42V to +65V. The MAX16173's wide protection range helps minimize power dissipation in TVS diodes used for extended protection at the input. When the input transient exceeds the maximum operating voltage of 50V, the MAX16173 disables the gate to prevent gate voltage from exceeding its absolute maximum ratings.

Ideal Diode Reverse-Current Protection

The MAX16173 triggers reverse-voltage protection to prevent reverse-current flow after the input falls 10mV lower than the output. See Electrical Characteristics for more detail. Disabling the gate drive in such a short time helps prevent reverse-current flow from the holdup capacitor at the output into the source, thus preventing damage to the battery and effectively increasing system runtime. See Figure 1 for more detail.

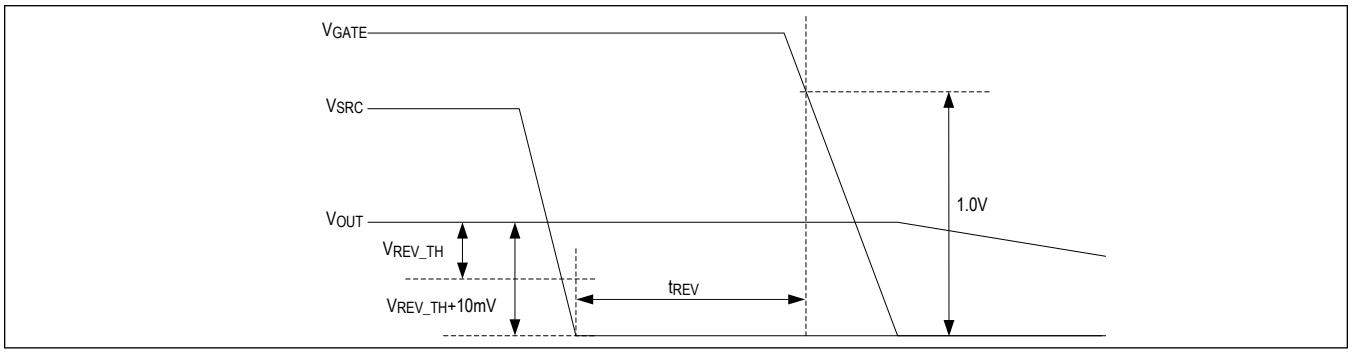


Figure 1. Reverse Voltage vs. GATE Response Timing Characteristics

Reverse-Voltage Protection

The MAX16173 integrates reverse-voltage protection, thus preventing damage to the downstream circuitry caused by battery reversal or negative transients. The MAX16173 withstands a reverse voltage to -42V without damage to itself or the load. During a reverse-voltage condition, an internal 2.5MΩ resistor between GATE and SRC pulls GATE to SRC to keep the MOSFET off and isolate the load from the source.

Active Rectifier

When $V_{SRC} < V_{DRN} + 20mV$, the MAX16173's GATE pin is driven to low and reduces external MOS's conduction until the V_{SRC} is higher 20mV than the V_{DRN} (this is the regulation operation). When $V_{SRC} < V_{DRN} – 10mV$, the MAX16173's GATE pin is shorted to SRC fast through a small resistance to turn MOS off (this is the reverse protection), and when $V_{SRC} > V_{DRN} + 75mV$, the MAX16173's GATE pin is driven to its highest point as CD voltage to turn MOS on fully until V_{SRC} is not higher 75mV than V_{DRN}, and then the MAX16173 is back to regulation operation. When the V_{SRC} is an AC wave input, the MAX16173 works alternately between these three modes and achieves the active rectifier function.

Aux Boost Regulator

The aux boost regulation provides the swing voltage range for GATE drive, and it can convert DRN voltage to a higher CD output voltage. Boost regulation is achieved by turning an internal low side switch on or off, which draws charge current through the external inductor. The discharge current of the inductor is discharged into the output CD capacitor through an internal or external Schottky diode. When the CD-DRN voltage falls down to its nominal value of 11V (typ), the low side switch of boost regulation is turned on until the current of the inductor rises to a current limit of 100mA, then the inductor discharges to CD until its current falls to zero. The low side switch turns on unless the CD-DRN voltage has reached its nominal value. Its switching frequency is not fixed and depends on the GATE's load, DRN voltage, and leakage current of the external diode.

MOSFET Diagnostic Test

If a reverse condition does not exist, the MAX16173 initiates a diagnostic procedure to check the health of the power MOSFET after power-up or shutdown recovery; otherwise, it waits until the reverse condition is removed. Before the GATE drive is enabled, the MAX16173 performs the initial test to ensure that the voltage across the source and drain of the external FET is between 0.2V and 2V. Once the gate is enabled, the MAX16173 performs another test to ensure that the voltage across the source and drain of the external MOSFET is lower than 0.2V. If the results of both tests are okay, then the MAX16173 keeps the FETOK high; otherwise, it pulls FETOK low to indicate a FET fault. FETOK is an open-drain output to indicate external FET health condition, and requires external pull-up whether it is used or not.

PG Output

The MAX16173 has a power-good open-drain output that is high-impedance if no fault conditions are present. The power-good function is activated after power-on reset. PG asserts low during shutdown mode, when V_{DRN} falls below 90% of V_{SRC}, or when the output voltage of aux boost regulator V_{CD} is lower than V_{DRN} + 2V.

$\overline{\text{SHDN}}$ Input

A logic input ($\overline{\text{SHDN}}$) enables/disables the gate drive of the MAX16173 during normal operation. The MAX16173 enables the gate in 1.5ms (typ) when $\overline{\text{SHDN}}$ is forced high. When SHDN is forced low, the MAX16173 enters shutdown mode, the aux boost regulator and GATE driver are disabled, and the GATE goes down. Upon entering shutdown mode, the power flows from the source to the load through the body diode of the nFET, but the shutdown current of the part remains at a low 3µA (typ). This helps support low-power system operation while extending battery life due to the MAX16173's low shutdown current consumption. $\overline{\text{SHDN}}$ has an internal pulldown resistor to ground and cannot be left floating for normal operation.

Overvoltage

The MAX16173 detects SRC an overvoltage condition when V_{SRC} exceeds the maximum of Input Voltage Range. In an overvoltage condition, the aux boost regulator is disabled, GATE is pulled to SRC, and the external MOSFET is turned off. PG asserts low because V_{CD}, the output of aux boost regulator, falls down to VDRN. Thus for the typical operating circuit, the load current only flows through the body diode of external MOSFET.

Applications Information

Component Selection

Input Capacitor and Output Capacitor

A minimum 0.22µF input capacitor is recommended for the supply of the MAX16173. The output capacitors include the C_{OUT} and the C_{LOAD} capacitors. The C_{OUT} capacitor is used to bypass the AUX boost supply and DRN supply, and a low ESR, 1.0µF, ceramic capacitor is recommended. It is also recommended to be closed to the DRN pin. The C_{LOAD} is used on the output for many reasons, such as power interruption, micro cut, AC Rectifier, to hold the output, and to reduce the ripple voltage of output. The ripple voltage V_{RIPPLE} behind the rectification mainly depends on C_{LOAD}, AC frequency, AC amplitude, and load current I_{LOAD}. Figure 2 shows waveforms for the rectification of a sine SRC input. The remaining ripple voltage V_{RIPPLE} can be considered as a triangle wave to simplify the calculation.

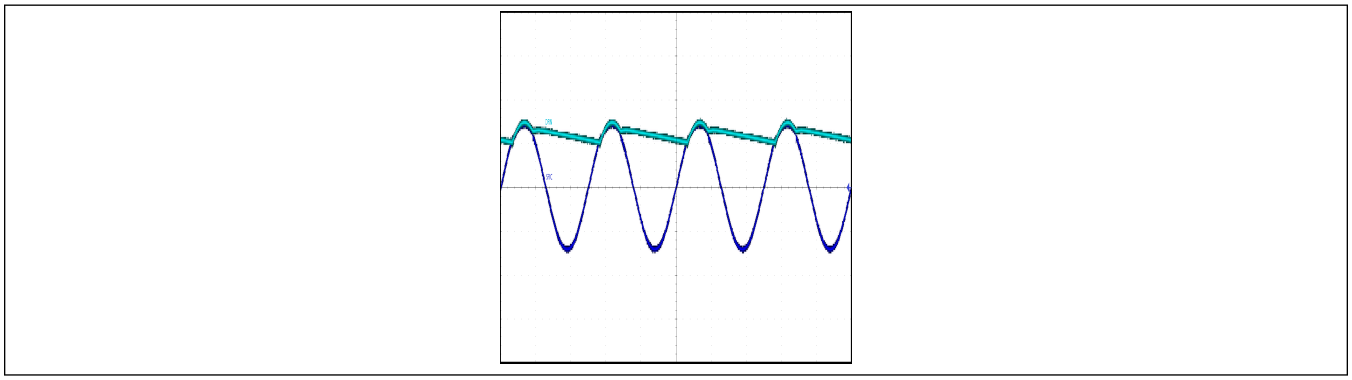


Figure 2. Rectification Waveforms of a Sinusoidal Input

The duty time proportion in a period is approximately:

$$\frac{V_{RIPPLE}}{4V_{AC}}$$

where:

V_{RIPPLE} is the ripple voltage of output

V_{AC} is the amplitude of the sine input

Since the reverse response also discharges C_{LOAD} partly, the necessary minimum capacitance C_{LOAD} can be calculated approximately from:

$$C_{LOAD} \approx \frac{4V_{AC} - V_{RIPPLE}}{4V_{AC}fV_{RIPPLE}} I_{LOAD} + \frac{I_{REV}t_{REV}}{V_{RIPPLE}}$$

where:

I_{REV} is the reverse current, and its maximum to trigger the reverse response is calculated from: $\frac{V_{REV\_TH}}{R_{DS}}$

V_{REV_TH} is the Reverse-Current Threshold

R_{DS} is the resistance of external MOSFET

t_{REV} is the reverse current response time

V_{AC}, V_{RIPPLE} and V_{REV_TH} are in volts, the ripple frequency f in hertz, I_{LOAD} and I_{REV} in amp, and C_{LOAD} in farad.

Note that the ESR of C_{LOAD}, inductance of loader, and source resistance of supply also increase V_{RIPPLE} accordingly, especially at high frequencies. Since the AC rectification is a discontinuous loader for power supply, load regulation and

output current ability of the power supply should have full performance to meet the target frequency of AC rectification. Otherwise, the charging duration and reverse response time is lengthened, the sine SRC input wave is deformed, and V_{RIPPLE} is increased, which is more apparent at high frequencies.

Inductor Selection

The boost regulator is designed to work with a 100µH to 220µH inductor that depends the supply voltage; if the supply is the max 50V, then 220µH is recommended and if the supply is 12V, then 100µH is acceptable. The saturation current of the inductor should be more than the boost regulator internal FET current limit maximum value, which is recommend as 150mA rated minimum.

Diode Selection for Boost

The boost regulator of MAX16173 requires an external diode for operation under high temperatures and high supply voltage. A Schottky diode is required for applications due to its low forward voltage drop and short reverse recovery time. Make sure that this Schottky can deliver the peak boost current with a <0.4V forward voltage, and that the reverse leakage current is as small as possible (less than 50µA is recommended).

MOSFET Selection

MOSFET selection is critical to designing a proper protection circuit, and several factors must be considered: drain-to-source voltage rating, gate capacitance, on-resistance ($R_{DS(ON)}$), peak power dissipation capability, and the average power dissipation limit.

The drain-to-source voltage rating must be higher than the maximum reverse voltage from DRN to SRC that might be applied to the application circuit.

The gate capacitance is related to the response time of turn on and turn off, MOSFETs with more gate capacitance tend to respond more slowly.

The MOSFET's on-resistance ($R_{DS(ON)}$) affects the forward voltage drop and power dissipation for the high load application and the maximum load current for the regulator light load application.

Since all load current goes through the external MOSFET, the $R_{DS(ON)}$ must be low enough to limit the MOSFET power dissipation during normal operation. Power dissipation during normal operation can be calculated using this formula:

$P_d = (I_{LOAD})2 \times R_{DS(ON)}$

where P_d is the power dissipated in each MOSFET and I_{LOAD} is the average load current.

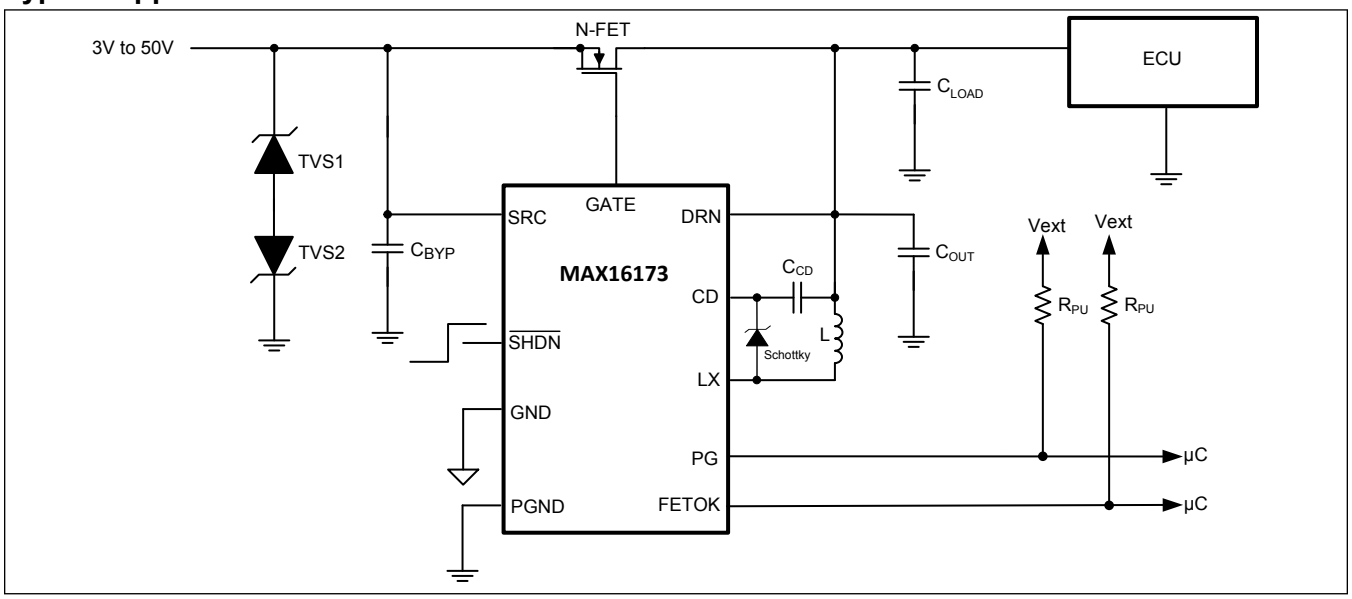
Layout Recommendations

To optimize device operation, use the following recommendations:

- Bypass the input voltage (SRC) to ground with a capacitor connected as close as possible between the input and ground pins.
- Minimize trace length and impedance when connecting SRC and DRN to the source and drain pins of the external MOSFET, respectively.
- Connect GATE to the gate of the external MOSFET directly with as few traces and vias as possible in between.
- Minimize stray capacitance between GATE and the gate of the MOSFET to minimize gate response time fault conditions.
- For high-current applications, minimize IR losses and heat dissipation by mounting the appropriate heat sink, air-flow, and low-resistance traces between the source and load.
- Connect the exposed pad to the ground pin of the IC and do not use the exposed pad as the only ground connection.

Typical Application Circuits

Typical Application Circuit



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX16173ATB/VY+T	-40°C to +125°C	10-TDFN

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

/V denotes an automotive qualified part.

Y = Side-wettable package.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	5/22	Release for Market Intro	—