Click here for production status of specific part numbers.

MAX14828

Low-Power, Ultra-Small IO-Link Device Transceiver

General Description

The MAX14828 integrates the high-voltage functions commonly found in industrial sensors. The MAX14828 features one ultra low-power driver (C/Q) with active reverse-polarity protection. An auxiliary digital input is provided to allow firmware updates through a UART interface. Transient protection is simplified due to high voltage tolerance allowing the use of micro TVS.

The device features a flexible control interface. Pin-control logic inputs allow for operation with switching sensors that do not use a microcontroller. For sensors that use a microcontroller, an SPI interface is available with extensive diagnostics. For IO-Link operation, a UART interface is provided, allowing interfacing to the microcontroller UART. Finally, a multiplexed UART/SPI option allows using one serial microcontroller interface for shared SPI and UART interfaces.

The device includes on-board 3.3V and 5V linear regulators for low-noise analog/logic supply rails.

The MAX14828 is available in a (4mm x 4mm) 24-pin TQFN package and a (2.5mm x 2.5mm) wafer-level package (WLP) and is specified over the extended -40°C to +125°C temperature range.

Applications

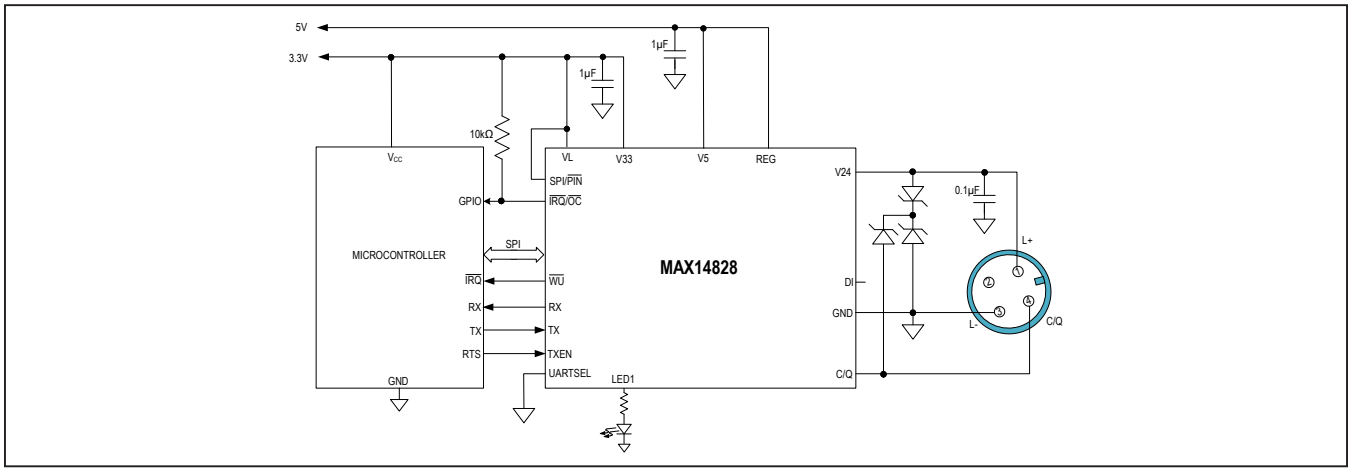
- Industrial sensors
- IO-Link sensors and actuators
- Safety applications

Benefits and Features

- Low Power Dissipation for Small Sensors
  - 1.2Ω (typ) Driver On-Resistance
  - 50mW (typ) Power Dissipation When Driving 100mA Load
- High Configurability and Integration Reduce SKUs
  - Auxiliary 24V Digital Input
  - Selectable Driver Current: 50mA to 250mA
  - SPI or Pin-Control Interface for Configuration and Monitoring
  - Multiplexed SPI/UART Interface Option
  - 5V and 3.3V Linear Regulators
  - Optional External Transistor Supports Higher Regulator Loads
  - Integrated LED Drivers
  - Pin and Software Compatible to MAX14827A
- Robust Communication
  - 65V Absolute Maximum Ratings on Interface and Supply Pins Allows for Flexible TVS Protection
  - Glitch Filters for Improved Burst Resilience and Noise
  - Thermal Shutdown
  - Hot-Plug Supply Protection
  - Reverse Polarity Protection of All Sensor Interface Inputs/Outputs
  - -40°C to +125°C Operating Temperature Range

***Ordering Information* appears at end of data sheet.**

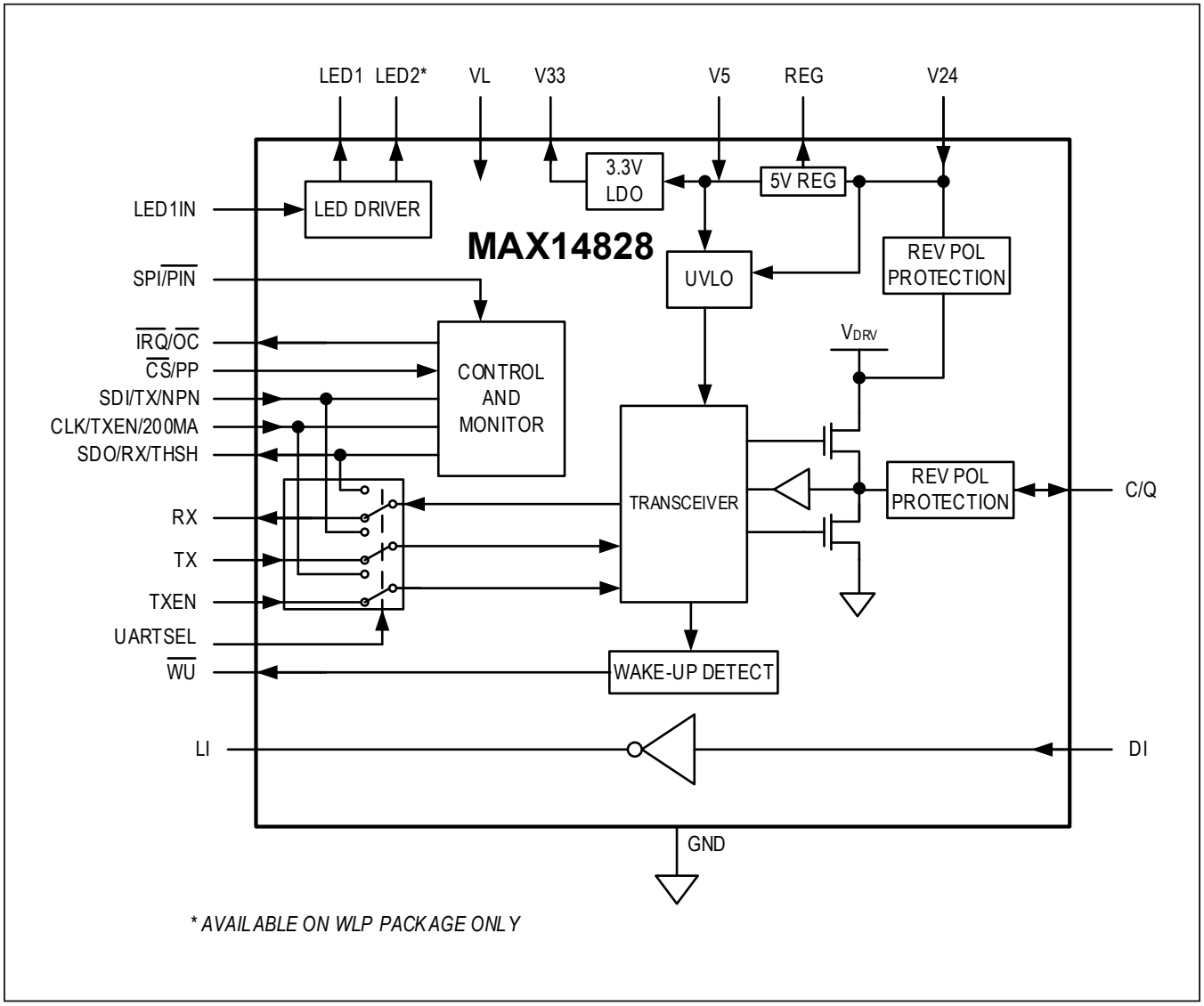
Typical Operating Circuit



IO-Link is a registered trademark of Profibus User Organization (PNO).
SPI is a trademark of Motorola, Inc.

maxim integrated™

Functional Diagram



Absolute Maximum Ratings

(All voltages referenced to GND, unless otherwise noted.)
V24 .....-70V to +65V
REG.....-0.3V to (V_5 + 16V)
V5, VL.....-0.3V to +6V
V33 .....-0.3V to (V_5 + 0.3V)
C/Q, DI ..... MIN: Larger of -70V and (V_{24} - 70V) to MAX: the lower of +70V and (V_{24} + 70V)
Logic Inputs:
$\overline{CS}$/PP, TXEN, TX, LED1IN, UARTSEL, CLK/TXEN/200MA, SPI/$\overline{PIN}$, SDI/TX/NPN .....-0.3V to (V_L + 0.3V)
Logic Outputs:
RX, LI, $\overline{WU}$, SDO/RX/THSH .....-0.3V to (V_L + 0.3V)
$\overline{IRQ/OC}$.....-0.3V to +6V
LED1, LED2 .....-0.3V to (V_5+0.3V)
Continuous Current Into GND and V24 .....±1A
Continuous Current Into C/Q.....±500mA
Continuous Current Into V5 and REG.....±100mA
Continuous Current Into Any Other Pin.....±50mA
Continuous Power Dissipation
TQFN (derate 27.8mW/°C above +70°C).....2222mW
WLP (derate 22.7mW/°C above +70°C) 1816mW
Operating Temperature Range..... -40°C to +125°C
Maximum Junction Temperature .....Internally Limited
Storage Temperature Range..... -65°C to +150°C
Soldering Temperature (reflow, TQFN and WLP) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 24 TQFN	
Package Code	T2444+4
Outline Number	**21-0139**
Land Pattern Number	**90-0022**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	36°C/W
Junction to Case (θ_{JC})	3°C/W

PACKAGE TYPE: 25 WLP	
Package Code	W252L2+1
Outline Number	**21-0787**
Land Pattern Number	Refer to **Application Note 1891**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	44°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

DC Electrical Characteristics

(V_{24} = 9V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{GND} = 0V; REG unconnected, all logic inputs at V_L or GND; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
V_{24} Supply Voltage	V_{24}			9		36	V
V_{24} Undervoltage Lockout Threshold	V_{24UVLO}	V_{24} rising		6	7.8	9	V
		V_{24} falling		6	7.2	9	
V_{24} Undervoltage Lockout Threshold Hysteresis	V_{24UVLO_HYST}				570		mV
V_{24} Supply Current	I_{24}	V_5 powered externally, REG is unconnected	C/Q disabled (CQ_Dis = 1)		0.14	0.5	mA
			C/Q in push-pull configuration, CL[10] = 11, C/Q is high, no load on C/Q		0.5	0.75	
			C/Q in push-pull configuration, CL[10] = 11, C/Q is low, no load on C/Q		0.58	0.85	
V_{24} Low-Voltage Warning Threshold	V_{24W}			14.5	16.5	18	V
V_5 Supply Voltage				4.5		5.5	V
V_5 Undervoltage Lockout Threshold	V_{5UVLO}	V_5 rising		2.8	3.5	4.5	V
		V_5 falling		2.8	3.45	4.5	
V_5 Supply Current	I_{5_IN}	External 5V applied to V_5, REG is unconnected, no load on LED1 or LED2	C/Q disabled (CQ_Dis = 1), V33 disabled (V33_Dis = 1)		0.54	0.85	mA
			C/Q in push-pull configuration, CL[10] = 11, C/Q is high, V33 enabled, no load on C/Q or V33		0.93	1.4	
			C/Q in push-pull configuration, CL[10] = 11, C/Q is low, V33 enabled, no load on C/Q or V33		1.0	1.4	
V_L Logic-Level Supply Voltage	V_L			2.5		5.5	V
V_L Undervoltage Threshold	V_{LUVLO}			0.9	1.7	2.4	V
V_L Logic-Level Supply Current	I_L	All logic inputs at V_L or GND, all logic outputs unconnected			0.25	3	µA

DC Electrical Characteristics (continued)

(V_{24} = 9V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{GND} = 0V; REG unconnected, all logic inputs at V_L or GND; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
5V LINEAR REGULATOR/CONTROLLER (V5)							
V_5 Output Voltage	V_5	REG = V_5, no load on V5, 9V ≤ V_{24} ≤ 60V		4.75	5.00	5.25	V
Load Regulation	ΔV_{5_LDR}	REG = V_5, 0mA < I_{LOAD} < 30mA, V_{24} = 24V			0.02	0.2	%
Line Regulation	ΔV_{5_LNR}	REG = V_5, I_{LOAD} = 1mA, V_{24} from 9V to 60V			0.01	4	mV/V
REG Output Current	I_{REG}	Internal regulator or external NPN				30	mA
V_{24} REG Dropout Voltage	ΔV_{REG}	V_{24} = 9V, V_5 = 4.5V, I_{REG} = 5mA			2.35		V
REG Open Voltage	V_{REG_OPN}	V_{24} = 60V, V_5 = 4.5V, no load on REG		10	13	16	V
V_5 Capacitance	CV_5	Allowed capacitance on V_5, REG connected to V_5 (Note 2)		0.8	1	2	µF
3.3V LINEAR REGULATOR (V33)							
V33 Output Voltage	V_{33}	No load on V33		3.1	3.3	3.5	V
V33 Load Regulation	V_{33_LDR}	0mA < I_{LOAD} < 30mA		0	0.4	0.8	%
V33 Capacitance	CV_{33}	Allowed capacitance on V33, V33 enabled (Note 2)		0.8	1		µF
C/Q DRIVER							
Driver On-Resistance	R_{OH}	High-side enabled, V_{24} = 24V, CL[10] = 11, I_{LOAD} = -200mA (Note 2)			1.25	2.4	Ω
	R_{OL}	Low-side enabled, V_{24} = 24V, CL[10] = 11, I_{LOAD} = +200mA (Note 2)			1.2	2.45	
Driver Current Limit	I_{CL}	SPI/$\overline{PIN}$ = high, V_{DRIVER} = (V_{24} – 3V) or 3V, CL_Dis = 0	CL[10] = 00	50	65	82	mA
			CL[10] = 01	100	120	150	
			CL[10] = 10	200	230	275	
			CL[10] = 11	250	290	350	
		SPI/$\overline{PIN}$ = low, V_{DRIVER} = (V_{24} – 3V) or 3V	CLK/TXEN/200MA = low	100	120	150	
			CLK/TXEN/200MA = high	200	230	275	
Driver Peak Current	I_{CL_PEAK}	DC current				490	mA
C/Q Leakage Current	I_{LEAK_CQ}	C/Q driver is disabled (C/Q_Dis = 1), RX disabled (Rx_Dis = 1), V_{24} = 24V, (V_{24} - 65V) ≤ $V_{C/Q}$ ≤ +60V		-70		+10	µA
		C/Q driver enabled	NPN mode, set to high impedance (TX = low), $V_{C/Q}$ = 24V		19.2		
			PNP mode, set to high impedance (TX = high), $V_{C/Q}$ = 0V		0		
C/Q Output Reverse Current	I_{REV_CQ}	C/Q driver enabled and in push-pull configuration, V_{24} = 30V, $V_{C/Q}$ = (V_{24} + 5V) or (V_{GND} - 5V)		-100		+1000	µA

DC Electrical Characteristics (continued)

(V_{24} = 9V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{GND} = 0V; REG unconnected, all logic inputs at V_L or GND; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Weak Pulldown Current	I_{PD}	SPI/$\overline{PIN}$ = high, driver disabled (CQ_Dis = 1)	V_{DRIVER} = 5V, CQ_WPD = 1, CQ_WPU = 0	200	300	400	µA
			V_{DRIVER} = 24V, CQ_WPD = 1, CQ_WPU = 0	200	470	1000	
Weak Pullup Current	I_{PU}	SPI/$\overline{PIN}$ = high, driver disabled (CQ_Dis = 1), V_{DRIVER} = V_{24} - 5V	CQ_WPU = 1, CQ_WPD = 0	-400	-300	-200	µA
C/Q, DI RECEIVER							
Input Voltage Range	V_{IN}	For valid RX logic		V_{24} - 65		+65	V
C/Q, DI Input Threshold High	V_{TH}	C/Q driver disabled	V_{24} > 18V	11	11.8	12.5	V
			V_{24} < 18V	59	65.5	72	% of V_{24}
C/Q, DI Input Threshold Low	V_{TL}	C/Q driver disabled	V_{24} > 18V	9	9.8	10.5	V
			V_{24} < 18V	45	54.5	63	% of V_{24}
C/Q, DI Input Hysteresis	V_{HYS_CQ}	C/Q driver disabled	V_{24} > 18V		2		V
			V_{24} < 18V		11		% of V_{24}
C/Q Input Capacitance	C_{IN_CQ}	Driver disabled, weak pullup and pulldown disabled, f = 100kHz			90		pF
DI Input Capacitance	C_{IN_DI}	f = 100kHz			10		pF
C/Q Input Current	I_{IN_CQ}	C/Q driver disabled (CQ_Dis = 1), C/Q receiver enabled, V_{24} = 24V	-5V ≤ $V_{C/Q}$ ≤ (V_{24} + 5V)	-10		+30	µA
			(V_{24} - 65V) ≤ $V_{C/Q}$ ≤ +60V	-70		+70	
DI Leakage Current	I_{LEAK_DI}	DI receiver disabled (DI_Dis = 1), V_{24} = 24V, (V_{24} - 65V) ≤ V_{DI} ≤ +60V		-40		+150	µA
DI Input Current	I_{IN_DI}	DI receiver enabled, V_{24} = 24V	-5V ≤ V_{DI} ≤ (V_{24} +5V)	-10		+35	µA
			(V_{24} - 65V) ≤ V_{DI} ≤ +60V	-40		+200	

DC Electrical Characteristics (continued)

(V_{24} = 9V to 36V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{GND} = 0V; REG unconnected, all logic inputs at V_L or GND; T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC INPUTS ($\overline{CS}$/PP, TXEN, TX, LED1IN, CLK/TXEN/200MA, SPI/$\overline{PIN}$, SDI/TX/NPN)						
Logic Input Voltage Low	V_{IL}				0.2 x V_L	V
Logic Input Voltage High	V_{IH}		0.8 x V_L			V
Logic Input Leakage Current	I_{LEAK}	Logic input = GND or VL	-1		+1	µA
LOGIC OUTPUTS (RX, LI, $\overline{WU}$, $\overline{IRQ}$/$\overline{OC}$, SDO/RX/THSH)						
Logic Output Voltage Low	V_{OL}	I_{OUT} = -5mA			0.4	V
Logic Output Voltage High	V_{OH}	I_{OUT} = 5mA	V_L - 0.4			V
$\overline{IRQ}$/$\overline{OC}$ Open-Drain Leakage Current	I_{LK_OD}	$\overline{IRQ}$/$\overline{OC}$ high impedance, $\overline{IRQ}$/$\overline{OC}$ = GND or VL	-1		+1	µA
SDO Leakage Current	I_{LK_SDO}	SPI/$\overline{PIN}$ = high, $\overline{CS}$/PP = high, SDO/RX/THSH = GND or VL	-1		+1	µA
RX, LI Leakage Current	I_{LK_RX}	SPI/$\overline{PIN}$ = high, DI_Dis = 1, RX_Dis = 1, RX/LI = GND or VL	-1		+1	µA
LED DRIVERS (LED1, LED2)						
LED Output Voltage Low	V_{LEDOL}	I_{OUT} = -5mA			0.4	V
LED Output Voltage High	V_{LEDOH}	I_{OUT} = 10mA	V_5 - 0.4			V
THERMAL MANAGEMENT						
Thermal Warning Threshold	T_{WRN}	Die junction temperature rising, TempW and TempWInt bits are set		+140		°C
Thermal Warning Threshold Hysteresis	T_{WRN_HYS}	Die junction temperature falling, TempW bit cleared		15		°C
Per-Driver Thermal Shutdown Temperature	T_{SHUT_D}	Driver temperature rising, temperature at which the driver is turned off		+160		°C
Per-Driver Thermal Shutdown Temperature Hysteresis	T_{SHUT_DHYS}	Driver temperature falling		15		°C
IC Thermal Shutdown	T_{SHUT_IC}	Die temperature rising, ThShut and ThuShutInt bits are set		+170		°C
IC Thermal-Shutdown Hysteresis	T_{SHUT_ICHYS}	Die temperature falling, ThShut bit is cleared		15		°C

AC Electrical Characteristics

(V_{24} = 18V to 30V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{GND} = 0V, REG unconnected, all logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
C/Q DRIVER							
Driver Low-to-High Propagation Delay	t_{PDLH_PP}	Push-pull and PNP configuration, Figure1			0.21	0.45	µs
		NPN configuration, Figure 1			0.16		
Driver High-to-Low Propagation Delay	t_{PDHL_PP}	Push-pull and NPN configuration, Figure1			0.47	0.7	µs
		PNP configuration, Figure 1			0.28		
Driver Skew	t_{SKEW}	Push-pull configuration, Figure 1 | t_{PDLH} - t_{PDHL} |		-0.4		+0.4	µs
Driver Rise Time	t_{RISE}	Push-pull and PNP configuration, Figure 1			0.17	0.4	µs
Driver Fall Time	t_{FALL}	Push-pull and NPN configuration, Figure 1			0.17	0.4	µs
Driver Enable Time High	t_{ENH}	Push-pull and PNP configuration, Figure 2			0.19	0.5	µs
Driver Enable Time Low	t_{ENL}	Push-pull and NPN configuration, Figure 3			0.44	0.7	µs
Driver Disable Time High	t_{DISH}	Push-pull and PNP configuration, Figure 2			1.8	3	µs
Driver Disable Time Low	t_{DISL}	Push-pull and NPN configuration, Figure 3			1.5	3	µs
C/Q, DI RECEIVER (Figure 4)							
C/Q Receiver Low-to-High Propagation Delay	t_{PRLH_CQ}	SPI/$\overline{PIN}$ = high or low, CQFil = 0		0.85	1.3	2.1	µs
		SPI/$\overline{PIN}$ = high, CQFil = 1		0.2	0.3	0.5	
C/Q Receiver High-to-Low Propagation Delay	t_{PRHL_CQ}	SPI/$\overline{PIN}$ = high or low, CQFil = 0		0.85	1.3	2.1	µs
		SPI/$\overline{PIN}$ = high, CQFil = 1		0.2	0.3	0.5	
DI Receiver Low-to-High Propagation Delay	t_{PRLH_DI}			1.3	2.2	3.5	µs
DI Receiver High-to-Low Propagation Delay	t_{PRHL_DI}			1.3	2.2	3.5	
DRIVER CURRENT LIMITING							
Blanking Time	t_{CL_ARBL}	SPI/$\overline{PIN}$ = high	CL_BL[10] = 00		0.128		ms
			CL_BL[10] = 01		0.5		
			CL_BL[10] = 10		1		
			CL_BL[10] = 11		5		
		SPI/$\overline{PIN}$ = low			0.128		
Autoretry Period	t_{CL_ARP}	SPI/$\overline{PIN}$ = high, ArEn = 1 (Note 3)	TAr[10] = 00		50		ms
			TAr[10] = 01		100		
			TAr[10] = 10		200		
			TAr[10] = 11		500		

AC Electrical Characteristics (continued)

(V_{24} = 18V to 30V, V_5 = 4.5V to 5.5V, V_L = 2.5V to 5.5V, V_{GND} = 0V, REG unconnected, all logic inputs at V_L or GND, T_A = -40°C to +125°C, unless otherwise noted. Typical values are at V_{24} = 24V, V_5 = 5V, V_L = 3.3V, and T_A = +25°C, unless otherwise noted.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
WAKE-UP DETECTION (Figure 5)						
Wake-Up Input Minimum Pulse Width	t_{WUMIN}	C_L = 3nF	55	66	75	µs
Wake-Up Input Maximum Pulse Width	t_{WUMAX}		85	95	110	µs
$\overline{WU}$ Output Low Time	t_{WUL}	Valid wake-up condition on C/Q	100	200	300	µs
SPI TIMING ($\overline{CS}$/PP, CLK/TXEN/200MA, SDI/TX/NPN, SDO/RX/THSH) (Figure 6)						
Maximum SPI Clock Frequency			12.5			MHz
CLK/TXEN/200MA Clock Period	t_{CH+CL}		80			ns
CLK/TXEN/200MA Pulse-Width High	t_{CH}		40			ns
CLK/TXEN/200MA Pulse-Width Low	t_{CL}		40			ns
$\overline{CS}$/PP Fall to CLK/TXEN/200MA Rise Time	t_{CSS}		20			ns
CLK/TXEN/200MA Rise to $\overline{CS}$/PP Rise Hold Time	t_{CSH}		40			ns
SDI/TX/NPN Hold Time	t_{DH}		10			ns
SDI/TX/NPN Setup Time	t_{DS}				25	ns
Output Data Propagation Delay	t_{DO}				20	ns
SDO/RX/THSH Rise and Fall Times	t_{FT}				20	ns
Minimum $\overline{CS}$/PP Pulse	t_{CSW}				10	ns

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 2: Not production tested. Guaranteed by design.

Note 3: Autoretry functionality is not available in pin-mode.

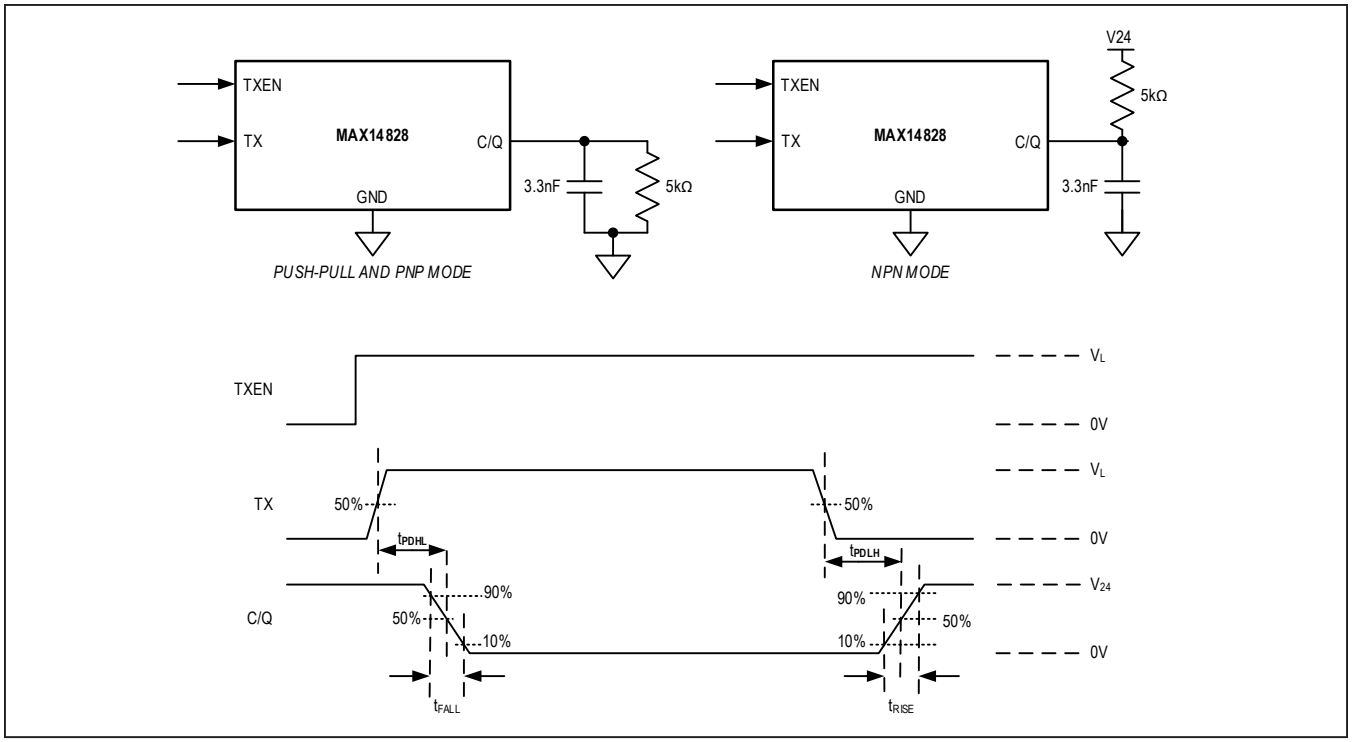


Figure 1. C/Q Driver Propagation Delays and Rise/Fall Times

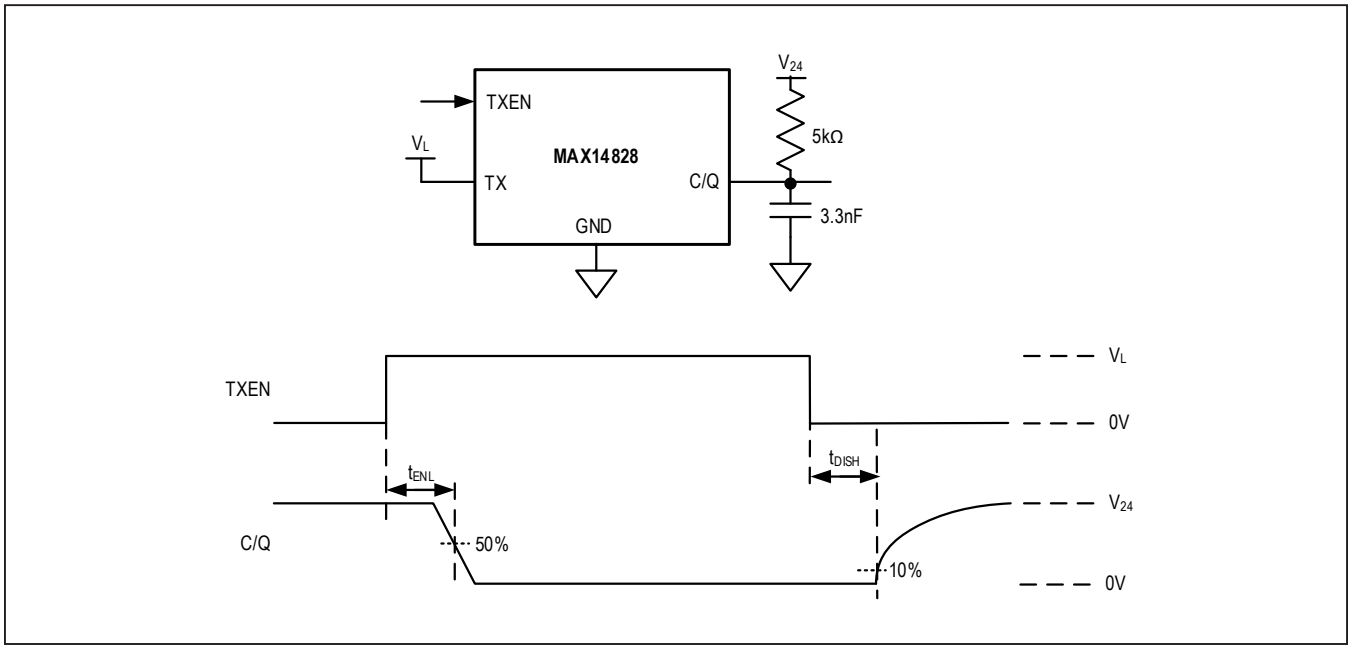


Figure 2. C/Q Driver Enable Low and Disable High Timing with External Pullup Resistor

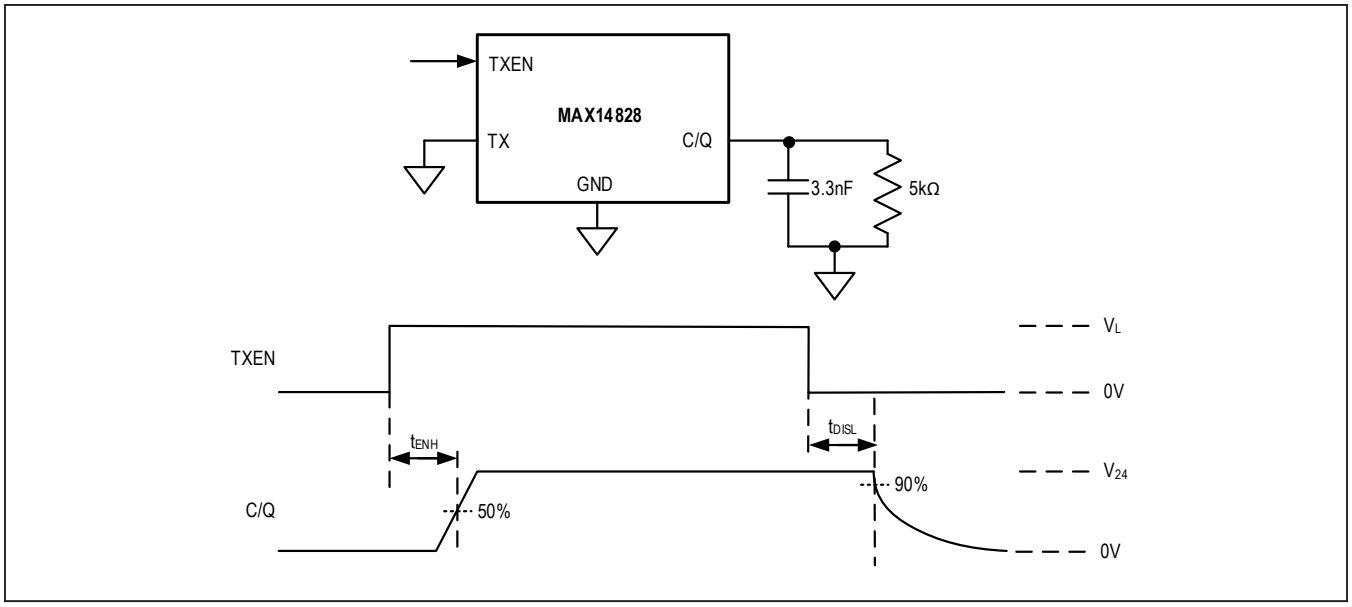


Figure 3. C/Q Driver Enable High and Disable Low Timing

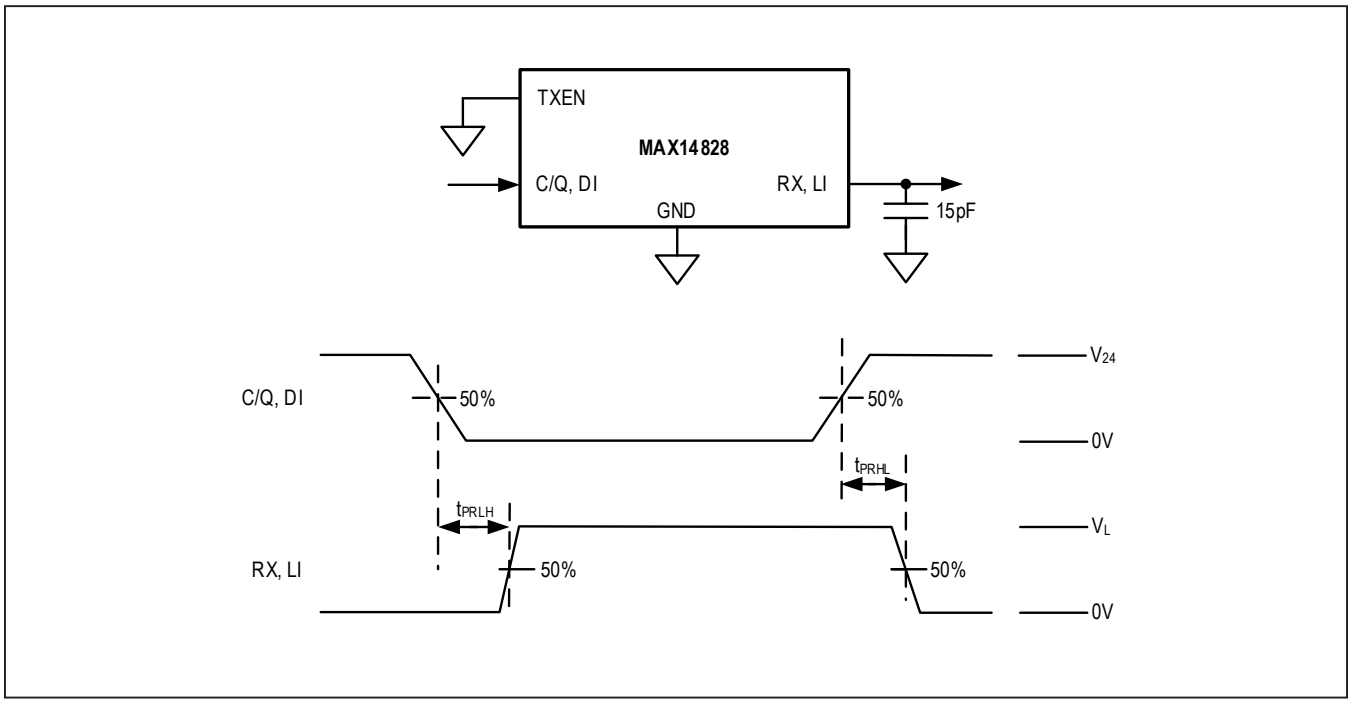


Figure 4. C/Q and DI Receiver Propagation Delays

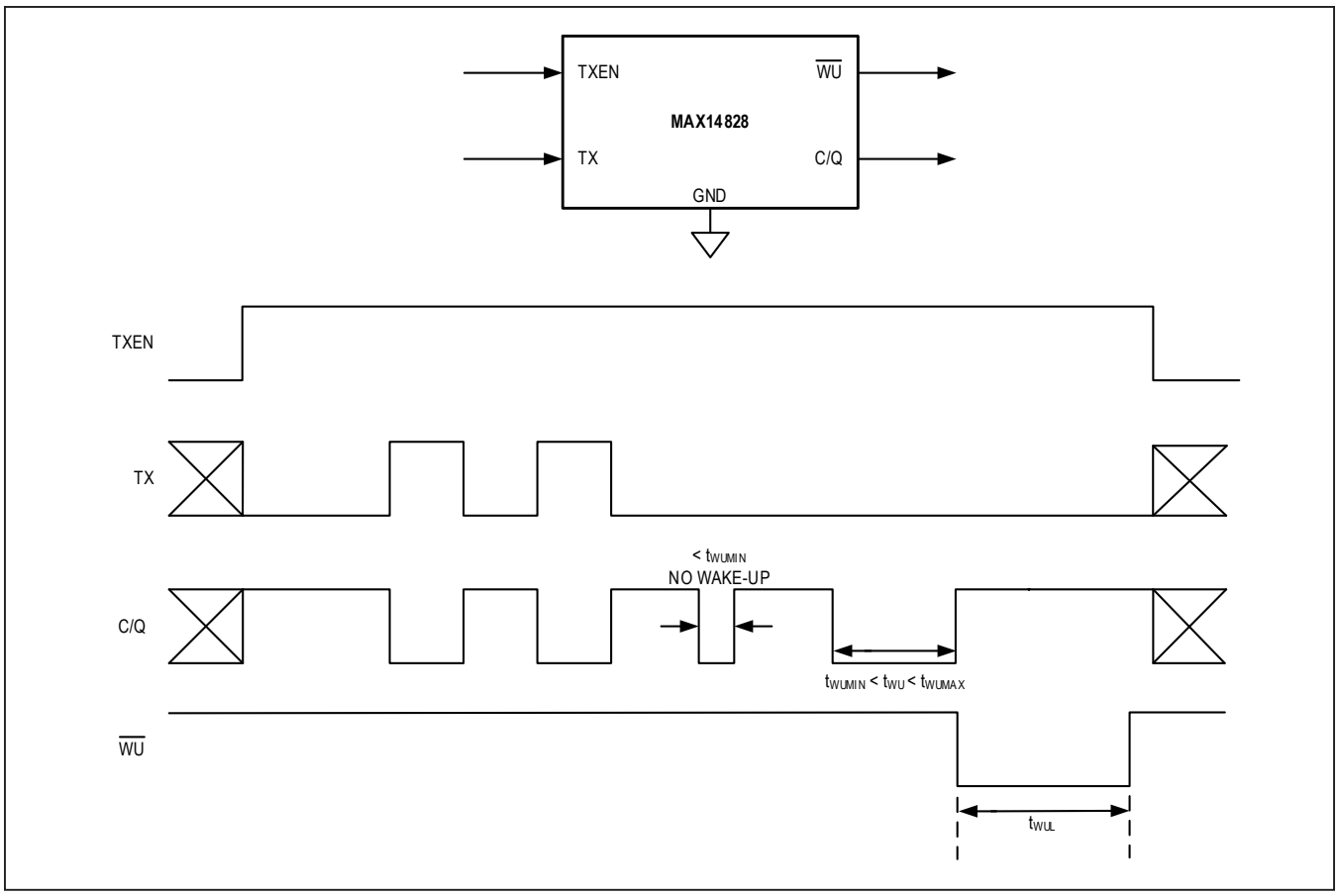


Figure 5. Wake-Up Detection Timing

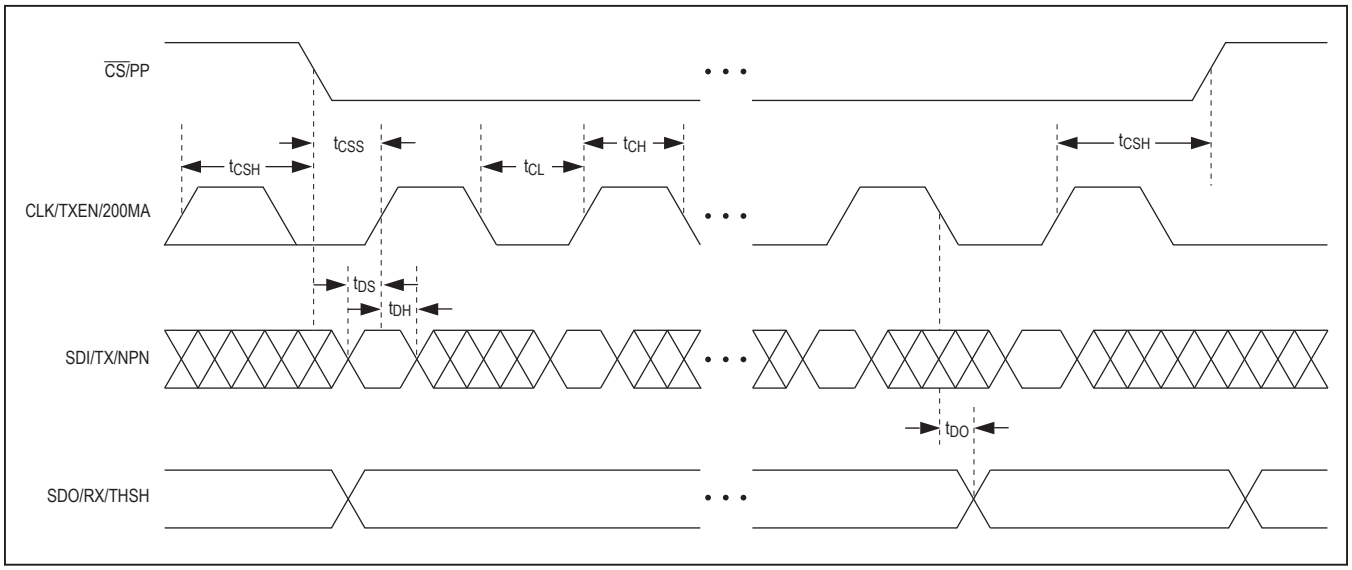
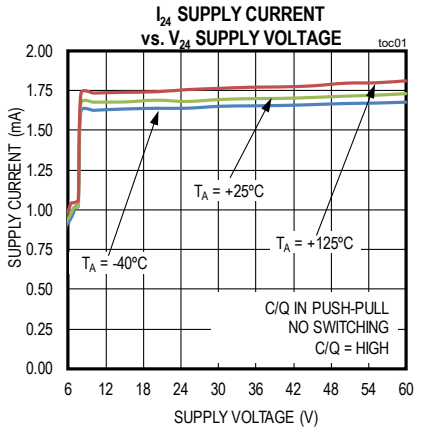
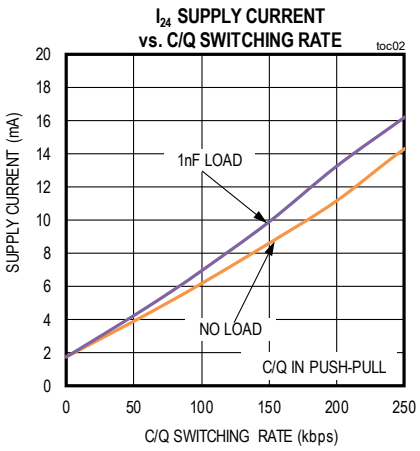


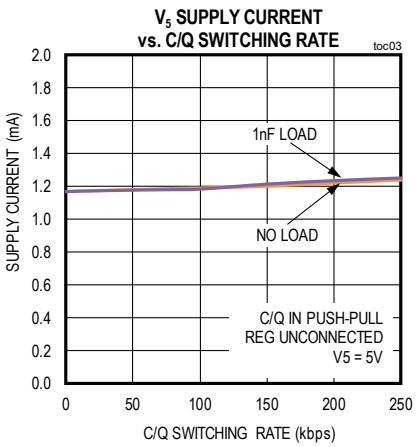
Figure 6. SPI Timing Diagram

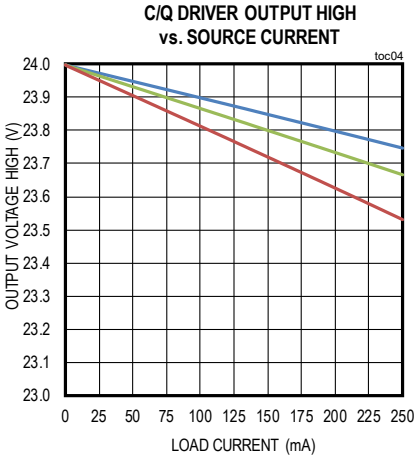
Typical Operating Characteristics

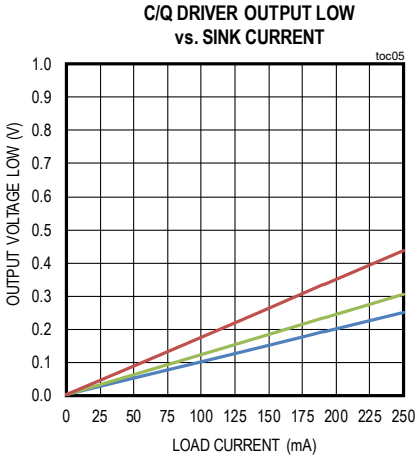
(V_{24} = 24V, V_L = V_{33}, REG is shorted to V5, C/Q in push-pull configuration, T_A = +25°C, unless otherwise noted.)

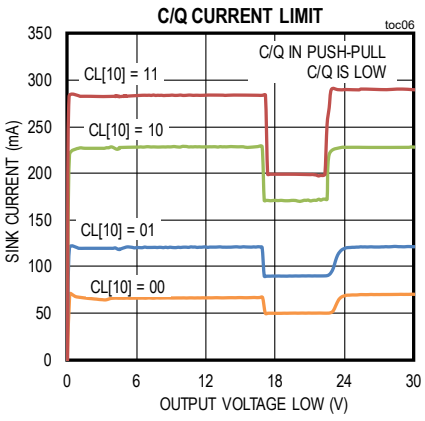


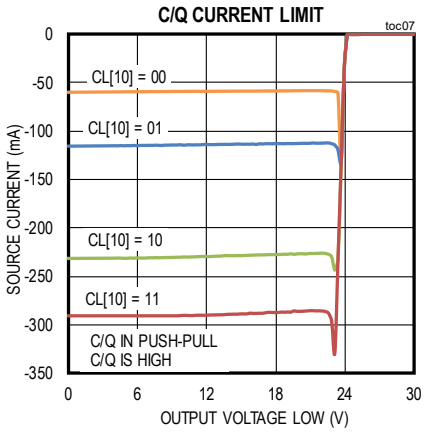








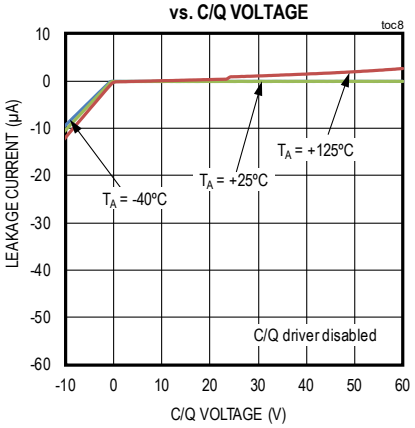




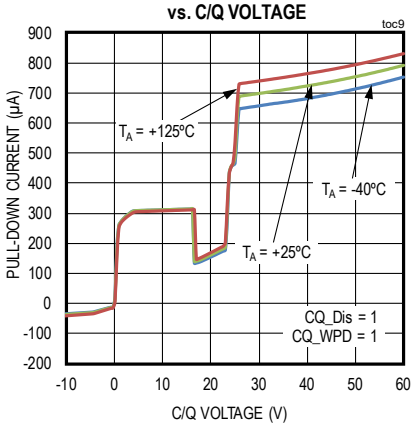
Typical Operating Characteristics (continued)

(V_{24} = 24V, V_L = V_{33}, REG is shorted to V5, C/Q in push-pull configuration, T_A = +25°C, unless otherwise noted.)

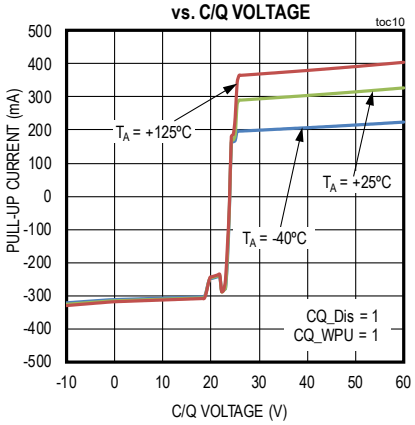
C/Q DRIVER LEAKAGE CURRENT vs. C/Q VOLTAGE



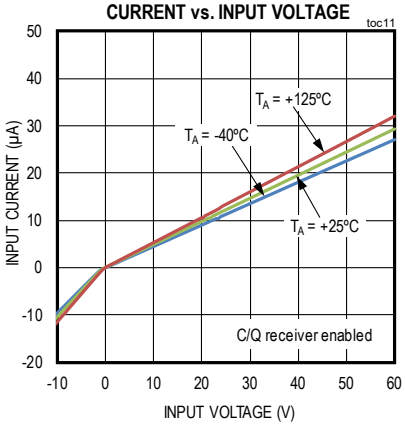
C/Q WEAK PULLDOWN CURRENT vs. C/Q VOLTAGE



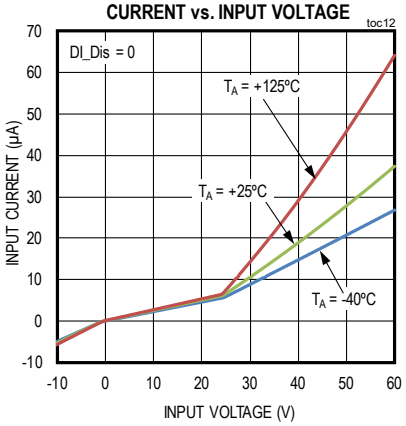
C/Q WEAK PULLUP CURRENT vs. C/Q VOLTAGE



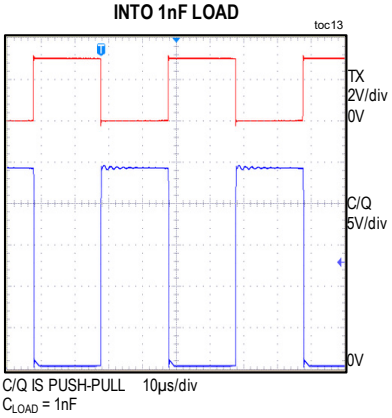
C/Q RECEIVER INPUT CURRENT vs. INPUT VOLTAGE



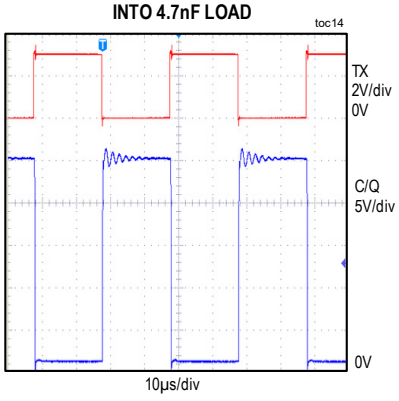
DI RECEIVER INPUT CURRENT vs. INPUT VOLTAGE



C/Q DRIVER SWITCHING INTO 1nF LOAD



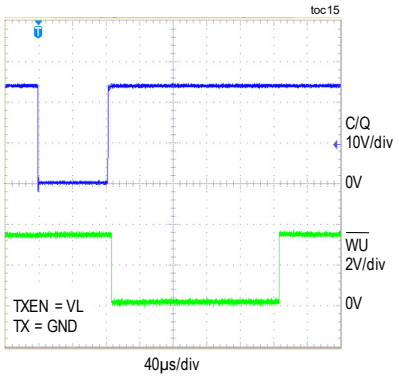
C/Q DRIVER SWITCHING INTO 4.7nF LOAD



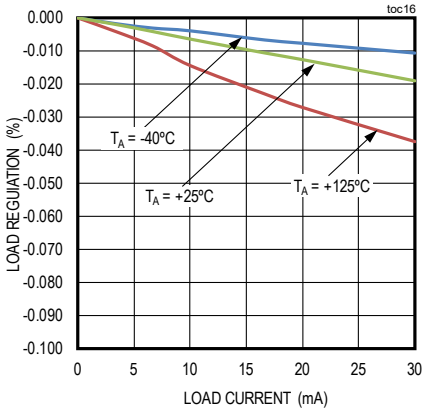
Typical Operating Characteristics (continued)

(V_{24} = 24V, V_L = V_{33}, REG is shorted to V5, C/Q in push-pull configuration, T_A = +25°C, unless otherwise noted.)

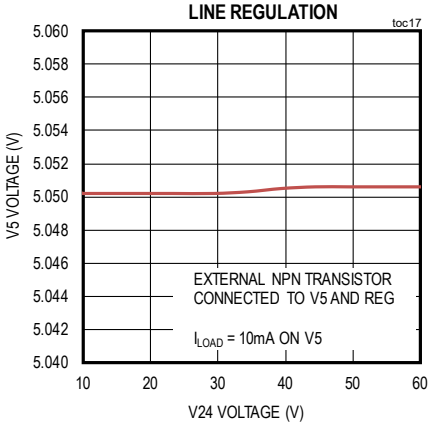
WAKE-UP DETECTION



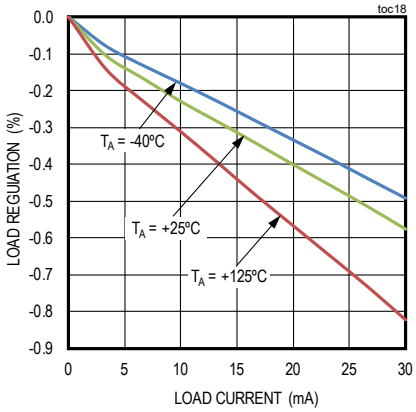
V5 LINEAR REGULATOR LOAD REGULATION



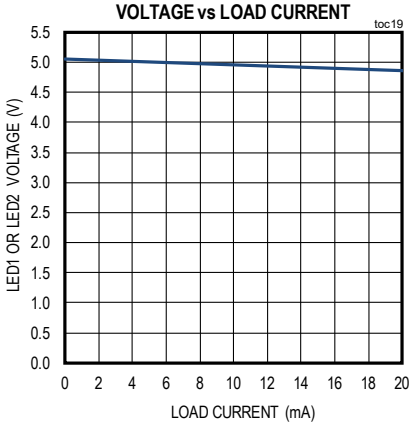
V5 LINEAR REGULATOR LINE REGULATION



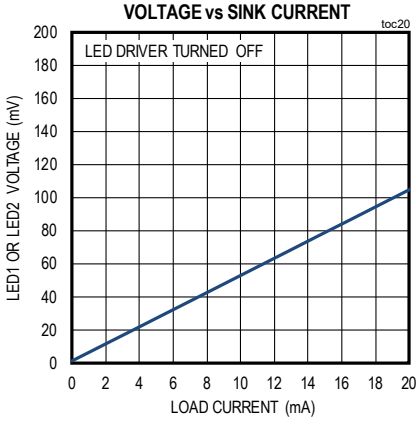
V33 LINEAR REGULATOR LOAD REGULATION



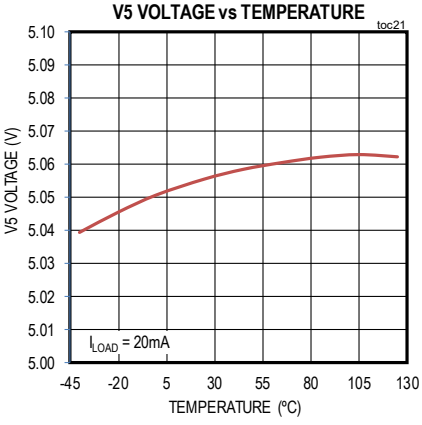
LED DRIVER OUTPUT HIGH VOLTAGE vs LOAD CURRENT



LED DRIVER OUTPUT LOW VOLTAGE vs SINK CURRENT



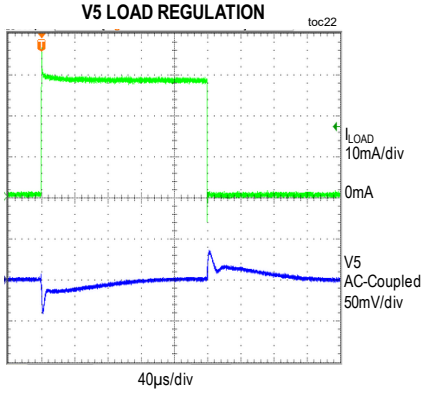
V5 VOLTAGE vs TEMPERATURE



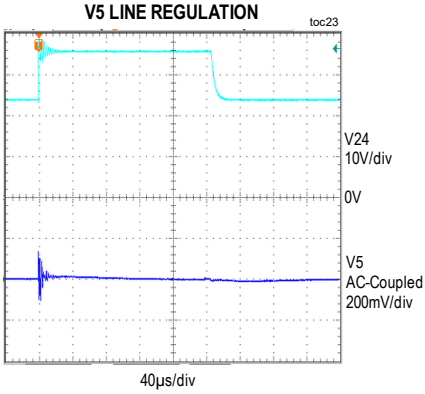
Typical Operating Characteristics (continued)

(V_{24} = 24V, V_L = V_{33}, REG is shorted to V5, C/Q in push-pull configuration, T_A = +25°C, unless otherwise noted.)

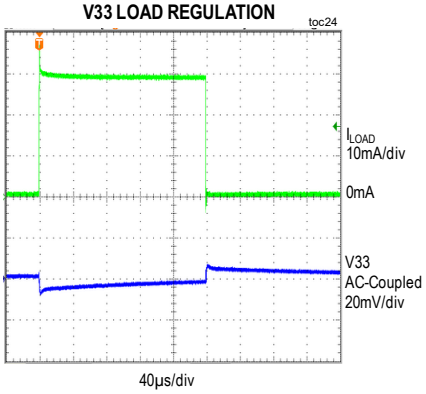
V5 LOAD REGULATION



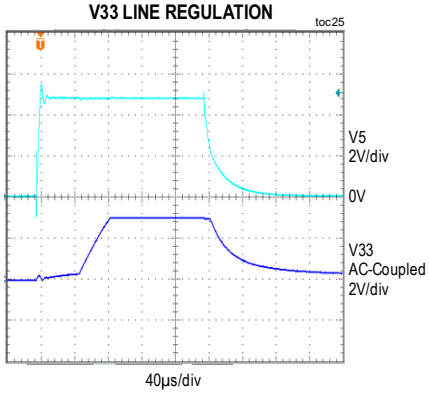
V5 LINE REGULATION



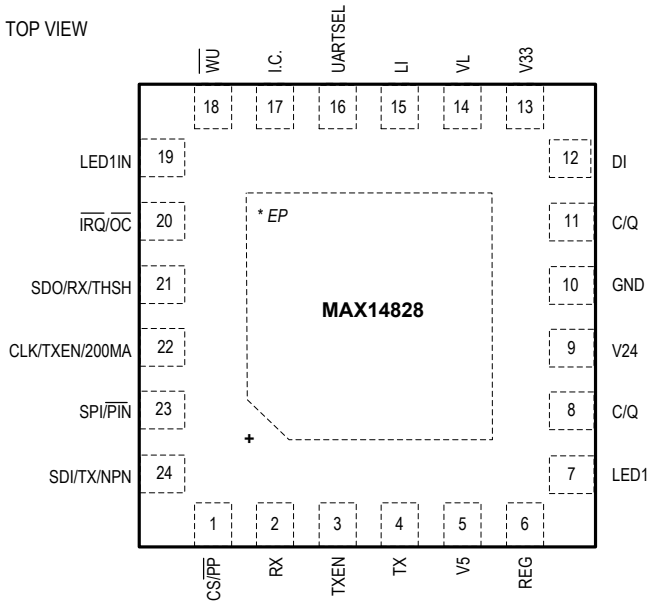
V33 LOAD REGULATION



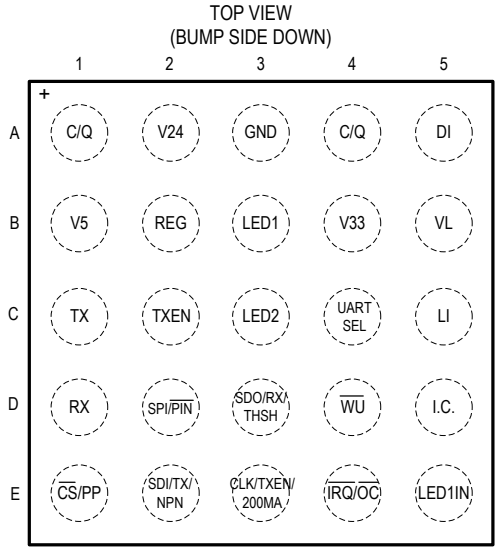
V33 LINE REGULATION



Pin Configuration



TQFN
4mm x 4mm



WLP
2.5mm x 2.5mm

Pin Description

PIN		NAME	PIN DESCRIPTION	FUNCTION		
TQFN	WLP			PARALLEL MODE (SPI/$\overline{PIN}$ = High)	MULTIPLEXED MODE (SPI/$\overline{PIN}$ = High)	PIN MODE (SPI/$\overline{PIN}$ = Low)
				UARTSEL = Low	UARTSEL = High	
1	E1	$\overline{CS}$/PP	$\overline{CS}$/PP Logic Input	SPI active-low chip-select input. Drive $\overline{CS}$/PP low to start the SPI read/write cycle. Drive $\overline{CS}$/PP high to end the SPI cycle. UART interface is enabled on RX, TX, and TXEN.	SPI chip-select and UART signal select input. When $\overline{CS}$/PP is high, the SPI interface is disabled and UART interface mode is enabled on the SDO/RX/THSH, SDI/TX/NPN, and CLK/TXEN/200MA logic pins.	Push-pull select input. Drive $\overline{CS}$/PP high to enable push-pull mode for the C/Q and DO drivers. Drive $\overline{CS}$/PP low to select PNP or NPN operation for the drivers.
2	D1	RX	C/Q Receiver Logic Output	RX is the inverse logic of C/Q. RX can be disabled with the SPI interface. RX is high impedance when Rx_Dis = 1.		RX is the inverse logic of C/Q. RX is always active.

Pin Description (continued)

PIN		NAME	PIN DESCRIPTION	FUNCTION		
TQFN	WLP			PARALLEL MODE (SPI/$\overline{PIN}$ = High)	MULTIPLEXED MODE (SPI/$\overline{PIN}$ = High)	PIN MODE (SPI/$\overline{PIN}$ = Low)
				UARTSEL = Low	UARTSEL = High	
3	C2	TXEN	C/Q Driver Enable Logic Input	Drive TXEN high to enable the C/Q driver. See Table 1.	With $\overline{CS}$/PP low and ENMPX = 0, drive TXEN high to enable C/Q.	Drive TXEN high to enable the C/Q driver. Drive TXEN low to disable the C/Q driver and enable the C/Q receiver.
4	C1	TX	C/Q Driver Communication Input	The logic on the C/Q output is the inverse logic level of the signal on the TX input. See Table 1.	With $\overline{CS}$/PP low and ENMPX = 0, the logic on the C/Q output is the inverse logic level of the signal on the SDI/TX/NPN input. Signals on TX are ignored. See the Mode Selection table.	The logic on the C/Q output is the inverse logic level of the signal on the TX input when TXEN is high.
5	B1	V5	5V Power-Supply Input/ Output	5V must be present on V5 for normal operation. Bypass V5 to GND with a 1µF capacitor. V5 can be supplied by the internal 5V linear regulator or by an external regulator. To use the internal regulator, connect V5 to REG, or to the emitter of an external NPN transistor. To bypass the internal regulator, connect an external 5V supply directly to V5.		
6	B2	REG	5V Regulator Control Output	To use the internal linear regulator, connect REG to V5 or connect REG to the base of an external NPN pass transistor. Leave REG unconnected and connect V5 to an external 5V supply to bypass the internal regulator.		
7	B3	LED1	LED Driver Output 1	LED1 is a 5V logic output. Connect a current-limiting resistor in series between LED1 and the LED to limit the LED current. LED1 can be controlled by driving the LED1IN high or low, or through the SPI interface. Set the LED1b bit high to turn on the LED, clear the LED1b bit to turn off the LED. Alternatively, drive the LED1IN input high to turn on the LED, drive LED1IN low to turn off the LED. See Table 2.		LED1 is a 5V logic output. Connect a current-limiting resistor in series between LED1 and the LED to limit the LED current. Drive the LED1IN input high to turn on the LED, drive LED1IN low to turn off the LED.
—	C3	LED2	LED Driver Output 2	LED2 is a 5V logic output. Connect a current-limiting resistor in series between LED2 and the LED to limit the LED current. Set the LED2b bit high to turn on the LED, clear the LED2b bit to turn off the LED.		LED2 cannot be controlled in pin-mode. LED2 is off.

Pin Description (continued)

PIN		NAME	PIN DESCRIPTION	FUNCTION		
TQFN	WLP			PARALLEL MODE (SPI/$\overline{PIN}$ = High)	MULTIPLEXED MODE (SPI/$\overline{PIN}$ = High)	PIN MODE (SPI/$\overline{PIN}$ = Low)
				UARTSEL = Low	UARTSEL = High	
8, 11	A1, A4	C/Q	C/Q Transceiver Output/ Input	The C/Q driver can be controlled and monitored with the logic input/output pins or through the SPI interface. Drive TXEN high to enable the C/Q driver. The logic on the C/Q output is the inverse logic-level of the signal in the TX input. RX is the logic inverse of C/Q. Connect the two C/Q pins together.		Drive TXEN high to enable the C/Q driver. The logic on the C/Q output is the inverse logic-level of the signal in the TX input. RX is the logic inverse of C/Q. Configure the C/Q driver with the pin-mode inputs. Connect the two C/Q pins together.
9	A2	V24	Power-Supply Input	Bypass V24 to GND with a 0.1µF ceramic capacitor as close to the device as possible.		
10	A3	GND	Ground			
12	A5	DI	DI Receiver Input	The DI receiver can be monitored on the LI output or through the SPI interface. The LI output is the inverse logic-level of the signal on the DI input. Connect a 1kΩ resistor in series with the DI pin.		The LI output is the inverse logic-level of the signal on the DI input. The DI receiver cannot be disabled in pin-mode. Connect a 1kΩ resistor in series with the DI pin.
13	B4	V33	3.3V Linear Regulator Output	Bypass V33 to GND with a 1µF capacitor as close to the IC as possible. The V33 regulator can be disabled through the SPI interface.		Bypass V33 to GND with a 1µF capacitor as close to the IC as possible. V33 cannot be disabled in pin-mode.
14	B5	VL	Logic-Level Supply Input	VL defines the logic levels on all of the logic inputs and outputs. Apply a voltage from 2.5V to 5.5V on VL. Bypass VL to GND with a 0.1µF ceramic capacitor.		
15	C5	LI	DI Receiver Logic Output	The LI output is the inverse logic-level of the signal on the DI input. Disable the LI output through the SPI interface. LI is high impedance when the DI_Dis bit is set.		The LI output is the inverse logic-level of the signal on the DI input. LI cannot be disabled in pin-mode.
16	C4	UARTSEL	UART Interface Select Logic Input	Drive UARTSEL low to use RX, TX, and TXEN for UART signaling.	When $\overline{CS}$/PP is high, use SDO/RX/THSH, SDI/TX/NPN, and CLK/ TXEN/200MA for UART signaling.	UARTSEL is inactive when SPI/$\overline{PIN}$ is low.
17	D5	I.C.	Internally Connected	Internally connected. Connect to GND or VL.		

Pin Description (continued)

PIN		NAME	PIN DESCRIPTION	FUNCTION		
TQFN	WLP			PARALLEL MODE (SPI/$\overline{PIN}$ = High)	MULTIPLEXED MODE (SPI/$\overline{PIN}$ = High)	PIN MODE (SPI/$\overline{PIN}$ = Low)
				UARTSEL = Low	UARTSEL = High	
18	D4	$\overline{WU}$	Wake-Up Request Push-Pull Output	$\overline{WU}$ asserts low for 200µs when an IO-Link 80µs wake-up condition is detected on the C/Q line.		
19	E5	LED1IN	LED1 Driver Logic Input	Drive LED1IN high or low to enable/disable the LED1 driver. The LED1 driver can also be controlled through the SPI interface. See Table 2.		Drive LED1IN high to turn on the LED connected to LED1. Drive LED1IN low to turn the LED driver off.
20	E4	$\overline{IRQ}$/$\overline{OC}$	Open-Drain Interrupt/ Over-current Output	$\overline{IRQ}$/$\overline{OC}$ asserts when any bit in the INTERRUPT register is set. $\overline{IRQ}$/$\overline{OC}$ deasserts when the INTERRUPT register is read.		$\overline{IRQ}$/$\overline{OC}$ asserts low when the load current on the C/Q or DO output exceeds the set current limit.
21	D3	SDO/ RX/ THSH	SPI Serial Data Output/ RX Logic Output/ Thermal Shutdown Indicator	SPI serial data output	When $\overline{CS}$/PP is high, the SPI interface is disabled and UART interface mode is enabled. SDO/RX/THSH is the logic inverse of C/Q.	SDO/RX/THSH asserts low when the IC enters thermal shutdown. SDO/RX/THSH deasserts when the device returns to normal operation.
22	E3	CLK/ TXEN/ 200MA	SPI Clock Input/ UART TXEN Input/ Current Limit Setting Input	SPI clock input	When $\overline{CS}$/PP is high, the SPI interface is disabled and UART interface mode is enabled. Drive CLK/ TXEN/200MA high to enable the C/Q driver.	Drive CLK/TXEN/200MA high to enable a 200mA current limit on the C/Q and DO driver outputs. Drive CLK/TXEN/200MA low to set the current limit for the driver outputs to 100mA.
23	D2	SPI/$\overline{PIN}$	SPI or Pin-Mode Select Input	Drive SPI/$\overline{PIN}$ high for SPI or UART interface operation. Drive SPI/$\overline{PIN}$ low for pin-mode operation.		
24	E2	SDI/TX/ NPN	SPI Serial Data Input/ TX Logic Input/ NPN Driver Mode Select Input	SPI serial data input	When $\overline{CS}$/PP is high, the SPI interface is disabled and UART interface mode is enabled. Drive SDI/TX/ NPN to switch C/Q. C/Q is the logic inverse of the SDI/TX/NPN input.	Drive SDI/TX/NPN high to set the C/Q and DO driver outputs in NPN mode. Drive SDI/TX/NPN low to set the driver outputs in PNP mode. SDI/TX/NPN is ignored when the $\overline{CS}$/PP input is high.
EP	—	EP	Exposed pad. Connect to ground. Not intended as the main ground connection.			

Table 1. C/Q Control

SPI/$\overline{PIN}$	TXEN	TX	CQ_Dis	CQ_Q	C/Q OUTPUT		
					NPN MODE	PNP MODE	PP MODE
L	L	X	—	—	Z	Z	Z
	H	L	—	—	Z	H	H
		H	—	—	L	Z	L
H	L	X	0	0	Z	Z	Z
		X	0	1	Z	H	H
	H	L	0	X	Z	H	H
		H	0	0	L	Z	L
		H	0	1	Z	H	H
	X	X	1	X	Z	Z	Z

X = Don't care, Z = High impedance

Table 2. LED1 Configuration

LED1IN	LED1b BIT	LED1 DRIVER STATUS
L	0	OFF
	1	ON
H	0	ON
	1	ON

Table 3. Driver NPN, PNP, PP Selection in Pin Mode

SPI/$\overline{PIN}$	$\overline{CS}$/PP	SDI/TX/NPN	C/Q DRIVER MODE
L	L	L	PNP
L	L	H	NPN
L	H	L	PUSH-PULL
L	H	H	PUSH-PULL
H	X	X	C/Q mode is set with the SPI interface

Detailed Description

The MAX14828 is an industrial sensor output driver/IO-Link device transceiver. The IC integrates the high voltage functions commonly found in sensors, including a single 24V line driver and two on-board linear regulators (LDOs). The MAX14828 can be configured and monitored either through the SPI interface or by setting logic interface pins.

The MAX14828 features multiple programmable functions that allow the user to optimize operation and power dissipation for various loads and application scenarios.

The integrated 3.3V and 5V LDOs provide the power needed for low noise analog and logic supply rails.

SPI, UART, or Pin-Mode Interface

Pin Mode

The MAX14828 provides a selectable SPI or pin interface to configure and monitor device operation. Drive the SPI/$\overline{PIN}$ input high to use the SPI. Drive SPI/$\overline{PIN}$ low to use the pin interface (pin-mode control).

When operating in pin mode, the following functionality is set and cannot be changed:

- RX and DI are enabled (cannot be disabled)
- RX deglitch filter is enabled
- Weak pull-ups/pull-downs on C/Q are disabled
- Autoretry functionality is disabled
- The blanking time on C/Q is 128µs

SPI Operation (Parallel Operating Mode)

When the MAX14828 is operated in SPI mode, an external UART can be connected to separate UART interface pins (TX, RX, TXEN). This is called the parallel SPI/UART operating mode. This is the common approach used when the microcontroller offers a UART and a separate SPI port in the Typical Operating Circuit. Drive UARTSEL low for operation in parallel mode.

SPI Operation (Multiplexed Mode)

In cases where only one microcontroller serial port is available with both SPI and UART functions, the MAX14828 can be operated in multiplexed SPI/UART mode. This is feasible in IO-Link operation due to the defined idle times in the IO-Link cycle time. In multiplexed mode, the UART and SPI pins are shared. Two operating modes are available in multiplexed mode, as selected by the ENMPX bit.

When ENMPX = 0, UART and SPI operation are selected by setting the $\overline{CS}$/PP input. In this mode the SPI interface is active when $\overline{CS}$/PP is low and UART operation when $\overline{CS}$/PP is high.

When ENMPX = 1, UART and SPI operations are selected by setting the UARTSEL input. To avoid glitches on C/Q, CLK/TXEN/200MA and SDI/TX/NPN are sampled on the falling edge of UARTSEL in this mode. See Mode Selection Table for more information.

When entering multiplexed mode, set TXEN low and TX high to disable the driver.

$\overline{IRQ}/\overline{OC}$ is active in both multiplexed modes during UART communication.

24V Interface

The MAX14828 features an IO-Link transceiver interface tolerant of voltages from (V_{24}-70V) to +65V. This is the 24V interface and includes the C/Q input/output (C/Q), the logic-level digital input (DI), and the V24 supply.

The MAX14828 features a selectable push-pull, high-side (PNP), or low-side (NPN) switching driver at C/Q.

Configurable Drivers (Pin Mode)

In pin mode, use SDI/TX/NPN and $\overline{CS}$/PP inputs to configure the C/Q driver in push-pull, PNP, or NPN modes (Table 3). In this mode, toggle TXEN and TX to switch the C/Q output.

Configurable Drivers (SPI Mode)

Set the bits in the CQConfig register to configure the C/Q driver, enable/disable the weak pull-up and pull-down currents on C/Q. The C/Q driver can be disabled by setting the CQ_Dis bit. The driver output is high impedance and power dissipation is reduced when this bit is set. See the *Register Functionality* section for more information on configuring the C/Q driver.

For IO-Link operation, TX, TXEN, and RX are the UART interface to control C/Q communication. Set CQ_Dis = CQ_Q = 0 and drive TX and TXEN inputs for C/Q driver control.

Register bits can also be used to control the C/Q driver for lower rate switching. For bit control, drive TXEN and TX high and use the CQ_Q bit to control the C/Q driver state. The CQ_Dis bit is used to enable/disable the driver in this mode.

C/Q Driver Enable/Disable

In pin-mode, the C/Q driver is enabled/disabled with the TXEN input. Drive TXEN high to enable the C/Q driver. C/Q is the logic inverse of the TX input.

In SPI mode, the C/Q driver can also be enabled/disabled, configured, and controlled in the CQConfig register.

IO-Link is a registered trademark of Profibus User Organization (PNO).
SPI is a trademark of Motorola, Inc.

C/Q Current Limit

The C/Q driver is optimized for driving large capacitive loads and dynamic impedances like incandescent lamps. In pin-mode, the driver current limit is selectable by setting the CLK/TXEN/200MA input high or low. Set CLK/TXEN/200MA low for 100mA maximum load current. Set CLK/TXEN/200MA high for a 200mA maximum load current.

In SPI operation, the maximum driver current limit is selectable as 50mA, 100mA, 200mA, or 250mA by setting the CL1 and CL0 bits in the CURRLIM register.

C/Q Driver Fault Detection

The MAX14828 senses a fault condition on the C/Q driver when it detects a short-circuit for longer than the blanking time. A short condition exists when the C/Q driver's load current exceeds the current limit. In SPI mode, both the current limit and blanking time may be configured.

In pin-mode, the $\overline{IRQ}/\overline{OC}$ output asserts low when a short circuit fault occurs on C/Q. In SPI mode, the C/QFault and C/QFaultInt bits are set and $\overline{IRQ}/\overline{OC}$ asserts.

When a short-circuit event occurs on C/Q, the driver can either be set to continue supplying the selected current until the device enters thermal shutdown or to enter autoretry mode when an overcurrent event occurs. In autoretry mode the driver is automattically disabled after the current blanking time and is then re-enabled.

C/Q Receiver Output (RX)

RX is the output of the C/Q receiver. RX is the inverse logic of the C/Q input.

In pin-control mode, the C/Q receiver is always on.

In SPI mode, the receiver can be disabled by setting the Rx_Dis bit in the CQConfig register. RX is high impedance when Rx_Dis is set. Note that the CQLvl bit in the Status register is invalid when the Rx_Dis bit is set.

When operating in multiplexed mode, SDO/RX/THSH is the output of the C/Q receiver. In this mode, SDO/RX/THSH is high impedance when $\overline{CS}$/PP is high and Rx_Dis bit is set.

C/Q Receiver Threshold

The IO-Link standard defines device operation with a sensor supply between 18V and 30V. Industrial sensors, however, commonly operate with supply voltages as low as 9V. The MAX14828 C/Q receiver supports operation with lower supply voltages by scaling the receiver thresholds when V24 is less than 18V (V_{24} < 18V).

Reverse-Polarity Protection

The MAX14828 is protected against reverse-polarity connections on V24, C/Q, DI, and GND. Any combination of these pins can be connected to DC voltages up to 65V (max), resulting in a current flow of less than 1mA.

Ensure that the maximum voltage between any of these pins does not exceed 65V.

Driver Short-Circuit Detection

The MAX14828 monitors the C/Q driver output for overcurrent and driver overheating conditions.

In pin-mode, the driver short-circuit current limit is set with the CLK/TXEN/200mA input. $\overline{IRQ}/\overline{OC}$ asserts when an overcurrent or overheating condition occurs on the C/Q driver. $\overline{IRQ}/\overline{OC}$ deasserts when the overcurrent or overheating condition is removed.

In SPI mode, the current limit for the driver is set using the CL1 and CL0 bits in the CURRLIM register. When an overcurrent or overheating condition occurs on C/Q, the CQFault and CQFaultInt bits are set and $\overline{IRQ}/\overline{OC}$ asserts. The CQFault bit is cleared as soon as the overcurrent or overheating condition on the C/Q driver is removed. $\overline{IRQ}/\overline{OC}$ deasserts and the CQFaultInt bit is cleared only when the INTERRUPT register is read.

5V and 3.3V Linear Regulators

The MAX14828 includes two internal regulators to generate 5V (V5) and 3.3V (V33).

The V5 regulator is capable of driving external loads up to 30mA, including device and 3.3V LDO current consumption. To drive larger loads, use an external pass transistor to generate the required 5V. When using an external transistor, connect REG to the base of the transistor to regulate the voltage and connect V5 to the emitter (Figure 10).

When the internal 5V linear regulator is not used, V5 is the supply input for the internal analog and digital functions and must be supplied externally. Ensure that V5 is present for normal operation.

The 3.3V regulator is capable of driving external loads up to 30mA. In SPI mode, the 3.3V LDO can be enabled/disabled by setting the V33Dis bit in the Mode register.

V5 and V33 are not protected against short circuits.

Power-Up

The C/Q driver output is high impedance when V24, V5, VL, and/or V33 voltages are below their respective undervoltage thresholds during power-up.

The drivers are automatically disabled if V24, V5, or VL falls below its threshold.

Low Voltage and Undervoltage Detection

In SPI mode, the device monitors the V24 supply for low voltage and undervoltage conditions. Low voltage warnings must be enabled in the MODE register.

When V_{24} falls below the 16V (typ) low-voltage warning threshold, the V_{24W} bit in the STATUS register is set. If V24WEn is set to 1, the V24WInt interrupt bit is also set and $\overline{IRQ}/\overline{OC}$ asserts.

When V24 falls below the 7.4V (typ) undervotlage lockout (UVLO) threshold, the UV24 bit in the STATUS register is set. Similarly, the UV24Int bit in the INTERRUPT register is set and $\overline{IRQ}/\overline{OC}$ asserts. UVLO monitoring and interrupts cannot be disabled.

Wake-Up Detection

The MAX14828 detects an IO-Link wake-up condition on the C/Q line in push-pull, high-side (PNP), or low-side (NPN) operation modes. A wake-up condition is detected when the C/Q output is shorted for 80µs (typ). $\overline{WU}$ pulses low for 200µs (typ) when the device detects a wake-up pulse on C/Q (Figure 5).

In SPI mode, the WuInt bit in the INTERRUPT register is set and $\overline{IRQ}/\overline{OC}$ asserts when an IO-Link wake-up event is detected.

Wake-up detection can be disabled in SPI mode by setting the WU_Dis bit in the MODE register to 1. Wake-up detection cannot be disabled in pin-mode.

The device includes a wake-up detection algorithm to avoid false wake-up detection on C/Q. The false wake-up blanking time is defined by the current limit blanking time. In pin-mode, this is 128µs. In SPI-mode, this is set by the CL_BL0 and CL_BL1 bits in the CURRLIM reigster.

Thermal Protection and Considerations

The internal LDOs and the driver can generate more power than the package for the device can safely dissipate. Ensure that the driver and LDO loading is less than the package can dissipate. Total power dissipation for the device is calculated using the following equation:

$$P_{TOTAL} = P_{C/Q} + P_{V5} + P_{33} + P_{24} + P_{PU} + P_{PD}$$

where $P_{C/Q}$ is the power generated in the C/Q driver, P_{V5} and P_{V33} are the power generated by the LDOs, P_{24} is the quiescent power generated by the device, and P_{PU} and P_{PD} are the power generated in the C/Q weak pullup/pulldown current source/sink, respectively.

Ensure that the total power dissipation is less than the limits listed in the *Absolute Maximum Ratings* section.

Use the following to calculate the power dissipation (in mW) due to the C/Q driver:

$$P_{C/Q} = [I_{C/Q}(max)]^2 \times R_O$$

where R_O driver on-resistance.

Calculate the power dissipation in the 5V LDO, V_5, using the following equation:

$$P_5 = (V_{24} - V_5) \times I_5$$

where I_5 includes the I_{33} current sourced from V33.

Calculate the power dissipated in the 3.3V LDO, V33, using the following equation:

$$P_{33} = 1.7V \times I_{LOAD33}$$

Calculate the quiescent power dissipation in the device using the following equation:

$$P_{24} = I_{24}(max) \times V_{24}(max)$$

If the weak current sinks/sources are enabled, calculate their associated power dissipation as:

$$P_{PD} = I_{PD}(max) \times V_{C/Q}(max)$$
$$P_{PU} = I_{PU}(max) \times [V_{24} - V_{C/Q}](max)$$

Overtemperature Warning

In SPI mode, the device generates interrupts when the junction temperature of the C/Q driver exceeds +140°C (typ) warning threshold. The TempW bit in the STATUS register is set and the TempWInt in the INTERRUPT register is set and $\overline{IRQ}/\overline{OC}$ asserts under these conditions.

The TempW bit is cleared when the die temperature falls to +125°C. The INTERRUPT register must be read to clear the TempWInt bit and deassert $\overline{IRQ}/\overline{OC}$.

The device continues to operate normally unless the die temperature reaches the +165°C thermal shutdown threshold, when the device enters thermal shutdown.

The device does not generate overtemperature warnings when operating in pin-mode.

Thermal Shutdown

The C/Q driver and the V5 and V33 regulators are automatically switched off when the junction temperature exceeds the +165°C (typ) thermal shutdown threshold. SPI communication and and the internal regulators are not disabled during thermal shutdown. In SPI mode, the ThShut bit in the STATUS register and the ThShutInt in the INTERRUPT register are set.

Regulators are automatically switched on when the internal die temperature falls below the thermal shutdown threshold plus hysteresis. If the internal V5 regulator is used, the internal registers return to their default state when the V5 regulator is switched back on.

Mode Selection Table

OPERATING MODE	SPI/$\overline{PIN}$	UARTSEL	ENMPX BIT	$\overline{CS}$/PP	PIN NAME	PIN FUNC-TION	FUNCTION
PIN	L	X	X	LOW OR HIGH	SDI/TX/NPN	NPN	Parallel configuration/monitoring
					SDO/RX/THSH	THSH	Parallel configuration/monitoring
					CLK/TXEN/200MA	200MA	Parallel configuration/monitoring
					$\overline{CS}$/PP	PP	Parallel configuration/monitoring
					$\overline{IRQ}$/$\overline{OC}$	$\overline{OC}$	Parallel configuration/monitoring
					RX	C/Q RX	Parallel configuration/monitoring/ UART communication
					TX	C/Q TX	Parallel configuration/monitoring/ UART communication
					TXEN	C/Q TXEN	Parallel configuration/monitoring/ UART communication
PARALLEL UART + SPI	H	L	0	LOW OR HIGH	SDI/TX/NPN	SDI	SPI configuration/monitoring
					SDO/RX/THSH	SDO	SPI configuration/monitoring
					CLK/TXEN/200MA	CLK	SPI configuration/monitoring
					$\overline{CS}$/PP	CS	SPI configuration/monitoring
					$\overline{IRQ}$/$\overline{OC}$	$\overline{IRQ}$	SPI configuration/monitoring
					RX	C/Q RX	UART communication
					TX	C/Q TX	UART communication
					TXEN	C/Q TXEN	UART communication
MULTIPLEXED UART/SPI	H	H	0	L	SDI/TX/NPN	SDI	SPI configuration/monitoring
					SDO/RX/THSH	SDO	SPI configuration/monitoring
					CLK/TXEN/200MA	CLK	SPI configuration/monitoring
					$\overline{CS}$/PP	LOW	SPI configuration/monitoring
					$\overline{IRQ}$/$\overline{OC}$	$\overline{IRQ}$	SPI configuration/monitoring
					RX	C/Q RX	UART communication
					TX	C/Q TX	UART communication
					TXEN	C/Q TXEN	UART communication
				H	SDI/TX/NPN	C/Q TX	UART communication
					SDO/RX/THSH	C/Q RX	UART communication
					CLK/TXEN/200MA	C/Q TXEN	UART communication
					$\overline{CS}$/PP	HIGH	
					$\overline{IRQ}$/$\overline{OC}$	$\overline{IRQ}$	SPI configuration/monitoring
					RX	C/Q RX	Active
					TX	C/Q TX	Ignored
					TXEN	C/Q TXEN	Ignored

Mode Selection Table (continued)

OPERATING MODE	SPI/$\overline{\text{PIN}}$	UARTSEL	ENMPX Bit	$\overline{\text{CS}}$/PP	PIN NAME	PIN FUNCTION	FUNCTION
MULTIPLEXED UART/SPI	H	0	1	LOW OR HIGH	SDI/TX/NPN	SDI	SPI configuration/monitoring
					SDO/RX/THSH	SDO	SPI configuration/monitoring
					CLK/TXEN/200MA	CLK	SPI configuration/monitoring
					$\overline{\text{CS}}$/PP	$\overline{\text{CS}}$	SPI configuration/monitoring
					$\overline{\text{IRQ}}$/$\overline{\text{OC}}$	$\overline{\text{IRQ}}$	SPI configuration/monitoring
					RX		Active
					TX		Ignored
					TXEN		Ignored
		1			SDI/TX/NPN	C/Q TX	UART communication
					SDO/RX/THSH	C/Q RX	UART communication
					CLK/TXEN/200MA	C/Q TXEN	UART communication
					$\overline{\text{CS}}$/PP		Not used
					$\overline{\text{IRQ}}$/$\overline{\text{OC}}$	$\overline{\text{IRQ}}$	SPI monitoring
					RX		Active
					TX		Ignored
					TXEN		Ignored

Register Functionality

The MAX14828 has seven 8-bit-wide registers for configuration and monitoring (Table 4).

Table 4. Register Summary

REGISTER	ADD	R/W	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
INTERRUPT	00h	R	ThShutInt	WuInt	—	CQFaultInt	V24WInt	UV24Int	-	TempWInt
STATUS	01h	R	ThShut	DiLvl	—	CQFault	V24W	UV24	CQLvl	TempW
MODE	02h	R/W	RST	WU_Dis	V33_Dis	ENMPX	V24WEn	CQFil	LED2b	LED1b
CURRLIM	03h	R/W	CL1	CL0	CLDis	CL_BL1	CL_BL0	TAr1	TAr0	ArEn
CQConfig	04h	R/W	Rx_Dis	CQ_WPD	CQ_WPU	—	CQ_NPN	CQ_PP	CQ_Q	CQ_Dis
DIOConfig	05h	R/W	DI_Dis	—	—	—	—	—	—	—
CQInvert	06h	R/W	CQInv	—	—	—	—	—	—	—

INTERRUPT Register [A2, A1, A0] = [000]

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	ThShutInt	WuInt	—	CQFaultInt	V24WInt	UV24Int	—	TempWInt
Read/Write	R	R	R	R	R	R	R	R
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	Y	Y	Y	Y	Y	Y	Y	Y

The INTERRUPT register reflects current state of various fault conditions. The $\overline{IRQ/OC}$ output asserts when any of the bits in the INTERRUPT register is set. INTERRUPT register bits are latched and are not cleared when the initiating condition is removed. Reading the INTERRUPT register clears all the bits and deasserts $\overline{IRQ/OC}$. $\overline{IRQ/OC}$ reasserts only when another fault condition occurs.

BIT	NAME	DESCRIPTION
7	ThShutInt	**Thermal Shutdown Interrupt** 1: This bit is set when the MAX14828 has entered thermal shutdown mode. Once set, this bit is not cleared until the register is read. The current status of the thermal shutdown condition can be read in the STATUS register. 0: The MAX14828 is not in thermal shutdown.
6	WuInt	**Wake-Up Event Interrupt** 1: This bit is set when an IO-Link wake-up condition is detected on the C/Q line. 0: No wake-up condition is detected. The wake-up interrupt can be disabled by setting the WuDis bit to 1.

INTERRUPT Register [A2, A1, A0] = [000] (continued)

BIT	NAME	DESCRIPTION
5	—	This bit is not used.
4	CQ_FaultInt	**C/Q Driver Fault Interrupt** 1: This bit is set when a fault occurs on the C/Q driver (over current or over heating). Once set, this bit is not cleared until the register is read. The current status of the thermal shutdown condition can be read in the STATUS register. 0: No fault on the C/Q driver.
3	V24WInt	**V24 Low Voltage Warning Interrupt** 1: This bit is set when V_{24} falls below the IO-Link low-voltage warning threshold fault ($V_{24} < V_{24W}$). Once set, this bit is not cleared until the register is read. The current status of the thermal shutdown condition can be read in the STATUS register. 0: V_{24} is greater than the low-voltage warning threshold.
2	UV24Int	**V24 Supply Undervoltage Interrupt** 1: This bit is set when V_{24} falls below the UVLO threshold ($V_{24} < V_{24UVLO}$). Once set, this bit is not cleared until the register is read. The current status of the thermal shutdown condition can be read in the STATUS register. 0: V_{24} is greater than the UVLO threshold.
1	—	This bit is not used.
0	TempWInt	**Overtemperature Warning Interrupt** 1: This bit is set when the die temperature exceeds the warning threshold ($T_J > T_{WRN}$). Once set, this bit is not cleared until the register is read. The current status of the thermal shutdown condition can be read in the STATUS register. 0: The die temperature has not exceeded the overtemperature warning threshold.

STATUS Register [A2, A1, A0] = [000]

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	ThShut	DiLvl	—	CQFault	V24W	UV24	CQLvl	TempW
Read/Write	R	R	R	R	R	R	R	R
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	N	N	N	N	N	N	N	N

The STATUS register reflects current state of various IC functions.

BIT	NAME	DESCRIPTION
7	ThShut	**Thermal Shutdown Status** 1: This bit is set when the MAX14828 has entered thermal shutdown mode. 0: This bit is cleared automatically when the device exits thermal shutdown.
6	DiLvl	**DI Logic Level** 1: This bit is set when the DI voltage is a logic-low ($V_{DI} < V_{TL}$) 0: This bit is clear when the DI voltage is a logic-high ($V_{DI} > V_{TH}$).
5	—	This bit is not used.
4	CQ_Fault	**C/Q Driver Fault Status** 1: This bit is set when a fault occurs on the C/Q driver (overcurrent or overheating). 0: This bit is cleared automatically when the fault on C/Q is removed.
3	V24W	**V24 Low Voltage Warning Status** 1: This bit is set when V24 falls below the IO-Link low-voltage warning threshold ($V_{24} < V_{24W}$). 0: This bit is cleared automatically when V24 rises above the low-voltage warning threshold.
2	UV24	**V24 Supply Status** 1: This bit is set when V24 falls below the UVLO threshold ($V_{24} < V_{24UVLO}$). 0: This bit is cleared automatically when V24 rises above the UVLO threshold.
1	CQLvl	**C/Q Logic Level** 1: This bit is set when the C/Q voltage is a logic-low ($V_{C/Q} < V_{TL}$) (CQInv = 0 or 1) 0: This bit is clear when the C/Q voltage is a logic-high ($V_{C/Q} > V_{TH}$) (CQInv = 0 or 1).
0	TempW	**Overtemperature Warning** 1: This bit is set when the die temperature exceeds the warning threshold ($T_J > T_{WRN}$). 0: This bit is cleared automatically when the when the die temperature falls below the warning threshold and hysteresis ($T_J < T_{WRN} - T_{WRN_HYST}$).

MODE Register [A2, A1, A0] = [010]

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	RST	WU_Dis	V33_Dis	ENMPX	V24WEn	CQFil	LED2b	LED1b
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	0
Reset upon Read	N	N	N	N	N	N	N	N

Use the mode register to configure the MAX14828 and manage the 3.3V LDO.

BIT	NAME	DESCRIPTION
7	RST	**Register Reset** 1: Reset all registers to their default power-up state. The Status register is cleared and $\overline{IRQ}$ deasserts (if asserted) when RST = 1. Interrupts are not generated while RST = 1. 0: Normal operation.
6	WU_Dis	**Wake-Up Interrupt Disable/Enable** 1: Wake-up detection is disabled. 0: Enable IO-Link wake-up detection.
5	V33_Dis	**V33 Enable/Disable** 1: Disable the V33 linear regulator. 0: Enable the V33 linear regulator.
4	ENMPX	**Enable/Disable SPI/UART Multiplexing** 1: Enable UART multiplexing on SPI interface pins. See the Mode Selection Table for more information. 0: Disable UART multiplexing on SPI interface pins.
3	V24WEn	**V24 Undervoltage Warning Enable** 1: Enable the V24 undervoltage warning interrupt. V24WInt is set when V24 falls below the UVLO threshold. 0: Disable the V24 undervoltage warning interrupt.
2	CQFil	**C/Q Deglitch Filter Enable/Disable** 1: Deglitch filter is disabled on RX. 0: Deglitch filter is enabled on RX.
1	LED2b	**LED2 Driver Logic** 1: Set the LED2 output high. 0: Set the LED2 output low.
0	LED1b	**LED1 Driver Logic.** 1: Set the LED1 output high. 0: LED1 output is driven by the LED1IN logic input.

CURRLIM Register [A2, A1, A0] = [011]

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	CL1	CL0	CL_Dis	CL_BL1	CL_BL0	TAr1	TAr0	ArEN
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	N	N	N	N	N	N	N	N

The CURRLIM register sets the C/Q driver current limit and the fixed off-time once the driver has exceeded the thermal shutdown threshold.

BIT	NAME	DESCRIPTION
7	CL1	**Driver Current Limit** Set the CL1 and CL0 bits to select the active current limit for the C/Q driver when CL_Dis = 0. 00: Driver current limit is set to 50mA 01: Driver current limit is set to 100mA 10: Driver current limit is set to 200mA 11: Driver current limit is set to 250mA
6	CL0	
5	CL_Dis	**Driver Current Limit Disable/Enable** 1: Disable the driver current limit for the C/Q driver. 0: Enable the driver current limit (as set by the CL1 and CL0 bits).
4	CL_BL1	**Current Limit Blanking Time** Set the CL_BL1 and CL_BL0 bits to select the minimum blanking time to signal a current limit or thermal fault. 00: Blanking time is 128µs 01: Blanking time is 500µs 10: Blanking time is 1ms 11: Blanking time is 5ms
3	CL_BL0	
2	TAr1	**Auto-Retry Fixed Off-Time** Set the TAr1 and TAr0 bits to select the fixed driver off-time after a fault has been generated when auto-retry functionality is enabled (ArEn = 1). The driver is re-enabled automatically after the fixed off-delay. 00: Fixed off-time is 50ms 01: Fixed off-time is 100ms 10: Fixed off-time is 200ms 11: Fixed off-time is 500ms
1	TAr0	
0	ArEN	**Auto-Retry Fixed Off-Time Enable/Disable** 1: Fixed off-time functionality is enabled. C/Q driver is disabled for a fixed time after an overcurrent or thermal fault occurs. The driver is re-enabled automatically after the fixed off-delay. 0: Fixed off-time functionality is disabled. The driver is re-enabled after temperature falls below the thermal hysteresis.

CQConfig Register [A2, A1, A0] = [100]

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	RX_Dis	CQ_WPD	C/Q_WPU	—	C/Q_NPN	CQ_PP	CQ_Q	CQ_Dis
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	1
Reset Upon Read	N	N	N	N	N	N	N	N

Use the CQConfig register to control the C/Q driver and receiver parameters. All bits in the CQConfig register are read-write.

BIT	NAME	DESCRIPTION
7	RX_Dis	**Receiver Disable/Enable** 1: The RX receiver output is disabled. RX is high impedance when disabled. 0: RX is enabled.
6	CQ_WPD	**C/Q Weak Pull-Down Enable** 1: Enable the weak pull-down current sink on the C/Q driver. 0: Disable the weak pull-down current sink on the C/Q driver.
5	CQ_WPU	**C/Q Weak Pull-Up Enable** 1: Enable the weak pull-up current source on the C/Q driver. 0: Disable the weak pull-up current source on the C/Q driver.
4	—	This bit is not used.
3	CQ_NPN	**C/Q Driver NPN/PNP Mode** 1: Enable NPN operation (when CQ_PP = 0) on the C/Q driver. 0: Enable PNP operation (when CQ_PP = 0) on the C/Q driver. CQ_NPN is ignored when CQ_PP = 1.
2	CQ_PP	**C/Q Driver Push-Pull Mode** 1: Enable push-pull operation on the C/Q driver. 0: Enable open-drain (PNP or NPN mode) operation on the C/Q driver.
1	CQ_Q	**C/Q Driver Output Logic** 1: Set the C/Q driver high (push-pull mode), set the C/Q PNP switch on (PNP mode), or set the C/Q NPN switch off (NPN mode). See Table 1. 0: CQ is high impedance when CQ_Q = 0 and TXEN is low (or CQ_Dis = 1). CQ logic is the inverse of TX logic when TXEN is high (and CQ_Dis = 0) and CQ_Q = 0. See Table 1.
0	CQ_Dis	**C/Q Driver Disable/Enable** 1: Disable the C/Q driver, regardless of the state of the TXEN input. The driver is high impedance in this mode. 0: Status of the C/Q driver is determined by the TXEN input or CQ_Q bit.

DIOConfig Register [A2, A1, A0] = [101]

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	DI_Dis	—	—	—	—	—	—	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	N	N	N	N	N	N	N	N

Use the DIOConfig register to enable or disable the DI receiver input.

BIT	NAME	DESCRIPTION
7	DI_Dis	**DI Receiver Enable/Disable** 1: The DI receiver is disabled. LI is high-impedance when the DI receiver is disabled. 0: DI receiver is enabled.
6:0	—	These bits are not used.

CQInvert Register [A2, A1, A0] = [110]

Bit	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Bit Name	CQInv	—	—	—	—	—	—	—
Read/Write	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR State	0	0	0	0	0	0	0	0
Reset Upon Read	N	N	N	N	N	N	N	N

Use the CQInvert register to control the polarity of the C/Q driver.

BIT	NAME	DESCRIPTION
7	CQInv	**CQ Invert Enable/Disable** 1: The CQ driver logic follows the TX input logic (if driver is enabled). RX logic follows the CQ driver/receiver logic. 0: The CQ driver logic is the inverse of the TX input logic (if driver is enabled). RX logic is the inverse of the CQ driver/receiver logic.
6:0	—	These bits are not used.

SPI Interface

The device communicates through an SPI-compatible 4-wire serial interface. The MAX14828 supports burst read/write access. The maximum SPI clock rate for the device is 12MHz. The SPI interface complies with clock polarity CPOL = 0 and clock phase CPHA = 0 (see Figure 7 and Figure 8).

The SPI interface is not available when V_5 or V_L are not present.

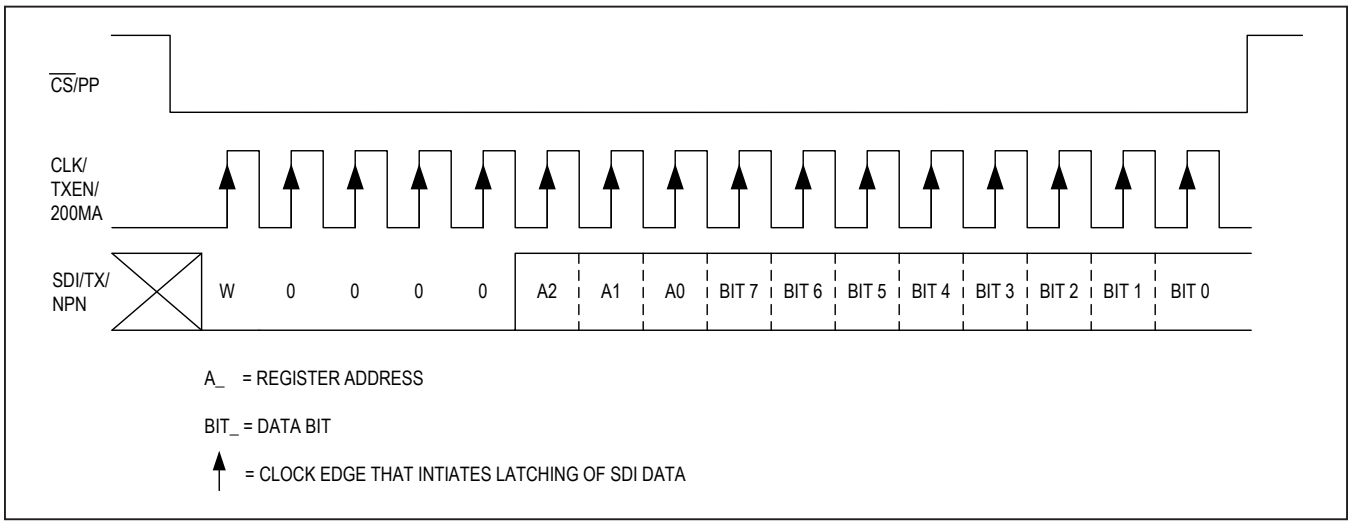


Figure 7. SPI Write Cycle

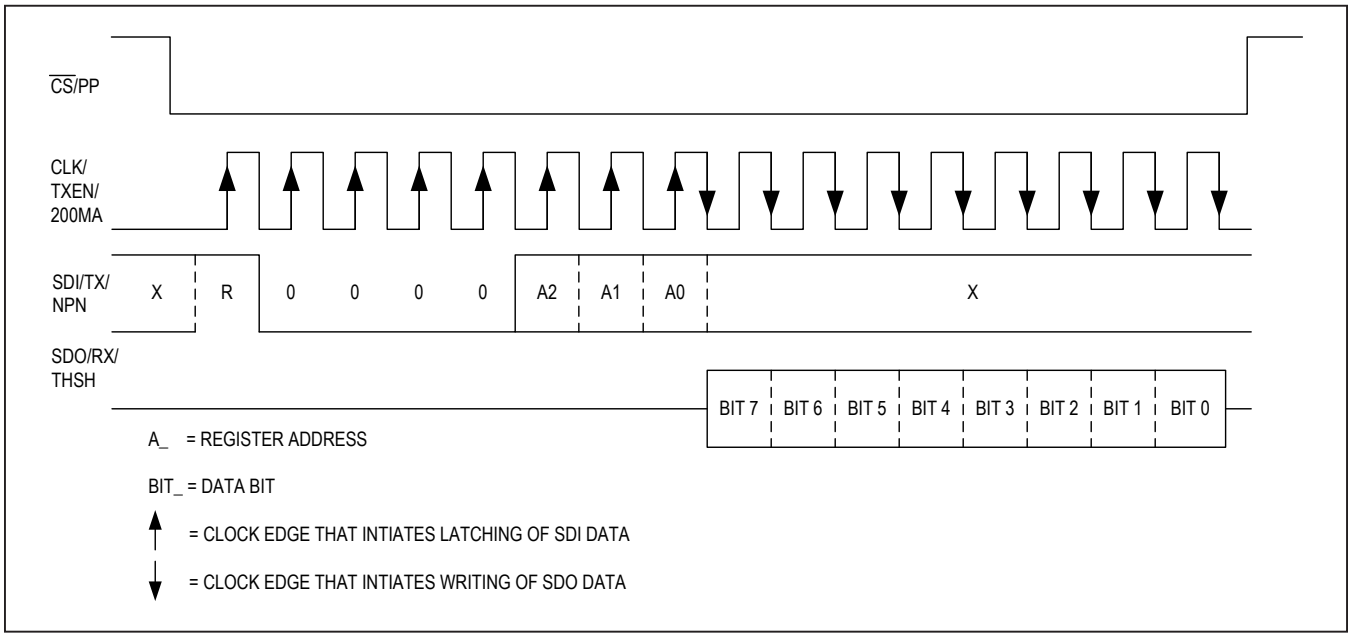


Figure 8. SPI Read Cycle

SPI Burst Access

Burst access allows writing or reading in one block, by only defining the initial register address in the SPI command byte. Once the initial SPI address is received, the MAX14828 automatically increments the register after each SPI data byte. Efficient programming of multiple consecutive registers is thus possible. Chip select, $\overline{CS}$/PP, must be kept low during the whole write/read cycle.

The SPI clock continues clocking throughout the burst access cycle. The burst cycle ends when the SPI master pulls $\overline{CS}$/PP high.

Applications Information

Microcontroller Interfacing

The logic levels of the microcontroller interface I/Os are defined by V_L. Apply a voltage from 2.5V to 5.5V to VL for normal operation. Logic outputs are supplied by VL.

The device can be configured for simultaneous or multiplexed UART communication. When configured for a multipexed UART interface, the SPI interface and UART interface pins are shared. See the Mode Selection Table for more information.

Transient Protection

Inductive load switching, ESD, bursts, and surges create high transient voltages. V24, C/Q, and DI should be protected against high overvoltage and undervoltage transients. Positive voltage transients on V24, C/Q, and DI must be limited to +70V relative to GND. Negative voltage transients must be limited to -70V relative to V24. Use protection diodes on C/Q and DI as shown in Figure 9.

For standard ESD and burst protection demanded by the IO-Link specification, small package TVS can be used (like the uClamp3603T or the SPT01-335). If higher level surge ratings need to be achieved (IEC 61000-4-5 ±1kV/ 42Ω), SMAJ33A or SMBJ36A TVS protectors can also be used.

Note that these are recommended protection components. Results may vary based on layout.

Using an External Transistor with the 5V Regulator

The internal 5V regulator (V5) can provide up to 30mA of total load current (including the current on to the V33 LDO) when V5 is connected to REG. To achieve larger load currents or to shunt the power dissipation away from the MAX14828, an external NPN transistor can be connected as shown in Figure 10.

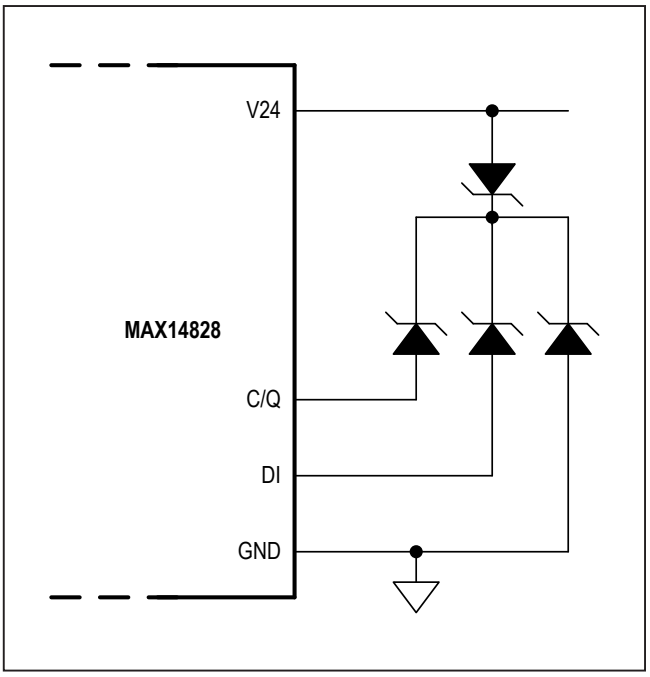


Figure 9. MAX14828 Operating Circuit with TVS Protection

Select an NPN transistor with high VCE voltage to support the max L+ supply voltage. In order to protect the NPN transistor against reverse polarity of the L+/L- supply terminals, connect a silicon or a Schottky diode in series with the NPN transistor's collector that has a reverse voltage capability large enough for reverse connected L+/L-. A 1µF capacitor on the V5 is required for stability.

Using an Step-Down Regulator with the 5V Regulator

To decrease power dissipation in the MAX14828, V5 can be powered by an external step-down regulator. Connect the external regulator's output to the V5 input and leave REG unconnected (Figure 11).

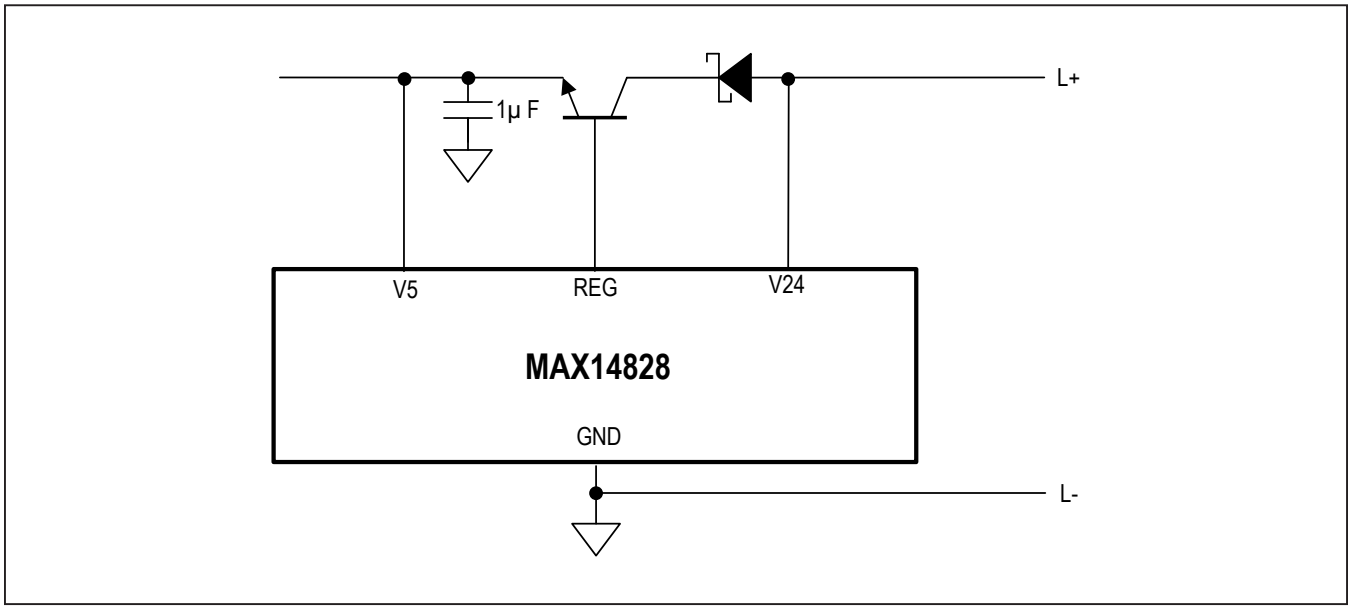


Figure 10. Using an External NPN Transistor with the 5V Regulator

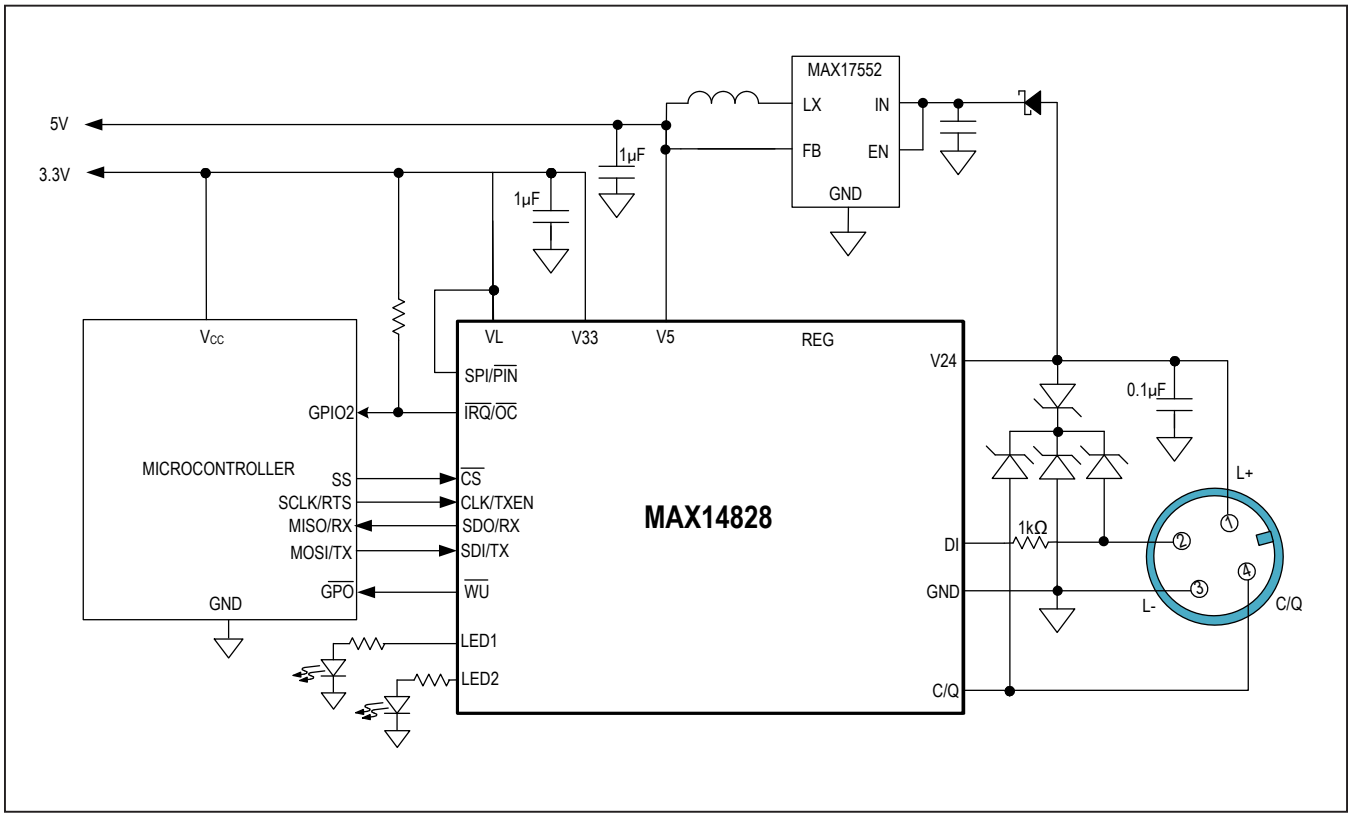


Figure 11. Using an External Step-Down with the 5V Regulator

Shared SPI/UART Interface

Figure 12 is an example of the use of a minimum pin-count microcontroller. A microcontroller serial port, which supports both UART and SPI functions, is used for managing both transceiver control (SPI) and IO-Link data communication (UART). The microcontroller's shared UART and SPI interface pins are multiplexed. The transceiver's SPI is typically only used for configuration at power-up and occasionally afterwards for reconfiguration, and diagnostics. During an IO-Link master-device communication cycle, the idle time on the C/Q interface can be used for SPI activity. This is possible by slightly increasing the IO-Link device' minimum cycle time.

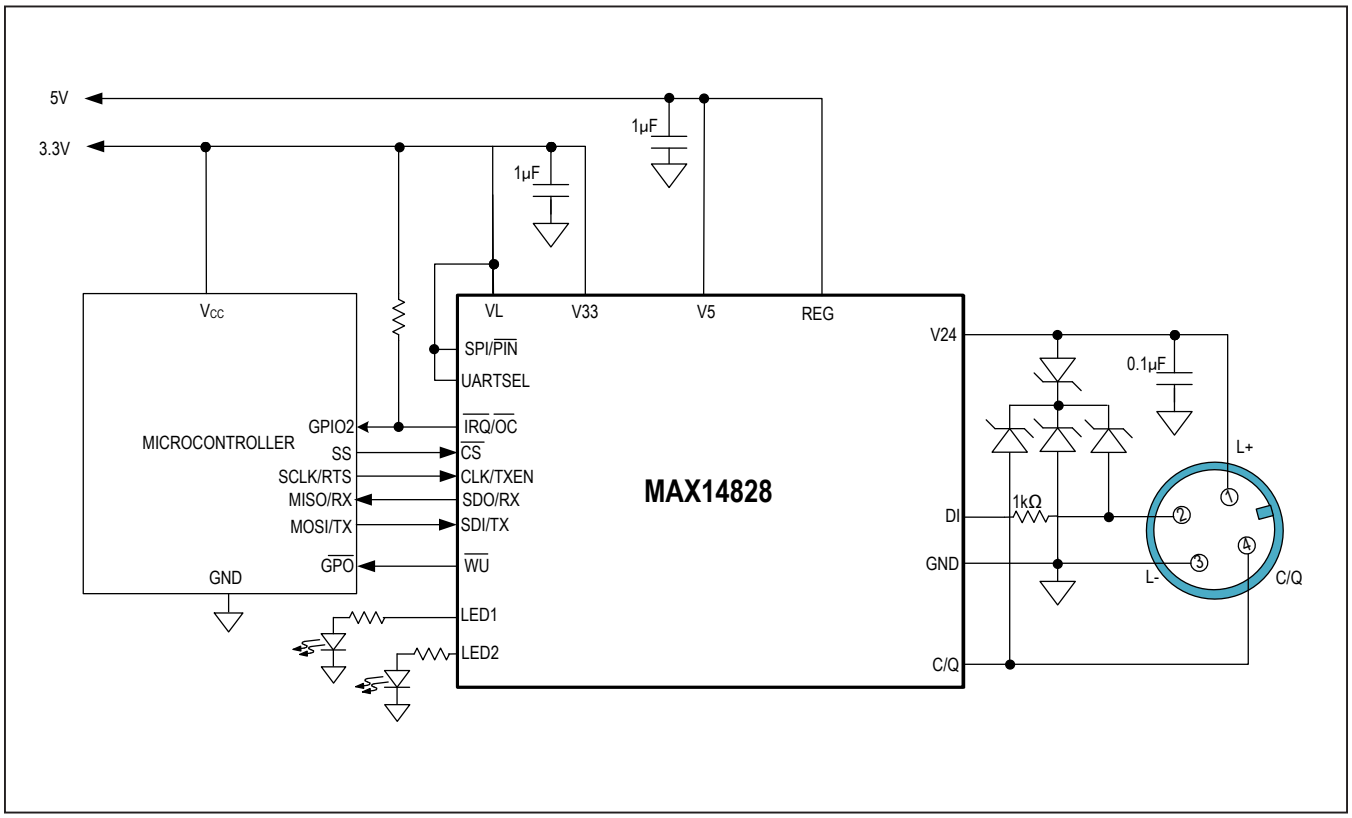


Figure 12. Multiplexed SPI/UART Mode Configuration

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14828ATG+	-40°C to +125°C	24 TQFN-EP*
MAX14828ATG+T	-40°C to +125°C	24 TQFN-EP*
MAX14828AWA+	-40°C to +125°C	25 WLP
MAX14828AWA+T	-40°C to +125°C	25 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
T = Tape and Reel.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/17	Initial release	—
1	2/19	Updated the *Pin Description, Wake-Up Detection* section, Figure 11, and Figure 12	19, 24, 36–37

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.

Maxim Integrated cannot assume responsibility for use of any circuitry other than circuitry entirely embodied in a Maxim Integrated product. No circuit patent licenses are implied. Maxim Integrated reserves the right to change the circuitry and specifications without notice at any time. The parametric values (min and max limits) shown in the Electrical Characteristics table are guaranteed. Other parametric values quoted in this data sheet are provided for guidance.

Maxim Integrated and the Maxim Integrated logo are trademarks of Maxim Integrated Products, Inc. © 2019 Maxim Integrated Products, Inc.