Click here for production status of specific part numbers.

MAX14690

PMIC with Ultra-Low I_Q Voltage Regulators and Battery Charger for Small Lithium Ion Systems

General Description

The MAX14690 is a battery-charge-management solution ideal for low-power wearable applications. The device includes a linear battery charger with a smart power selector and several power-optimized peripherals. The MAX14690 features two ultra-low-power buck regulators with a typical quiescent current of 900nA. In addition, three ultra-low power low-dropout (LDO) linear regulators, with a typical quiescent current of 600nA are included. In total, the MAX14690 can provide up to five regulated voltages, each with an ultra-low quiescent current, critical to battery life for the unique power profile in 24/7 operation devices, such as those in the wearable market.

The battery charger features a smart power selector that allows operation on a dead battery when connected to a power source. To avoid overloading a power adapter, the input current to the smart power selector is limited based on an I^2C register setting. If the charger power source is unable to supply the entire system load, the smart power control circuit supplements the system load with current from the battery.

The two synchronous, high-efficiency step-down buck regulators feature a fixed-frequency PWM mode for tighter regulation and a burst mode for increased efficiency during light-load operation. The output voltage of these regulators can be programmed through I^2C with the default preconfigured.

The three configurable LDOs each have a dedicated input pin. Each LDO regulator output voltage can be programmed through I^2C with the default preconfigured. The linear regulators can also be configured to operate as power switches that may be used to disconnect the quiescent load of the system peripherals.

The MAX14690 features a programmable power controller that allows the device to be configured for applications that require the device be in a true-off, or always-on, state. The controller also provides a delayed reset signal and voltage sequencing.

The MAX14690 is available in a 36-bump, 0.4mm pitch, 2.72mm x 2.47mm wafer-level package (WLP).

***Ordering Information* appears at end of data sheet.**

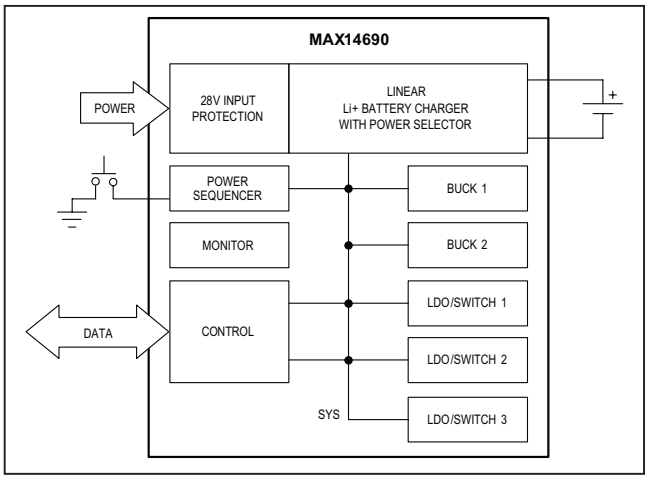
Benefits and Features

- Extend System Use Time Between Battery Charging
  - Dual Ultra-Low-I_Q 200mA Buck Regulators
    - Output Programmable from 0.8V to 1.8V and 1.5V to 3.3V
    - 0.9µA (typ) Quiescent Current
    - Automatic Burst or Forced-PWM Modes
  - Three Ultra-Low-I_Q 100mA LDOs
    - Output Programmable from 0.8V to 3.6V
    - 0.6µA (typ) Quiescent Current
    - 2.7V to 5.5V Input with Dedicated Pin
- Easy-to-Implement Li+ Battery Charging
  - Smart Power Selector
  - 28V/-5.5V Tolerant Input
  - Thermistor Monitor
- Minimize Solution Footprint Through High Integration
  - Provides Five Regulated Voltage Rails
  - Switch Mode Option on Each LDO
- Optimize System Control
  - Monitors Pushbutton for Ultra-Low Power Mode
  - Power-On Reset Delay and Voltage Sequencing
  - On-Chip Voltage Monitor Multiplexer

Applications

- Wearable Electronics
- Fitness Monitors
- Portable Medical Devices

Block Diagram



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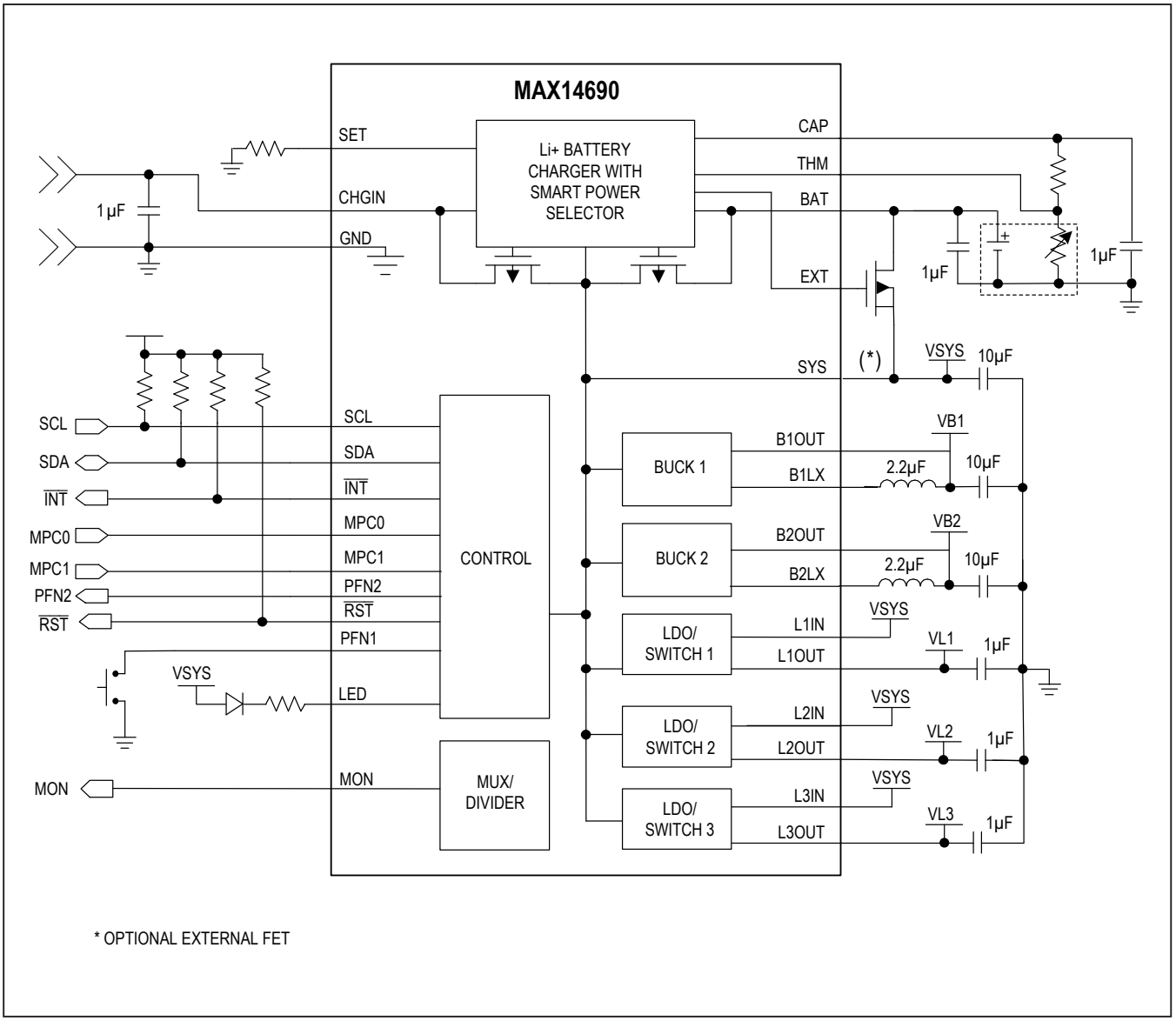
Typical Application Circuit



Absolute Maximum Ratings

(Voltages referenced to GND.)
SDA, SCL, THM, $\overline{RST}$, SYS, PFN1, PFN2, MPC0, MPC1, $\overline{INT}$, MON, BAT LED, L1IN, L2IN, L3IN ..... -0.3V to +6.0V
B1LX, B2LX, B1OUT, B2OUT, EXT ..... -0.3V to (V_{SYS} + 0.3V)
L1OUT ..... -0.3V to (V_{L1IN} + 0.3V)
L2OUT ..... -0.3V to (V_{L2IN} + 0.3V)
L3OUT ..... -0.3V to (V_{L3IN} + 0.3V)
CHGIN ..... -6V to +30V
CAP ..... -0.3V to min (V_{CHGIN} + 0.3V, +6V)
SET ..... -0.3V to V_{BAT} + 0.3V
Continuous Current into CHGIN, BAT, SYS ..... ±1000mA
Continuous Current into any other terminal ..... ±100mA
Continuous Power Dissipation (multilayer board at +70°C):
6 x 6 Array 36-Bump 2.72mm x 2.47mm 0.4mm Pitch WLP (derate 21.70mW/°C)..... 1.74W
Operating Temperature Range ..... -40°C to +85°C
Junction Temperature ..... +150°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature Soldering (10s) ..... +300°C
Soldering Temperature (reflow) ..... +260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

PACKAGE TYPE: 36 WLP	
Package Code	W362D2+1
Outline Number	**21-0897**
Land Pattern Number	Refer to **Application Note 1891**
THERMAL RESISTANCE, FOUR-LAYER BOARD	
Junction to Ambient (θ_{JA})	46°C/W

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GLOBAL SUPPLY CURRENT (L_IN Connected to SYS)						
Charger Input Current	I_{CHG}	All functions disabled		0.26		mA
		Power on, V_{CHGIN} = 5V SYS switch closed, buck regulators in burst mode, LDO1 enabled, I_{SYS} = 0A, I_{B_OUT} = 0A, I_{L_OUT} = 0A			2	
BAT Input Current	I_{BAT}	Power off, V_{CHGIN} = 0V, SYS switch open		0.95		µA
		Power on, V_{CHGIN} = 0V SYS switch closed, 2x buck regulators in Burst mode, LDOs disabled. I_{SYS} = 0A, I_{B_OUT} = 0A		3		
		Power on, V_{CHGIN} = 0V SYS switch closed, 2x buck regulators in Burst mode, LDO1 enabled, I_{SYS} = 0A, I_{B_OUT} = 0A, I_{L_OUT} = 0A		3.5		
		Power on, V_{CHGIN} = 0V SYS switch closed, 2x buck regulators in burst mode, 3x LDOs enabled, I_{SYS} = 0A, I_{B_OUT} = 0A, I_{L_OUT} =0A		4.6		
BUCK REGULATOR 1 (V_{SYS} = +3.7V, Burst mode operation, L = 2.2µH, C = 10µF, V_{B1OUT} = 1.2V)						
Input Voltage	V_{IN_BUCK1}	Input voltage = V_{SYS}	2.7		5.5	V
Output Voltage	V_{OUT_BUCK1}	25mV step resolution (Note 2)	0.8		1.8	V
Quiescent Supply Current	I_{Q_BUCK1}	Burst mode, I_{OUT} = 0mA (Note 3)		0.915	2	µA
	I_{PWM1_BUCK1}	FPWM mode, L = 4.7µH (ESR = 0.6Ω, 2MHz RAC = 2.13Ω), I_{OUT} = 0mA		2.5	3.5	mA
Output Accuracy	ACC_{BUCK1}	I_{OUT} = 1mA (V_{OUT_BUCK1} > 1V, C > 50µF)	-2.6		+2.9	%
Load Regulation	V_{ERR_BUCK1}	From I_{OUT} = 0 to 200mA (V_{B1OUT} = 1.2V average voltage)	-3	-1		%
Peak-to-Peak Ripple in Burst Mode	$V_{PPRIPPLE1}$	I_{OUT} = 10mA, C = 20µF		25		mV
		I_{OUT} = 10mA, C = 10µF		43		
Maximum Operative Output Current	I_{OUT_BUCK1}		200			mA
B1OUT Pulldown Current	I_{LEAK_B1OUT}	V_{OUT} = V_{SYS}		200	350	µA
		V_{REG} < V_{OUT} < V_{REG} + 0.1V		10	100	nA
pMOS On-Resistance	R_{ONP_BUCK1}			0.22	0.4	Ω
nMOS On-Resistance	R_{ONN_BUCK1}			0.18	0.3	Ω
Oscillator Frequency	f_{BUCK1}	FPWM mode	1.78	2	2.24	MHz

Electrical Characteristics (continued)

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Maximum Duty Cycle	D_{MAX_BUCK1}			100		%
Short-Circuit Current Limit	I_{SHRT_BUCK1}		1.1	1.3	1.62	A
BLX Leakage Current	I_{BLX_BUCK1}				1	µA
Active Discharge Current	I_{D_BUCK1}	V_{B1OUT} = 1.2V	8	18	36	mA
Full Turn-On Time	T_{ON_BUCK1}	Time from enable to full current capability		58		ms
Thermal-Shutdown Temperature	T_{SHDN_BUCK1}			150		°C
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_HYST\_BUCK1}$			20		°C
BUCK REGULATOR 2 (V_{SYS} = +3.7V, Burst mode operation, L = 2.2µH, C = 10µF, V_{B2OUT} = 1.8V.)						
Input Voltage	V_{IN_BUCK2}	Input voltage = V_{SYS}	2.7		5.5	V
Output Voltage	V_{OUT_BUCK2}	50mV step resolution	1.5		3.3	V
Quiescent Supply Current (Note 3)	I_{Q_BUCK2}	Burst mode, I_{OUT} = 0mA (Note 3)		1	2	µA
	I_{PWM1_BUCK2}	FPWM mode, L = 4.7µH (ESR = 0.6Ω, 2MHz RAC = 2.13Ω) I_{OUT} = 0mA		2.4	3.5	mA
Output Accuracy	ACC_{BUCK2}	I_{OUT} = 1mA, V_{OUT_BUCK2} > 1.5V, C > 50µF, V_{SYS} > V_{B2OUT} + 150mV	-2		+2.93	%
Load Regulation	V_{ERR_BUCK2}	From I_{OUT} = 0 to 200mA, V_{B2OUT} = 1.8V average voltage	-3.1	-1		%
Peak-to-Peak Ripple In Burst Mode	$V_{PPRIPPLE2}$	I_{OUT} = 10mA, C = 20µF		38		mV
		I_{OUT} = 10mA, C = 10µF		54		
Maximum Operative Output Current	I_{OUT_BUCK2}		200			mA
B2OUT Pulldown Current	I_{LEAK_B2OUT}	V_{OUT} = V_{SYS}		5	10	µA
		V_{REG} < V_{OUT} < V_{REG} + 0.1V		10		nA
pMOS On-Resistance	R_{ONP_BUCK2}			0.22	0.4	Ω
nMOS On-Resistance	R_{ONN_BUCK2}			0.18	0.3	Ω
Oscillator Frequency	f_{BUCK2}	FPWM mode	1.78	2.00	2.24	MHz
Maximum Duty Cycle	D_{MAX_BUCK2}			100		%
Short-Circuit Current Limit	I_{SHRT_BUCK2}		1.4	1.8	2.2	A
BLX Leakage Current	I_{BLX_BUCK2}				1	µA
Active Discharge Current	I_{D_BUCK2}	V_{B2OUT} = 1.8V	8	18	36	mA
Full Turn-On Time	t_{ON_BUCK2}	Time from enable to full current capability		58		ms
Thermal-Shutdown Temperature	T_{SHDN_BUCK2}			150		°C
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_HYST\_BUCK2}$			20		°C

Electrical Characteristics (continued)

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
LDOs (C = 1µF, unless otherwise noted. Typical values are at V_{L_IN} = 3.7V, with I_{L_OUT} = 10mA, V_{L_OUT} = 3V.)						
Input Voltage	V_{IN_LDO}	LDO_Mode = 0	2.7		5.5	V
		LDO_Mode = 1	1.8		5.5	V
Quiescent Supply Current	I_{Q_LDO}	I_{L_OUT} = 0mA		0.56	1.2	µA
	$I_{Q\_LDO\_AD}$	I_{L_OUT} = 0mA, VL_IN = 1.8V, LDO_ActDSC = 1, LDO_En = 00		40		µA
Maximum Output Current	$I_{L\_OUT\_MAX}$		100			mA
Output Voltage	V_{L_OUT}		0.8		3.6	V
Output Accuracy	ACC_{LDO}	V_{L_IN} = (V_{L_OUT} + 0.5V) or higher, I_{L_OUT} = 100µA			3	%
Dropout Voltage	V_{DROP_LDO}	V_{L_IN} = 3.3V, $I_{L\_OUT\_}$ = 100mA, V_{L_OUT} = 3.3V			100	mV
Line Regulation Error	$V_{LINEREG\_LDO}$	V_{L_IN} = (V_{L_OUT} + 0.5V) to 5.5V	-0.09		0.09	%/V
Load Regulation Error	$V_{LOADREG\_LDO}$	I_{L_OUT} = 100µA to 100mA	0.003		0.008	%/mA
Line Transient	$V_{LINETRAN\_LDO}$	V_{L_IN} = 4V to 5V, 200ns rise time		±36		mV
		V_{L_IN} = 4V to 5V, 1µs rise time		±28		mV
Load Transient	$V_{LOADTRAN\_LDO}$	I_{L_OUT} = 0mA to 10mA, 200ns rise time		145		mV
		I_{L_OUT} = 0mA to 100mA, 200ns rise time		290		mV
Active Discharge Current	I_{PDL}	V_{L_IN} = 3.7V	9	21	37	mA
Turn-On Time	t_{ON_LDO}	I_{L_OUT} = 0mA, time to 90% of final value		2.3		ms
		V_{L_IN} = 3V, switch mode, I_{L_OUT} = 0mA, time to 90% of final value		0.45		ms
Short-Circuit Current Limit	I_{SHRT_LDO}	V_{L_OUT} = GND		385		mA
		V_{L_OUT} = GND, switch mode		375		mA
Switch Mode Resistance	R_{ON_LDO}	V_{L_IN} = 2.7V, switch mode		0.58	0.9	Ω
		V_{L_IN} = 1.8V, switch mode		0.89	1.35	Ω
Thermal-Shutdown Temperature	T_{SHDN_LDO}			150		°C
Thermal-Shutdown Temperature Hysteresis	$T_{SHDN\_HYST\_LDO}$			16		°C
Output Noise	OUT_{NOISE}	10Hz to 100kHz, V_{L_IN} = 5V, V_{L_OUT} = 3.3V		110		µVRMS
		10Hz to 100kHz, V_{L_IN} = 5V, V_{L_OUT} = 2.5V		95		
		10Hz to 100kHz, V_{L_IN} = 5V, V_{L_OUT} = 1.2V		60		
		10Hz to 100kHz, V_{L_IN} = 5V, V_{L_OUT} = 0.8V		60		

Electrical Characteristics (continued)

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHGIN TO SYS PATH (V_{CHGIN} = 5.0V, V_{SYS} = V_{SYS_REG}.) (Note 1)						
Allowed CHGIN Input Voltage Range	V_{CHGIN_RNG}		-5.5		28	V
Allowed BAT Voltage Range	V_{BAT_RNG}		0		5.5	V
V_{CHGIN} Detect Threshold	V_{CHGIN_DET}	Rising	3.8	3.9	4.1	V
		Falling	3.0	3.1	3.2	
V_{CHGIN} Overvoltage Threshold	V_{CHGIN_OV}	Rising	7.2	7.5	7.8	V
V_{CHGIN} Overvoltage Threshold Hysteresis	$V_{CHGIN\_OV\_HYS}$			200		mV
V_{CHGIN} Valid Trip Point	$V_{CHGIN-SYS\_TP}$	V_{CHGIN} - V_{SYS}, rising, V_{BAT} = 4V	45	145	280	mV
V_{CHGIN} Valid Trip-Point Hysteresis	$V_{CHGIN-SYS\_TP\_HYS}$			200		mV
Input Limiter Current	I_{LIM}	ILimCntl[1:0] = 00		0		mA
		ILimCntl[1:0] = 01		90		
		ILimCntl[1:0] = 10		450		
		ILimCntl[1:0] = 11		1000		
Internal CAP Regulator	V_{CAP}	V_{CHGIN} = 5V	3.9	4.2	4.7	V
SYS Regulation Voltage	V_{SYS_REG}	V_{CHGIN} = 5V, I_{SYS} = 1mA	4.55	4.65	4.75	V
SYS Regulation Voltage Dropout	$V_{CHGIN-SYS}$	V_{CHGIN} = 4V, I_{SYS} = 1mA		40		mV
CHGIN-to-SYS On-Resistance	$R_{CHGIN-SYS}$	V_{CHGIN} = 4.4V, I_{SYS} = 400mA		0.370	0.66	Ω
Thermal-Shutdown Temperature	T_{CHGIN_SHDN}	(Note 4)		+150		°C
Thermal-Shutdown Temperature Hysteresis	$T_{CHGIN\_SHDN\_HYS}$			20		°C
Input Current Soft-Start Time	t_{SFST_LIM}			1		ms
Internal Supply Switchover Threshold	V_{CCINT_TH}	V_{CHGIN} = V_{CAP} rising, V_{BAT} = 4.2V	2.5	2.8	3.0	V

Electrical Characteristics (continued)

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SYS, BATTERY, AND V_{CCINT} UVLOs						
SYS UVLO Threshold	$V_{SYSUVLO\_R}$	Rising		2.644	2.69	V
	$V_{SYSUVLO\_F}$	Falling	2.57	2.618	2.67	V
SYS UVLO Threshold Hysteresis	$V_{SYSUVLO\_HYS}$	Hysteresis		26		mV
SYS UVLO Falling Debounce Time	$t_{SYSUVLO\_FDEB}$	SYS falling		20		µs
V_{CCINT} UVLO Threshold (POR)	V_{UVLO}	V_{CCINT} rising	0.8	1.82	2.6	V
V_{CCINT} UVLO Threshold Hysteresis	V_{UVLO_HYS}			140		mV
BAT UVLO Threshold	V_{BAT_UVLO}	Rising (valid only when CHGIN is present, when $V_{BAT} < V_{BAT\_UVLO}$, the BAT-SYS switch opens and BAT is connected to SYS through a diode.)	1.9	2.05	2.2	V
BAT UVLO Threshold Hysteresis	$V_{BAT\_UVLO\_HYS}$	Hysteresis		50		mV
BATTERY CHARGER (V_{BAT} = 4.2V. Typical values are at V_{CHRGIN} = 5.0V, V_{SYS} = V_{SYS_REG}.)						
BAT-to-SYS On-Resistance	$R_{BAT-SYS}$	V_{BAT} = 4.2V, I_{BAT} = 300mA		80	140	mΩ
Current Reduce Thermal Threshold Temperature	T_{CHG_LIM}	(Note 5)		120		°C
BAT-to-SYS Switch On Threshold	$V_{BAT-SYS-ON}$	SYS falling	10	22	35	mV
BAT-to-SYS Switch Off Threshold	$V_{BAT-SYS-OFF}$	SYS rising	-3	-1.5	0	mV
SYS Threshold Voltage Charger Limiting Current	V_{SYS_LIM}	Threshold at which the charger starts to limit the current due to SYS falling		4.36		V
FChg-MtChg Threshold	$V_{FCHG-MTCHG}$	If V_{SYS} drops below this value the charger will not move to maintain charge		4.49		V
FChg-MtChg Threshold Hysteresis	$V_{FCHG-MTCHG\_HYS}$			50		mV
Charger Current Soft-Start Time	t_{CHG_SOFT}			1		ms
PRECHARGE						
Precharge Current	I_{PCHG}	IPChg = 00		5		%IFChg
		IPChg = 01	9	10	11	
		IPChg = 10		20		
		IPChg = 11		30		

Electrical Characteristics (continued)

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Prequalification Threshold	V_{BAT_PChg}	VPChg = 000, V_{BAT} rising			2.1		V
		VPChg = 001, V_{BAT} rising		2.15	2.25	2.35	
		VPChg = 010, V_{BAT} rising			2.40		
		VPChg = 011, V_{BAT} rising			2.55		
		VPChg = 100, V_{BAT} rising			2.7		
		VPChg = 101, V_{BAT} rising			2.85		
		VPChg = 110, V_{BAT} rising			3.0		
		VPChg = 111, V_{BAT} rising			3.15		
Prequalification Threshold Hysteresis	$V_{BAT\_PChg\_HYS}$				90		mV
FAST CHARGE							
SET Current Gain Factor	K_{SET}				2000		A/A
SET Regulation Voltage	V_{SET}				1		V
Fast-Charge Current	I_{FChg}	R_{SET} = 400kΩ			5		mA
		R_{SET} = 40kΩ		45	50	55	
		R_{SET} = 4kΩ			500		
1/2 Fast-Charge Current Comparator Threshold	I_{FC_HALF}				50		%IFChg
1/5 Fast-Charge Current Comparator Threshold	I_{FC_FIFTH}				20		%IFChg
MAINTAIN CHARGE							
Charge Done Qualification	I_{Chg_DONE}	ChgDone = 00			5		%IFChg
		ChgDone = 01		8.5	10	11.5	
		ChgDone = 10			20		
		ChgDone = 11			30		
BAT Regulation Voltage	V_{BatReg}	BatReg = 000			4.05		V
		BatReg = 001			4.10		
		BatReg = 010			4.15		
		BatReg = 011	T_A = +25°C	4.179	4.2	4.221	
			T_A = -40°C to +85°C	4.158	4.2	4.242	
		BatReg = 100			4.25		
		BatReg = 101			4.3		
		BatReg = 110	T_A = +25°C	4.32	4.35	4.38	
			T_A = -40°C to +85°C	4.30	4.35	4.40	
BAT Recharge Threshold	$V_{BatReChg}$	BatReChg = 00			70		mV
		BatReChg = 01			120		
		BatReChg = 10			170		
		BatReChg = 11			220		

Electrical Characteristics (continued)

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CHARGER TIMER						
Maximum Prequalification Time	t_{PChg}	PChgTmr = 00		30		min
		PChgTmr = 01		60		
		PChgTmr = 10		120		
		PChgTmr = 11		240		
Maximum Fast-Charge Time	t_{FChg}	FChgTmr = 00		75		min
		FChgTmr = 01		150		
		FChgTmr = 10		300		
		FChgTmr = 11		600		
Maintain-Charge Time	t_{MTChg}	TOChgTmr = 00		0		min
		TOChgTmr = 01		15		
		TOChgTmr = 10		30		
		TOChgTmr = 11		60		
Timer Accuracy	t_{CHG_ACC}		-10		+10	%
Timer Extend Threshold	TIM_{EXD_THRES}	If charge current is reduced due to I_{LIM} or TDIE, this is the percentage of charge current below which timer clock operates at half speed		50		%
Timer Suspend Threshold	TIM_{SUS_THRES}	If charge current is reduced due to I_{LIM} or TDIE, this is the percentage of charge current below which timer clock pauses		20		%
THERMISTOR MONITOR AND NTC DETECTION (RPU = 10k, RTHM = 10k, 3380ß)						
THM Hot Threshold	T_4	V_{THM} falling	21.3	23.3	25.3	%CAP
THM Warm Threshold	T_3	V_{THM} falling	30.9	32.9	34.9	
THM Cool Threshold	T_2	V_{THM} rising	62.5	64.5	66.5	
THM Cold Threshold	T_1	V_{THM} rising	71.9	73.9	75.9	
THM Disable Threshold	THM_{DIS}	V_{THM} rising	91	93	95	
THM Threshold Hysteresis	THM_{HYS}			60		mV
THM Input Leakage	I_{LKG_THM}		-1		+1	µA

Electrical Characteristics (continued)

(V_{CHGIN} = 5.0V, V_{BAT} = 3.7V, T_A = -40°C to +85°C, all registers in their default state, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DIGITAL SIGNALS						
PFN1 PFN2 Button Timer Accuracy			-10		+10	%
Input Logic-High (SDA, SCL, MPC0, MPC1, PFN1, PFN2)	V_{IH}		1.4			V
Input Logic-Low (SDA, SCL, MPC0, MPC1, PFN1, PFN2)	V_{IL}				0.5	V
Output Logic-Low (SDA, $\overline{RST}$, $\overline{INT}$, LED, PFN2)	V_{OL}	I_{OL} = 4mA			0.4	V
High Level Leakage Current (SDA, $\overline{RST}$, $\overline{INT}$, LED, PFN2)	I_{LK}		-1		+1	µA
SCL Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and START Condition	t_{BUF}		1.3			µs
START Condition (Repeated) Hold-Time	$t_{HD:STA}$	(Note 6)	0.6			µs
Low Period of SCL Clock	t_{LOW}		1.3			µs
High Period of SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$	(Notes 7)	0		0.9	µs
Data Setup Time	$t_{SU:DAT}$	(Note 7)	100			ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Spike Pulse Widths Suppressed by Input Filter	t_{SP}	(Note 8)		50		ns

Note 1: All devices are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.

Note 2: For input voltages larger than 4.4V, output regulated voltage below 1V are available ONLY in burst mode.

Note 3: This value is included in the I_{BAT} quiescent current values for the on states.

Note 4: When the die temperature exceeds T_{CHGIN_SHDN}, the CHGIN-to-SYS path, and the charger is turned off.

Note 5: When the die temperature exceeds T_{CHG_LIM}, the charger current starts to decrease.

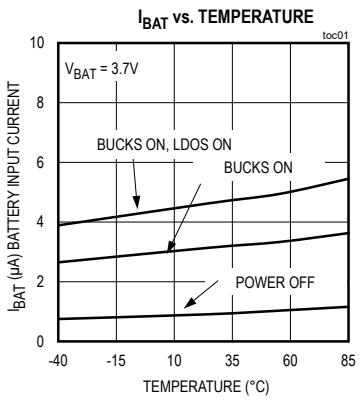
Note 6: f_{SCL} must meet the minimum clock low time plus the rise/fall times.

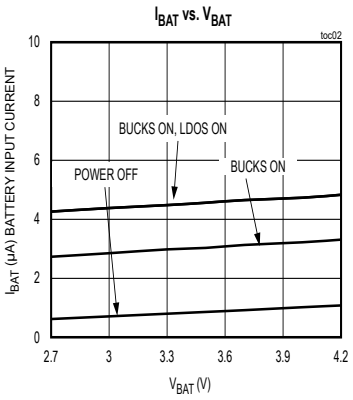
Note 7: The maximum $t_{HD:DAT}$ has to be met only if the device does not stretch the low period (t_{LOW}) of the SCL signal.

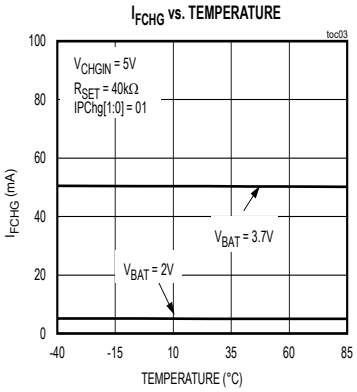
Note 8: Filters on SDA and SCL suppress noise spikes at the input buffers and delay the sampling instant.

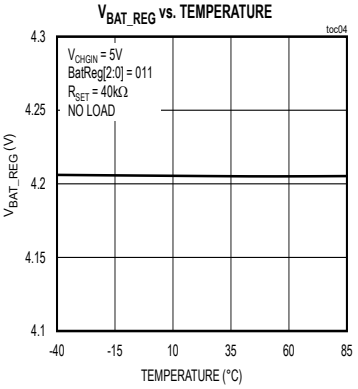
Typical Operating Characteristics

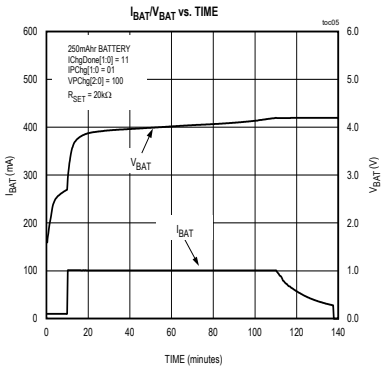
(V_{BAT} = 3.7V, V_{CHGIN} = 0V, registers in their default state, T_A = +25°C, unless otherwise noted.)

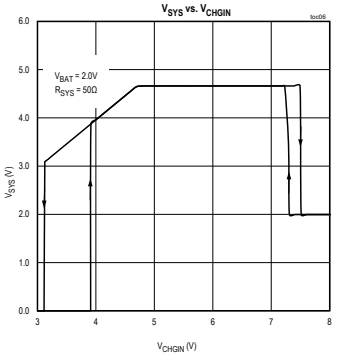


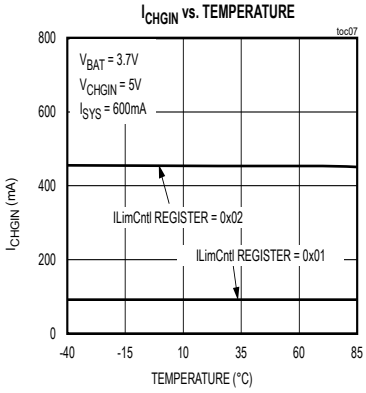


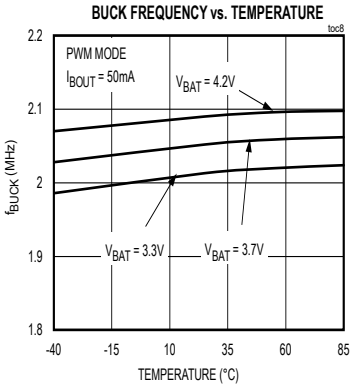






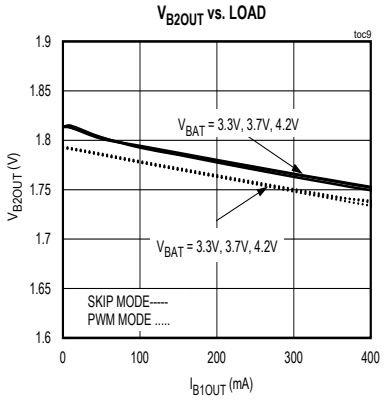


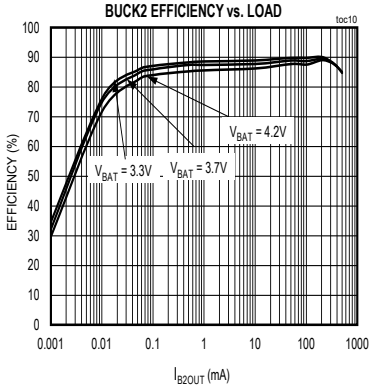


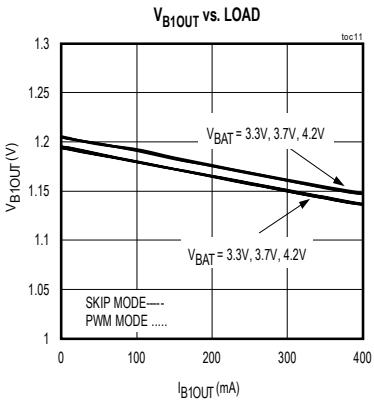


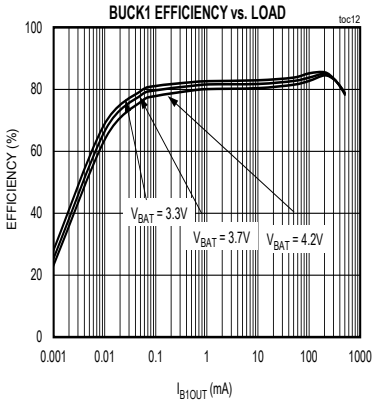
Typical Operating Characteristics (continued)

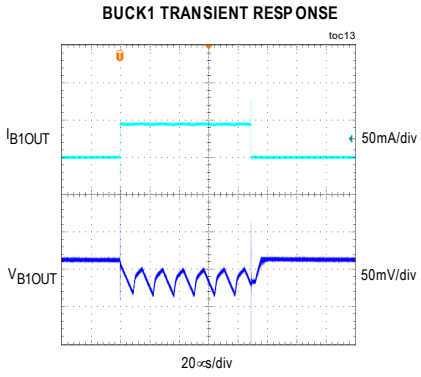
(V_{BAT} = 3.7V, V_{CHGIN} = 0V, registers in their default state, T_A = +25°C, unless otherwise noted.)

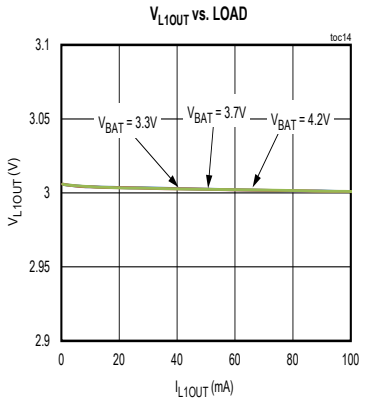


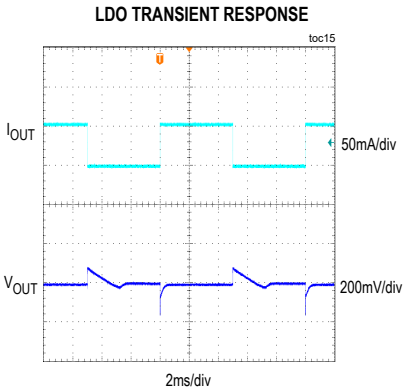


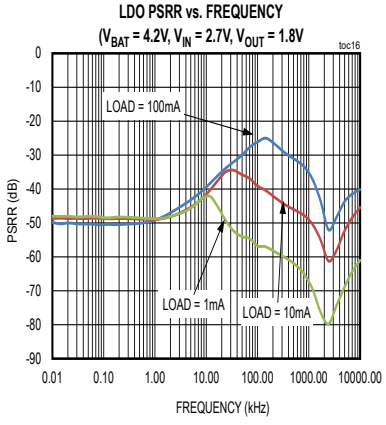


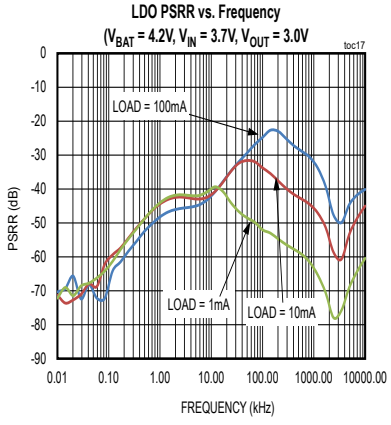




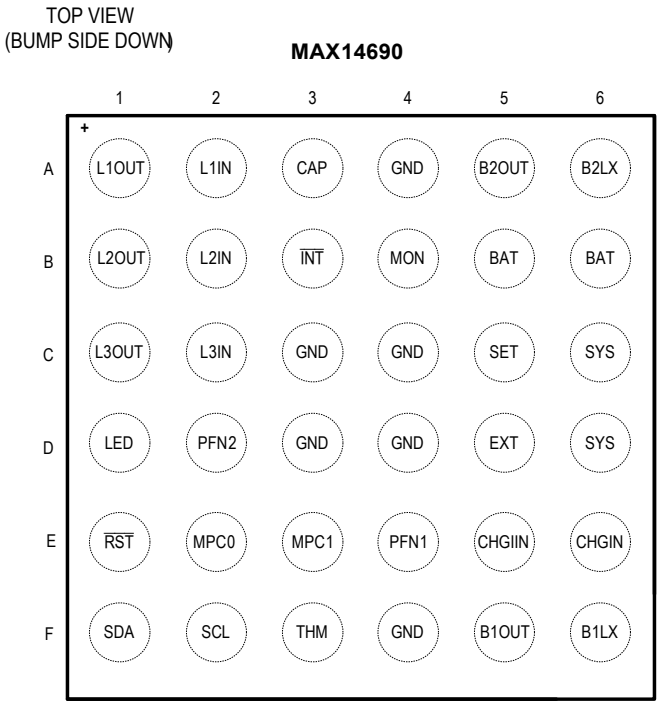








Pin Configuration



WLP
(2.72mm x 2.47mm)

Bump Description

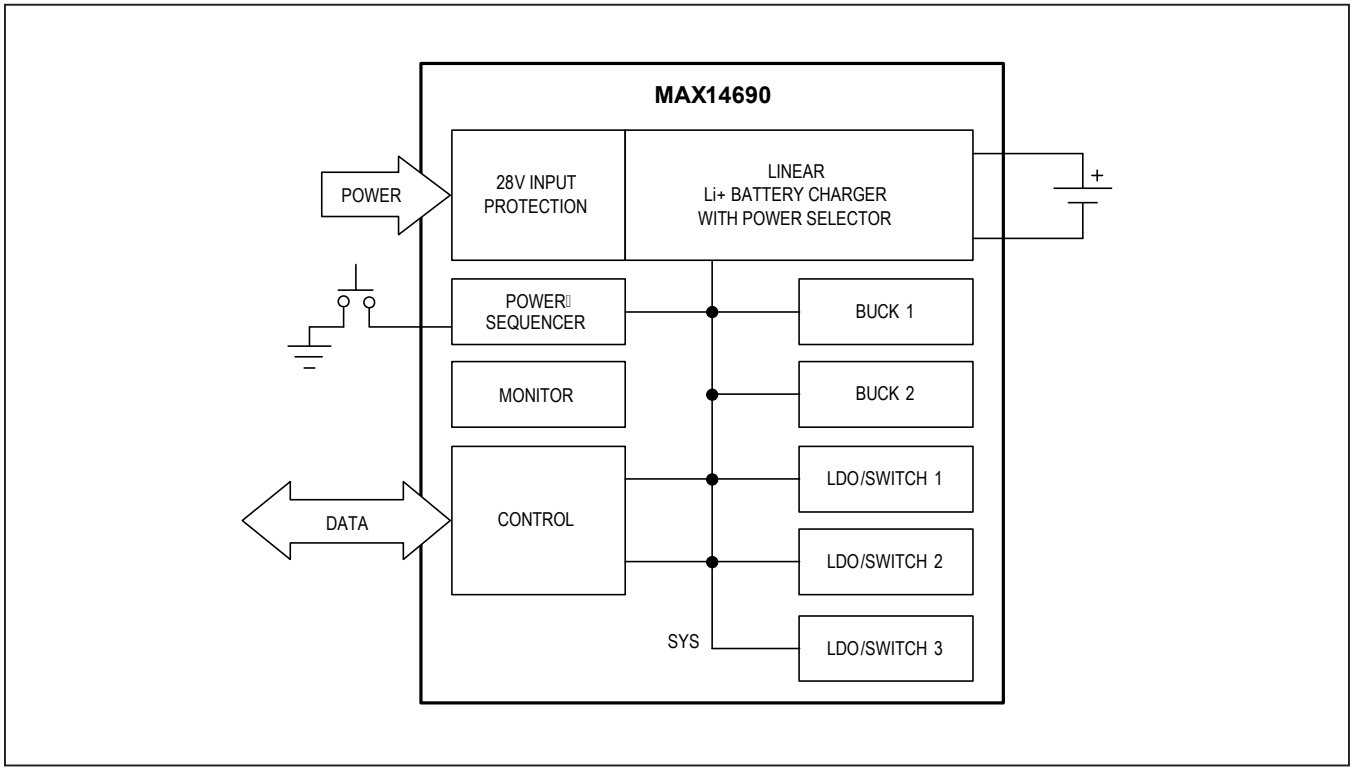
BUMP	NAME	FUNCTION
A1	L1OUT	LDO1 Output. Bypass with a minimum 1µF capacitor to GND.
A2	L1IN	LDO1 Input
A3	CAP	Bypass for Internal LDO. Bypass with a 1µF capacitor to GND.
A4, C3, C4 D3, D4, F4	GND	Ground
A5	B2OUT	1.5V – 3.3V Buck Regulator Output Feedback. Bypass with a minimum 10µF capacitor to GND.
A6	B2LX	1.5V – 3.3V Buck Regulator Switch. Connect 2.2µH inductor to B2OUT.
B1	L2OUT	LDO2 Output. Bypass with a minimum 1µF capacitor to GND.
B2	L2IN	LDO2 Input
B3	$\overline{INT}$	Open-Drain, Active-Low Interrupt Output.
B4	MON	Voltage Monitor Pin
B5,B6	BAT	Battery Connection. Connect BAT to a positive battery terminal, bypass BAT with a minimum 1µF capacitor to GND.

Pin Description (continued)

PIN	NAME	FUNCTION
C1	L3OUT	LDO3 Output. Bypass with a minimum 1µF capacitor to GND.
C2	L3IN	LDO3 Input
C5	SET	External Resistor For Battery Charge Current Level Setting. Do not connect any external capacitance on this pin; maximum allowed capacitance (C_{SET} < 5µs/R_{SET}) pF.
C6, D6	SYS	System Load Connection. Connect SYS to the system load. Bypass SYS with a minimum 10µF low-ESR ceramic capacitor to GND.
D1	LED	LED Open-Drain Pulldown Current. Add an external current limiting pullup resistor.
D2	PFN2	Power Function Control Input/Output. Programmable functionality via PwrFnMode. See Table 1.
D5	EXT	Push-Pull Gate Drive for Optional External pFET from BAT-to-SYS. Output is pulled to GND when charger is disconnected and internal BAT-SYS FET is switched on. Otherwise, this output is pulled high to the SYS voltage.
E1	$\overline{RST}$	Power-On Reset Output. Active-low, open-drain.
E2	MPC0	Multipurpose Configuration Input 0
E3	MPC1	Multipurpose Configuration Input 1
E4	PFN1	Power Function Control Input. Programmable functionality via PwrFnMode. See Table 1.
E5, E6	CHGIN	+28V Protected Charger Input. Bypass CHGIN with 1µF capacitor to GND.
F1	SDA	Open-Drain, I^2C Serial Data Input/Output.
F2	SCL	I^2C Serial Clock Input
F3	THM	Battery Temperature Thermistor Measurement Connection. Connect a 10kΩ resistor from THM to CAP and a 10kΩ, 3380A NTC thermistor from THM to GND.
F5	B1OUT	0.8V – 1.8V Buck Regulator Output Feedback. Bypass B1OUT with a minimum 10µF capacitor to GND.
F6	B1LX	0.8V – 1.8V Buck Regulator Switch Terminal. Connect B1LX to B1OUT with a 2.2µH inductor.

Note: *All capacitance values listed in this document refer to effective capacitance. Be sure to specify capacitors that will meet these requirements under typical system operating conditions taking into consideration the effects of voltage and temperature.*

Block Diagram



Detailed Description

Power Regulation

The MAX14690 family includes two high-efficiency, low quiescent current buck regulators, and three low quiescent current linear regulators that are also configurable as power switches. Excellent light-load efficiency allows the switching regulators to run continuously without significant energy cost. The standard operating mode for the buck regulators is burst mode, but they can be forced to operate in PWM mode through an I^2C register.

Power On/Off and Reset Control

The behavior of power function control pins (PFN1 and PFN2) is preconfigured to support one of the multiple types of wearable application cases. Table 1 describes the behavior of the PFN1 and PFN2 pins based on the PwrRstCfg[3:0] bits and Figure 1 shows basic flow diagrams associated with each mode.

A soft reset will reset all register values and pulls the $\overline{RST}$ line low. Hard reset initiates a complete Power-On Reset sequence.

Table 1. Power Function Input Control Modes

PwrRstCfg [3:0]	PFN1	PFN1 PU/PD PFNxResEna = 1 (0x1D[7])	PFN2	PFN2 PU/PD PFNxResEna = 1 (0x1D[7])	NOTES
0000	Enable	Pulldown	Active-Low Manual Reset	Pullup*	On/off Mode with 10ms debounce. Active-high on/off control on PFN1. Logic-low on PFN2 generates 10ms pulse on $\overline{RST}$. Note that, in this mode, the PWR_OFF_CMD in I^2C has no effect.
0001	Disable	Pullup*	Active-Low Manual Reset	Pullup*	On/off Mode with 10ms debounce. Active-low on/off control on PFN1. Logic-low on PFN2 generates 10ms pulse on $\overline{RST}$. Note that, in this mode, the PWR_OFF_CMD in I^2C has no effect.
0010	Hard-Reset on Rising Edge	Pulldown	Soft-Reset on Rising-Edge	Pulldown	Always-On Mode (i.e., device can only be put in off state through PWR_OFF_CMD). 50ms hard-reset off time. 10ms soft-reset pulse time. 200ms delay prior to both reset behaviors.
0011	Hard-Reset on Falling Edge	Pullup*	Soft-Reset Falling-Edge	Pullup*	Always-On Mode (i.e., device can only be put in off state via PWR_OFF_CMD). 50ms hard-reset off time. 10ms soft-reset pulse time. 200ms delay prior to both reset behaviors.
0100	Hard-Reset After CHGIN Attach When High	Pulldown	Soft-Reset After CHGIN Attach When High	Pulldown	Charger Reset High Mode (i.e., device can only be put in off state through PWR_OFF_CMD). 50ms hard-reset off time. 10ms soft-reset pulse time. 200ms delay prior to both reset behaviors.
0101	Hard-Reset After CHGIN Attach When Low	Pullup*	Soft-Reset After CHGIN Attach When Low	Pullup*	Charger Reset Low Mode (i.e., device can only be put in off state through PWR_OFF_CMD). 50ms hard-reset off time. 10ms soft-reset pulse time. 200ms delay prior to both reset behaviors.
0110	$\overline{KIN}$	Pullup*	$\overline{KOUT}$	None	On/Off mode through specific long-press button timing or PWR_OFF_CMD.
0111	$\overline{KIN}$	Pullup*	$\overline{KOUT}$	None	Custom Soft-Reset. Off mode through PWR_OFF_CMD (30ms delay). On mode through specific long-press (3s) or CHGIN insertion. Soft-reset through specific long press (12s).
1000-1111	—	—	—	—	Reserved

** Pullup is connected to V_{CCINT}.*

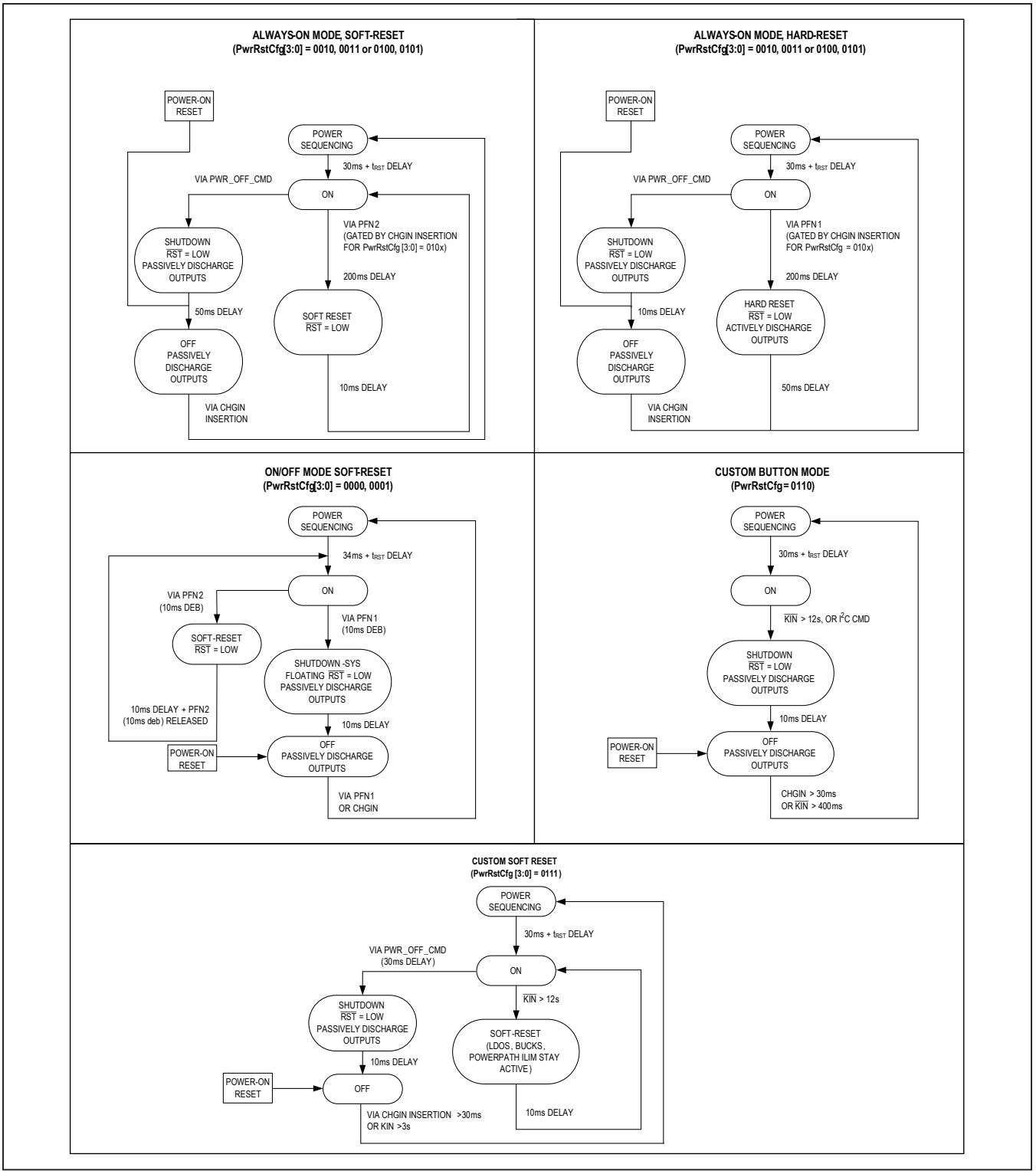


Figure 1. Power Function Input Control Modes Flow Diagrams

Power Sequencing

The sequencing of the buck regulators and LDOs during power-on is configurable. See Table 1 for details. Regulators can be configured to turn on at one of three points during the power-on process: 34ms after the power-on event, after the $\overline{RST}$ signal is released, or at two points in between. The two points between SYS and $\overline{RST}$ are fixed proportionally to the duration of the Power-On Reset (POR) process, but the overall time of the reset delay is configurable (80ms, 120ms, 220ms, 420ms). The timing relationship is presented graphically in Figure 2.

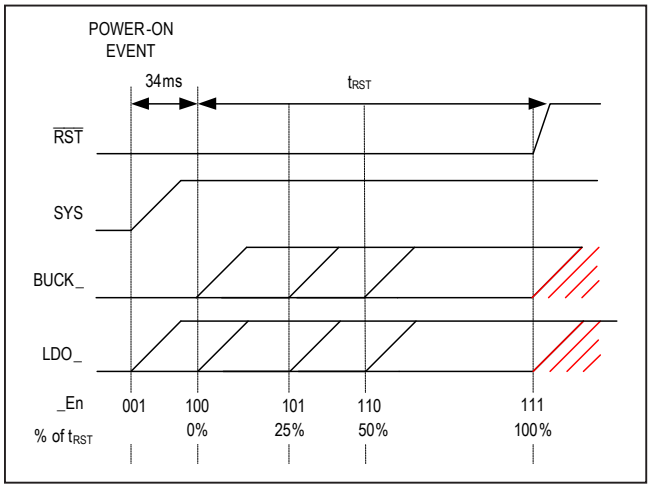


Figure 2. Reset Sequence Programming

Additionally, the regulators can be selected to default off and can be turned on with an I²C command after $\overline{RST}$ is released. Each LDO regulator can be configured to be always-on as long as SYS or BAT is present.

The SYS voltage is monitored during the power-on sequence. If an undervoltage condition is detected on SYS during the sequencing process with a valid voltage at CHGIN, the process repeats from the point where SYS was enabled to allow more time for the voltage to stabilize. If there is not a valid voltage at CHGIN, the device returns to the off state to avoid draining the battery. Power is also turned off if an undervoltage condition is detected on SYS.

Smart Power Selector

The smart power selector seamlessly distributes power from the external CHGIN input to the battery (BAT) and the system (SYS). With both an external adapter and battery connected, the smart power selector basic functions are:

- When the system load requirements are less than the input current limit, the battery is charged with residual power from the input.
- When the system load requirements exceed the input current limit, the battery supplies supplemental current to the load.
- When the battery is connected and there is no external power input, the system is powered from the battery.

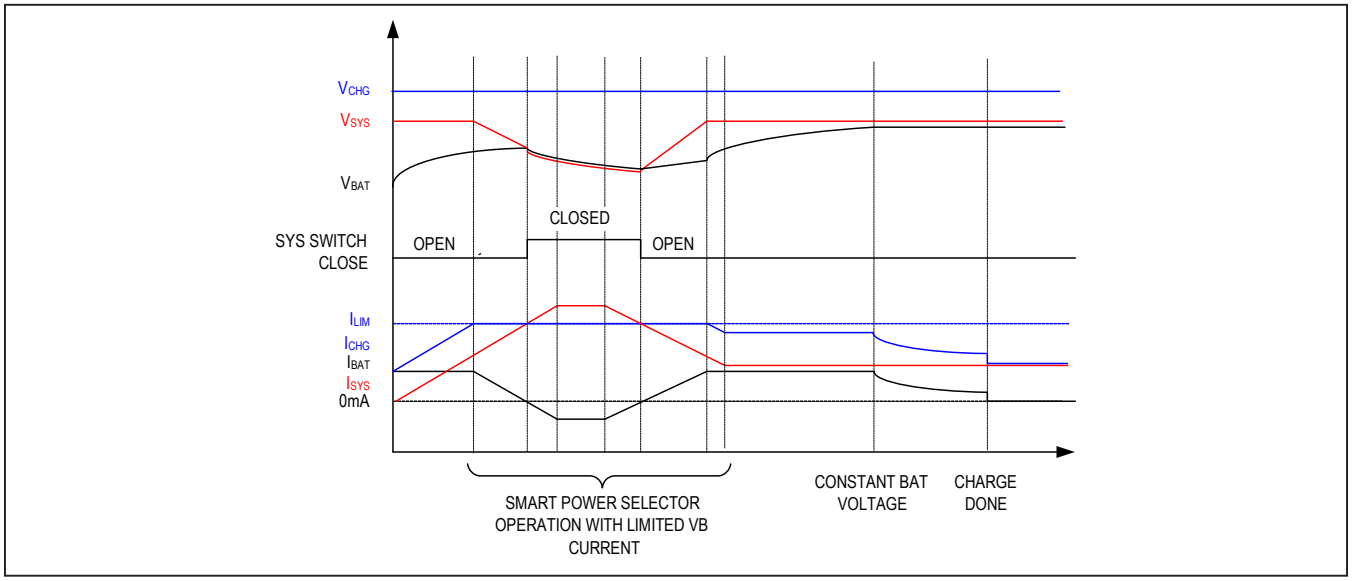


Figure 3. Smart Power Selector Current/Voltage Behavior

Thermal Current Regulation

In case the die temperature exceeds the normal limit, the MAX14690 will attempt to limit the temperature increase by reducing the input current from CHGIN. In this condition, the system load has priority over charger current, so the input current is first reduced by lowering the charge current. If the junction temperature continues to rise and reaches the maximum operating limit, no input current is drawn from CHGIN and the battery powers the entire system load.

System Load Switch

An internal 80mΩ (typ) MOSFET connects SYS to BAT when no voltage source is available on CHGIN. When an external source is detected at CHGIN, this switch opens and SYS is powered from the input source through the input current limiter. The SYS-to-BAT switch also prevents V_{SYS} from falling below V_{BAT} when the system load exceeds the input current limit. If V_{SYS} drops to V_{BAT} due to the current limit, the load switch turns on so the load is supported by the battery. If the system load continuously exceeds the input current limit the battery is not charged. This is useful for handling loads that are nominally below the input current limit but have high current peaks exceeding the input current limit. During these peaks, battery energy is used, but at all other times the battery charges. See Figure 3.

The pin EXT can drive the gate of an external pMOS connected between SYS (source, bulk) and BAT (drain) in parallel to the internal one.

EXT voltage is the buffered version of the internal gate command that controls the internal 80mΩ (typ) MOSFET.

Note: The body diode of an external pMOS connected between BAT and SYS remains present when the device is in off mode.

Input Limiter

The input limiter distributes power from the external adapter to the system load and battery charger. In addition to the input limiter's primary function of passing power to the system load and charger, it performs several additional functions to optimize use of available power:

Invalid CHGIN Voltage Protection: If CHGIN is above the overvoltage threshold, the MAX14690 enters overvoltage lockout (OVL). OVL protects the MAX14690 and downstream circuitry from high-voltage stress up to 28V and down to -5.5V. During OVL, the internal circuit remains powered and an interrupt is sent to the host. During OVL, the charger turns off and the system load switch closes, allowing the battery to power SYS. CHGIN is also invalid if it is less than V_{BAT}, or less than the USB undervoltage threshold. With an invalid input voltage, the SYS-to-BAT load switch closes and allows the battery to power SYS.

CHGIN Input Current Limit: The CHGIN input current is limited to prevent input overload. The input current limit is controlled by I^2C.

Thermal Limiting: In case the die temperature exceeds the normal limit (T_{CHG_LIM}), the MAX14690 attempts to limit temperature increase by reducing the input current from CHGIN. In this condition, the system load has priority over the charger current, so the input current is first reduced by lowering the charge current. If the junction temperature continues to rise and reaches the maximum operating limit (T_{CHGIN_SHDN}), no input current is drawn from CHGIN and the battery powers the entire system load.

Adaptive Battery Charging: While the system is powered from CHGIN, the charger draws power from SYS to charge the battery. If the total load exceeds the input current limit, an adaptive charger control loop reduces charge current to prevent V_{SYS} from collapsing.

When the charge current is reduced below 50% due to I_{LIM} or T_{DIE}, the timer clock operates at half speed. When the charge current is reduced below 20% due to I_{LIM} or T_{DIE}, the timer clock is paused.

Fast-Charge Current Setting

The MAX14690 uses an external resistor connected from SET to GND to set the fast-charge current. The pre-charge and charge-termination currents are programmed as a percentage of this value via I^2C registers. The fast-charge current resistor can be calculated as:

$$R_{SET} = K_{SET} \times V_{SET}/I_{FChg}$$

where K_{SET} has a typical value of 2000A/A and V_{SET} has a typical value of 1V. The range of acceptable resistors for R_{SET} is 4kΩ to 400kΩ.

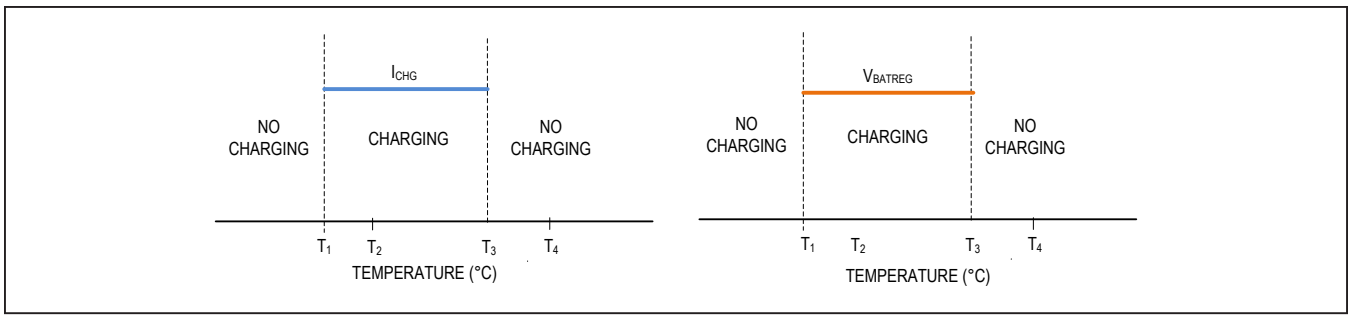


Figure 4a. Charging Behavior Using Thermistor Monitor

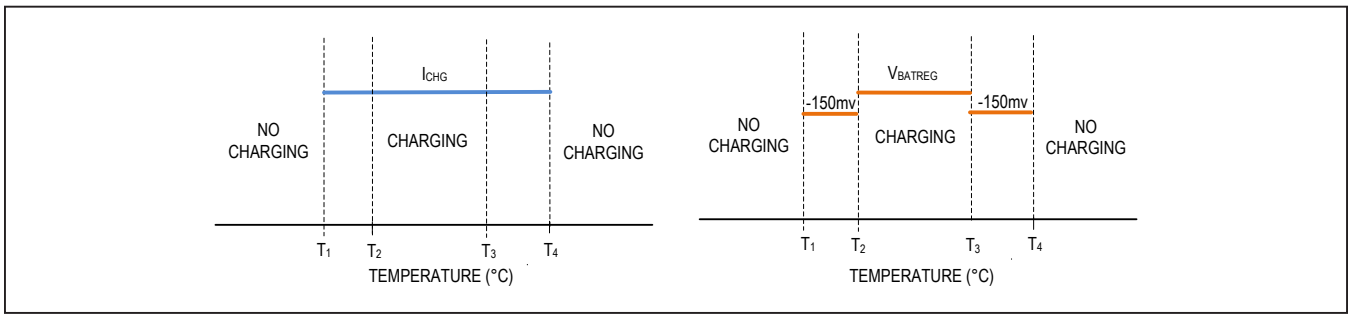


Figure 4b. Charging Behavior Using JEITA Monitor

Table 2. Thermistor Monitoring/JEITA Monitoring Enable Control

ThermEn	JEITAEn	FUNCTION
0	—	Thermistor/JEITA Monitoring Off
1	0	Thermistor Monitoring On
1	1	JEITA Monitoring On

Thermistor/JEITA Monitoring with Charger Shutdown

The MAX14690 includes thermistor and JEITA monitoring to enhance safety when charging Li+ batteries. The battery pack temperature is measured from a divider formed by a pullup resistor connected to CAP and the battery-pack thermistor. The THM pin measures the voltage across the resistor divider and converts it to temperature. There are five temperature zones that can be read from the ThermStat bits in I²C. When thermistor monitoring is enabled, the charger is disabled for temperatures below T1 or above T3, as shown in Figure 4a. When JEITA monitoring is enabled, the charger will be disabled for temperatures below T1 or above T4, as shown in Figure 4b. See Table 2 and Table 3 on configuring the thermistor/JEITA monitoring.

Table 3. Voltage and Example Temperature Thresholds

	%CAP Thresholds on THM	Temperature Thresholds R_{PU} = 10k, R_{THM} = 10k (β = 3380)
T1	73.9	0°C
T2	64.5	10°C
T3	32.9	45°C
T4	23.3	60°C

I²C Interface

The MAX14690 uses the two-wire I²C interface to communicate with the host microcontroller. The configuration settings and status information provided through this interface are detailed in the register descriptions.

I²C Addresses

The registers of the MAX14690 are accessed through the slave address of 0101000 (0x50 for writes/0x51 for reads).

Thermistor Monitoring with Charger Shutdown

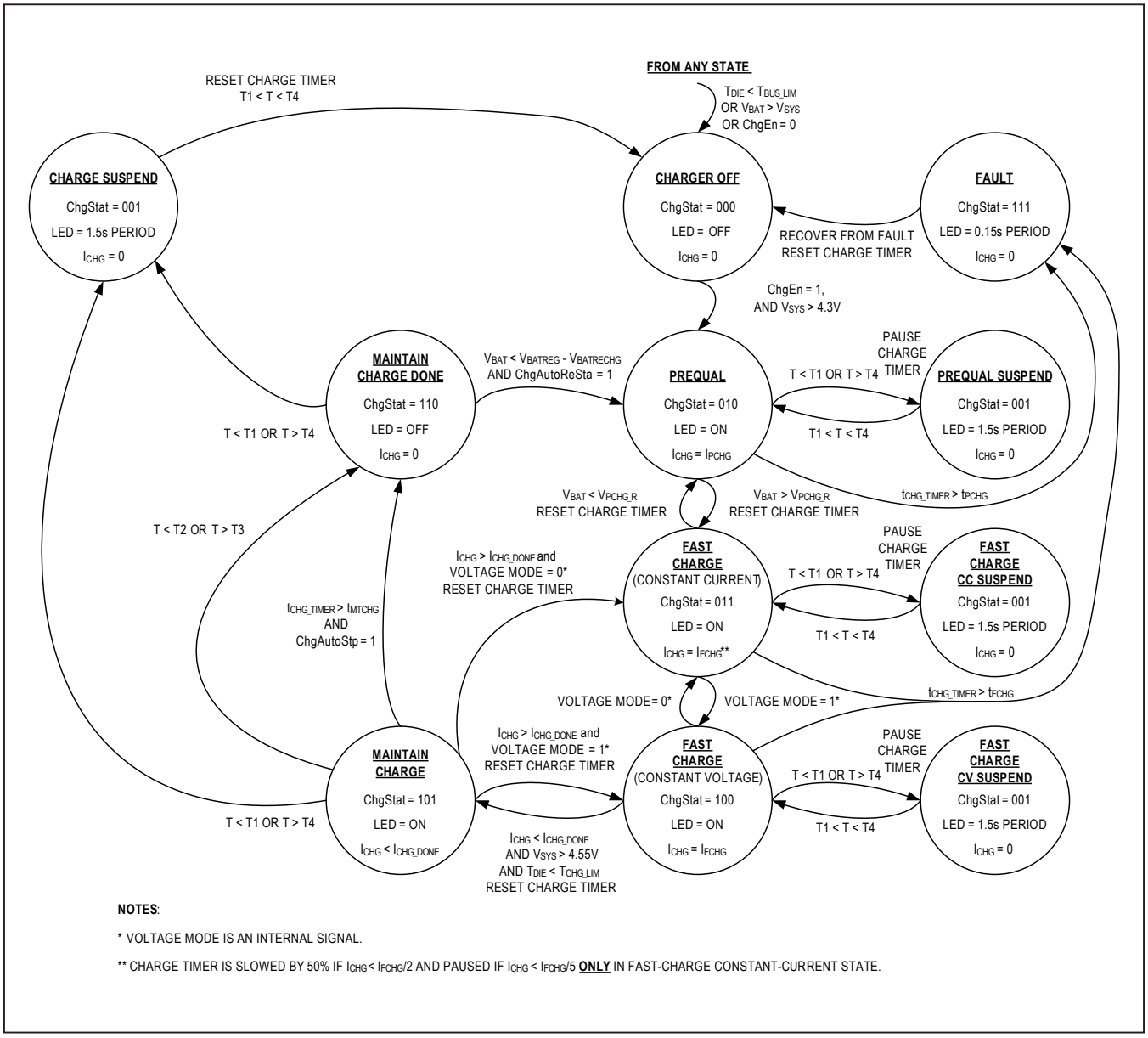


Figure 5. Battery Charger State Diagram

Applications Information

I²C Interface

The MAX14690_ contain an I²C-compatible interface for data communication with a host controller (SCL and SDA). The interface supports a clock frequency of up to 400kHz. SCL and SDA require pullup resistors that are connected to a positive supply.

Start, Stop, And Repeated Start Conditions

When writing to the MAX14690_ using I²C, the master sends a START condition (S) followed by the MAX14690_ I²C address. After the address, the master sends the register address of the register that is to be programmed. The master then ends communication by issuing a STOP condition (P) to relinquish control of the bus, or a REPEATED START condition (Sr) to communicate to another I²C slave. See Figure 6.

Table 4. I²C Slave Addresses

ADDRESS FORMAT	HEX	BINARY
7-Bit Slave ID	0x28	0101000
Write Address	0x50	01010000
Read Address	0x51	01010001

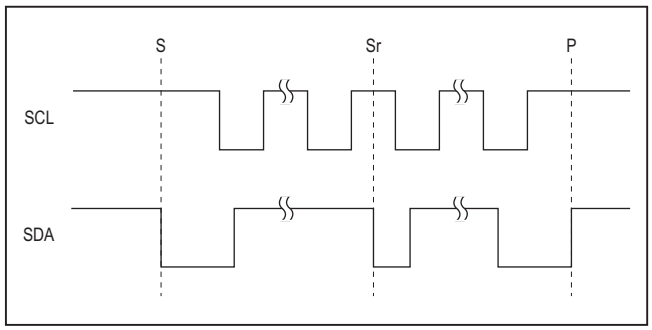


Figure 6. I²C START, STOP and REPEATED START Conditions

Slave Address

Set the Read/$\overline{\text{Write}}$ bit high to configure the MAX14690_ to read mode (Table 4). Set the Read/$\overline{\text{Write}}$ bit low to configure the MAX14690_ to write mode. The address is the first byte of information sent to the MAX14690_ after the START condition.

Bit Transfer

One data bit is transferred on the rising edge of each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high and stable are considered control signals (see the *Start, Stop, And Repeated Start Conditions* section). Both SDA and SCL remain high when the bus is not active.

Single-Byte Write

In this operation, the master sends an address and two data bytes to the slave device (Figure 7). The following procedure describes the single byte write operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends 8 data bits
- 7) The slave asserts an ACK on the data line
- 8) The master generates a STOP condition

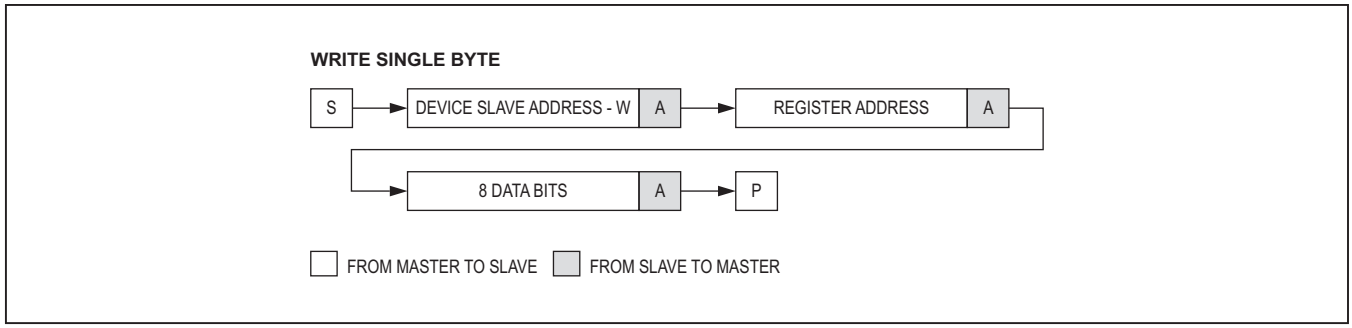


Figure 7. Write Byte Sequence

Burst Write

In this operation, the master sends an address and multiple data bytes to the slave device (Figure 8). The slave device automatically increments the register address after each data byte is sent, unless the register being accessed is 0x00, in which case the register address remains the same. The following procedure describes the burst write operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends eight data bits
- 7) The slave asserts an ACK on the data line
- 8) Repeat 6 and 7 N-1 times
- 9) The master generates a STOP condition

Single Byte Read

In this operation, the master sends an address plus two data bytes and receives one data byte from the slave device (Figure 9). The following procedure describes the single byte read operation:

- 1) The master sends a START condition
- 2) The master sends the 7-bit slave address plus a write bit (low)
- 3) The addressed slave asserts an ACK on the data line
- 4) The master sends the 8-bit register address
- 5) The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6) The master sends a REPEATED START condition
- 7) The master sends the 7-bit slave address plus a read bit (high)
- 8) The addressed slave asserts an ACK on the data line
- 9) The slave sends eight data bits
- 10) The master asserts a NACK on the data line
- 11) The master generates a STOP condition

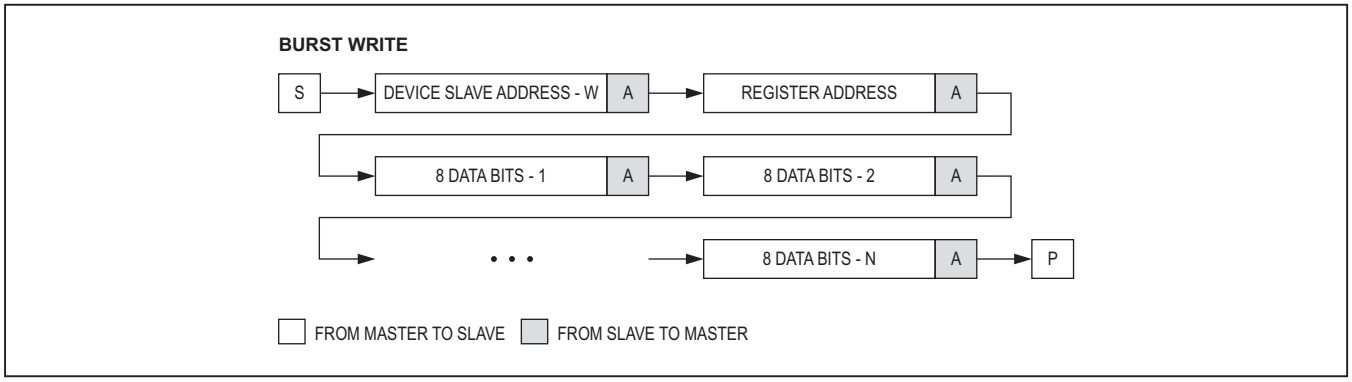


Figure 8. Burst Write Sequence

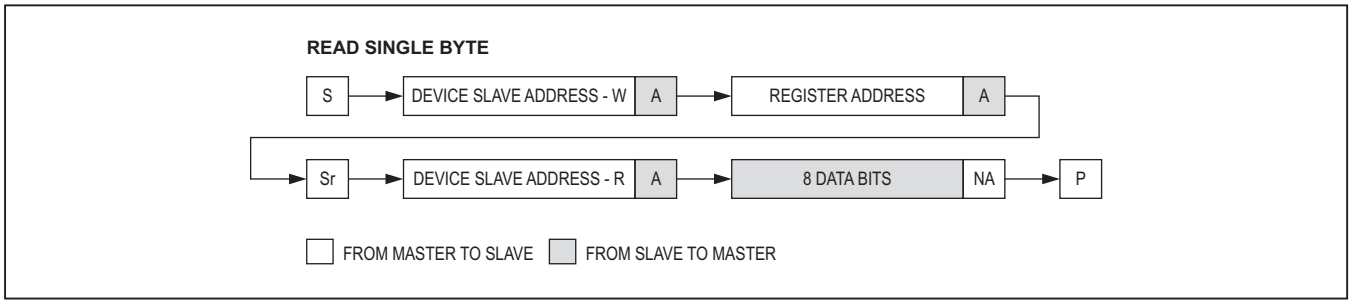


Figure 9. Read Byte Sequence

Burst Read

In this operation, the master sends an address plus two data bytes and receives multiple data bytes from the slave device (Figure 210). The following procedure describes the burst byte read operation:

- 1)The master sends a START condition
- 2)The master sends the 7-bit slave address plus a write bit (low)
- 3)The addressed slave asserts an ACK on the data line
- 4)The master sends the 8-bit register address
- 5)The slave asserts an ACK on the data line only if the address is valid (NAK if not)
- 6)The master sends a REPEATED START condition
- 7)The master sends the 7-bit slave address plus a read bit (high)
- 8)The slave asserts an ACK on the data line
- 9)The slave sends eight data bits
- 10) The master asserts an ACK on the data line
- 11) Repeat 9 and 10 N-2 times
- 12) The slave sends the last eight data bits
- 13) The master asserts a NACK on the data line
- 14) The master generates a STOP condition

Acknowledge Bits

Data transfers are acknowledged with an acknowledge bit (ACK) or a not-acknowledge bit (NACK). Both the master and the MAX14690_ generate ACK bits. To generate an ACK, pull SDA low before the rising edge of the ninth clock pulse and hold it low during the high period of the ninth clock pulse (see Figure 3a11). To generate a NACK, leave SDA high before the rising edge of the ninth clock pulse and leave it high for the duration of the ninth clock pulse. Monitoring for NACK bits allows for detection of unsuccessful data transfers.

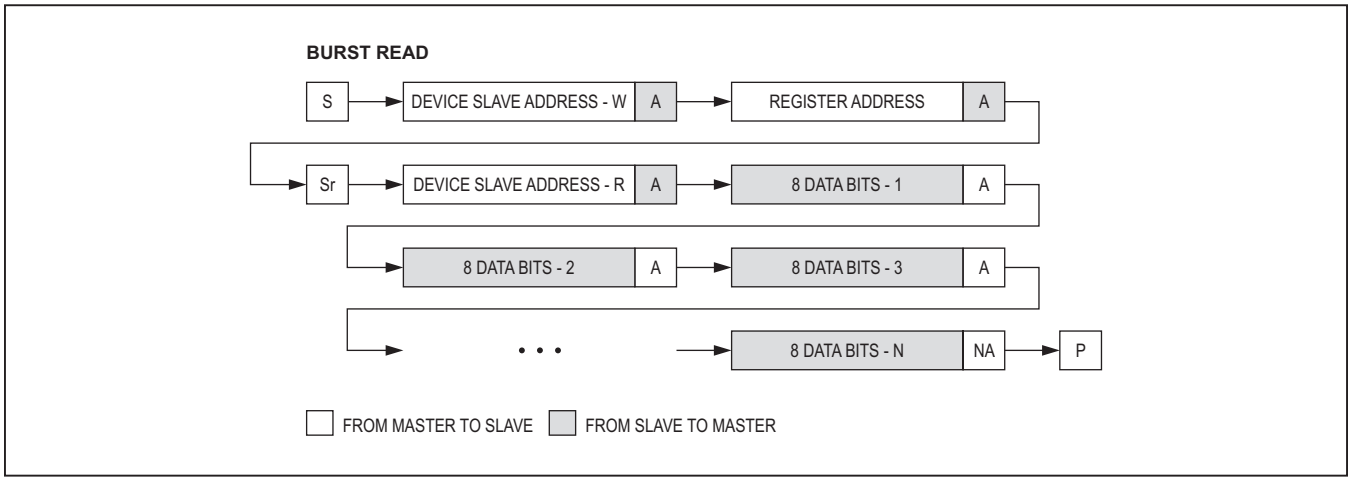


Figure 10. Burst Read Sequence

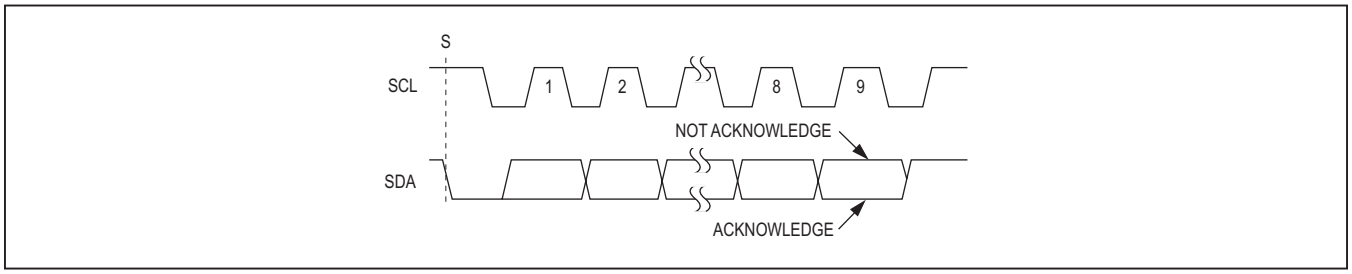


Figure 11. Acknowledge

I²C Register Map

REGISTER ADDRESS	REGISTER NAME	R/W	B7	B6	B5	B4	B3	B2	B1	B0
0x00	ChipId	R	Chip_Id[7:1,0] (Read-Only)							
0x01	ChipRev	R	Chip_Rev[7:0] (Read-Only)							
0x02	StatusA	R	—	—	ThermStat[2:0]			ChgStat[2:0]		
0x03	StatusB	R	—	—	ILim	UsbOVP	UsbOk	ChgThrmSd	ChgThrmReg	ChgTmo
0x04	StatusC	R	—	—	—	ThrmBk1	ThrmBk2	ThrmLDO1	ThrmLDO2	ThrmLDO3
0x05	IntA	COR	ThermStatInt	ChgStatInt	ILimInt	UsbOVPInt	UsbOkInt	ChgThrm SdInt	ChgThrm RegInt	ChgTmoInt
0x06	IntB	COR	—	—	—	ThrmBk1Int	ThrmBk0Int	ThrmLDO1Int	ThrmLDO2Int	ThrmLDO3Int
0x07	IntMaskA	R/W	Therm StatIntM	ChgStatIntM	ILimIntM	UsbOVPIntM	UsbOkIntM	ChgThrm SdIntM	ChgThrm RegIntM	ChgTmoIntM
0x08	IntMaskB	R/W	—	—	—	ThrmBk1IntM	Thrm Bk0IntM	Thrm LDO1IntM	Thrm LDO2IntM	Thrm LDO3IntM
0x09*	ILimCntl	R/W**	—	—	—	—	—	—	ILimCntl[1:0]	
0x0A*	ChgCntlA	R/W**	ChgAutoStp	ChgAuto ReSta	BatReChg[1:0]		BatReg[2:0]			ChgEn
0x0B*	ChgCntlB	R/W**	-	VPChg[2:0]			IPChg[1:0]		ChgDone[1:0]	
0x0C*	ChTmr	R/W**	—	—	MtChgTmr[1:0]		FChgTmr[1:0]		PChgTmr[1:0]	
0x0D	Buck1Cfg	R/W	Buck1Seq[2:0]			Buck1En[1:0]		Buck1Md[1:0]		Buck1Ind
0x0E	Buck1VSet	R/W**	—	—	Buck1VSet[5:0]					
0x0F	Buck2Cfg	R/W	Buck2Seq[2:0]			Buck2En[1:0]		Buck2Md[1:0		Buck2Ind
0x10	Buck2VSet	R/W**	—	—	Buck2VSet[5:0]					
0x11	Reserved	—	—	—	—			—		
0x12	LDO1Cfg	R/W	LDO1Seq[2:0]			—	LDO1 ActDSC	LDO1En[1:0]		LDO1Mode

I²C Register Map (continued)

REGISTER ADDRESS	REGISTER NAME	R/W	B7	B6	B5	B4	B3	B2	B1	B0
0x13	LDO1VSet	R/W**	—	—	—	LDO1VSet[4:0]				
0x14	LDO2Cfg	R/W	LDO2Seq[2:0]			—	LDO2 ActDSC	LDO2En[1:0]		LDO2Mode
0x15	LDO2VSet	R/W**	—	—	—	LDO2VSet[4:0]				
0x16	LDO3Cfg	R/W	LDO3Seq[2:0]			—	LDO3 ActDSC	LDO3En[1:0]		LDO3Mode
0x17	LDO3VSet	R/W**	—	—	—	LDO3VSet[4:0]				
0x18*	ThrmCfg	R/W**	—	—	—	—	—	—	JEITAEn	ThermEn
0x19	MONCfg	R/W			MONRatioCfg[1:0]		MONHiZ	MONCtr[2:0]		
0x1A	BootCfg	R/W	PwrRstCfg[3:0]				SftRstCfg	BootDly[1:0]		—
0x1B	PinStat	R/W	ILim___T[2:0]			—	PFN1	PFN2	MPC1	MPC0
0x1C	Buck1/2 Extra	R/W	Reserved	Reserved	Buck2 ActDSC	Buck2FFET	Reserved	Reserved	Buck1ActDSC	Buck1FFET
0x1D	PwrCfg	R/W	PFNxResEnaa	—	—	—	—	—	—	StayOn
0x1E	NULL	R	—	—	—	—	—	—	—	—
0x1F	PwrOff	R/W	PWR_OFF_CMD							

Note: *COR = Clear-on-read*

**Register is reset to default value upon CHGIN rising edge.*

*** R if WriteProtect enabled (Table 35).*

All R/W registers are reset to default value when entering the off state.

Reserved bits must not be modified from their default states to ensure proper operation.

I²C Register Descriptions

Table 5. ChipId Register (0x00)

ADDRESS:	0x00							
MODE:	Read-Only							
BIT	7	6	5	4	3	2	1	0
NAME	Chip_Id[7:0]							
Chip_Id[7:0]	Chip_Id[7:0] bits show information about the version of the MAX14690_.							

Table 6. ChipRev Register (0x01)

ADDRESS:	0x01							
MODE:	Read-Only							
BIT	7	6	5	4	3	2	1	0
NAME	Chip_Rev[7:0]							
Chip_Rev[7:0]	Chip_Rev[7:0] bits show information about the revision of the MAX14690_ silicon.							

Table 7. StatusA Register (0x02)

ADDRESS:	0x02							
MODE:	Read-Only							
BIT	7	6	5	4	3	2	1	0
NAME	–	–	ThermStat[2:0]			ChgStat[2:0]		
ThermStat[2:0]	Status of Thermistor Monitoring 000 = T < T1 001 = T1 < T < T2 010 = T2 < T < T3 011 = T3 < T < T4 100 = T > T4 101 = No thermistor detected (THM high due to external pullup). Note that if a parallel resistor is used for thermistor monitoring, this mode may not function properly. 110 = NTC input disabled through ThermEn 111 = Detection disabled due to CHGIN not present.							
ChgStat[2:0]	Status of Charger Mode 000 = Charger off 001 = Charging suspended due to temperature (see Figure 5) 010 = Pre-charge in progress 011 = Fast-charge, constant current mode in progress 100 = Fast-charge, constant voltage mode in progress 101 = Maintain charge in progress 110 = Maintain charger timer done 111 = Charger fault condition (see Figure 5)							

Table 8. StatusB Register (0x03)

ADDRESS:	0x03							
MODE:	Read-Only							
BIT	7	6	5	4	3	2	1	0
NAME	—	—	ILim	UsbOVP	UsbOk	Chg ThrmSd	Chg ThrmReg	ChgTmo
ILim	CHGIN Input Current Limit 0 = CHGIN input current is within limit. 1 = CHGIN input is in current limit.							
UsbOVP	Status of CHGIN OVP 0 = CHGIN OVP is not active. 1 = CHGIN OVP is active.							
UsbOk	Status of CHGIN Input 0 = CHGIN Input is not present or outside of valid range. 1 = CHGIN Input is present and valid.							
ChgThrmSd	Status of Thermal Shutdown 0 = Charger and input current limiter is in normal operating mode. 1 = Charger and input current limiter is in thermal shutdown.							
ChgThrmReg	Status of Thermal Regulation 0 = Charger is functioning normally, or disabled. 1 = Charger is running in thermal regulation mode and charging current is being actively reduced to prevent device overheating.							
ChgTmo	Status of Time-Out Condition 0 = Charger is running normally, or disabled. 1 = Charger has reached a time-out condition. ChgStat =1 11 in this condition (see Figure 5).							

Table 9. StatusC Register (0x04)

ADDRESS:	0x04							
MODE:	Read-Only							
BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	ThrmBuck1	ThrmBuck2	ThrmLDO1	ThrmLDO2	ThrmLDO3
ThrmBuck1	0 = Buck1 NOT in Thermal Off mode 1 = Buck1 in Thermal Off Mode							
ThrmBuck2	0 = Buck2 NOT in Thermal Off mode 1 = Buck2 in Thermal Off Mode							
ThrmLDO1	0 = LDO1 NOT in Thermal Off mode 1 = LDO1 in Thermal Off Mode							
ThrmLDO2	0 = LDO2 NOT in Thermal Off mode 1 = LDO2 in Thermal Off Mode							
ThrmLDO3	0 = LDO3 NOT in Thermal Off mode 1 = LDO3 in Thermal Off Mode							

Table 10. IntA Register (0x05)

ADDRESS:	0x05							
MODE:	Clear On Read							
BIT	7	6	5	4	3	2	1	0
NAME	Therm StatInt	ChgStatInt	ILimInt	UsbOVPInt	UsbOk	Chg ThrmSdInt	Therm RegInt	Chg TmoInt
ThermStatInt	Change in ThermStat caused interrupt.							
ChgStatInt	Change in ChgStat caused interrupt, or first detection complete after POR.							
ILimInt	Input current limit triggered caused interrupt.							
UsbOVPInt	Change in UsbOVP caused interrupt.							
UsbOk	Change in UsbOk caused interrupt.							
ChgThrmSdInt	Change in ChgThrmSd caused interrupt.							
ThermRegInt	Change in ChgThrmReg caused interrupt.							
ChgTmoInt	Change in ChgTmo caused interrupt.							
ThermStatInt	Change in ThermStat caused interrupt.							

Table 11. IntB Register (0x06)

ADDRESS:	0x06							
MODE:	Clear On Read							
BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	Thrm Buck1Int	Thrm Buck2Int	Thrm LDO1Int	Thrm LDO2Int	Thrm LDO3Int
ThrmBuck1Int	Change in ThrmBuck1 caused interrupt.							
ThrmBuck2Int	Change in ThrmBuck2 caused interrupt.							
ThrmLDO1Int	Change in ThrmLDO1 caused interrupt.							
ThrmLDO2Int	Change in ThrmLDO2 caused interrupt.							
ThrmLDO3Int	Change in ThrmLDO3 caused interrupt.							

Table 12. IntMaskA Register (0x07)

ADDRESS:	0x07							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	Therm StatIntM	Chg StatIntM	ILimIntM	Usb OVPIntM	UsbOkM	ChgThrm SdIntM	Therm RegIntM	Chg TmoIntM
ThermStatIntM	ThermStatIntM masks the ThermStatInt interrupt in the IntA register (0x05). 0 = Mask 1 = Not masked							
ChgStatIntM	ChgStatIntM masks the ChgStatInt interrupt in the IntA register (0x05). 0 = Mask 1 = Not masked							
ILimIntM	ILimIntM masks the ILimInt interrupt in the IntB register (0x06). 0 = Mask 1 = Not masked							
UsbOVPIntM	UsbOVPIntM masks the UsbOVPInt interrupt in the IntA register (0x05). 0 = Mask 1 = Not masked							
UsbOkM	UsbOkM masks the UsbOk interrupt in the IntB register (0x06). 0 = Mask 1 = Not masked							
ChgThrm SdIntM	ChgThrmSdIntM masks the ChgThrmSdInt interrupt in the IntB register (0x06). 0 = Mask 1 = Not masked							
ThermRegIntM	ThermRegIntM masks the ThermRegInt interrupt in the IntA register (0x05). 0 = Mask 1 = Not masked							
ChgTmoIntM	ChgTmoIntM masks the ChgTmoInt interrupt in the IntA register (0x05). 0 = Mask 1 = Not masked							

Table 13. IntMaskB Register (0x08)

ADDRESS:	0x08							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	ThrmBuck1IntM	ThrmBuck2IntM	ThrmLDO1IntM	ThrmLDO2IntM	ThrmLDO3IntM
ThrmBuck1IntM	0 = Mask 1 = Not masked							
ThrmBuck2IntM	0 = Mask 1 = Not masked							
ThrmLDO1IntM	0 = Mask 1 = Not masked							
ThrmLDO2IntM	0 = Mask 1 = Not masked							
ThrmLDO3IntM	0 = Mask 1 = Not masked							

Table 14. ILimCntl Register (0x09)

ADDRESS:	0x09							
MODE:	Read/Write* or Read-Only if Write-Protect Enabled (see Table 35)							
BIT	7	6	5	4	3	2	1	0
NAME	—	—	—	—	—	—	ILimCntl [1:0]	
ILimCntl[1:0]	CHGIN Custom Input Current Limit (see Electrical Characteristics table for details) 00 = 0mA 01 = 100mA 10 = 500mA 11 = 1000mA							

**Register is reset to default value upon CHGIN rising edge.*

Table 15. ChgCntlA Register (0x0A)

ADDRESS:	0x0A							
MODE:	Read/Write* or Ready-Only if Write-Protect Enabled (see Table 35)							
BIT	7	6	5	4	3	2	1	0
NAME	ChgAuto Stp	ChgAuto ReSta	BatReChg[1:0]		BatReg[2:0]			ChgEn
ChgAutoStp	Charger Auto-Stop. Controls the transition from Maintain Charger to Maintain Charger Done. 0 = Autostop disabled. 1 = Autostop enabled.							
ChgAutoReSta	Charger Auto Restart Control 0 = Charger remains in maintain charge done even when VBAT is less than charge restart threshold (see Charger state diagram). 1 = Charger automatically restarts when VBAT drops below charge restart threshold.							
BatReChg[1:0]	Recharge Threshold in Relation to BatReg 00 = BatReg - 70mV 01 = BatReg - 120mV 10 = BatReg - 170mV 11 = BatReg - 220mV							
BatReg[2:0]	Setting the Battery Regulation Threshold 000 = 4.05V 001 = 4.10V 010 = 4.15V 011 = 4.20V 100 = 4.25V 101 = 4.30V 110 = 4.35V 111 = Reserved							
ChgEn	On/Off Control for Charger (does not affect SYS node). 0 = Charger disabled. 1 = Charger enabled.							

**Register is reset to default value upon CHGIN rising edge.*

Table 16. ChgCntlB Register (0x0B)

ADDRESS:	0x0B							
MODE:	Read/Write*							
BIT	7	6	5	4	3	2	1	0
NAME	-	VPChg[2:0]			IPChg[1:0]		ChgDone[1:0]	
VPChg[2:0]	Pre-charge voltage threshold setting 000 = 2.10V 001 = 2.25V 010 = 2.40V 111 = 2.55V 100 = 2.70V 101 = 2.85V 110 = 3.00V 111 = 3.15V							
IPChg[1:0]	Pre-charge current setting 00 = 0.05 x I_{FChg} 01 = 0.1 x I_{FCHG} 10 = 0.2 x I_{FChg} 11 = 0.3 x I_{FChg}							
ChgDone[1:0]	Charge Done Threshold Setting 00 = 0.05 x I_{FChg} 01 = 0.1 x I_{FChg} 10 = 0.2 x I_{FChg} 11 = 0.3 x I_{FChg}							

**Register is reset to default value upon CHGIN rising edge.*

Table 17. ChTmr Register (0x0C)

ADDRESS:	0x0C							
MODE:	Read/Write*							
BIT	7	6	5	4	3	2	1	0
NAME	-	-	MtChgTmr[1:0]		FChgTmr[1:0]		PChgTmr[1:0]	
MtChgTmr [1:0]	Maintain Charge Timer Setting 00 = 0min 01 = 15min 10 = 30min 11 = 60min							
FChgTmr[1:0]	Fast- Charge Timer Setting 00 = 75min 01 = 150min 10 = 300min 11 = 600min							
PChgTmr[1:0]	Pre-charge Timer Setting 00 = 30min 01 = 60min 10 = 120min 11 = 240min							

**Register is reset to default value upon CHGIN rising edge.*

Table 18. Buck1Cfg Register (0x0D)

ADDRESS:	0x0D							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	Buck1Seq[2:0] (Read-only)			Buck1En[1:0]		Buck1Md[1:0]		Buck1Ind
Buck1Seq[2:0]	Buck1 Enable Configuration (Read-Only) 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Reserved 110 = Reserved 111 = Controlled by Buck1En[1:0] after 100% of Boot/POR Process Delay Control							
Buck1En[1:0]	Buck1 Enable Configuration (effective only when Buck1Seq = 111) 00 = Disabled (Buck1 OUT not actively discharged unless in Hard Reset/ShutDown/Off Mode) 01 = Enabled 10 = Enabled when MPC0 is high (regardless of MPC1) 11 = Enabled when MPC1 is high (regardless of MPC0)							
Buck1Md[1:0]	Buck1 Mode Select 00 = Burst mode 01 = Forced PWM mode 10 = Forced PWM mode when MPC0 is high (regardless of MPC1) 11 = Forced PWM mode when MPC1 is high (regardless of MPC0)							
Buck1Ind	Buck1 Inductance select 0 = inductance is 2.2µH 1 = inductance is 4.7µH							

Table 19. Buck1VSet Register (0x0E)

ADDRESS:	0x0E							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	-	-	Buck1VSet[5:0]					
Buck1VSet [5:0]	Buck1 Output Voltage Setting This setting is internally latched and can change only when Buck1 is Disabled. Linear Scale from 0.8V to 1.8V in 25mV increments 000000 = 0.8V 000001 = 0.825V … 101000 = 1.8V >101000 = 1.8V							

Table 20. Buck2Cfg Register (0x0F)

ADDRESS:	0x0F							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	Buck2Seq[2:0] (Read-only)			Buck2En[1:0]		Buck2Md[1:0]		Buck2Ind
Buck2Seq[2:0]	Buck2 Enable Configuration (Read-only) 000 = Disabled 001 = Reserved 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Reserved 110 = Reserved 111 = Controlled by Buck2En [1:0] after 100% of Boot/POR Process Delay Control							
Buck2En[1:0]	Buck2 Enable Configuration (effective only when Buck2Seq = 111) 00 = Disabled (Buck2 OUT not actively discharged unless in Hard Reset/ShutDown/Off Mode) 01 = Enabled 10 = Enabled when MPC0 is high (regardless of MPC1) 11 = Enabled when MPC1 is high (regardless of MPC0)							
Buck2Md[1:0]	Buck2 Mode Select 00 = Burst mode 01 = Forced PWM mode 10 = Forced PWM mode when MPC0 is high (regardless of MPC1) 11 = Forced PWM mode when MPC1 is high (regardless of MPC0)							
Buck2Ind	Buck2 Inductance select 0 = inductance is 2.2µH 1 = inductance is 4.7µH (we may need to choose 4.7µH as default for Buck2)							

Table 21. Buck2VSet Register (0x10)

ADDRESS:	0x10							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	-	-	Buck2VSet[5:0]					
Buck2VSet [5:0]	Buck2 Output Voltage Setting This setting is internally latched and can change only when Buck2 is Disabled. Linear Scale from 1.5V to 3.3V in 50mV increments 000000=1.5V 000001=1.55V … 100100=3.3V >100100=3.3V							

Table 22. LDO1Cfg Register (0x12)

ADDRESS:	0x12							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	LDO1Seq[2:0] (Read Only)			RFU	LDO1Act DSC	LDO1En[1:0]		LDO1 Mode
LDO1Seq[2:0]	LDO1 Enable Configuration (Read-only) 000 = Disabled 001 = Enabled always when BAT/SYS is present 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Disabled 110 = Disabled 111 = Controlled by LDO1En[1:0] after 100% of Boot/POR Process Delay Control							
LDO1ActDSC	LDO1 Active Discharge Control 0: LDO1 output will be actively discharged only in HardReset mode 1: LDO1 output will be actively discharged in HardReset mode and also when its Enable goes Low							
LDO1En[1:0]	LDO1 Enable Configuration (effective only when LDO1Seq = 111) 00 = Disabled – LDOs OUT not actively discharged unless Hard-Reset/Shutdown/Off Mode 01 = Enabled 10 = Enabled when MPC0 is high (regardless of MPC1) 11 = Enabled when MPC1 is high (regardless of MPC0)							
LDO1Mode	LDO1 Mode Control 0 = Normal LDO operating mode 1 = Load switch mode. FET is either fully ON or OFF depending on state of LDO1En. When FET is ON, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled.							

Table 23. LDO1VSet Register (0x13)

ADDRESS:	0x13							
MODE:	Read-Only*							
BIT	7	6	5	4	3	2	1	0
NAME	-	-	-	LDO1Vset[4:0]				
LDO1VSet[4:0]	LDO1 Output Voltage Setting Linear Scale from 0.8V to 3.6V in 100mV increments 00000 = 0.8V 00001 = 0.9V … 11100 = 3.6V >11101 = N/A							

Table 24. LDO2Cfg Register (0x14)

ADDRESS:	0x14							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	LDO2Seq[2:0] (Read Only)			RFU	LDO2Act DSC	LDO2En[1:0]		LDO2 Mode
LDO2Seq [2:0]	LDO2 Enable Configuration (Read only) 000 = Disabled 001 = Enabled always when BAT/SYS is present 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Disabled 110 = Disabled 111 = Controlled by LDO2En[1:0] after 100% of Boot/POR Process Delay Control							
LDO2ActDSC	LDO2 Active Discharge Control 0 = LDO2 output will be actively discharged only in HardReset mode 1 = LDO2 output will be actively discharged in HardReset mode and also when its Enable goes Low							
LDO2En [1:0]	LDO2 Enable Configuration (effective only when LDO2Seq = 111) 00 = Disabled – LDO's OUT not actively discharged unless HardReset/ShutDown/Off Mode 01 = Enabled 10 = Enabled when MPC0 is high (regardless of MPC1) 11 = Enabled when MPC1 is high (regardless of MPC0)							
LDO2Mode	LDO2 Mode Control 0 = Normal LDO operating mode 1 = Load switch mode. FET is either fully ON or OFF depending on state of LDO2En. When FET is ON, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled.							

Table 25. LDO2VSet Register (0x15)

ADDRESS:	0x15							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	-	-	-	LDO2Vset[4:0]				
LDO2VSet[4:0]	LDO2 Output Voltage Setting Linear Scale from 0.8V to 3.6V in 100mV increments 00000 = 0.8V 00001 = 0.9V … 11100 = 3.6V >11101 = N/A							

Table 26. LDO3Cfg Register (0x16)

ADDRESS:	0x16							
MODE:	**Read/Write**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	LDO3Seq[2:0] (Read-Only)			RFU	LDO3Act DSC	LDO3En[1:0]		LDO3 Mode
LDO3Seq[2:0]	LDO3 Enable Configuration (Read only) 000 = Disabled 001 = Enabled always when BAT/SYS is present 010 = Enabled at 0% of Boot/POR Process Delay Control 011 = Enabled at 25% of Boot/POR Process Delay Control 100 = Enabled at 50% of Boot/POR Process Delay Control 101 = Disabled 110 = Disabled 111 = Controlled by LDO3En[1:0] after 100% of Boot/POR Process Delay Control							
LDO3ActDSC	LDO3 Active Discharge Control 0 = LDO3 output will be actively discharged only in HardReset mode 1 = LDO3 output will be actively discharged in HardReset modes and also when its Enable goes Low							
LDO3En[1:0]	LDO3 Enable Configuration (effective only when LDO3Seq == 111) 00 = Disabled. LDO's OUT not actively discharged unless in HardReset/ShutDown/Off Mode 01 = Enabled 10 = Enabled when MPC0 is high (regardless of MPC1) 11 = Enabled when MPC1 is high (regardless of MPC0)							
LDO3Mode	LDO3 Mode Control 0 = Normal LDO operating mode 1 = Load switch mode. FET is either fully ON or OFF depending on state of LDO3En. When FET is ON, the output is unregulated. This setting is internally latched and can change only when the LDO is disabled.							

Table 27. LDO3VSet Register (0x17)

ADDRESS:	0x17							
MODE:	**Read/Write**							
BIT	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
NAME	-	-	-	LDO3Vset[4:0]				
LDO3VSet[4:0]	LDO3 Output Voltage Setting Linear Scale from 0.8V to 3.6V in 100mV increments 00000 = 0.8V 00001 = 0.9V … 11100 = 3.6V >11101 = N/A							

Table 28. ThrmCfg Register (0x18)

ADDRESS:	0x18							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	-	-	-	-	-	-	JEITAEn	ThermEn
JEITAEn	Thermal or JEITA Monitoring Enable 0 = JEITA monitoring disabled 1 = JEITA Monitoring Enabled, only if ThermEn = 1							
ThermEn	Thermal or JEITA Monitoring Selector 0 = Thermal Monitoring Disabled 1 = Thermal Monitoring Enabled							

**Register is reset to default value upon CHGIN rising edge.*

Table 29. MONCfg Register (0x19)

ADDRESS:	0x19							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME			MONRatioCfg[1:0]		MONtHiZ	MONCtr[2:0]		
MONRatioCfg	MON Resistive Partition Selector 00 = 4:1 01 = 3:1 10 = 2:1 11 = 1:1							
MONtHiZ	MON OFF MODE condition 0 = Pulled LOW by 100k pull-down resistor 1 = Hi-Z							
MONCtr[2:0]	MON Pin Source selection (40µs BBM after any change of MONCtr) 000 = MON is not connected to any internal node and its state depends on MONHiZ 001 = MON connected to a resistive partition of BATT 010 = MON connected to a resistive partition of SYS 011 = MON connected to a resistive partition of BUCK1 OUT 100 = MON connected to a resistive partition of BUCK2 OUT 101 = MON connected to a resistive partition of LDO1 OUT 110 = MON connected to a resistive partition of LDO2 OUT 111 = MON connected to a resistive partition of LDO3 OUT							

Table 30. BootCfg Register (0x1A)

ADDRESS:	0x1A							
MODE:	Read-Only							
BIT	7	6	5	4	3	2	1	0
NAME	PwrRstCfg[3:0]				SftRstCfg	BootDly[1:0]		RFU
PwrRstCfg [3:0]	See Table 1							
SftRstCfg	Soft Reset Register Default 0 = Registers do not reset to default values on soft reset 1 = Registers reset to default values on soft reset							
BootDly[1:0]	Boot/POR Process Delay Control 00 = 80ms + 34ms 01 = 120ms + 34ms 10 = 220ms + 34ms 11 = 420ms + 34ms							

Table 31. PinStat Register (0x1B)

ADDRESS:	0x1B							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	ILim_T[2:0]			-	PFN1	PFN2	MPC1	MPC0
ILim_T[2:0]	Monitor of The Input limiter Current Setting 000 = Input Limiter Off 001 = 100mA 010 = 500mA 100 =1A							
PFN1	PFN1 Input State 0 = pin low 1 = pin high							
PFN2	PFN2 In/Out State 0 = pin low 1 = pin high							
MPC1	MPC1 Input State 0 = pin low 1 = pin high							
MPC0	MPC0 Input State 0 = pin low 1 = pin high							

Table 32. Buck1/2Extra Control Register (0x1C)

ADDRESS:	0x1C							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	Reserved	Reserved	Buck2 ActDSC	Buck2 FFET	Reserved	Reserved	Buck1 ActDSC	Buck1 FFET
Buck2ActDSC	Buck2 Active Discharge Control 0 = Buck2 output will be actively discharged only in HardReset mode 1 = Buck2 output will be actively discharged in HardReset mode and also when its Enable goes Low							
Buck2FFET	Buck2 Force FET scaling (it reduces I_Q by lowering the nMOS power to 20% of the nominal value) 0 = FET Scaling only enabled during the Buck2 Turn-On Sequence 1 = FET Scaling enabled during the Buck2 Turn-On Sequence and also in the Buck2 Steady On state							
Buck1ActDSC	Buck1 Active Discharge Control 0 = Buck1 output will be actively discharged only in HardReset mode 1 = Buck1 output will be actively discharged in HardReset mode and also when its Enable goes Low.							
Buck1FFET	Buck1 Force FET Scaling (it reduces I_Q by lowering the nMOS power to 20% of the nominal value) 0 = FET Scaling only enabled during the Buck1 Turn-On Sequence 1 = FET Scaling enabled during the Buck1 Turn-On Sequence and also in the Buck1 Steady ON state							

Table 33. PwrCfg Register (0x1D)

ADDRESS:	0x1D							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	PFNx ResEna	–	–	–	–	–	–	StayOn
PFNxResEna	PFN_ Automatic Internal Pull-Up/Pull-Down Enable 0 = No internal pullup/pulldown 1 = Automatic internal pullup/pulldown as per Table 1							
StayOn	This bit is used to ensure that the processor booted correctly. This bit must be set within 5s of power-on to prevent the part from shutting down and returning to the power-off condition. This bit has no effect after being set. 0 = Shut down 5s after power-on 1 = Stay on							

Table 34. PwrOff Register (0x1F)

ADDRESS:	0x1F							
MODE:	Read/Write							
BIT	7	6	5	4	3	2	1	0
NAME	PWR_CMD[7:0]							
PWR_CMD [7:0]	Power-Off Command Writing 0xB2 to this register will place the part in the off mode except in PwrRstCfg[3:0] modes 0000 and 0001 when it has no effect. Writing any other code has no effect. In PwrRstCfg[3:0] modes 0110 and 0111, the part can be turned back on by a button press or a valid voltage applied to CHGIN. In all other modes, only a valid voltage applied to CHGIN will turn the device back on. See Figure 1 for more details.							

Table 35. Register Bit Default Values

REGISTER BITS	MAX14690A	MAX14690B	MAX14690C	MAX14690D	MAX14690E	MAX14690N	MAX14690H	MAX14690I	MAX14690J	MAX14690K
ChgAutoStp	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
ChgAutoReSta	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
BatReChg[1:0]	-120mV	-220mV	-220mV	-220mV	-120mV	-120mV	-220mV	-120mV	-120mV	-220mV
BatReg[2:0]	4.20V	4.30V	4.35V	4.20V	4.20V	4.20V	4.35V	4.20V	4.35V	4.20V
ChgEn	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
Buck1En[1]	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled	Disabled
VPChg[2:0]	2.85V	3.00V	3.00V	3.00V	2.85V	3.00V	3.00V	3.00V	3.00V	3.00V
IPChg[1:0]	0.10 x IFChg	0.05 x IFChg	0.10 x IFChg	0.10 x IFChg	0.10 x IFChg	0.10 x IFChg	0.10 x IFChg	0.10 x IFCHg	0.10 x IFCHg	0.10 x IFCHg
ChgDone[1:0]	0.05 x IFChg	0.10 x IFChg	0.10 x IFChg	0.05 x IFChg	0.05 x IFChg	0.10 x IFChg	0.1 x IFChg	0.10 x IFChg	0.10 x IFChg	0.05 x IFChg
MtChgTmr[1:0]	60min	30min	0min	0min	60min	0min	0min	0min	0min	0min
FChgTmr[1:0]	300min	150min	300min	150min	600min	300min	300min	300min	300min	150min
PChgTmr[1:0]	30min	240min	60min	30min	30min	60min	60min	60min	60min	30min
Buck1Seq[2:0] (Read-Only)	Buck1En	25% boot	Disabled	0% boot	Buck1En	25% boot	0% boot	Buck1En	Buck1En	0% boot
Buck1Ind	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH	2.2mH
Buck1VSet[5:0]	1.2V	1.175V	1.8V	1.3V	1.2V	1.2V	1.8V	1.2V	1.2V	1.3V
Buck2Seq[2:0] (Read-Only)	0% boot	0% boot	25% boot	Buck2En	0% boot	25% boot	Buck2En	25% boot	25% boot	Buck2En
Buck2Ind	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH	2.2µH
Buck2VSet[5:0]	1.8V	1.8V	2.0V	1.8V	2.2V	1.8V	3.3V	2.85V	2.85V	1.8V
Buck1_Iup_SET[2:0]	100mA	100mA	100mA	100mA	100mA	100mA	100mA	100mA	100mA	100mA
Buck2_Iup_SET[2:0]	100mA	100mA	100mA	100mA	100mA	100mA	100mA	100mA	100mA	100mA
LDO1Seq[2:0] (Read-Only)	LDO1En	Always On	LDO1En	0% boot	Always On	Always On	LDO1En	LDO1En	LDO1En	0% boot
LDO1Mode	LDO	LDO	LDO	LDO	LDO	LDO	LDO	LDO	LDO	LDO
LDO1Vset[4:0]	3.0V	2.0V	3.1V	3.1V	2V	1.8V	3.0V	1.8V	1.8V	3.1V

Table 35. Register Bit Default Values (continued)

REGISTER BITS	MAX14690A	MAX14690B	MAX14690C	MAX14690D	MAX14690E	MAX14690N	MAX14690H	MAX14690I	MAX14690J	MAX14690K
LDO2Seq[2:0] (Read-Only)	LDO2En	LDO2En	LDO2En	LDO2En	LDO2En	LDO2En	LDO2En	LDO2En	LDO2En	LDO2En
LDO2Mode	Switch	LDO	LDO	Switch	LDO	LDO	LDO	LDO	LDO	Switch
LDO2Vset[4:0]	3.7V	3.2V	1.8V	0.8V	2.7V	3.2V	3.0V	1.2V	1.2V	0.8V
LDO3Seq[2:0] (Read-Only)	LDO3En	LDO3En	LDO3En	LDO3En	LDO3En	LDO3En	LDO3En	LDO3En	LDO3En	LDO3En
LDO3Mode	Switch	Switch	Switch	Switch	Switch	LDO	LDO	LDO	LDO	Switch
LDO3Vset[4:0]	3.7V	3.7V	1.8V	0.8V	3.7V	3.0V	3.0V	3V	3V	0.8V
JEITAEn	Disabled	Enabled	Enabled	Disabled	Enabled	Disabled	Enabled	Disabled	Disabled	Disabled
ThermEn	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
PwrRstCfg[3:0] (Read-Only)	KIN#	KIN#	Soft Reset	CR Low	Soft Reset	KIN	KIN	Soft Reset	Soft Reset	Soft Reset
SftRstCfg (Read-Only)	Hold	Reset	Reset	Reset	Hold	Hold	Reset	Hold	Hold	Reset
BootDly[1:0] (Read-Only)	(120 + 34)ms	(80 + 34)ms	(120 + 34)ms	(80 + 34)ms	(80 + 34)ms	(120 + 34)ms	(120 + 34)ms	(120 + 34)ms	(120 + 34)ms	(80 + 34)ms
PFNxResEna	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled	Enabled
StayOn	5s Turnoff	Stay On	Stay On	Stay On	Stay On	Stay On	Stay On	Stay On	Stay On	Stay On
WriteProtect	Writable	Writable	Writable	Writable	Writable	Writable	Writable	Writable	Writable	Writable
ILimCntl[1:0]	500mA	500mA	500mA	500mA	500mA	500mA	500mA	500mA	100mA	500mA

Table 36. Register Default Values

REGISTER ADDRESS	REGISTER NAME	DEFAULT VALUES									
		MAX14690A	MAX14690B	MAX14690C	MAX14690D	MAX14690E	MAX14690N	MAX14690H	MAX14690I	MAX14690J	MAX14690K
0x00	ChipId	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01	0x01
0x01	ChipRev	0x02	0x02	0x03	0x02	0x03	0x03	0x03	0x03	0x02	0x02
0x07	IntMaskA	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x08	IntMaskB	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x09	ILimCntl	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x02	0x01	0x02
0x0A	ChgCntlA	0xD7	0xFB	0xFD	0xF7	0xD7	0xD7	0xFD	0xD7	0xDD	0xF7
0x0B	ChgCntlB	0x54	0x61	0x65	0x64	0x54	0x65	0x65	0x65	0x65	0x64
0x0C	ChgTmr	0x38	0x27	0x09	0x04	0x3C	0x09	0x09	0x09	0x09	0x04
0x0D	Buck1Cfg	0xE0	0x60	0x00	0x40	0xE0	0x60	0x40	0xE0	0xE0	0x40
0x0E	Buck1VSet	0x10	0x0F	0x28	0x14	0x10	0x10	0x28	0x10	0x10	0x14
0x0F	Buck2Cfg	0x40	0x40	0x60	0xE0	0x40	0x60	0xE0	0x60	0x60	0xE0
0x10	Buck2VSet	0x06	0x06	0x0A	0x06	0x0E	0x06	0x24	0x1B	0x1B	0x06
0x11	Reserved	0x24	0x24	0x24	0x24	0x24	0x24	0x24	0x24	0x24	0x24
0x12	LDO1Cfg	0xE0	0x20	0xE0	0x40	0x20	0x20	0xE0	0xE0	0xE0	0x40
0x13	LDO1VSet	0x16	0x0C	0x17	0x17	0x0C	0x0A	0x16	0x0A	0x0A	0x17
0x14	LDO2Cfg	0xE1	0xE0	0xE0	0xE1	0xE0	0xE0	0xE0	0xE0	0xE0	0xE1
0x15	LDO2VSet	0x1D	0x18	0x0A	0x00	0x13	0x18	0x16	0x04	0x04	0x00
0x16	LDO3Cfg	0xE1	0xE1	0xE1	0xE1	0xE1	0xE0	0xE0	0xE0	0xE0	0xE1
0x17	LDO3VSet	0x1D	0x1D	0x0A	0x00	0x1D	0x16	0x16	0x16	0x16	0x00
0x18	ThrmCfg	0x01	0x03	0x03	0x01	0x03	0x01	0x03	0x01	0x01	0x01
0x19	MONCfg	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x1A	BootCfg	0x63	0x69	0x7B	0x59	0x71	0x63	0x6B	0x73	0x73	0x79
0x1C	Buck1/2Extra	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x1D	PwrCfg	0x80	0x81	0x81	0x81	0x81	0x81	0x81	0x81	0x81	0x81
0x1E	NULL	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x1F	PwrOff	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00	0x00

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX14690AEWX+	-40°C to +85°C	36 WLP
MAX14690AEWX+T	-40°C to +85°C	36 WLP
MAX14690BEWX+	-40°C to +85°C	36 WLP
MAX14690BEWX+T	-40°C to +85°C	36 WLP
MAX14690CEWX+	-40°C to +85°C	36 WLP
MAX14690CEWX+T	-40°C to +85°C	36 WLP
MAX14690DEWX+	-40°C to +85°C	36 WLP
MAX14690DEWX+T	-40°C to +85°C	36 WLP
MAX14690EEWX+	-40°C to +85°C	36 WLP
MAX14690EEWX+T	-40°C to +85°C	36 WLP
MAX14690HEWX+	-40°C to +85°C	36 WLP
MAX14690HEWX+T	-40°C to +85°C	36 WLP
MAX14690IEWX+	-40°C to +85°C	36 WLP
MAX14690IEWX+T	-40°C to +85°C	36 WLP
MAX14690JEWX+	-40°C to +85°C	36 WLP
MAX14690JEWX+T	-40°C to +85°C	36 WLP
MAX14690KEWX+*	-40°C to +85°C	36 WLP
MAX14690KEWX+T*	-40°C to +85°C	36 WLP
MAX14690NEWX+	-40°C to +85°C	36 WLP
MAX14690NEWX+T	-40°C to +85°C	36 WLP

+Denotes a lead(Pb)-free package/RoHS-compliant package.
T = Tape and reel.
**Future Product—contact marketing for availability.*
See Table 35 and Table 36 for the device differences.

Chip Information

PROCESS: BiCMOS

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	12/14	Initial release	—
1	4/15	BUCK1 default was changed to 1.175V from 2.0V	6, 13, 15, 16, 19, 22, 40
2	4/15	Removed future product designation from MAX14690AEWX+	41
3	4/15	Added additional Buck Ripple specifications in *Electrical Characteristics* table	5, 6
4	5/15	Added I^2C section and MAX14690C/D/N as future products	2, 11, 17-18, 22, 24, 39-42
5	7/15	Removed future product designation from MAX14690DEWX+ and MAX14690DEWX+T	45
6	10/15	Removed future product designation of MAX14690C and MAX14690N	2, 10, 13, 18, 29, 41-45
7	1/16	Added MAX14690I part numbers to data sheet	5, 11, 18, 43–45
8	2/16	Push Button Control diagram updated	18
9	2/16	Removed future product designation from MAX14690I	45
10	4/16	Removed future product designation from MAX14690H and added MAX14690J to *Ordering Information* table	43-45
11	5/16	Added MAX14690K future product	43-45
12	5/18	Updated title and Table 35.	1-47
13	1/20	Removed future product designation from MAX14690EEWX+ and MAX14690EEWX+T in the *Ordering Information* table	46

For pricing, delivery, and ordering information, please visit Maxim Integrated's online storefront at https://www.maximintegrated.com/en/storefront/storefront.html.