Features

- Gain: 14 dB @ 6 V, 30 GHz
- P1dB: 17 dBm @ 6 V, 30 GHz
- P3dB: 18.5 dBm @ 6 V, 30 GHz
- Integrated Power Detector
- Gain control with only positive bias voltages
- 50 Ω Input and Output Match
- Bias Voltage: V_{DD} = 4 - 6 V
- Bias Current: I_{DSQ} = 125 - 150 mA
- 5 mm SMT Package
- RoHS* Compliant

Applications

- Instrumentation and Communication Systems

Description

MAAM-011238 is an easy-to-use, wideband amplifier that operates from 100 kHz to 50 GHz. The amplifier provides 14 dB gain, 5 dB noise figure and 18.5 dBm of P3dB output power @ 30 GHz. It is matched to 50 Ω with typical return loss of 12 dB. The amplifier requires only positive bias voltages and would typically be operated at 6 V and 135 mA.

MAAM-011238 is suitable for a wide range of applications in instrumentation and communication systems.

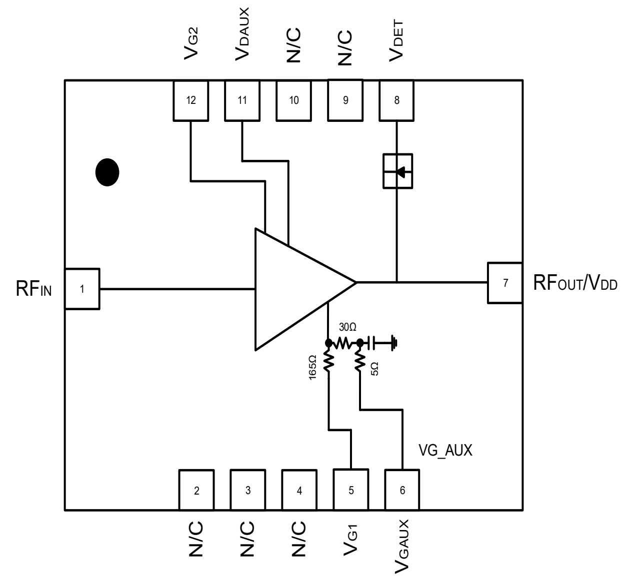
This part is also available as a bare die. Refer to datasheet MAAM-011238-DIE.

Ordering Information[1]

Part Number	Package
MAAM-011238-TR0100	100 part reel
MAAM-011238-TR0500	500 part reel
MAAM-011238-SB1	Sample Board

1. Reference Application Note M513 for reel size information.

Functional Schematic



Pin Configuration[2,3,4]

Pin #	Pin Name	Description
1	RF_{IN}	RF Input / Gate Voltage
5	V_{G1}	Gate Voltage 1
6	V_{GAUX}	Auxiliary Gate Voltage
7	RF_{OUT}/V_{DD}	RF Output / Drain Voltage
8	V_{DET}	Detector Voltage
11	V_{DAUX}	Auxiliary Drain Voltage
12	V_{G2}	Gate Voltage 2
2, 3, 4, 9, 10	N/C	No Connection

2. MACOM recommends connecting all no connection (N/C) pins to ground.
3. The exposed pad centered on the package bottom must be connected to RF, DC and thermal ground.
4. Internal to package are 100 pF decoupling capacitors on pins 5, 6, 8, 11, 12.

* Restrictions on Hazardous Substances, compliant to current RoHS EU directive.

Electrical Specifications[5,6,7]: T_A = 25 °C, V_{DD} = 6 V, I_{DSQ} = 135 mA, Z_0 = 50 Ω

Parameter	Test Conditions	Units	Min.	Typ.	Max.
Gain	0.01 - 10 GHz 10 - 20 GHz 20 - 30 GHz 30 - 40 GHz 40 - 43.5 GHz 43.5 - 50 GHz	dB	13.0 12.5 11.0 11.0 10.0 —	16.0 15.0 14.0 13.0 12.5 12.5	—
Noise Figure	2 - 10 GHz 10 - 20 GHz 20 - 30 GHz 30 - 40 GHz 40 - 43.5 GHz 43.5 - 50 GHz	dB	—	5.0 4.0 5.0 7.0 6.5 9.0	—
Input Return Loss	0.01 - 20 GHz 20 - 30 GHz 30 - 40 GHz 40 - 43.5 GHz 43.5 - 50 GHz	dB	—	20.0 12.0 10.0 11.0 10.5	—
Output Return Loss	0.01 - 10 GHz 10 - 20 GHz 20 - 30 GHz 30 - 40 GHz 40 - 43.5 GHz 43.5 - 50 GHz	dB	—	19.5 20.0 13.0 9.5 10.0 11.0	—
P_{OUT} @ P_{IN} = 11 dBm	0.1 - 10 GHz 10 - 20 GHz 20 - 30 GHz 30 - 40 GHz 40 - 43.5 GHz 43.5 - 50 GHz	dBm	20.0 19.5 18.0 17.0 17.0 —	21.5 21.0 19.5 19.0 18.7 18.3	—
P1dB	0.1 - 20 GHz 20 - 30 GHz 30 - 40 GHz 40 - 43.5 GHz 43.5 - 50 GHz	dBm	—	18.0 17.0 16.0 15.5 15.0	—
P3dB	0.1 - 10 GHz 10 - 20 GHz 20 - 30 GHz 30 - 40 GHz 40 - 50 GHz	dBm	—	20.5 20.0 18.5 18.0 17.0	—
Output IP3	0.01 - 10 GHz 10 - 20 GHz 20 - 30 GHz 30 - 40 GHz 40 - 43.5 GHz 43.5 - 50 GHz	dBm	—	28.0 29.0 27.0 25.0 24.0 20.5	—
Drain Current	Quiescent bias	mA	—	135	—

5. Set I_{DSQ} according to bias procedures in page 3.
6. Graphs in datasheet use test conditions shown unless otherwise stated.
7. All data measured with package assembled as per the Assembly Guideline.

Operating Conditions

One of the recommended biasing conditions is V_{DD} = 6 V, I_{DSQ} = 135 mA. (controlled with V_{G1}). I_{DSQ} is set by adjusting V_{G1} after correctly setting V_{DD}. (Refer to turn on sequence.)

Device biasing is achieved with the use of an external DC block on the input and a bias tee. The required V_{DD} is applied at RF_{OUT}/V_{DD} through the bias tee and V_{G1} is set to provide the required current bias (I_{DSQ}) This provides wide band performance of 40 MHz - 50 GHz. (depending on the bandwidth of the bias tee)

For low frequency extension, the addition of 1 µF and 0.01 µF bypass capacitors on both V_{G1} and VD_{AUX}, will improve the frequency of operation down to 100 kHz. These capacitors should be positioned as close to the device as possible.

Dynamic gain control is available when operating in the linear gain region through the application of 0 to 1.6 V to V_{G2}.

Data in this datasheet was measured using bypass capacitors on V_{G1} and VD_{AUX}.

The evaluation board is configured as shown in the Application Schematic with a direct connection to VG1 for lower gate voltage, typically 0.65 V with IG1 of 1 mA.

As an alternate configuration, VG1 can be shifted to >3 V by grounding VG_{AUX}. Note that this will increase IG1 to 21 mA. This is not a typical configuration and is available only for legacy applications that require VG1 > 3 V.

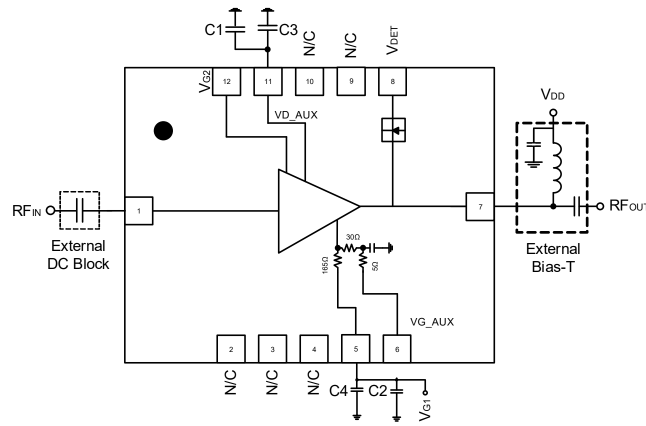
Operating the MAAM-011238
Turn-on

1. Apply V_{G1} to 0 V.
2. Apply V_{DD} to 6 V.
3. Set I_{DSQ} by adjusting V_{G1} more positive. (typically 0.65 V for I_{DSQ} = 135 mA).
4. Apply RF_{IN} signal.

Turn-off

1. Remove RF_{IN} signal.
2. Decrease V_{G1} to 0 V.
3. Decrease V_{DD} to 0 V.

Application Schematic



Component List

Part	Value	Case Style
C1, C2	1 µF	0603
C3, C4	0.01 µF	0402

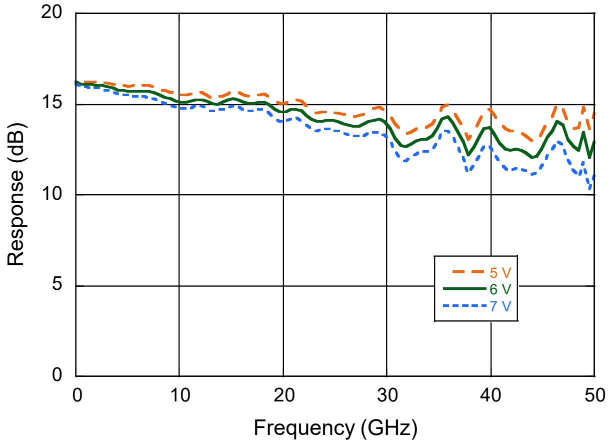
Absolute Maximum Ratings[8,9]

Parameter	Absolute Maximum
Input Power	16 dBm
Drain Supply Voltage	8 V
Junction Temperature[10,11]	+150°C
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C

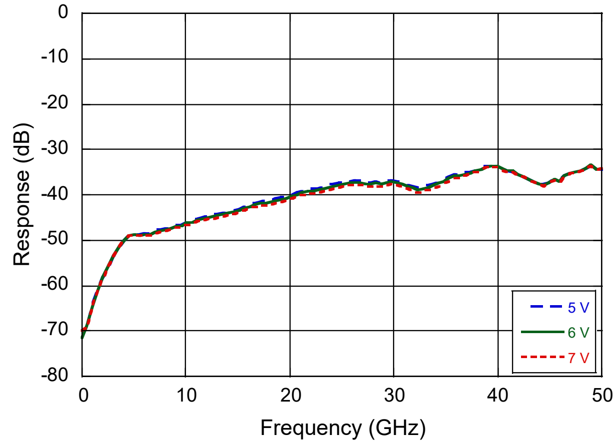
8. Exceeding any one or combination of these limits may cause permanent damage to this device.
9. MACOM does not recommend sustained operation near these survivability limits.
10. Operating at nominal conditions with $T_J \leq +150°C$ will ensure MTTF > 1 x 10^6 hours.
11. Junction Temperature (T_J) = T_A + Θ_{JC} * ((V * I) - (P_{OUT} - P_{IN}))
    Typical thermal resistance (Θ_{JC}) = 26.3°C/W.
    For T_A = +85°C,
    T_J = 105°C at V = 6 V, I = 0.135 A

Typical Performance Curves: V_{DD} = 6 V, I_{DSQ} = 135 mA, T_A = +25°C

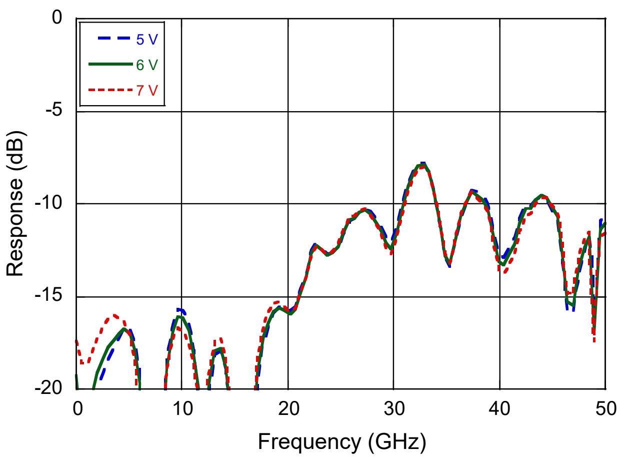
Gain



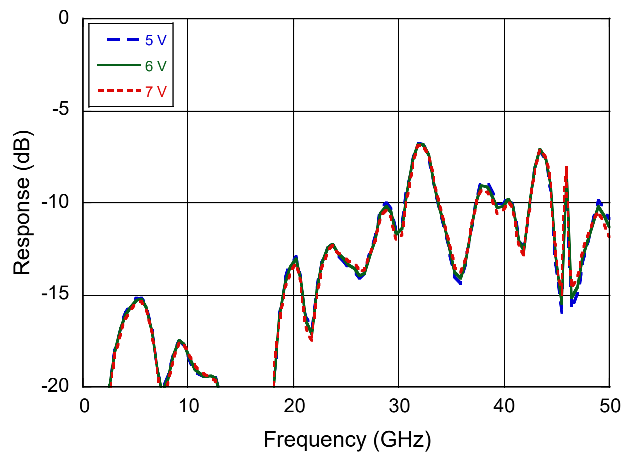
Reverse Isolation



Input Return Loss

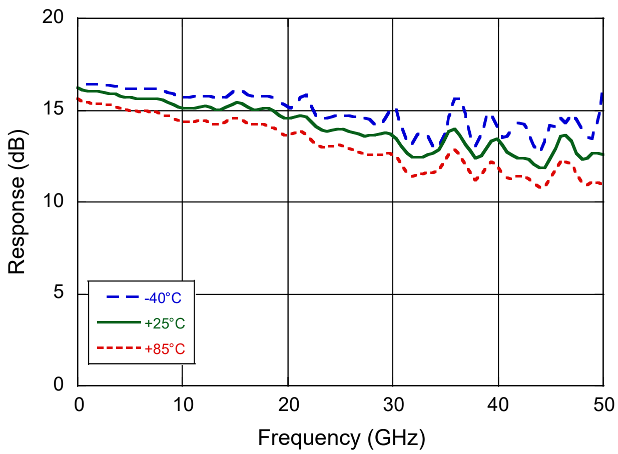


Output Return Loss

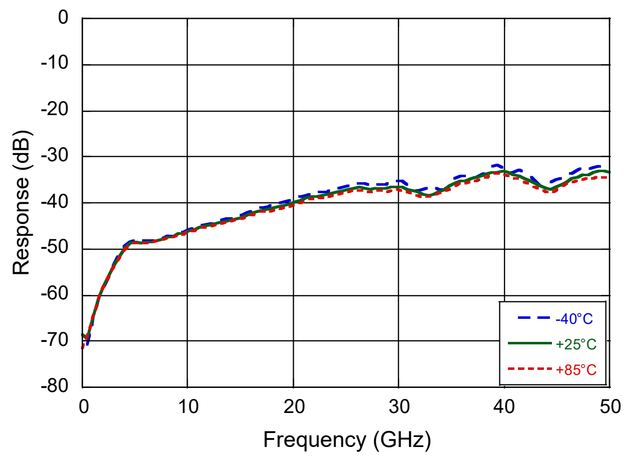


Typical Performance Curves: V_{DD} = 6 V, I_{DSQ} = 135 mA

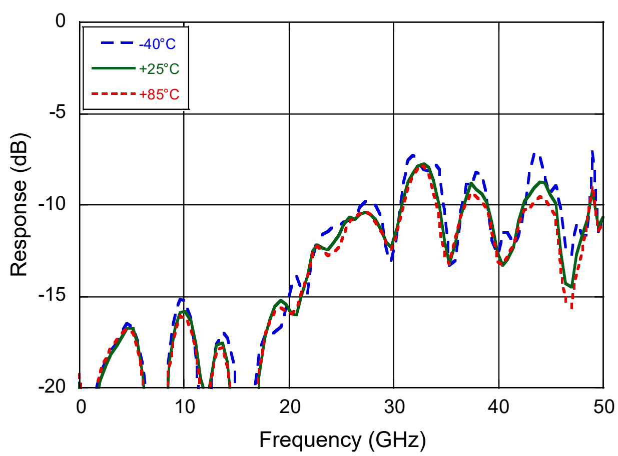
Gain



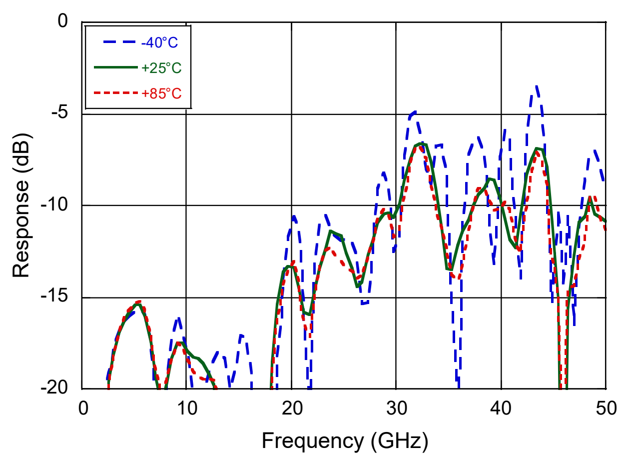
Reverse Isolation



Input Return Loss

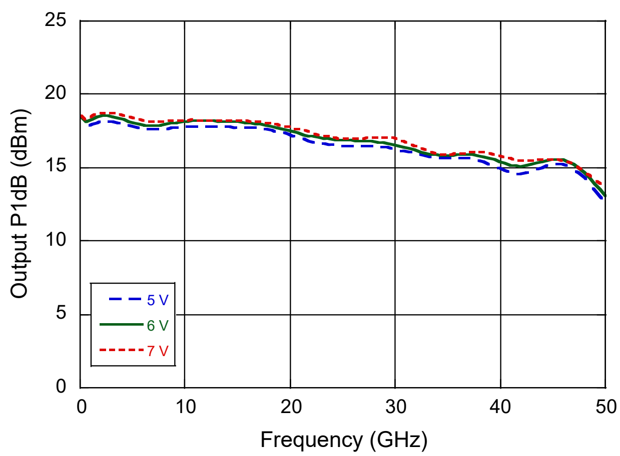


Output Return Loss

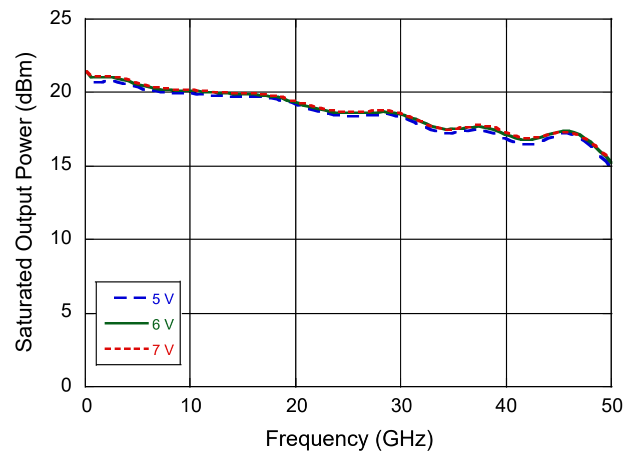


Typical Performance Curves: V_{DD} = 6 V, I_{DSQ} = 135 mA, T_A = +25°C

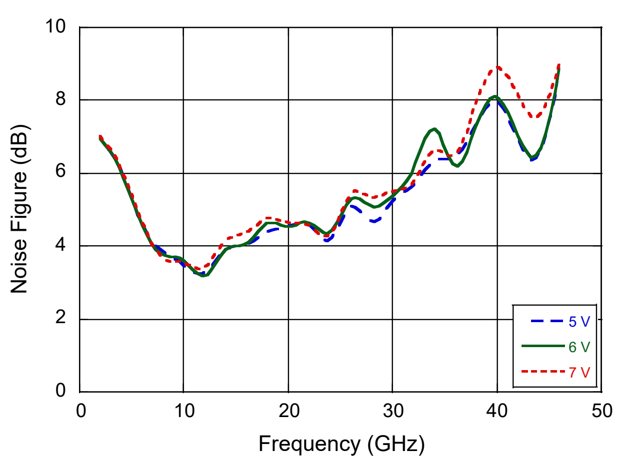
Output P1dB



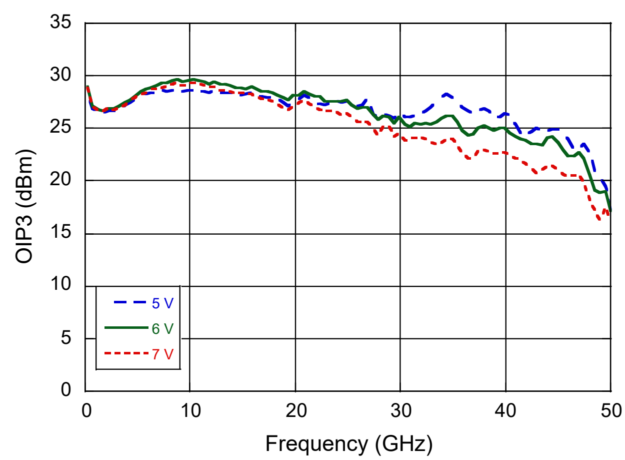
Output P3dB



Noise Figure

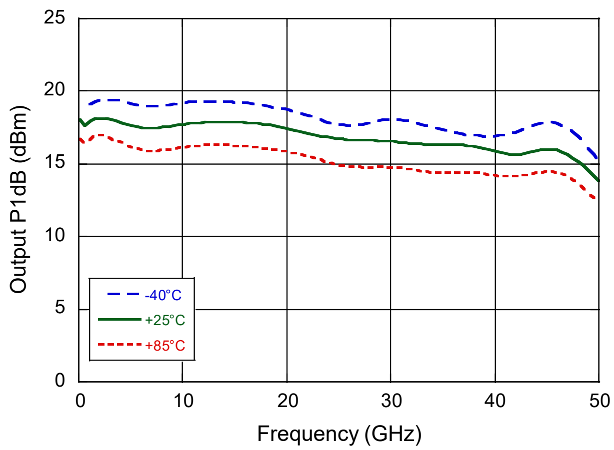


OIP3

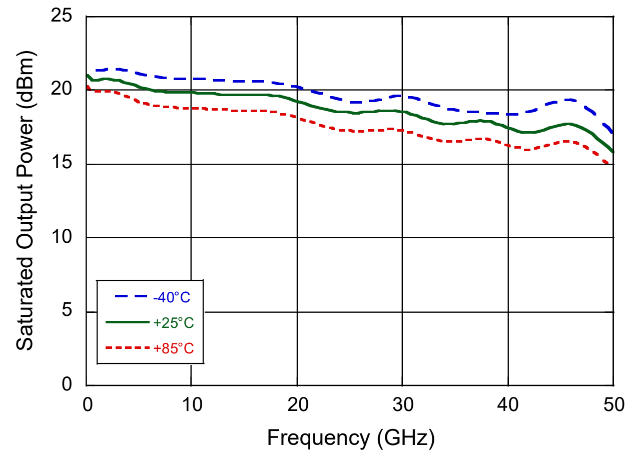


Typical Performance Curves: V_D = 6 V, I_D = 135 mA

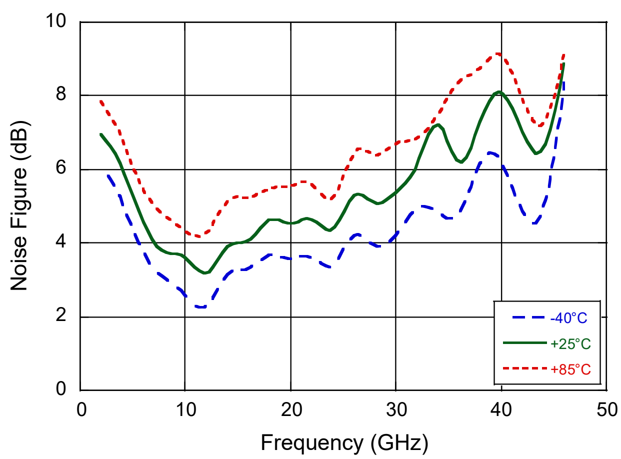
Output P1dB



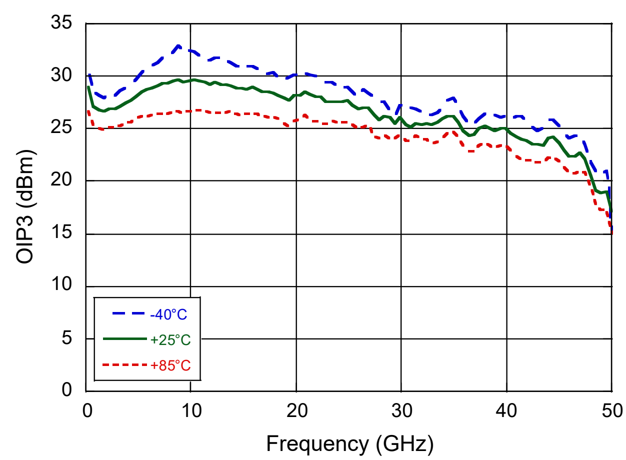
Output P3dB



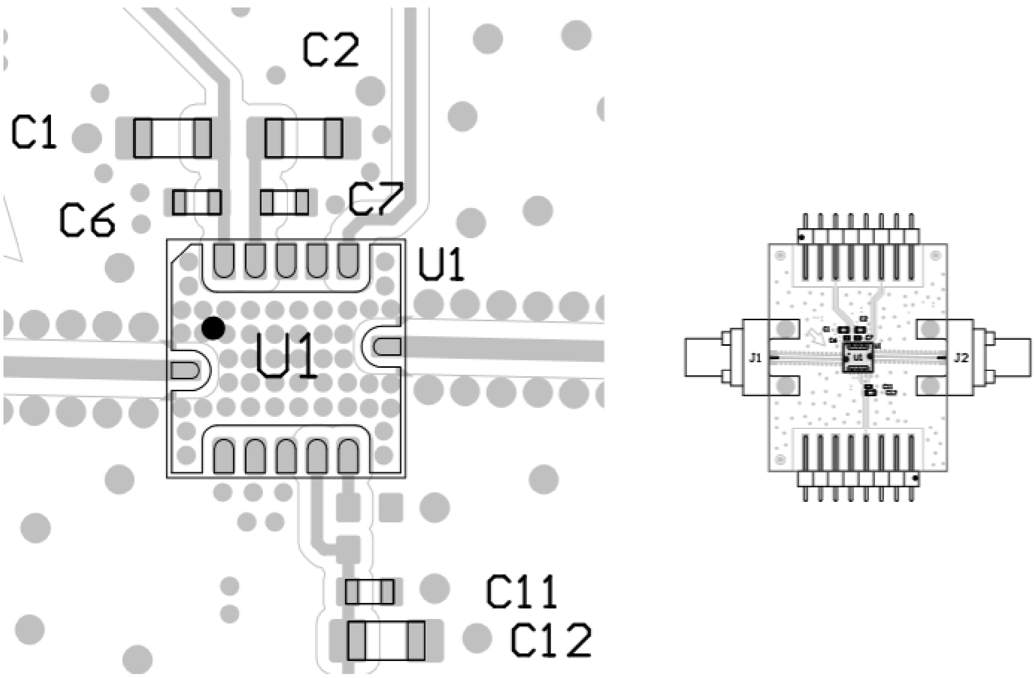
Noise Figure



OIP3



Recommended PCB Layout



Evaluation Board Parts List

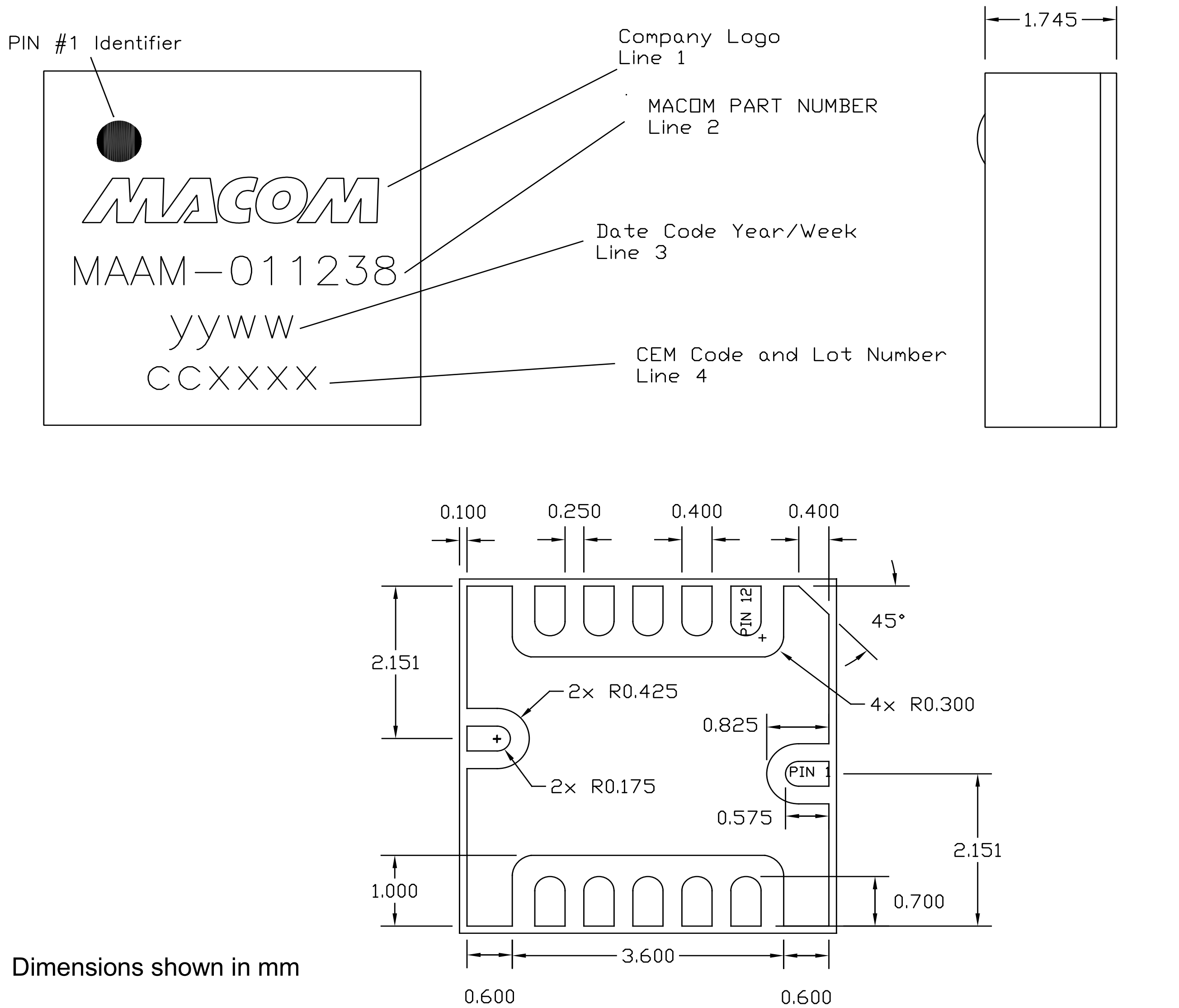
Part	Value	Case Style
C1, C2, C12	1 µF	0603
C6 C7, C11	0.01 µF	0402

Evaluation PCB Specifications[12,13]

Top Layer: 1 oz Copper Cladding *Dielectric Layer:* Rogers RO4350B 10 mil *Bottom Layer:* 1 oz Copper Cladding *Finished overall thickness: 12.8* mil

12. PCB finish is ENEPIG. The vias (quantity of 50) located under the device are 8 mil in diameter and filled with thermally conductive material, capped over and planarized
13. Evaluation board should be mounted on a heat sink.

Lead-Free 5 mm 12-Lead QFN Package†



Dimensions shown in mm

† Reference Application Note S2083 for lead-free solder reflow recommendations.
Meets JEDEC moisture sensitivity level 3 requirements.
Plating is ENEPIG over Copper.