Lattice Avant Platform - Overview

Advance Data Sheet

FPGA-DS-02107-0.73

March 2023

Disclaimers

Lattice makes no warranty, representation, or guarantee regarding the accuracy of information contained in this document or the suitability of its products for any particular purpose. All information herein is provided AS IS, with all faults and associated risk the responsibility entirely of the Buyer. Buyer shall not rely on any data and performance specifications or parameters provided herein. Products sold by Lattice have been subject to limited testing and it is the Buyer's responsibility to independently determine the suitability of any products and to test and verify the same. No Lattice products should be used in conjunction with mission- or safety-critical or any other application in which the failure of Lattice's product could create a situation where personal injury, death, severe property or environmental damage may occur. The information provided in this document is proprietary to Lattice Semiconductor, and Lattice reserves the right to make any changes to the information in this document or to any products at any time without notice.

Contents

Figures

Tables

Acronyms in This Document

A list of acronyms used in this document.

Acronym	Definition
DDR	Double Data Rate
DDRPHY	DDR Physical Layer
DLLDEL	DLL Delay
DSP	Digital Signal Processing
EBR	Embedded Block RAM
ECC	Error Correction Coding
ECLK	Edge Clock
FIFO	First In First Out
GCLK	Global Clock
LC	Logic Cell
LPDDR	Low Power DDR
LVCMOS	Low-Voltage Complementary Metal Oxide Semiconductor Interface Signaling
LVDS	Low-Voltage Differential Signaling
LUT	Look Up Table
MPPCS	Multi-Protocol PCS
MPPHY	Multi-Protocol PHY
PCIe	Peripheral Component Interconnect Express
PCS	Physical Coding Sublayer
PCLK	Primary Clock
PDP	Pseudo Dual Port
PFU	Programmable Functional Unit
PIC	Programmable I/O Cells
PIO	Programmable I/O
PLL	Phase Locked Loops
RCLK	Regional Clock
SEU	Single Event Upset
SLVS	Scalable Low-Voltage Signaling
SPI	Serial Peripheral Interface
SP	Single Port
SRAM	Static Random-Access Memory

1. General Description

Lattice Avant™ is a low-power mid-range density FPGA platform optimized for a wide range of applications across multiple markets – optimized for edge computing workloads requiring large memories and DSP resources and delivering a variety of high bandwidth interfaces ideal for video processing, communications and machine learning inferencing. A platform is built upon a programmable FPGA fabric optimized for a specific range of logic densities coupled with a collection of features that are assembled into unique device families utilizing varying amounts of features and I/O. The Avant platform will enable logic capacities up to 477k Logic Cells and capable of delivering up to 25Gb multi-protocol SerDes, hardened PCIe Gen 4, DDR5, DDR4/LPDDR4, and DDR3L memory interfaces, advanced security, and packages as small as 11 × 9 mm. This datasheet describes features which are part of the entire Avant FPGA platform, as well as the features that are unique to the Avant-E family.

The Avant platform delivers best-in-class power efficiency while meeting performance requirements for a wide range of applications. The following families are available in the Avant Platform.

- **Avant-E** family, the first set of devices from the Avant Platform – optimized for edge compute workloads. Featuring fast and flexible I/O (with support for 3.3 V I/O), it provides connectivity to external DRAM memory and fast differential interfaces.
- Future families will leverage additional features of the Avant platform such as multi-protocol SerDes support and advance security.

Avant platform-based devices are supported by the Lattice Radiant™ integrated design software environment. Synthesis library support for Avant devices is available for popular logic synthesis tools. Radiant uses synthesis tool output along with constraints from its floor planning tools to place and route the user design in Avant devices. The tool extracts timing from the routing and back-annotates it into the design for timing verification.

Lattice provides many pre-engineered IP (Intellectual Property) modules for Avant families. By using these configurable soft IP cores as standardized blocks, users are free to concentrate on the unique aspects of their design, increasing productivity.

1.1. Features

Table 1.1 shows the key features of the Avant platform.

Table 1.1. Avant Platform Key Features

Programmable Architecture	**System Performance**
• 196k to 477k logic cells • 700 to 1800 multipliers (18 × 18) in sysDSP™ blocks • 14.4 to 35.6 Mb of embedded memory (EBR) • Smallest package size 11 × 9 mm	• Improved low power performance • Timing closure for a typical design of up to 350 MHz • EBR/DSP/Clocks up to 625 MHz
External Memory Interface Support	**SerDes**
• DDR5 up to 2133 Mbps data rate[1] • DDR4/LPDDR4 up to 2400 Mbps data rate[2] • DDR3L up to 1866 Mbps data rate • Hardened DFI (DDR PHY Interface) training layer	• 25G SerDes and hardened PCIe Gen 1/2/3/4 • 4-28 SerDes
Device Security	**High-speed and Flexible Programmable I/O**
• AES256-GCM encryption • Up to ECC521 and RSA4096 authentication • Anti-tamper and PUF/Unique ID • User data encryption • Side channel resistance • TRNG (True Random Number Generator)	• 200 to 572 programmable sysI/O - High Performance (HP) and Wide Range (WR) • 1.8 Gbps MIPI D-PHY • 1.6 Gbps LVDS • 3.3 V support

Notes:

1. While Avant HPIO can support DDR5 up to 2400 Mbps, Avant has defined DDR5 operation only up to 2133 Mbps. DDR5 operational ranges defined by JEDEC are up to 2100 Mbps and >2400 Mbps.
2. Avant-E supports DDR4/LPDDR4 up to 1866 Mbps.

Table 1.2. Avant Families

Features		Avant-E
Fabric	**LCs, DSP, EBR**	Yes
Memory	**DDR4/LPDDR4**	Yes
SerDes	**PCS/PMA/Protocols**	Future Avant Families
Security	**Hardened Crypto**	Future Avant Families
Other	**JTAG, x1/x2/x4 SPI Configuration**	Yes
	x8 SPI Configuration	Future Avant Families
	Soft Error Detection/Soft Error Correction	Future Avant Families

Table 1.3. Avant-E Family Selection Guide

Device	LAV-AT-200E	LAV-AT-300E	LAV-AT-500E
Logic Cells[1]	196k	306k	477k
Embedded Memory (EBR) Blocks (36 kb)	400	630	990
Embedded Memory (Mb)	14.4	22.7	35.6
Distributed RAM Bits (kb)	1700	2660	4140
DSP (18 × 18 Multipliers)	700	1120	1800
High Frequency Oscillator	1	1	1
GPLL	6	9	11
Packages (Type, Size, Ball Pitch)[2]	**Total I/O (WR – Wide Range, HP – High Performance)**		
ASG324 (WLCSP, 11 × 9 mm, 0.5 mm)	208 (52, 156)	—	—
CSG484 (FCCSP, 12 × 12 mm, 0.5 mm)	—	230 (52, 178)	—
CSG676 (FCCSP, 15 × 13 mm, 0.5 mm)	—	—	312 (52, 260)
LBG484 (FCBGA, 19 × 19 mm, 0.8 mm)	230 (52, 178)	230 (52, 178)	—
LFG676 (FCBGA, 27 × 27 mm, 1.0 mm)	312 (52, 260)	312 (52, 260)	312 (52, 260)
LFG1156 (FCBGA, 35 × 35 mm, 1.0 mm)	—	468 (104, 364)	572 (104, 468)

Notes:

1. Logic Cells = LUTs × 1.2 effectiveness.
2. Refer to Ordering Information for more package details.

2. Architecture

2.1. Overview

Each Avant device contains arrays of logic blocks, arranged into Clock Regions (CKR). Each CKR comprises blocks such as PFUs, EBRs, DSPs, and a Clock Network that clocks synchronous elements in the CKR. Each CKR is associated with an I/O bank. An I/O bank may be a group of high-speed SerDes I/O blocks, a High-Performance I/O (HPIO) bank or a Wide-Range I/O (WRIO) bank. The Clock Regions are arranged in two rows and multiple columns depending on the density of the device, and vary in size from 20k up to 27k logic cells.

The top and bottom periphery of the device contain Programmable I/O Cells (PIC) and SerDes I/O blocks. Interspersed within the arrays are sysMEM Embedded Block RAM (EBR) blocks and sysDSP Digital Signal Processing blocks.

In addition, Avant devices provide various system level hard IP functional and interface blocks such as PCIe, Multiple Protocol PCS, and Security blocks. The PCIe hard IP supports PCIe Generation 4.0. The Avant platform also provide security and tamper detection features to help protect user designs, and cryptographic functions to help secure user data. Avant devices deliver more robust reliability by offering enhanced frame based Soft Error Detection/ Soft Error Correction (SED/SEC) functions.

The sysMEM EBR blocks are large, dedicated 36 kb fast memory blocks with built-in ECC and FIFO support. Each sysMEM block can be configured to a single, pseudo dual or true dual port memory in a variety of depths and widths as RAM or ROM. The DSP block supports a variety of multiplier and adder configurations, up to 54 × 54 MULT and 48-bit accumulator, which are the building blocks for complex signal processing capabilities.

The Avant device's sysI/O buffers contain two types of I/O blocks, Wide-Range and High-Performance I/O (WRIO and HPIO). The sysI/O buffers of the Avant devices are arranged in up to 15 banks allowing the implementation of a wide variety of I/O standards. The WRIO are located in the top banks, providing flexible ranges of general purpose I/O configurations up to 3.3 V VCCIO. The banks located on the bottom side of the device are dedicated to High Performance (HP) interfaces such as LVDS, MIPI, DDR5, DDR4/LPDDR4, and DDR3L supporting up to 1.8 V VCCIOs.

The Programmable Functional Unit (PFU) contains the building blocks for logic, arithmetic, RAM and ROM functions. The PFU block is optimized for flexibility, allowing complex designs to be implemented quickly and efficiently. Avant delivers a much higher FPGA LC capacity and performance than previous Lattice product families and is optimized for increased routability and utilization performance. The Avant fabric is based on LUT4s, which minimize power consumption due to its area efficiency. The registers in the PFU and sysI/O blocks in Avant devices can be configured to be SET or RESET, allowing the device to power up in a known state for predictable system function.

Other blocks provided include PLLs, DLLs, and configuration functions. There is one PLL per HPIO bank and one PLL per WRIO bank group throughout the device. Avant devices also include Lattice Memory Mapped Interface (LMMI) which is a Lattice standard to support simple read and write dynamic control register operations for select internal IP.

Every device in the family has a JTAG port. This family also provides a High Frequency on-chip oscillator, and soft error detect capability. The Avant devices use 0.82 V as their core voltage.

Figure 2.1, Figure 2.2, and Figure 2.3 show the high-level device floorplan of LAV-AT-200E, LAV-AT-300E, and LAV-AT-500E, respectively.

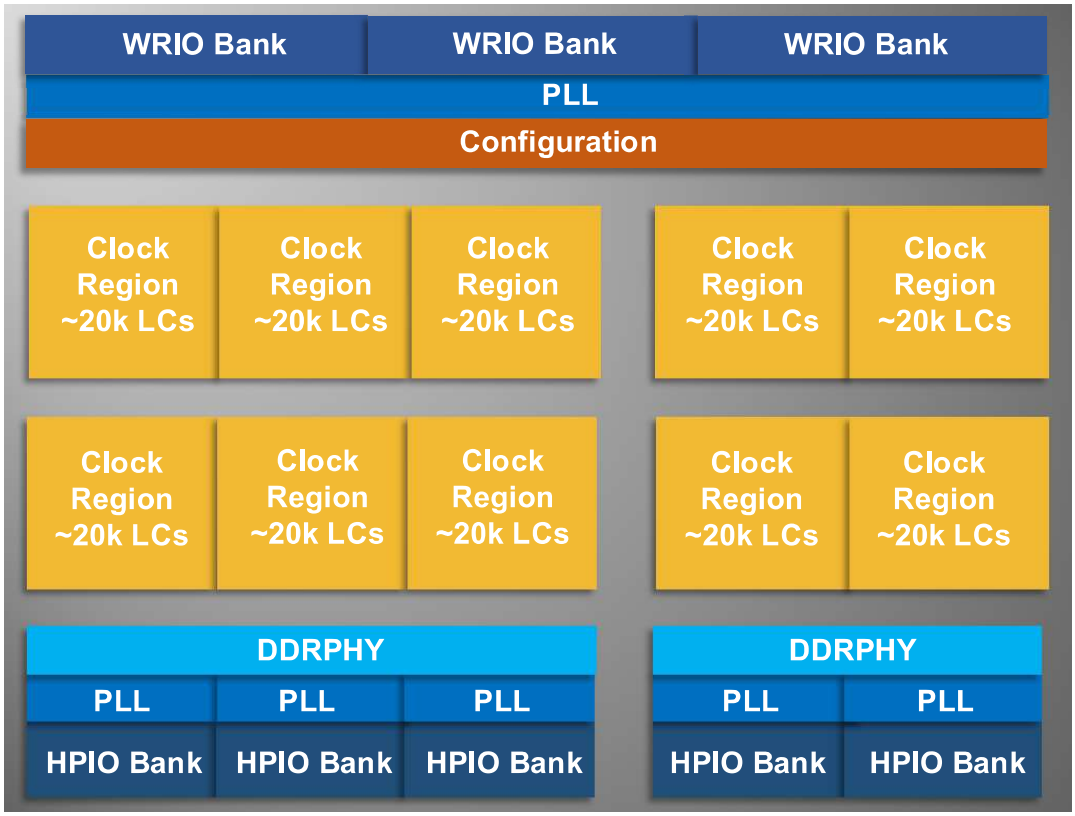


Figure 2.1. High-level Device Floorplan (LAV-AT-200E Device)

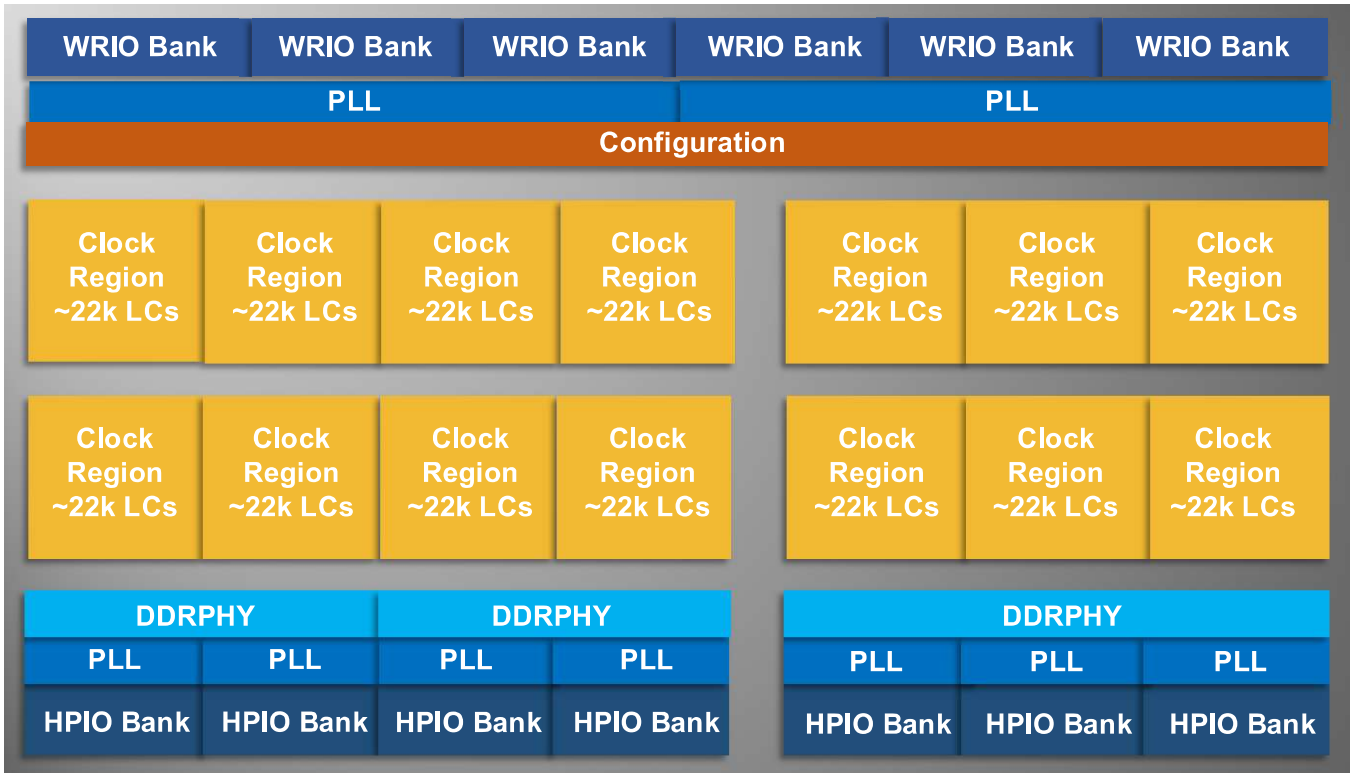


Figure 2.2. High-level Device Floorplan (LAV-AT-300E Device)

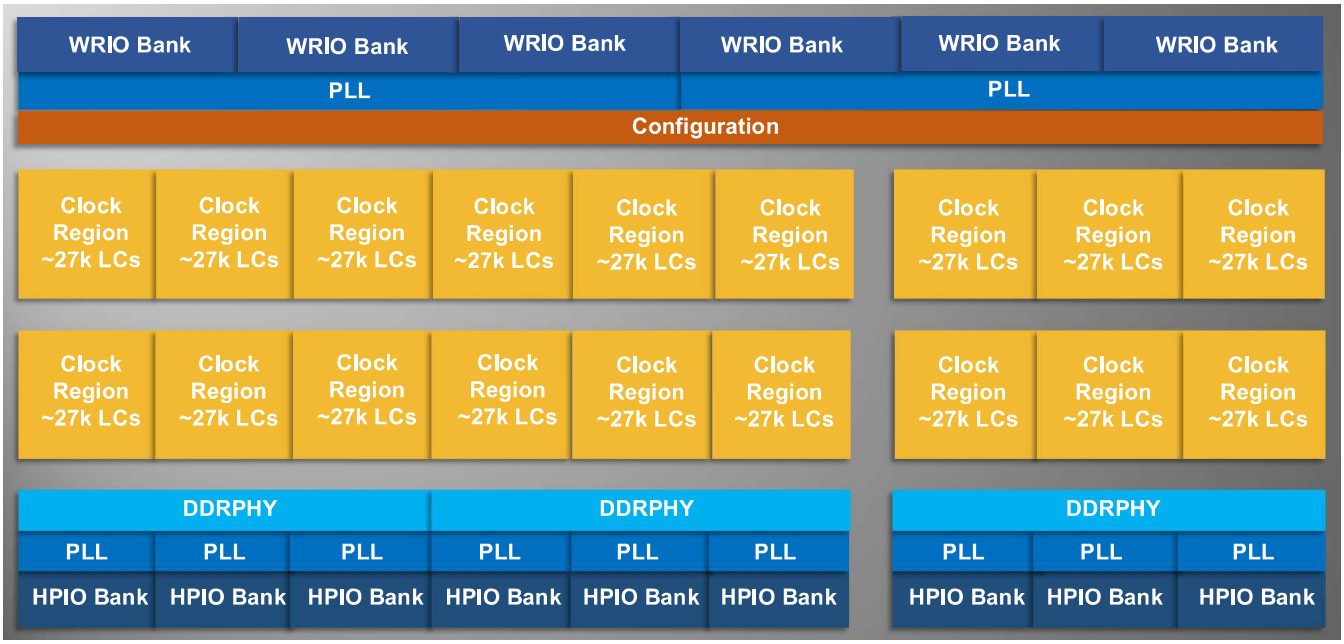


Figure 2.3. High-level Device Floorplan (LAV-AT-500E Device)

2.2. Programmable Functional Unit (PFU) Blocks

Avant delivers a higher FPGA Logic Count capability and performance compared to previous Lattice product families. It is optimized for Best-in-Class routability and utilization performance. The core of the Avant device consist of Programmable Functional Unit (PFU) blocks and each block can be used to perform Logical, Arithmetic, RAM or ROM functions. The PFU blocks are made up of LUTs and registers. Avant's fabric leverages its LUT4 area efficiency to generate its low power differentiation.

Each Avant PFU block includes the following resources:

- 12 LUT4+FF pairs (arranged as six slices, two LUT+FF per slice)
- Fast LUT4 input to output delay path
- Dedicated MUX to enable LUT5 support
- S44 Fast LUT-to-LUT connection
- Single port and pseudo dual port distributed RAM support
- Single Port Distributed RAM: 16 × 4, 16 × 8, 32 × 2, 32 × 4
- Pseudo Dual Port Distribute RAM: 16 × 4, 16 × 8, 32 × 2, 32 × 4

2.2.1. Slices

Each PFU contains six slices and each slice contains two LUT4s and two FFs. All slices have 16 inputs from routing and one from the carry-chain (from the adjacent slice or PFU). There are seven outputs: six from routing and one to carry-chain (to the adjacent PFU).

2.2.2. Modes of Operation

Slices 0-5 of the PFU have up to four potential modes of operation: Logic, Ripple, RAM, and ROM.

Logic Mode

The LUTs in each slice are configured as 4-input combinatorial lookup tables in logic mode. A LUT4 can have 16 possible input combinations. Any 4-input logic functions can be generated by programming this lookup table. A LUT5 can be constructed within one slice.

Ripple Mode

Ripple mode supports the efficient implementation of small arithmetic functions. Ripple mode also includes an optional configuration that performs arithmetic using fast carry chain methods. In this configuration (also referred to as CCU2C mode) two additional signals, Carry Generate and Carry Propagate, are generated on a per slice basis to allow fast arithmetic functions to be constructed by concatenating slices.

RAM Mode

In RAM mode, two sets of 16 × 4-bits of distributed single port RAM or pseudo dual port RAM can be constructed within one PFU. Slices 0, 1 and 2 make up one distributed RAM block and Slices 3, 4 and 5 make up the 2nd distributed RAM block. The RAM data is stored in Slices 0 and 1 of the 1st block and Slices 3 and 4 of the 2nd block. Slice 2 is used to provide memory address and control signals for the first block while Slice 5 is for the 2nd block. Avant device also supports distributed memory initialization.

The Lattice design tools support the creation of a variety of different sized memories. Where appropriate, the software constructs these using distributed memory primitives that represent the capabilities of the PFU. Table 2.1 lists the number of slices required to implement different distributed RAM primitives. For more information about using RAM in Avant devices, refer to Lattice Avant Embedded Memory User Guide (FPGA-TN-02289).

Table 2.1. Number of Slices Required to Implement Distributed RAM

	SP 16 × 4	SP 32 × 2	PDP 16 × 4	PDP 32 × 4
Number of slices	3	3	3	3

Note: SP = Single Port, PDP = Pseudo Dual Port

ROM Mode

ROM mode uses the LUT logic; hence, Slice 0 through 5 can be used in ROM mode. Preloading is accomplished through the programming interface during PFU configuration.

For more information, refer to Lattice Avant Embedded Memory User Guide (FPGA-TN-02289).

2.3. Routing

There are many resources provided in the Avant devices to route signals individually or as busses with related control signals. The routing resources consist of switching circuitry, buffers and metal interconnect (routing) segments.

The Avant family has an enhanced routing architecture that produces a compact design. The Radiant software tool takes the output of the synthesis tool and places and routes the design.

2.4. Clocking Structure

The Avant device core architecture is constructed of a number of similar sized Clock Regions (CKR). Each CKR comprises blocks such as PFUs, EBRs, DSPs, and a Regional Clock Network. For the LAV-AT-500E device, each CKR is about 27k Logic Cells (LCs). Each CKR is also associated with an I/O bank. An I/O bank may be a group of high speed SerDes I/O, a High-Performance I/O (HPIO) bank or a Wide-Range I/O (WRIO) bank. The Clock Regions are arranged in two rows and multiple columns depending on the density of the device.

The Avant clocking structure consists of clock synthesis blocks (PLLs), clock tree networks (GCLK, ECLK, RCLK and PHYCLK), on-chip oscillators, and clock modules: Clock Synchronizers and Dividers (ECLKSYNC and ECLKDIV), Dynamic Clock Selection (DCS), Dynamic Clock Control (DCC), and DLLDEL delay elements. Each of these functions is described as follows.

An overview of the Clocking Network is shown in Figure 2.4 for the Avant device.

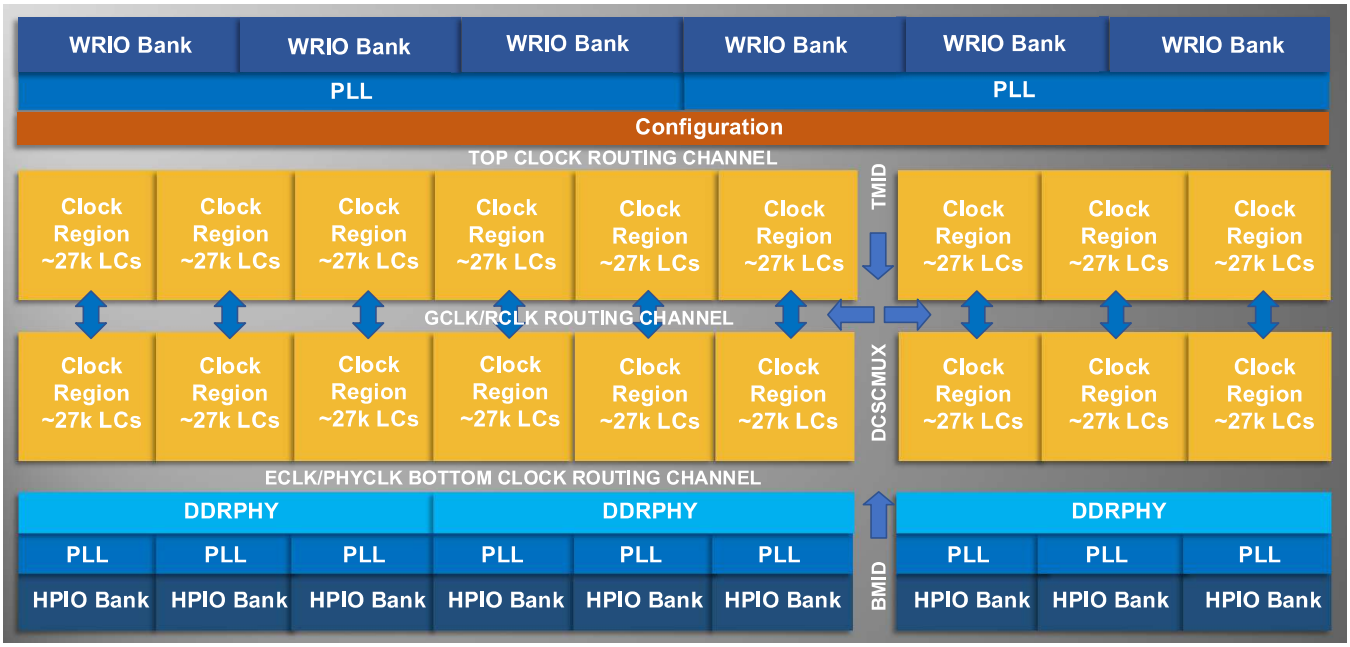


Figure 2.4. High-Level View of Clock Networks and Elements (LAV-AT-500E Device)

2.4.1. On-Chip Oscillator

The Avant device offers on board oscillator, which provides various clocks for the FPGA clock tree, Configuration block, and the system monitoring/ATM (anti-tampering) block. First, the OSC generates the user clock that drives the FPGA clock tree; this user clock is dynamically selectable between 400 MHz or 320 MHz, with 1-256 programmable divider options. Secondly, the OSC generates separate clocks for Configuration block with different frequencies of 400 and 320 MHz to support xSPI interface. Lastly, the OSC generates a hardened 112 MHz clock for system monitoring/ATM block.

2.4.2. PLL

The Avant PLL IP can be used for a variety of clock management applications such as frequency synthesis (multiplication and division of a clock), clock injection delay removal, clock phase adjustment and clock timing adjustment. The Avant PLL supports frequency synthesis by enabling the input reference clock to be multiplied up or divided down. The reference clock and feedback clock can come from various sources. The PLL (WRIO) supports six output clock selections, with each output clock having a different frequency. Each clock output can then be dynamically enabled or disabled by the user. The PLL (HPIO) supports seven output clock selections, six of which are similar to the PLL (WRIO) and an additional high-speed PHYCLK output for high-speed I/O interfaces. The Avant PLL also supports the clock injection delay removal feature where delays associated with the PLL and clock tree are removed. This feature is typically used to reduce clock path delays and is performed by aligning the PLL input clock with a feedback clock from the clock tree. Optional delay may also be added to the feedback path to further reduce the clock injection time. The Avant PLL further supports a clock phase adjustment feature. This feature provides the ability to set a specific phase offset between the outputs of the PLL. Each clock output can support an independent phase shift value.

The PLL IP supports the following key features:

- Frequency clock synthesis
- Clock tree delay cancellation
- Multiple reference and feedback clock selections
- Multiple and independent output clock controls
- Reference clock divider values – 1 to 64
- Integer Feedback divider values – 2 to 4095
- Output divider values – 1 to 256
- Supports Fractional-N divider

- Supports Spread Spectrum Clock Generation
  - Spreading rate adjustment range 15 kHz – 4 MHz
  - Spreading depth 0% to -10%
- VCO phase shift – 8 VCO phases
- Post Divider phase shift
- Dynamic VCO and divider phase shift
- Output clock bypass
- Programmable bandwidth
- Output synchronization to one main clock output (CLKOP)
- Dynamic programmability of PLL registers through the LMMI interface
- Dynamic reset GPLL operation
- Glitchless Dynamic output phase selections, controlled through fabric ports
- CLKOPHY with output up to 2400 MHz

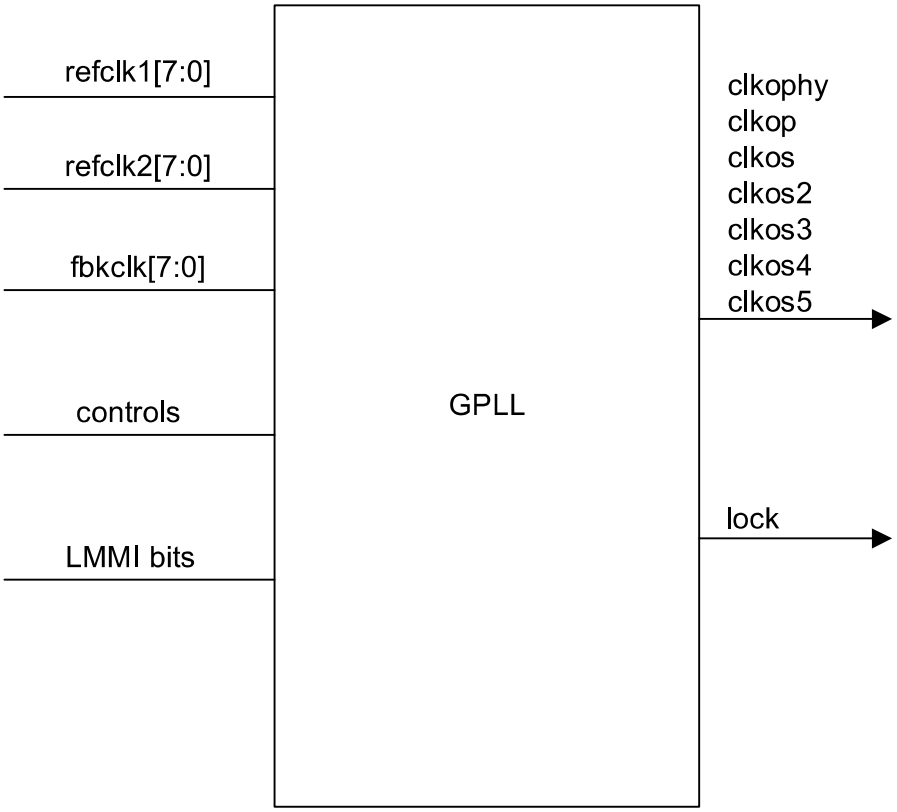


Figure 2.5. Avant PLL Block Diagram

For more details on the PLL, refer to the Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298).

2.4.3. Global Clock (GCLK)

The Global Clock Network (GCLK) provides the main clock sources in the Avant devices. The GCLK network drives the Regional Clock Networks (RCLK) of all Clock Regions (CKRs) in the device. The GCLK structure has two clock domains for all device densities, left half and right half. Each domain takes all available Global Clock sources and generates 24 independent GCLKs. These 24 GCLKs, combined with other Regional Clock sources provide 16 clocks to drive each row within a Clock Region.

Avant supports glitchless Dynamic Clock Control (DCC) feature which enables the GCLKs to be enabled or disabled to save dynamic power. There are also Dynamic Clock Selection (DCS) logic to allow glitchless selection between two clocks for the GCLK network.

2.4.4. Regional Clocks (RCLK)

The Regional Clock Network (RCLK) is the main clock network within a Clock Region. It is driven by the Global Clock Network and provides clock sources to all blocks (PFU, EBR, and DSP) within a Clock Region. The RCLK network also provide clock sources for other blocks such as the I/O banks, PLLs, SerDes, and internally generated clocks (Fabric_CLK) from the FPGA.

The RCLK network can bridge to adjacent Clock Regions to form Multi-Region Clock Networks. Specifically, it can bridge to one other Clock Region either to the left, right, top or bottom of the current Clock Region. The multi-region clock can be formed in the following topology: 1 × 1, 1 × 2, 2 × 1, 2 × 2, or 3 × 2 (column × row).

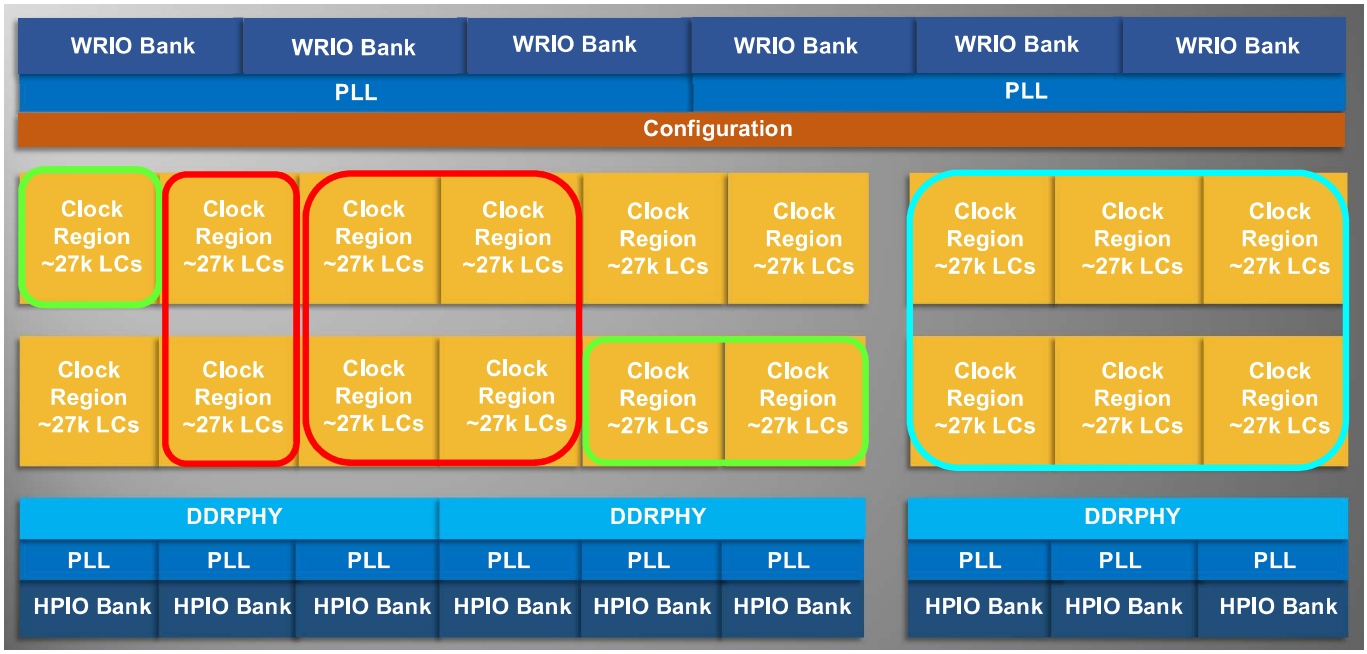


Figure 2.6. Multi-Region Clock Formation

The RCLKs are sourced from multiple inputs, referred to as Regional Clock sources. The Regional Clock sources that can drive the RCLKs are:

- Dedicated Clock Pins (PCLKT pins)
- GCLKs
- SerDes Clocks
- PLL (HPIO) outputs (CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, CLKOS5, CLKOPHY)
- PLL (WRIO) outputs (CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, CLKOS5)
- Clocks from neighboring regions, that is Regional Bridge clocks (RSBRG_* [0:3])
- Internally generated clocks (Fabric_CLK)

2.4.5. Edge Clock (ECLK)

Avant FPGAs have a number of high-speed Edge Clocks that are intended for use with the PIO in the implementation of high-speed DDR I/O interfaces. These clocks, which have low injection time and skew, are suitable to drive the high-speed I/O interfaces with high fan-out capability, such as DDR Memory or Generic DDR interfaces. The Avant device has Edge Clocks (ECLK) at the bottom of the device where the HPIO banks are located. Each HPIO bank has four Edge Clocks supporting each Clock Region (CKR). The ECLK network is also able to bridge to adjacent left or right Clock Regions to form a wider ECLK network.

The Edge clock network is powered by a separate power domain VCCHP to reduce power noise injection from the core and reduce overall noise induced jitter.

Each Edge Clock can be sourced from the following:

- Dedicated Clock Pins (PCLKT pins)
- DLLDEL outputs
- PLL (HPIO) outputs (CLKOP, CLKOS, CLKOS2, CLKOS3, CLKOS4, CLKOS5)
- ECLK Bridge clocks (EBRG_* [0:3])
- Internally generated clocks (Fabric_CLK)

For detailed information on Edge Clock connections, refer to Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298).

2.4.6. PHYCLK

The PHYCLK network is a special high frequency clock network that is used to support high frequency clocks for interface protocols for Fmax up to 2.4 GHz. The PHYCLK is driven only by a special output of the PLL (HPIO) and there is one PHYCLK per I/O bank. The PHYCLK drives the High-Speed I/O interfaces and the DDRPHY hard IP at the same time. The DDRPHY hard IP spans three HPIO sectors and the full rate PHYCLK drives the DDRPHY full-rate clock port located at the center HPIO sector. The PHYCLK also drives ECLKDIV module to provide a quad-rate clock, divided by 4, frequency clock.

2.4.7. Clock Synchronizers and Dividers

Edge Clock Synchronizer (ECLKSYNC) and Divider (ECLKDIV) provide clock synchronization and clock divider functions in Avant devices.

For further information, refer to Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298).

2.4.8. Dynamic Clock Select

The Dynamic Clock Select (DCS) is a smart multiplexer function available in the global clock network. It switches between two independent input clock sources. Depending on the operational mode, it switches between two (2) independent input clock sources either with or without any glitches. This is achieved regardless of when the select signal is toggled. Both input clocks must be running to achieve a functioning glitchless DCS output clock, but running clocks are not required when used as a non-glitchless normal clock multiplexer.

There are four dynamic clock select blocks in the Avant devices. The DCS block allows dynamic and glitchless selection between two GCLK clock sources. The output of the DCS drives the GCLKs.

Figure 2.7 shows the timing waveforms of one of the several DCS operating mode. The DCS block can be programmed to other modes. For more information about the DCS, refer to Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298).

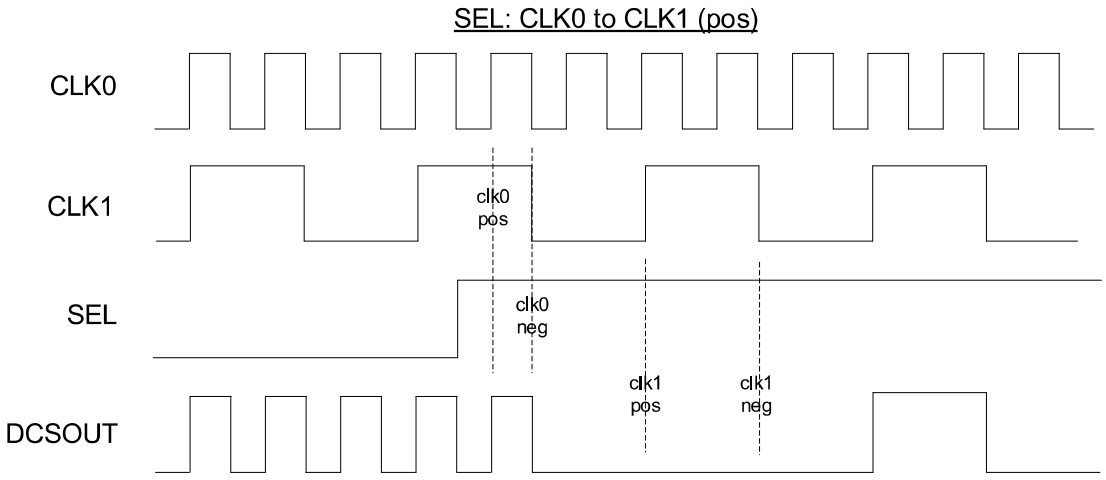


Figure 2.7. DCS Waveforms

2.4.9. Dynamic Clock Control

The Avant device has a power-saving feature known as Dynamic Clock Control. This feature allows internal logic to dynamically enable or disable the GCLKs, thus enabling overall dynamic power consumption of the device. This gating function does not create glitches or increase the clock latency to the Global Clock network. There is a DCC element associated with each 48 GCLKs.

For more information about the DCC, refer to Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298).

2.4.10. DLL Delay (DLLDEL)

DLLDEL is a passive delay component to provide necessary clock phase shift for the dedicated clock pins before driving the GCLK and ECLK network. The adjusted phase can be dynamic or static controlled. In dynamic control mode, the delay code comes from the associated DDRDLL available on the device. In static control mode, the delay control is set by software. The delay element inside the DLLDEL can be bypassed if it is not used.

There are four DLLDEL elements for each HPIO bank. Each associates with one ECLK. There is only one DLLDEL code common to all DLLDEL modules, provided by one DDRDLL within each HPIO section.

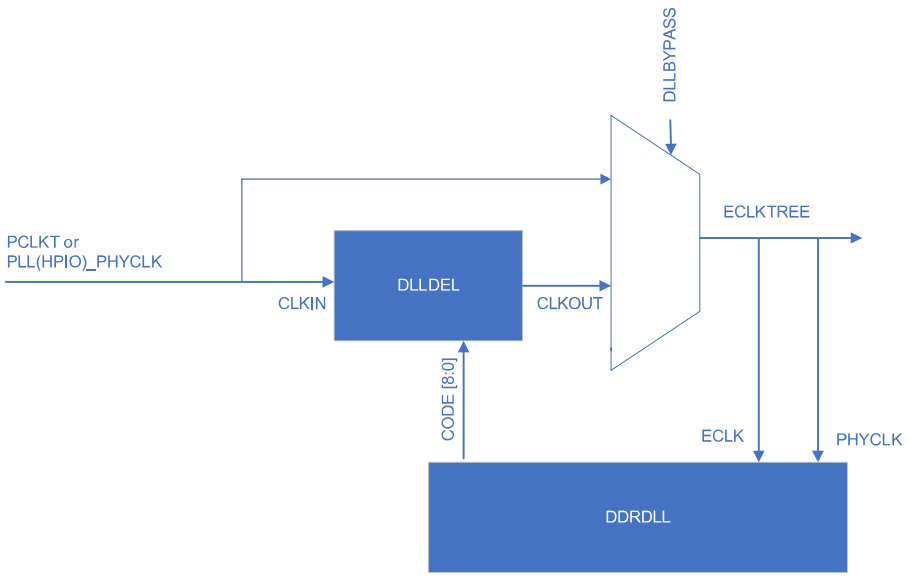


Figure 2.8. High-Level Implementation of DLLDEL and Code Control

2.5. sysMEM Memory

The Avant devices contain a number of sysMEM Embedded Block RAM (EBR). For each vertical block, it has 70 to 110 EBRs depending on the device density. The EBR consists of a 36 kb RAM with memory core, dedicated input registers and output registers as well as optional pipeline registers at the outputs. Each EBR includes functionality to support true dual-port, pseudo dual-port, single-port RAM, ROM and built in FIFO. In Avant, unused EBR blocks is powered down to minimize power consumption.

2.5.1. sysMEM Memory Block

The sysMEM block can implement single port, dual port or pseudo dual port memories. Each block can be used in a variety of depths and widths as listed in Table 2.2. FIFOs can be implemented using the built in read and write address counters and programmable full, almost full, empty and almost empty flags. The EBR block facilitates parity checking by supporting an optional parity bit for each data byte. EBR blocks provide byte-enable support for configurations with up to 72-bit data widths. For more information, refer to Lattice Avant Embedded Memory User Guide (FPGA-TN-02289).

EBR also provides a build in ECC engine. The ECC engine supports a write data width of 64 bits and it can be cascaded for larger data widths such as x128, ECC read may be performed in x1, x2, x4, x8, x16, x32, or x64 modes. The ECC parity generator creates and stores parity data for each 64-bit word written. When a read operation is performed, it compares the data with its associated parity data and report back if any Single Event Upset (SEU) event has disturbed the data. Any single bit data disturb is automatically corrected at the data output. In addition, two dedicated error flags indicate if a single-bit or two-bit error has occurred.

Table 2.2 sysMEM Block Configurations

Single Port	Pseudo Dual Port	True Dual Port
32,768 × 1	32,768 × 1	32,768 × 1
16,384 × 2	16,384 × 2	16,384 × 2
8,192 × 4	8,192 × 4	8,192 × 4
4,096x 9	4,096 × 9	4,096 × 9
2,048 × 18	2,048 × 18	2,048 × 18
1,024 × 36	1,024 × 36	1,024 × 36

2.5.2. Bus Size Matching

All of the multi-port memory modes support different widths on each of the ports (except ECC mode, which only supports a write data width of 64 bits). The RAM bits are mapped LSB word 0 to MSB word 0, LSB word 1 to MSB word 1, and so on. Although the word size and number of words for each port varies, this mapping scheme applies to each port.

2.5.3. RAM Initialization and ROM Operation

If desired, the contents of the RAM can be pre-loaded during device configuration. By preloading the RAM block during the chip configuration cycle and disabling the write controls, the sysMEM block can also be utilized as a ROM.

2.5.4. Memory Cascading

Larger and deeper blocks of RAM can be created using EBR sysMEM Blocks. Typically, the Lattice design tools cascade memory transparently, based on specific design inputs.

2.5.5. Single, Dual and Pseudo-Dual Port Modes

In all the sysMEM RAM modes, the input data and address for the ports are registered at the input of the memory array. The output data of the memory is optionally registered at the output.

2.5.6. FIFO Modes

Avant platform devices support two different types of FIFOs with sysMEM: Single Clock FIFO (FIFO) and Dual Clock FIFO (FIFO_DC). FIFO Controller Implementation has options as LUT-Based, or hardware-based. It also supports the First Word Fall Through mode.

2.5.7. Memory Output Reset

The EBR utilizes latches at the A and B output ports. These latches can be reset asynchronously or synchronously. RSTA and RSTB are local signals, which reset the output latches associated with Port A and Port B, respectively. The Global Reset (GSRN) signal can reset both ports. The output data latches and associated resets for both ports are as shown in Figure 2.9. The optional Pipeline Registers at the outputs of both ports are also reset in the same way.

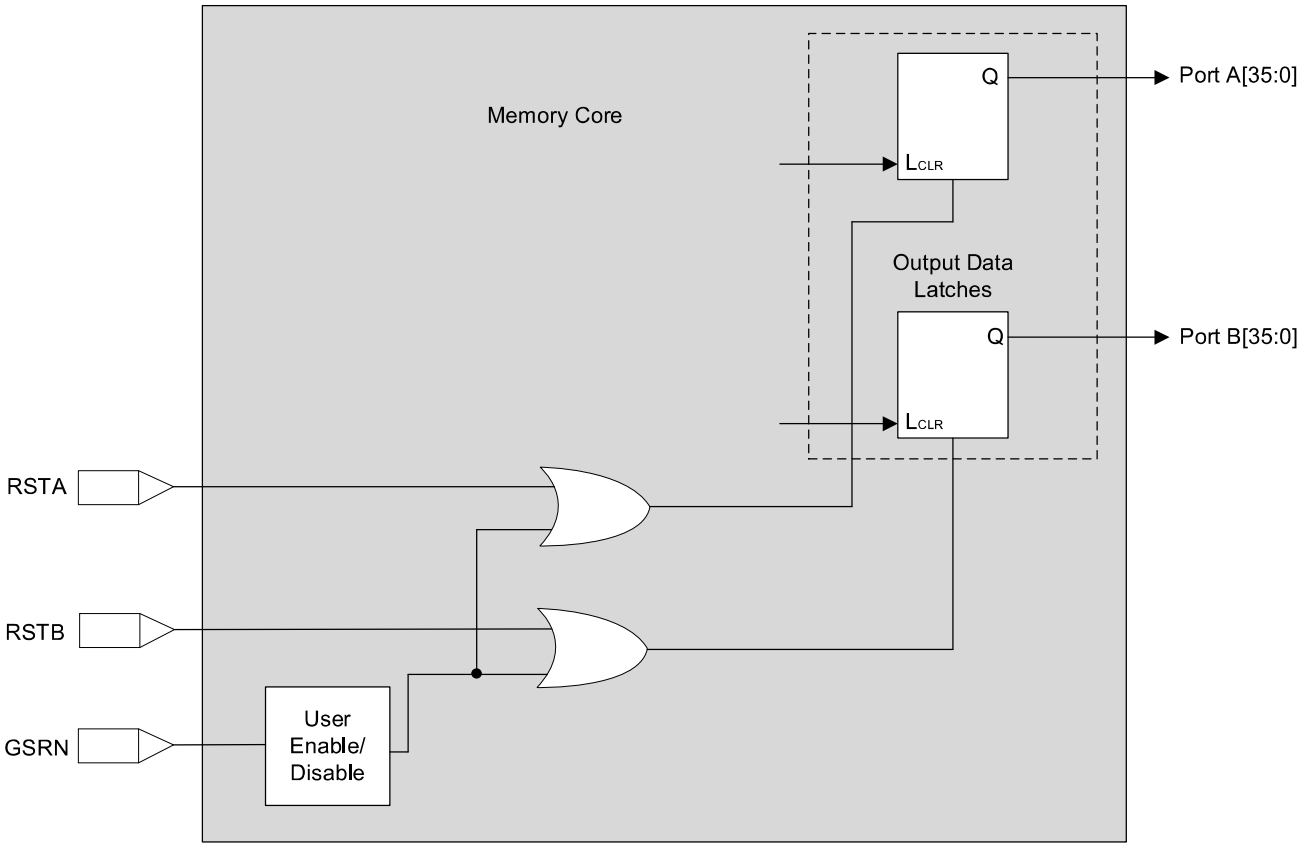


Figure 2.9. Memory Core Reset

For further information on the sysMEM EBR block, see the list of technical documentation in Supplemental Information section.

2.6. sysDSP

The Avant platform provides an enhanced sysDSP architecture, making it ideally suitable for low-cost, high-performance Digital Signal Processing (DSP) applications. The internal DSP can also run up to 625 MHz maximum frequency on a fully-pipelined input and output registers. Table 2.3 shows the summary of the DSP features.

Table 2.3. DSP Features

Overall	
Slice Base Architecture – 2 slices per DSP block	One 18 × 18 per DSP block
8 × 8 MULT	Four 8 × 8 per DSP block
9 × 9 MULT	Three 9 × 9 per DSP block
27 × 18 MULT (competition)	Two blocks
54 × 54 MULT (double precision FP)	Nine blocks
Inferable Elements	
Inferable MULT + ACCUM	One MULT + ACCUM
Internal representation number format	2's complement
Pre-Adder	18-bit
Accumulator Size	48-bit
AI/ML Kernel Support	
Dot Product MULT+ADD	9 × 9, 18 × 18
ML N-bit Accumulated Saturation	Yes
3 × 3 Kernel (8-bit) dot-product	Three blocks
Miscellaneous	
Accumulator (ALU Functions)	No
Input register chaining	Yes
Input register shift/update chaining	Yes

The Avant DSP block is a single-clock domain block with simpler structures to enable streamlined RTL implementation. Figure 2.10 shows the simplified DSP functional block, which consists of four 9 × 9 multiplier. The results of the 9 × 9 multiplier are combined to form the 18 × 18 multiplier. However, the Avant DSP only supports three 9 × 9 multiplier due to routing limitations.

Each DSP block contains an 18-bit pre-adder to support the symmetric filter and complex multiply. The 48-bit adder is also used to combine the multiplication result from the adder to any external C input or cascade the DSP input.

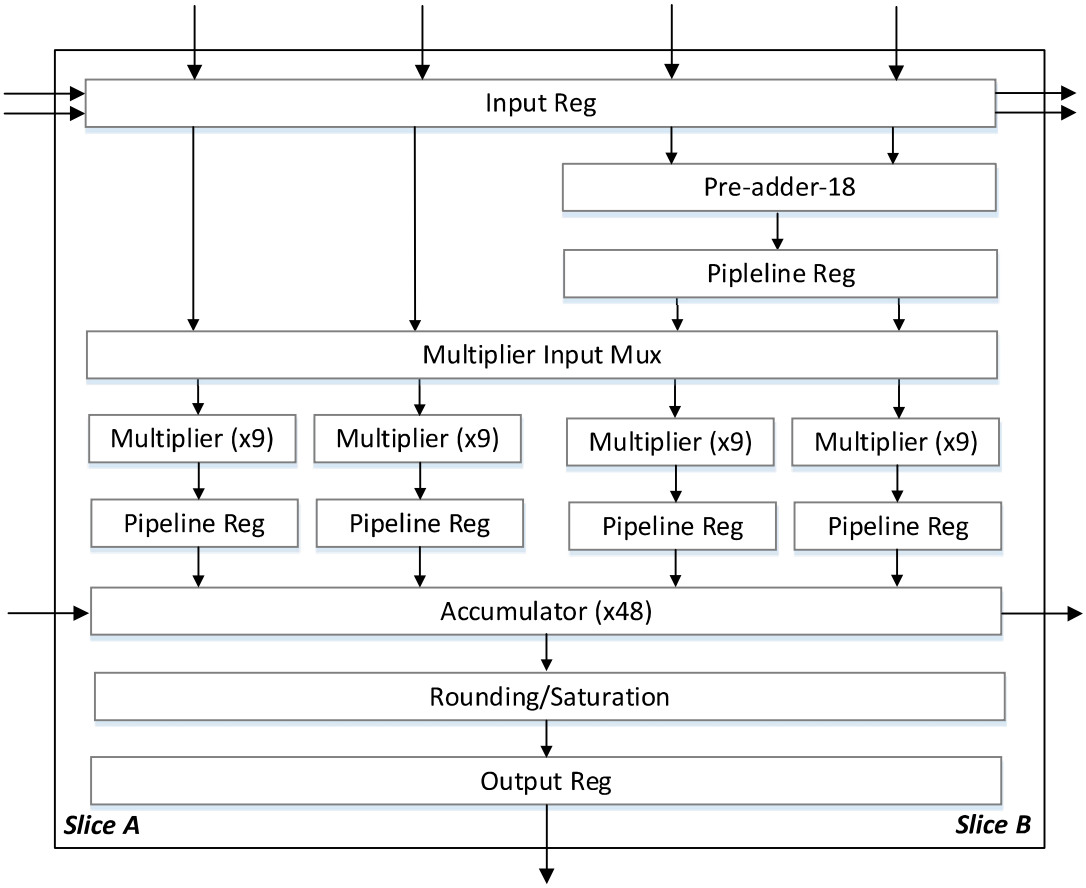


Figure 2.10. DSP Functional Block

The Avant sysDSP block supports the following basic elements.

- MULT (Multiply)
- MAC (Multiply, Accumulate)
- MULTADDSUB (Multiply, Addition/Subtraction)
- MULTADDSUBSUM (Multiply, Addition/Subtraction, Summation)

For further information, refer to Lattice Avant sysDSP User Guide (FPGA-TN-02293).

2.7. Programmable I/O (PIO)

The programmable logic associated with an I/O is called a PIO. The individual PIO are connected to their respective sysI/O buffers and pads. These buffers are arranged around the periphery of the device in groups referred to as banks. The sysI/O buffers allow users to implement a wide variety of standards that are found in today's systems including LVDS, HSUL, SSTL, POD, LVSTL, SLVS, SUBLVDS, LVCMOS and MIPI.

The Avant family contains multiple Programmable I/O Cell (PIC) blocks. Each PIC contains two Programmable I/O, PIOA and PIOB. Each PIO includes a sysI/O buffer and I/O logic. Two adjacent PIO can be joined to provide a differential I/O pair referred to as True and Comp, where True Pad is associated with the positive side of the differential I/O, and the complement with the negative.

Avant offers two types of I/O banks. The top bank I/O are WRIO (Wide Rage I/O), and the bottom bank I/O are HPIO (High Performance I/O), with following feature summary:

WRIO (Wide Range I/O) operating with a VCCIO of 3.3 V down to 1.2 V:

- LVCMOS33/25/18/12
- Programmable Drive Strengths (4 to 12 mA)
- Programmable Slew rate: Fast and Slow
- Bus Keeper, Weak Pull-up and Weak Pulldown
- Open-drain support
- Complementary Outputs through the PIC
- Bypassable glitch filter on every input
- Always on Hysteresis in the Input buffer
- Per I/O Early I/O Selection
- 50 Ω Driver Impedance to mitigate reflections on board
- Supports complementary outputs via external resistors for LVDS and subLVDS

HPIO (High-Performance I/O) operating with a VCCIO of 1.8 V down to 0.9 V:

- DDR5 @ 2133 Mbps[1]
- DDR4/LPDDR4 @ 2400 Mbps[2]
- DDR3L @ 1866 Mbps
- LVDS Differential on every pair of I/O @ 1600 Mbps
- SUBLVDSE on every pair of I/O @ 800 Mbps
- SUBLVDS RX on every pair of I/O @ 1600 Mbps
- MIPI DPHY - SLVS-200 @1800 Mbps
- SGMII TX/RX compatible with LVDS Electrical signaling
- LVCMOS18/12/10/09
- Programmable Drive Strengths (2 to 12 mA)
- On-Chip Termination.
- Dynamic control, trimmed on-chip 100 Ω differential termination resistor
- External and Internal (trainable) VREF in each bank
- Polarity Control for Differential RX and TX Paths
- Open-drain
- Programmable Slew rates: Fast and Slow
- Programmable Tx pre-emphasis
- Complementary Outputs

Notes:

1. While Avant HPIO can support DDR5 up to 2400 Mbps, Avant has defined DDR5 operation only up to 2133 Mbps. DDR5 operational ranges defined by JEDEC are up to 2100 Mbps and >2400 Mbps.
2. Avant-E supports DDR4/LPDDR4 up to 1866 Mbps.

For more information about DDR implementation in I/O Logic and DDR memory interface support, refer to Lattice Avant High-Speed I/O and External Memory Interface (FPGA-TN-02300).

2.7.1. Supported sysI/O Standards

Avant sysI/O buffers support both single-ended differential and differential standards. Single-ended standards can be further subdivided into internally ratioed standards such as LVCMOS, and externally referenced standards such as HSUL and SSTL. The buffers support the LVCMOS 0.9 V, 1.0 V, 1.2 V, 1.8 V, 2.5 V, and 3.3 V standards. Differential standards supported include LVDS, SLVS, differential LVCMOS, differential SSTL, differential HSUL, differential LVSTL, and differential POD. For better support of video standards, subLVDS and MIPI D-PHY are also supported. Table 2.4 and Table 2.5 provide a list of sysI/O standards supported in Avant devices.

2.7.2. sysI/O Banking Scheme

Avant devices have up to 15 banks in total. For 500k device, there are six banks on top and nine banks on the bottom side of device. The lower density Avant device has less banks. The top banks support up to VCCIO 3.3 V while bottom banks support up to VCCIO 1.8 V. In addition, bottom banks support one external VREF input for flexibility to receive the referenced input level on the same bank. And it also has the internal generated VREF input, which can be trained. DDR5 and DDR4/LPDDR4 must use internal VREF. For the top bank 0, bank 1, and bank 2, these provide 52 total I/O, which is also the same for the bank 12, bank 13, and bank 14. For bottom banks, each bank is built with 52 data I/O and other power/ground pads. The data I/O is divided into four DQS Groups comprised of 12 I/O each, and four addition shared function I/O, like VREF_EXT, PLL clock input and external resistor input. Figure 2.11 shows the location of each bank.

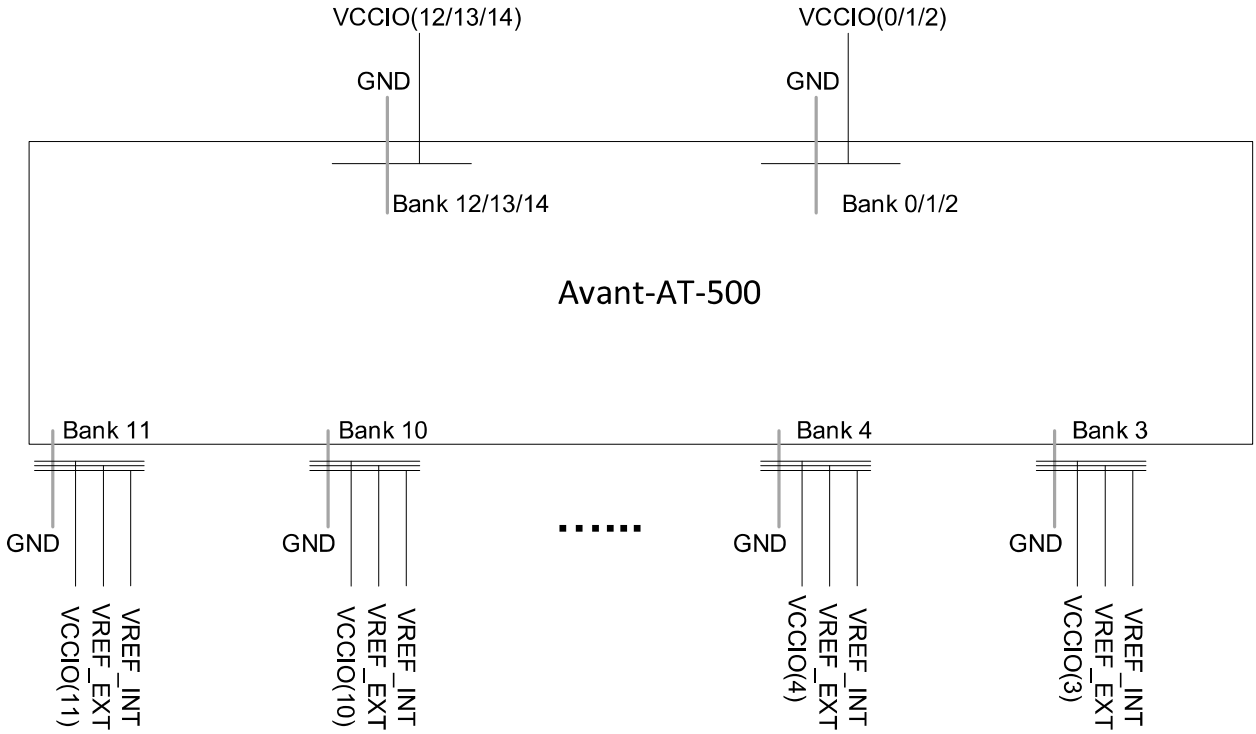


Figure 2.11. sysI/O Banking

Typical sysI/O Behavior During Power-up

The internal Power-On-Reset (POR) signal is deactivated when V_{CC} and V_{CCAUX} have reached satisfactory levels. After the POR signal is deactivated the FPGA core logic becomes active. It is the responsibility of the user to ensure that all other V_{CCIO} banks are active with valid input logic levels to properly control the output logic states of all the I/O banks that are critical to the application. For more information about controlling the output logic state with valid input logic levels during power-up in Avant devices, see the list of technical documentation in Supplemental Information section.

V_{CC} and V_{CCAUX} supply the power to the FPGA core fabric, whereas V_{CCIO} supplies power to the I/O buffers. For the different power supply voltage levels supported by the I/O banks, refer to Lattice Avant sysI/O User Guide (FPGA-TN-02297) for detailed information.

sysI/O Standards Supported by I/O Bank

All banks can support multiple I/O standards under the VCCIO rules discussed above. Table 2.4 and Table 2.5 summarize the I/O standards supported on various sides of the Avant device.

Table 2.4. Single-Ended I/O Standards Supported on Various Sides

Standard	Top(WRIO)	Bottom(HPIO)	Input	Output	Bi-directional
LVCMOS33	Yes	—	Yes	Yes	Yes
LVCMOS25	Yes	—	Yes	Yes	Yes
LVCMOS18	Yes	Yes	Yes	Yes	Yes
LVCMOS12	Yes	Yes	Yes	Yes	Yes
LVCMOS10	—	Yes	Yes	Yes	Yes
LVCMOS09	—	Yes	Yes	Yes	Yes
SSTL 135	—	Yes	Yes	Yes	Yes
HSUL12	—	Yes	Yes	Yes	Yes
LVSTL11_I	—	Yes	Yes	Yes	Yes
LVSTL11_II	—	Yes	Yes	Yes	Yes
POD12	—	Yes	Yes	Yes	Yes
POD11	—	Yes	Yes	Yes	Yes

Table 2.5. Differential I/O Standards Supported on Various Sides

Standard	Top(WRIO)	Bottom(HPIO)	Input	Output	Bi-directional
LVDS	—	Yes	Yes	Yes	Yes
SUBLVDS	—	Yes	Yes	—	—
SLVS	—	Yes	Yes	Yes	—
SUBLVDSE	Yes	Yes	—	Yes	—
LVDSE	Yes	—	—	Yes	—
MIPI_D-PHY	—	Yes	Yes	Yes	Yes
SSTL135D	—	Yes	Yes	Yes	Yes
HSUL12D	—	Yes	Yes	Yes	Yes
LVSTL11D_I	—	Yes	Yes	Yes	Yes
LVSTL11D_II	—	Yes	Yes	Yes	Yes
POD12D	—	Yes	Yes	Yes	Yes
POD11D	—	Yes	Yes	Yes	Yes

For more information on the various sysI/O features available on the Avant device, refer to Lattice Avant sysI/O User Guide (FPGA-TN-02297).

2.8. Programmable I/O Cell (PIC)

The programmable I/O cells (PIC) provides I/O function and necessary gearing logic associated with PIO. Avant consists of base PIC and gearing PIC.

Base PICs contain three blocks: an input register block, output register block, and tri-state register block. These blocks contain registers for operating in a variety of modes along with the necessary clock and selection logic. Base PICs cover the top bank. Gearing PICs contain gearing logic and edge monitor used for locating the center of data window. Gearing PICs cover the bottom banks to support DDR operation.

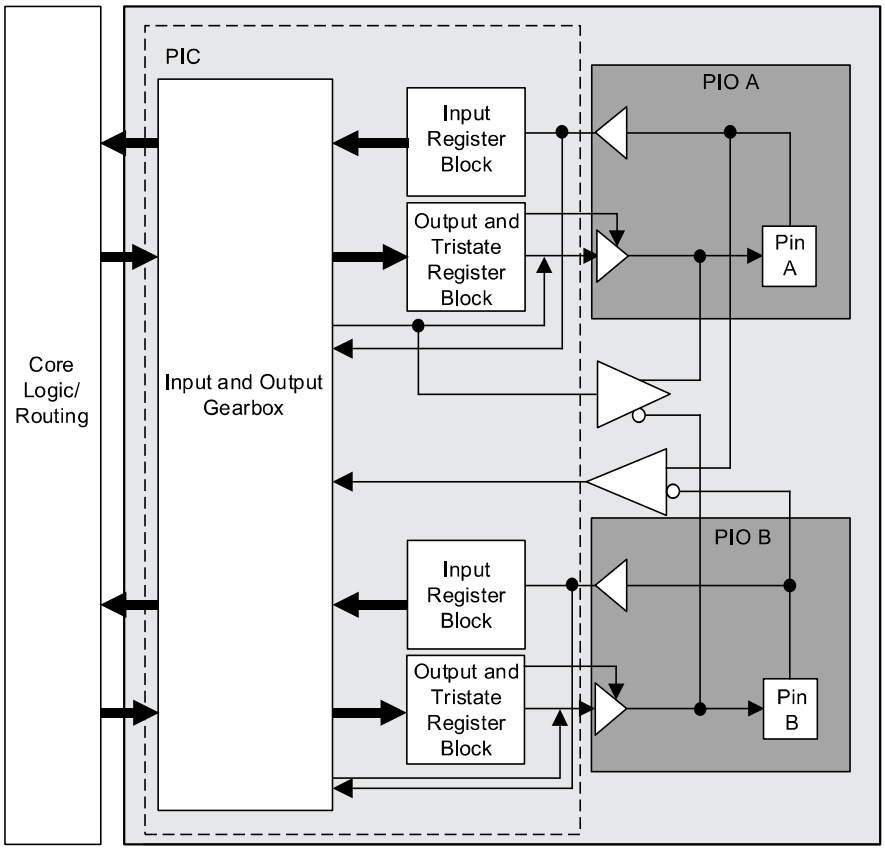


Figure 2.12. Group of Two High Performance Programmable I/O Cells

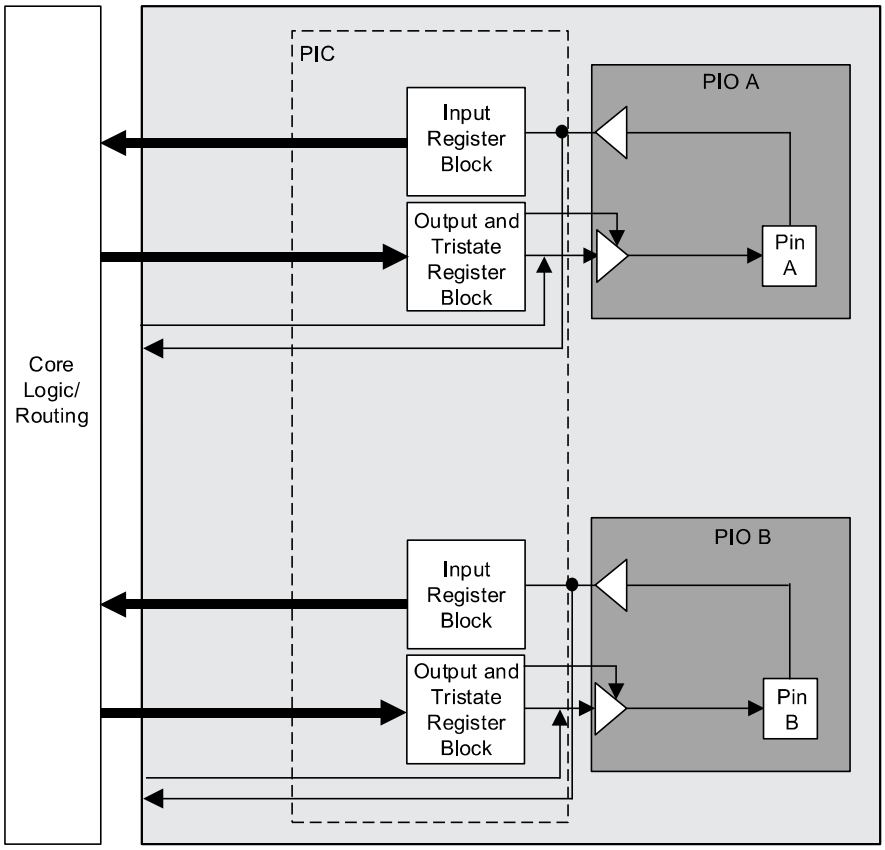


Figure 2.13. Wide Range Programmable I/O Cells

2.8.1. Input Register Block

The input register blocks for the PIO contain delay elements and registers that can be used to condition high-speed interface signals before they are passed to the device core. In addition, the input register blocks for the PIO on the bottom edges include built-in FIFO logic to interface to GDDR and Octal SPI.

The Input register block on the bottom side includes gearing logic and registers to implement 2:1, 4:1, 8:1, and 10:1 gearing functions. It can also implement the 7:1 gearing function used for 7:1 LVDS interfaces. It uses three sets of registers – shift, update, and transfer to implement gearing and the clock domain transfer. The first stage registers sample the high-speed input data by the high-speed edge clock on its rising and falling edges. The second stage registers perform data alignment based on the control signals. The third stage pipeline registers pass the data to the device core synchronized to the low-speed system clock. For more information on gearing function, refer to Lattice Avant High-Speed I/O and External Memory Interface (FPGA-TN-02300).

2.8.2. Output Register Block

The output register block registers signals from the core of the device before they are passed to the sysI/O buffers.

The Avant output data path has programmable registers and output gearing logic. On the bottom side, the output register block can support 2:1, 4:1, 8:1, 10:1, and 7:1 gearing GDDR interfaces. On the top side, the banks support 2:1 gearing. The programmable delay cells are also available in the output data path.

For more information on gearing function, refer to Lattice Avant High-Speed I/O and External Memory Interface (FPGA-TN-02300).

2.8.3. Tri-state Register Block

The tri-state register block registers tri-state control signals from the core of the device before they are passed to the sysI/O buffers. The block contains a register for SDR operation. In SDR, the TD input feeds one of the flip-flops that then feeds the output.

2.9. DDR Memory Support

Avant DDRPHY is compliant with the DFI 4.0+ specification and supports multiple DDR memory standards: DDR5, DDR4/LPDDR4, and DDR3L. Table 2.6 lists a summary of Avant supported memory standards and the max speed rates.

Table 2.6. Summary of DDR Standards and Max Rates

Standard	Max Speed	Number of Ranks
DDR5	2133 Mbps[1]	2
DDR4/LPDDR4	2400 Mbps[2]	2
DDR3L	1866 Mbps	2

Notes:

1. While Avant HPIO can support DDR5 up to 2400 Mbps, Avant has defined DDR5 operation only up to 2133 Mbps. DDR5 operational ranges defined by JEDEC are up to 2100 Mbps and >2400 Mbps.
2. Avant-E supports DDR4/LPDDR4 up to 1866 Mbps.

2.9.1. DDRPHY Overview

The Avant DDRPHY interface provides a physical interface between the FPGA soft memory controller and DRAM device. It consists of two logic blocks: 2:1 gearing logic and sync logic IP wrapper to implement quarter rate DDRPHY functionality.

Avant DDRPHY shares routing resources between the PIC and DDRPHY. In cases where the DDRPHY is partially used, the I/O can be configured in GDDR mode.

For DQ and CA lanes, the PHYCLK can operate up to 2.4 GHz to achieve 2.4 Gbps performance while leveraging a 300 MHz fabric interface clock.

For additional details on the Avant DDRPHY, refer to the Lattice Avant High-Speed I/O and External Memory Interface (FPGA-TN-02300).

2.9.2. DQS Grouping for DDR Memory

Avant DDRPHY occupies three HPIO banks, where each HPIO bank has 52 I/O.

Avant memory interfaces can support up to:

- x72 full DIMMs (three HPIO banks)
- x40 half DIMM (two HPIO banks)
- x16 interfaces (one HPIO banks)

In DDRPHY DDRx memory mode, the digital logic is partitioned into two types of lanes: DQ/DQS lanes and CA lanes. A DQS group contains six I/O pairs to provide 12 high-speed I/O. These can be configured as differential/complementary I/O or individual I/O. Within each DQS group, there are two pre-placed pins for DQS and DQSN signals. The rest of the pins in the DQS group can be used as DQ and DM/DMI/DBI signals. The number of pins bonded out in each DQS group is package dependent. For all Avant supported memory standards, a data lane occupies 11 bits in total: 8-bit DQ, DQS/DQSN, and DM/DMI/DBI. DDRPHY CA lane pin assignments are different based on the DDR standard used.

2.10. Device Configuration

All Avant devices contain two ports that can be used for device configuration. The Test Access Port (TAP), which supports bit-wide configuration, and the sysCONFIG port, support serial, quad, and byte configuration. The TAP, which has dedicated I/O, supports the IEEE Standard 1149.1 Boundary Scan specification. CFGMODE, PROGRAMN, INITN, and DONE arededicated configuration pins. The remaining sysCONFIG pins are used as dual function pins. Refer to Lattice Avant sysCONFIG User Guide (FPGA-TN-02299) for more information about using the dual-use pins as general purpose I/O.

The following configuration interfaces are supported:

- Master SPI – x1, x2, x4, Octal SPI[1] (x8, dual transfer rate)
- Slave SPI – x1, x2, x4, Octal SPI[1] (x8, dual transfer rate)
- JTAG (proprietary protocol)

Note:

1. Octal SPI is not supported in Avant-E.

On power-up, based on the voltage level (high or low) of the CFGMODE pin, the FPGA SRAM is configured by the appropriate sysCONFIG port. If CFGMODE pin is *low*, the FPGA is in Slave configuration mode (Slave SPI or TAP). If CFGMODE pin is driven high, the FPGA is in Master SPI booting mode. In Master SPI booting mode, the FPGA boots from an external SPI flash.

2.10.1. Enhanced Configuration Options

The Avant devices have enhanced configuration features such as:

- Early I/O release
- Bitstream Decryption
- Decompression Support
- Watchdog Timer support
- Dual and Multi-boot image support

Early I/O Release is the configuration feature in which certain I/O banks are released earlier so that customer systems have minimal disruption. For more details, refer to Lattice Avant sysCONFIG User Guide (FPGA-TN-02299).

Watchdog Timer is the configuration feature that helps the user to add a programmable timer option for timeout applications.

Dual-Boot and Multi-Boot Image Support

Dual-boot and multi-boot images are supported for applications requiring reliable remote updates of configuration data for the system FPGA. After the system is running with a basic configuration, a new boot image can be downloaded remotely and stored in a separate location in the configuration storage device. Any time after the update the Avant devices can be re-booted from this new configuration file. If there is a problem, such as corrupt data during download or incorrect version number with this new boot image, the Avant device can revert back to the original backup golden configuration and try again. This all can be done without power cycling the system. For more information, refer to Lattice Avant sysCONFIG User Guide (FPGA-TN-02299).

2.10.2. JTAG

All Avant devices contain various ports that can be used for configuration, including a Test Access Port (TAP). This allows functional testing of the circuit board on which the device is mounted through a serial scan path that can access all critical logic nodes. Internal registers are linked internally, allowing test data to be shifted in and loaded directly onto test nodes, or test data to be captured and shifted out for verification. The test access port consists of dedicated I/O: TDI, TDO, TCK, and TMS. The test access port uses VCCIO2 for power supply.

For more information, refer to Lattice Avant sysCONFIG User Guide (FPGA-TN-02299).

2.10.3. Single Event Upset (SEU) Handling

Avant devices have an improved, hardware implemented, Soft Error Detection (SED) circuit which can be used to detect SRAM errors so they can be corrected, either automatically or after notification and consent. There are two layers of SED implemented in Avant making it more robust and reliable.

The SED hardware in Avant devices is part of the Configuration block. The SED module in Avant is an enhanced version as compared to the SED modules implemented in other Lattice devices. The configuration data is divided into frames so that the entire FPGA can be programmed precisely with ease. The SED hardware reads data from the FPGAs configuration memory and performs an Error Correcting Code (ECC) calculation on every frame of configuration data. With Automatic operation, once a single error is detected it is corrected, a notification is generated and SED resumes operation. With Consent operation, once a single error is detected the SED hardware halts and a fabric notification is generated. Upon consent from the fabric, the single error is corrected and the SED resumes operation. For single bit errors, the corrected value is rewritten to the particular frame using ECC information. In all modes, if more than one-bit error is detected within one frame of configuration data, a fabric error notification is generated and the SED continues operation. Avant devices also have dedicated logic to perform Cycle Redundancy Code (CRC) checks for the entire bitstream, which runs in parallel along with ECC.

After the ECC is calculated on all frames of configuration data, CRC is calculated and checked for the entire bitstream. ECC and CRC checks do not include the contents of RAMs (EBR and distributed RAM).

For further information on SED support, refer to Lattice Avant Soft Error Detection (SED)/Correction (SEC) User Guide (FPGA-TN-02290).

2.11. Trace ID

Each Avant device contains a unique (per device) TraceID that can be used for tracking purposes or for IP security applications. The TraceID is 64 bits long. Eight out of 64 bits are user-programmable, the remaining 56 bits are factory-programmed. The TraceID is accessible through the SSPI and JTAG interfaces. For further information on TraceID, refer to Using TraceID (FPGA-TN-02084).

2.12. SerDes and PCS

The Avant platform SerDes/PCS is a multi-protocol PHY design with quad (x4) base. Each quad consists of the following:

- Quad x4 PMA: 4 Tx, 4 Rx, 1 common block (REFCLK, PLL)
- Multiple Protocol PCS (MPPCS)

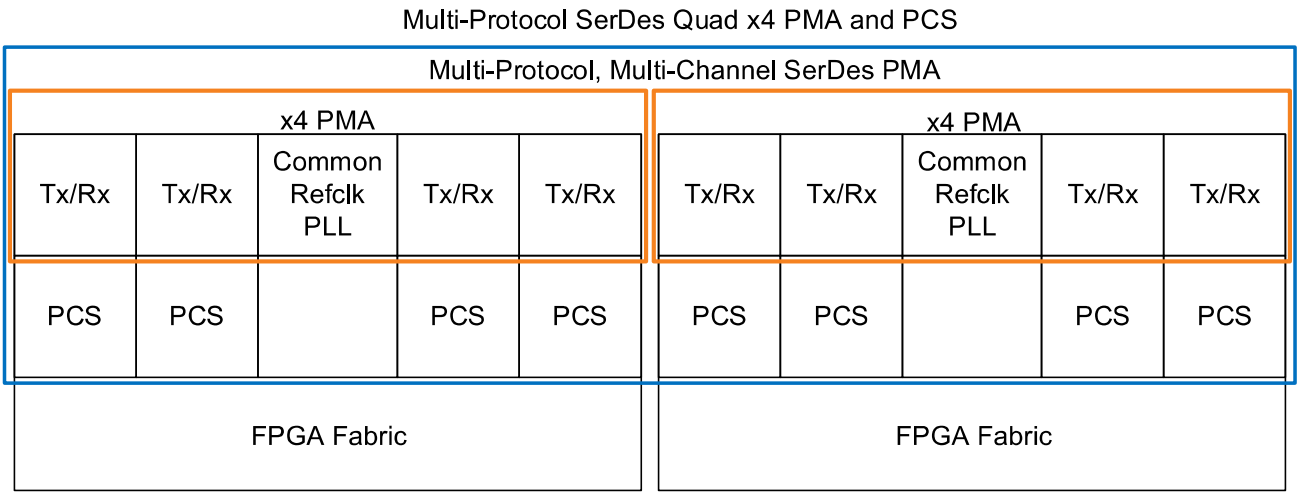


Figure 2.14. SerDes Overview Diagram

The Avant SerDes is in Quad x4 units. Each device may support multiple instances of quad x4 units.

The PMA covers multiple sub-ranges of 1.25 Gbps to 26.5625 Gbps. Table 2.7 shows the list of supported protocols.

Table 2.7. SerDes/PCS Supported Protocols

Protocol	PMA Support	PCS Support	Link and Upper Layer Support
PCIe Gen1/2/3	Yes	Yes	Hard DLL, TL and DMA
PCIe Gen4	Yes	Yes	Hard DLL, TL and DMA
10G Ethernet	Yes	Yes	Soft MAC in Fabric
25G Ethernet	Yes	Yes	Soft MAC in Fabric
DisplayPort	Yes	Yes	Soft logic in Fabric
SLVS-EC	Yes	Yes	Soft logic in Fabric
CoaXPress	Yes	Yes	Soft logic in Fabric
CPRI (x1, x2, x4, x8)	Yes	Yes	Soft logic in Fabric
eCPRI	Yes	Yes	Soft logic in Fabric
ROE	Yes	Yes	Soft logic in Fabric
SyncE	Yes	Yes	Soft logic in Fabric
JESD204B, C	Yes	Yes	Soft logic in Fabric

Table 2.8. Avant SerDes Protocol Width Support

Protocol	Typical Width	Rate (Gbps) × Width Examples
PCIe	x1, x2, x4, x8	(2.5, 5, 8, 16) × (1, 2, 4, 8)
Ethernet	x1	1.25 × 1, 3.125 × 1, 3.125 × 4, 5 × 1, 6.25 × 2, 10.3125 × 1, 25.78125 × 1x12/x16 Port Ethernet Switches
DP/eDP	x1, x2, x4	(1.62, 2.7, 5.4, 8.1) × (1, 2, 4)
SLVS-EC	x4, x8	(1.25, 2.5, 5) × (4, 8)
CoaXPress	x1, x2, x4, x8	(3, 6.25, 10, 12.5) × (1, 2, 4, 8)
CPRI	x1, x2, x4, x8	(1.2288, 2.4576, 3.072, 4.915, 6.144, 8.11008, 9.8304, 10.1376, 12.16512, 24.3) x (1, 2, 4, 8)
eCPRI	x1	10.3125 × 1, 25.78125 × 1
ROE	x1	10.3125 × 1, 25.78125 × 1

Protocol	Typical Width	Rate (Gbps) × Width Examples
SyncE	x1	1.25 × 1, 3.125 × 1, 3.125 × 4, 5 × 1, 10.3125 × 1, 25.78125 × 1
JESD204B/C	x1, x2, x4, x8	(3.125, 6.25, 12.5, 25) × (2, 4, 8)

In Avant, the wide bus width is supported with running reference clock distribution to each quad. Synchronization logic provided to ensure multiple x4 is in sync in the PMA IP.

The SerDes feature is not supported in the Avant-E family.

2.12.1. SerDes/PMA Block

The PMA hard macro comprises of four lanes with a full duplex transceiver for each lane, each lane includes Transmitter (TX), Receiver (RX), Support, and test features. The TX lane receives 8, 10, 16, or 20 bits of transition-encoded data synchronous with a Tx clock, serializes it into a single stream of differential transmitted data and transmits to the lane. The transmitter supports multi-level output driver, multi-level transition emphasis, and multi-level Common Mode levels. The RX lane performs a series functions such as adaptive continuous-time linear equalization (CTLE), decision feedback equalization (DFE) and clock data recovery (CDR) to ensure recovered clock is used to retime received data with channel loss compensated and optimized, and send it to deserializer which produces parallel data and a parallel data clock for the relevant PCS lane. The Support block provides all the common functions for the RX/TX link, TX clock generation, TX/RX termination calibration, biasing voltage, and reference clock buffering.

2.12.2. Multi-Protocol PCS (MPPCS)

There are two major modes of operations:

- Lower data rate, up to 10 Gbps
- Higher data rate, up to 25 Gbps

The Avant SerDes supports multi-protocol PCS with key features below:

- Encoder/Decoder: 8B10B, 64B/66B, 128B/130B.
- Comma detection, and word alignment
- Clock tolerance Elastic FIFO
- Gearing to FPGA by 8/10/16/20/32/40/64/80/128
- Built in Pipe Control Interface for PCIe
- GMII/XGMII/XLGMII/CGMII for Ethernet
- Forward Error Correction (FEC) supporting both:
  - BASE-R/Fire Code FEC
  - KR RS-FEC 528,514 FEC (Reed-Solomon)
  - Primary use in 25G Ethernet, 24.3 Gbps CPRI, and 25G JESD204C
- Programmable Interface Width/Speed to connect to either hard IP (PCIe LL controller) or FPGA fabric
- Channel bonding, for channels within quads, and between quads: Rx FIFO alignment and Tx FIFO delay adjustment to minimize channel to channel skew.
- Parallel loopback mode for testability

2.12.3. Multi-Protocol PHY (MPPHY) Integration

Figure 2.15 shows the MPPHY top-level integration block diagram.

Each PMA lane has a corresponding PCS lane. The 40-bit SerDes interface between PMA and PCS and the 32-bit PIPE interface between PCS and link layer follow the Intel Standard PHY Interface [PHY].

Since both PMA and PCS are APB clients, a two-way APB splitter is required at the MPPHY top level. For standalone instantiation of the MPPHY block, support of the native Lattice Memory-Mapped Interface (LMMI) protocol is required. The required functionality is LMMI initialization per Lattice protocol and a bridge for translation into APB protocol.

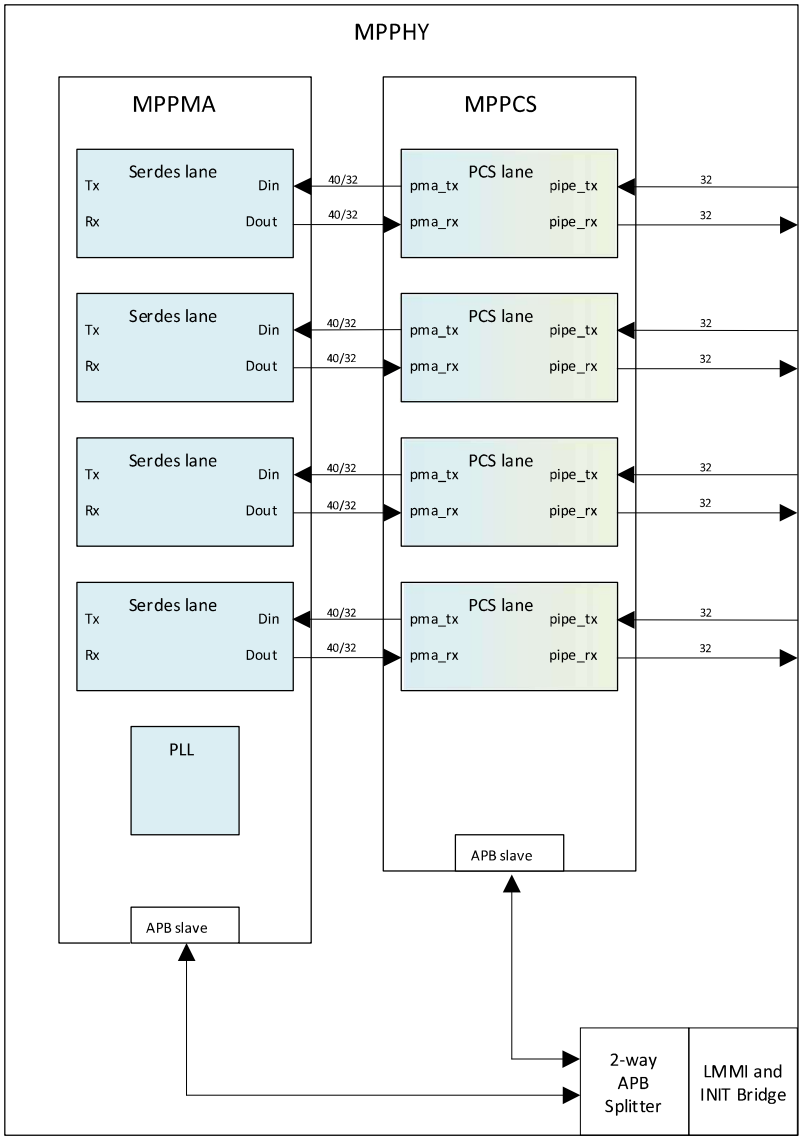


Figure 2.15. MPPHY Top-Level Block Diagram

2.12.4. Peripheral Component Interconnect Express (PCIe)

The Avant Device features up to 24 lanes of hardened PCIe, with a maximum PCIe link width of x8. The PCIe block implements all three layers defined by the PCI Express Specification: Physical, Data Link, and Transaction as shown in Figure 2.16. Below is a summary of the features supported by the PCIe block:

- PCIe Express Base Specification 4.0 compliant including compliance with earlier PCI Express Specifications
- Support for link width of x8 PCI Express Lanes with support for bifurcation, including 1 × 8, 1 × 4, 1 × 2, 1 × 1
- 16.0 GT/s, 8.0 GT/s, 5.0 GT/s, and 2.5 GT/s line rate support
- Endpoint and Root Complex support (Implements Type 0 Configuration Registers in Endpoint Mode, and Type 1 Configuration Registers in Root Complex Mode)
- Multi-function support with up to eight physical functions
- Support for Autonomous and Software-Controlled Equalization
- Support for Figure of Merit and Up/Down PIPE PHY Equalization
- Flexible Equalization methods (Algorithm, Preset, User-Table, Adaptive-Table, Firmware-controlled)
- ECC RAM and Parity Data Path Protection
- 64-bit Core Data Width (per lane)
- Robust Error-Handling support, including AER, ECRC generation/checking, recovery from parity and ECC errors, and error injection diagnostics.
- Optional Hardened high-performance multi-channel scatter-gather DMA controller
- Support for power management features including ASPM L0s and L1, L1 PM states with CLKREQ, Power Budgeting, and Dynamic Power Allocation

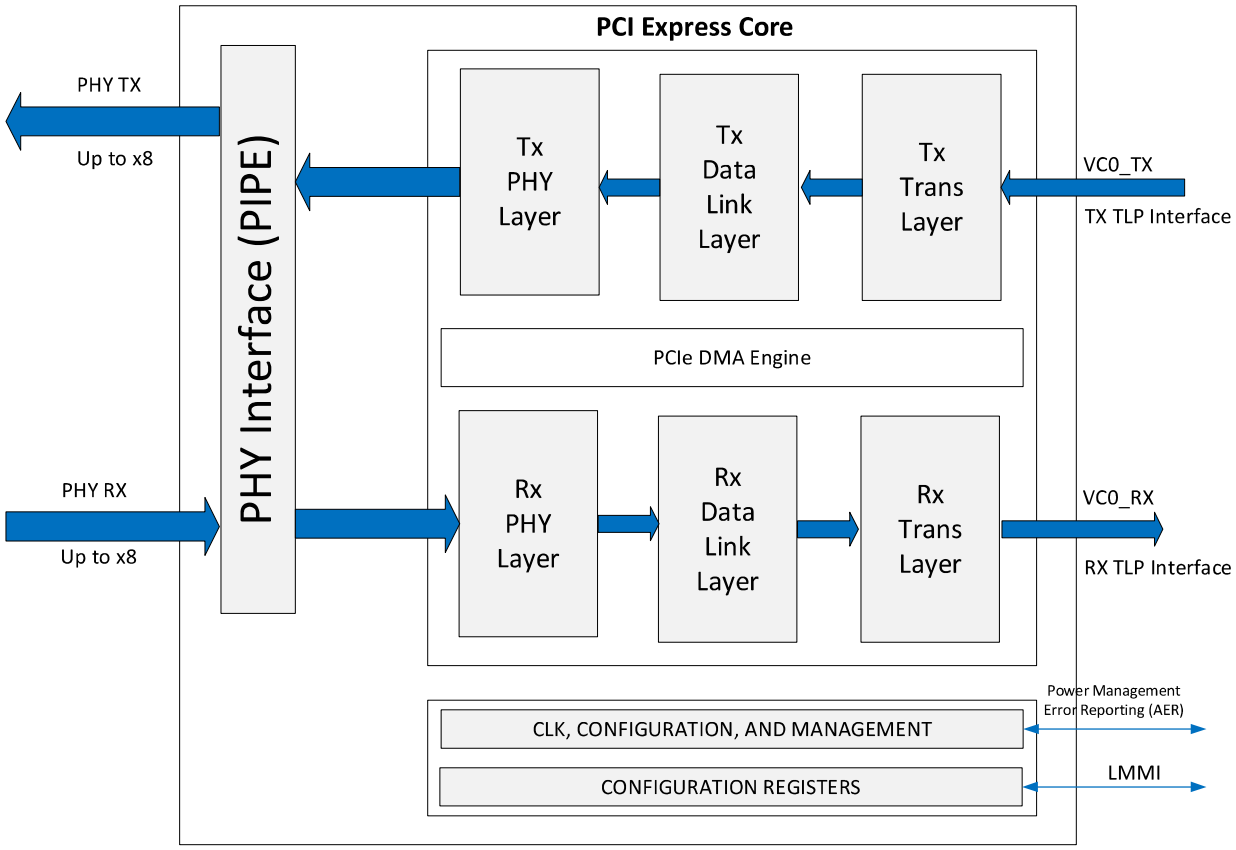


Figure 2.16. PCIe Core

The hardened PCIe block can be instantiated using the PCIe IP Core through the Radiant IP Catalog and IP Block Wizard. In Figure 2.17, the PCIe core is configured as an Endpoint using a soft IP wrapper that provides useful functions such as bridging support for bus interfaces and DMA applications. In addition to the standard Transaction Layer Packet (TLP) interface, the data interface can also be configured to be AXI4 as well. The PCIe hardened block also features a register interface for the Lattice Memory Mapped Interface (LMMI). The PCIe block has many registers which contain information about the current status of the PCIe block as well as the capability to dynamically switch PCIe settings. These registers can also be accessed through the Reveal Controller Tool.

For more information about the PCIe soft IP, refer to the PCIe Endpoint IP Core document.

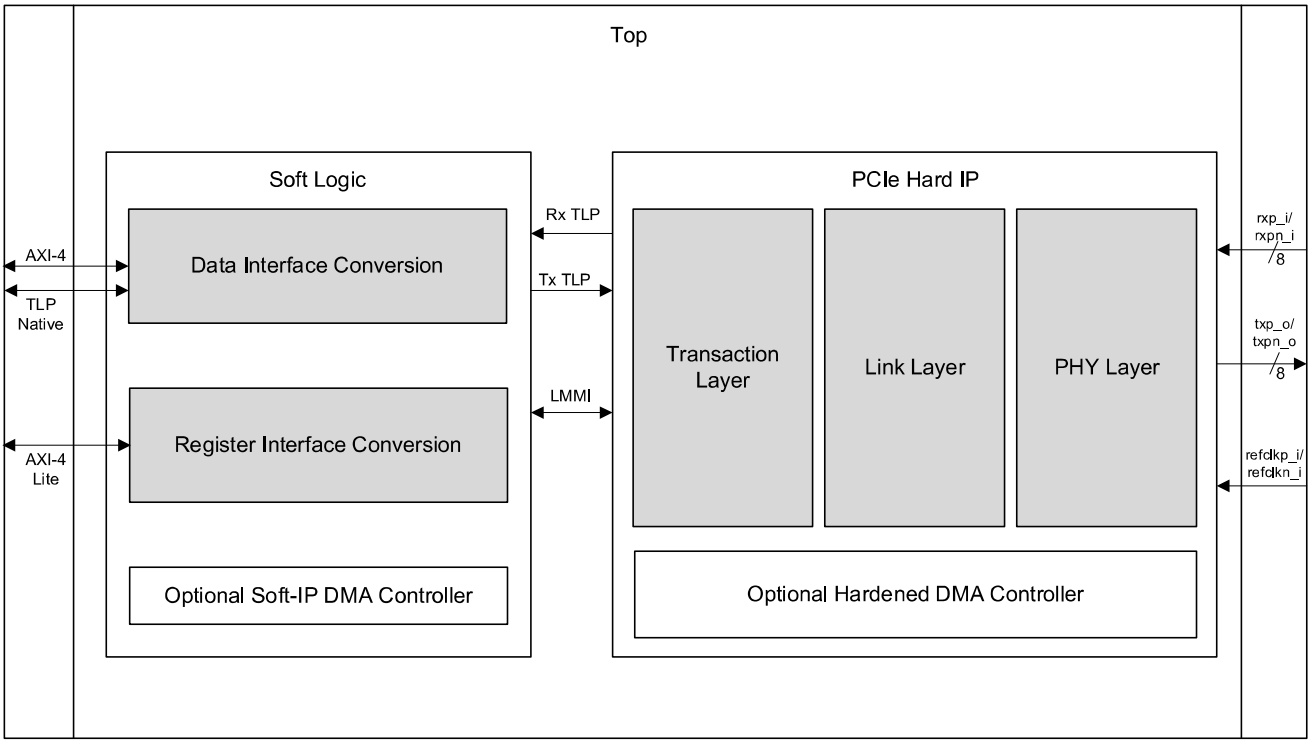


Figure 2.17. PCIe Soft IP Wrapper

2.13. Pin Migration

The Avant family is designed to ensure that different density devices in the same family and in the same package have the same pinout. Furthermore, the architecture ensures a high success rate when performing design migration from lower density devices to higher density devices. In many cases, it is also possible to shift a low utilization design targeted for a high-density device to a lower density device. However, the exact details of the final resource utilization impact the likelihood of success in each case. An example is that some user I/O may become No Connects in smaller devices in the same package. Refer to the Avant Pin Migration Tables and Lattice Radiant software for specific restrictions and limitations.

2.14. Security Engine

The Avant family of devices are equipped with several security features to protect and help customers secure their design. The high-level security features are:

- Bitstream Encryption
- Bitstream Authentication
- User accessible security APIs
- Physically Unclonable Function (PUF)
- Resistance to side channel analysis (SCA) and fault injection attack (FIA)
- Anti-tamper remedies, such as zeroing of storage (key storage, BBRAM, OTP) used for sensitive information storing such as keys.

These security features are a significant step up in capabilities and performance compared to existing products.

Avant security engine provides several cryptographic features that customers could utilize in their design. Some of the key cryptographic features include Advanced Encryption Standard (AES), Hashing Algorithms and true random number generator (TRNG). The Avant device also features bitstream encryption (using AES-256-GCM), used for protecting confidential FPGA bitstream data, and bitstream authentication (using ECDSA), which maintains bitstream integrity and protects the FPGA design bitstream from copying and tampering.

The security engine is responsible for the bitstream encryption as well as authentication of the Avant device. Once the bitstream is authenticated and the device is ready for user functions, the security engine is available for the user to implement various cryptographic functions in the FPGA design. The security engine utilizes a message-passing protocol through a hardware mailbox to provide an interface for calling security API. The security engine receives request messages, translates them into API calls in the Security CPU, and then sends a response message when the requested operation is complete.

The Avant platform supports the following encryption algorithms and security functions:

- True Random Number Generator (TRNG)
- AES, side channel attack resistant (256 bit keys, >3.2 Gbps throughput)
- AES, high-speed (256 bit keys, >10 Gbps throughput)
- Secure Hashing Algorithm (up to SHA3 in 512 bit mode)
- Side channel attack resistant Message Authentication Codes (up to HMAC-SHA2 in 512 bit mode)
- Side channel attack resistant RSA (up to 4k)

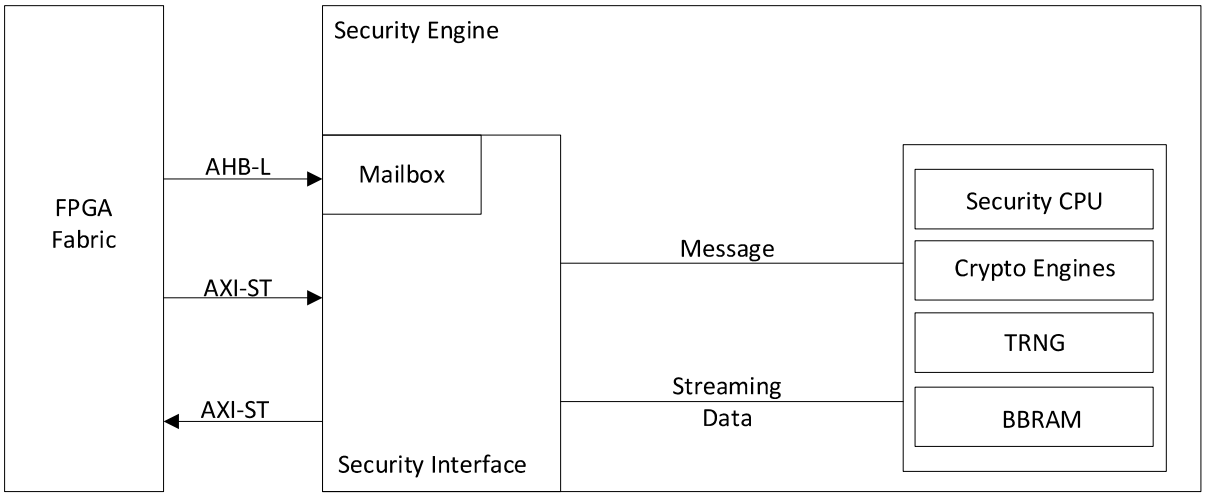


Figure 2.18. Cryptographic Engine Block Diagram

Avant includes a hardened PUF with 256 bits of entropy and a stable lifetime > 20 years. The PUF provides an unclonable device-unique value which is used to derive device-specific keys for various purpose. This can be used to provide an extra layer of security unique to each device. PUF is located inside the security engine and the data it generates are never exposed outside of security engine.

Avant security engine has direct access to Battery backed RAM (BBRAM), which can be used as nonvolatile storage for sensitive information. Unlike OTP, BBRAM can be programmed more than once and the content cannot be easily read through physical inspection. Usage of BBRAM is optional (enabled by a user writable OTP bit). By default, OTP is used for persistent storage of user-programmed secrets (such as customer public key hashes). If BBRAM is enabled, security engine shall use BBRAM instead for user-programmed secrets.

The Security Engine feature is not supported in the Avant-E family.

2.15. System Monitor/Anti-Tamper Monitor

The Anti-Tamper Monitor (ATM) measures on-die temperatures and voltages of critical power supplies using analog sensors with corresponding ADCs. Each ADC communicates with ATM using digital interface. The main usage of ATM in user application are:

- Provides continuous data samples of voltages and temperatures from multiple locations on the die so that user logic can monitor the status of the device.
- Provide interface to user logic to trigger remedy action

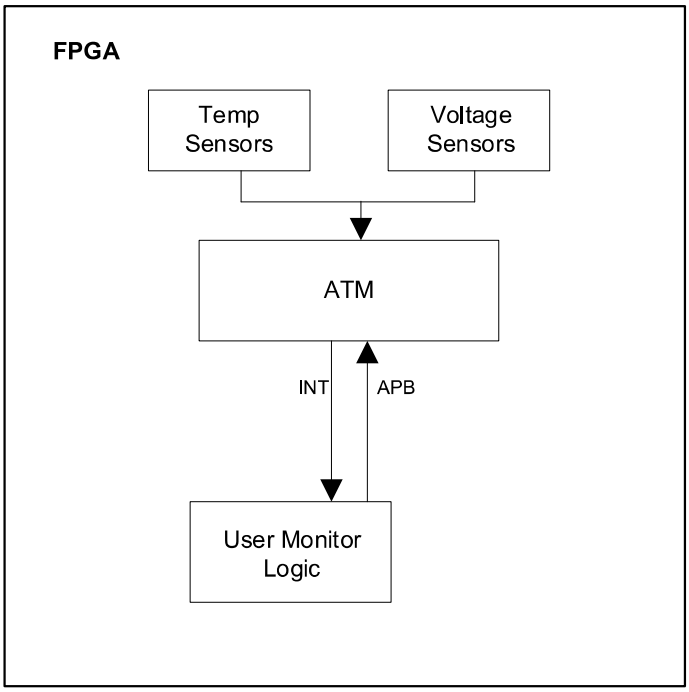


Figure 2.19. ATM Block Diagram

User logic can monitor certain power rail voltages and on die temperatures from sensors distributed across the die through ATM. User logic can read sample data through ATM interface and set upper/lower threshold values to trigger alarms through interrupt. User logic can trigger one of fixed set of remedy actions if required, such as zeroization of CRAMs and EBRs, zeroization of user secrets in temporary storage (SRAM) or persistent storage (OTP or BBRAM), even permanently disabling of the device through the fabric interface.

The System Monitor/Anti-Tamper Monitor feature is not supported in the Avant-E family.

3. Pinout Information

3.1. Signal Descriptions

Signal Name	Bank	Type	Description
Power and GND			
Vss	—	GND	Ground for internal FPGA logic and I/O
V_{CC}	—	Power	Power supply pins for core logic. V_{CC} is connected to 0.82 V (nom.) supply voltage. Power On Reset (POR) monitors this supply voltage.
V_{CCAUXA}	—	Power	Auxiliary power supply pin for internal analog circuitry. This supply is connected to 1.8 V (nom.) supply voltage. POR monitors this supply voltage.
V_{CCAUX}	—	Power	Auxiliary power supply. This supply is connected to 1.8 V (nom.) supply voltage, and is used for generating stable drive current for the I/O.
V_{CCHP}	—	Power	Used by high speed logic, mainly in the HPIO sectors. This supply is connected to 0.82 V (nom.) supply voltage.
V_{CCCLK}	—	Power	Used to supply the clock tree. This supply is connected to 0.82 V (nom.) supply voltage.
V_{CCA_PLLx}	—	Power	Used by the PLL blocks. This supply is connected to 0.82 V (nom.) supply voltage. X can be various PLL numberings.
V_{CC_BAT}	—	Power	This supply can be connected to 1.5 V (nom.) supply voltage. It allows a battery to be used to keep the volatile RAM configuration when the other DC supply source is absent.
V_{CCIOx}	0-14	Power	Power supply pins for I/O bank x. For x = 0, 1, 2, 12, 13, and 14, VCCIO can be connected to (nom.) 1.2 V, 1.8 V, 2.5 V, or 3.3 V. For x = 3, 4, 5, 6, 7, 8, 9, 10 and 11, VCCIO can be connected to (nom.) 0.9, 1.0 V, 1.1 V, 1.2 V, 1.35 V, 1.5 V, or 1.8 V. There are dedicated and shared configuration pins in banks 1 and 2. POR monitors these banks supply voltages.
V_{CCA_MPQx}	—	Power	Power supply for the SerDes blocks. X = 0, 1, 2, 3, 4, 5, 6
V_{CCH_MPQx}	—	Power	Power supply for the SerDes blocks. X = 0, 1, 2, 3, 4, 5, 6
Dedicated SerDes I/O Pins			
MPQx_RXyP/N	MPQ0:6	Input	SerDes Data Differential Input Pairs. X=0, 1, 2, 3, 4, 5, 6. Y=0, 1, 2, 3
MPQx_TXyDP/N	MPQ0:6	Output	SerDes Data Differential Output Pairs. X=0, 1, 2, 3, 4, 5, 6. Y=0, 1, 2, 3
MPQx_REFCLKP/N	MPQ0:6	Input	SerDes Reference Clock Differential Input Pairs. X=0, 1, 2, 3, 4, 5, 6
REXT_MPQx	MPQ0:6	Input	SerDes External Reference Resistor Input. This is used to adjust the on-chip differential termination impedance, based on the external resistance value. X=0, 1, 2, 3, 4, 5, 6
Misc Pins			
NC		—	No connect.

Signal Name	Bank	Type	Description
General Purpose I/O Pins			
WRIO[BankNumber]_[Number][A/B]	0, 1, 2, 12, 13, 14	Input, Output, Bi-Dir	Programmable Wide Range User I/O: [BankNumber] indicates the package pin/ball is in the bank specified. [Number] identifies the PIO [A/B] pair. [A/B] shows the package pin/ball is A or B signal in the pair. PIO A and PIO B are grouped as a pair. Each A/B pair in the top bank does not support true differential input or output buffer. It supports all single-ended inputs and outputs, and can be used for emulated differential output buffer. Some of these user-programmable I/O are used during configuration, depending on the configuration mode. The user needs to make appropriate connection on the board to isolate the two different functions before/after configuration. During configuration the user-programmable I/O are tri-stated with an internal weak pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tri-stated and default to have weak pull-down enabled after configuration.
HPIO[BankNumber]_[Number][A/B]	3, 4, 5, 6, 7, 8, 9, 10, 11	Input, Output, Bi-Dir	Programmable High Performance User I/O: [BankNumber] indicates the package pin/ball is in the bank specified. [Number] identifies the PIO [A/B] pair. [A/B] shows the package pin/ball is A or B signal in the pair. PIO A and PIO B are grouped as a pair. Each A/B pair in the bottom banks supports true differential input and output buffers. When configured as differential input, differential termination of 100 Ω can be selected. During configuration the user-programmable I/O are tri-stated with an internal weak pull-down resistor enabled. If any pin is not used (or not bonded to a package pin), it is tri-stated and default to have weak pull-down enabled after configuration.
Shared Configuration Pins **1. These pins can be used for configuration during configuration mode. When configuration is completed, these pins can be used as GPIO, or shared function in GPIO. When these pins are used in dual function, the user needs to isolate the signal paths for the dual functions on the board.** **2. The pins used are defined by the configuration modes detected. Slave SPI modes are detected during slave activation. Pins that are not used in the configuration mode selected are tri-stated during configuration, and can connect directly as GPIO in user's function.**			
WRIO2_yy/SDQ0:7	2	Input, Output, Bi-Dir	Configuration: Slave SPI Mode: Slave Parallel Data User Mode: WRIO2_yy: GPIO
WRIO2_yy/SSDO	2	Input, Output, Bi-Dir	Configuration: Slave SPI Mode: Slave Serial Output User Mode: WRIO2_yy: GPIO
WRIO2_yy/SCSN	2	Input, Output, Bi-Dir	Configuration: Slave SPI Mode: Slave Chip Select User Mode: WRIO2_yy: GPIO
WRIO2_yy/SCLK	2	Input, Output, Bi-Dir	Configuration: Slave SPI Mode: Slave Clock Input User Mode: WRIO2_yy: GPIO

Signal Name	Bank	Type	Description
WRIO2_yy/SDS	2	Input, Output, Bi-Dir	Configuration: Slave SPI Mode: Slave Data Strobe User Mode: WRIO2_yy: GPIO
WRIO1_yy /MCSN	1	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Master Chip Select User Mode: WRIO1_yy: GPIO
WRIO1_yy /MSDO	1	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Master Serial Data Out User Mode: WRIO1_yy: GPIO
WRIO1_yy /MDS	1	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Master Data Strobe User Mode: WRIO1_yy: GPIO
WRIO1_yy /MDQ0:7	1	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Master Parallel Data User Mode: WRIO1_yy: GPIO
WRIO1_yy /MCLK	1	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Master Clock Output User Mode: WRIO1_yy : GPIO
WRIO1_yy /MCLKN	1	Input, Output, Bi-Dir	Configuration: Master SPI Mode: Master Clock Output User Mode: WRIO1_yy : GPIO
Dedicated Pins **1. Dedicated pins are used for specific configuration functions**			
Dedicated Pins			
TDO	2	Output	Used as TDO signal for JTAG
TDI	2	Input	Used as TDI signal for JTAG
TMS	2	Input	Used as TMS signal for JTAG
TCK	2	Input	Used as TCK signal for JTAG
CFGMODE	2	Input	When low, enables JTAG and SSPI modes. When high, enables MSPI mode.
PROGRAMN	2	Input	Initiate configuration sequence when asserted LOW.
INITN	2	Input, Output, Bi-Dir	Open Drain I/O pin. This signal is driven to LOW when configuration sequence is started, to indicate the device is in initialization state. This signal is released after initialization is completed, and the configuration download can start. User can keep drive this signal LOW to delay configuration download to start.
DONE	2	Input, Output, Bi-Dir	Open Drain I/O pin. This signal is driven to LOW during configuration time. It is released to indicate the device has completed configuration. User can keep drive this signal LOW to delay the device to wake up from configuration.

Signal Name	Bank	Type	Description
ERASEKEY	1	Input	Trigger erase of BBRAM and OTP security keys.
Shared CLOCK Pins **1. Some PCLK pins can also be used as GPLL reference clock input pin. Refer to Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298).**			
WRIOx_zz/PCLK[R]T[0,1,2]_[0, 1]/yyyy	0, 1, 2, 12, 13, 14	Input, Output, Bi-Dir	User Mode: WRIOx_zz: GPIO PCLK: Primary Clock Refclk signal [0,1,2,12,13,14] = Bank [0,1] Up to 2 signals in the bank yyyy: Other possible selectable specific functional
WRIOx_zz/PLLT[FB][0,12]_IN/yyyy	0, 12	Input, Output, Bi-Dir	User Mode: HPIOx_zz: GPIO PLL: PLL signal [0,12] = Bank [FB] Used if input is for PLL feedback yyyy: Other possible selectable specific functional
HPIOx_zz/PCLK[R][T,C][3,4,5,6, 7,8,9,10,11]_[0,1,2,3]/yyyy	3, 4, 5, 6, 7, 8, 9, 10, 11	Input, Output, Bi-Dir	User Mode: HPIOx_zz: GPIO PCLK: Primary Clock Refclk signal [T,C] = True or Complement if using differential signaling [3,4,5,6,7,8,9,10,11] = Bank [0,1,2,3] Up to 4 signals in bank yyyy: Other possible selectable specific functional
HPIOx_zz/PLL[T,C][3,4,5,6,7,8, 9,10,11]_IN	3, 4, 5, 6, 7, 8, 9, 10, 11	Input, Output, Bi-Dir	User Mode: HPIOx_zz: GPIO PLL: PLL input signal [T,C] = True or Complement if using differential signaling [3,4,5,6,7,8,9,10,11] = Bank
Shared Reference Pins			
HPIOx_zz/VREF[3,4,5,6,7,8,9,1 0,11]	3, 4, 5, 6, 7, 8, 9, 10, 11	Input, Output, Bi-Dir	User Mode: HPIOx_zz: GPIO VREF: External voltage reference [3,4,5,6,7,8,9,10,11] = Bank
HPIOx_zz/EXT_RES[3,4,5,6,7,8, 9,10,11]	3, 4, 5, 6, 7, 8, 9, 10, 11	Input, Output, Bi-Dir	User Mode: HPIOx_zz: GPIO EXT_RES: External reference resistor [3,4,5,6,7,8,9,10,11] = Bank

Note:

1. Not all signals are available as external pins in all packages. Refer to the Pinout List file for various package details.

3.2. Pin Information Summary

3.2.1. Avant-E Family

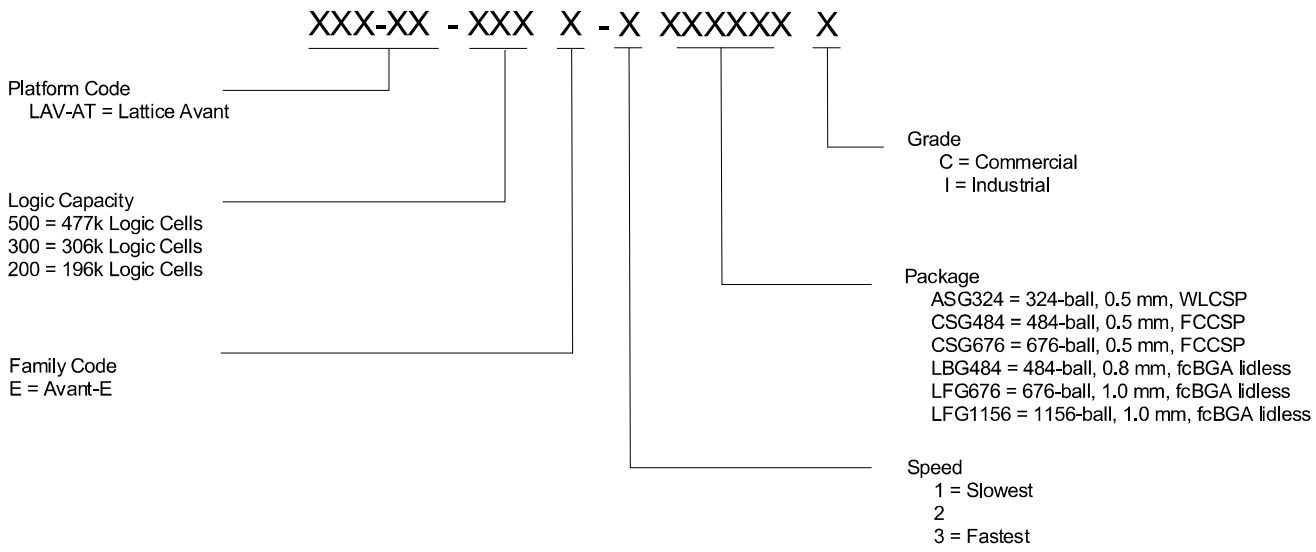
Pin Information Summary		LAV-AT-200E			LAV-AT-300E				LAV-AT-500E		
		ASG324	LBG484	LFG676	CSG484	LBG484	LFG676	LFG1156	CSG676	LFG676	LFG1156
User I/O Pins											
Wide Range Inputs/Outputs per Bank	Bank 0	—	—	—	—	—	—	—	—	16	16
	Bank 1	—	—	—	—	—	—	—	—	15	15
	Bank 2	—	—	—	—	—	—	—	—	12	12
	Bank 12	—	—	—	—	—	—	—	—	16	16
	Bank 13	—	—	—	—	—	—	—	—	16	16
	Bank 14	—	—	—	—	—	—	—	—	20	20
Total Wide Range User I/O		—	—	—	—	—	—	—	—	95	95
High Performance Input / Output Pairs	Bank 3	—	—	—	—	—	—	—	—	52	52
	Bank 4	—	—	—	—	—	—	—	—	0	52
	Bank 5	—	—	—	—	—	—	—	—	0	52
	Bank 6	—	—	—	—	—	—	—	—	0	52
	Bank 7	—	—	—	—	—	—	—	—	0	52
	Bank 8	—	—	—	—	—	—	—	—	52	52
	Bank 9	—	—	—	—	—	—	—	—	52	52
	Bank 10	—	—	—	—	—	—	—	—	52	52
	Bank 11	—	—	—	—	—	—	—	—	52	52
Total High Performance I/O		—	—	—	—	—	—	—	—	260	468
Power Pins											
V_{CC}		—	—	—	—	—	—	—	—	11	11
V_{CCCLK}		—	—	—	—	—	—	—	—	8	8
V_{CCHP}		—	—	—	—	—	—	—	—	3	5
V_{CC_PLL}		—	—	—	—	—	—	—	—	3	3
V_{CC_BAT}		—	—	—	—	—	—	—	—	1	1
V_{CCAUXA}		—	—	—	—	—	—	—	—	1	1
V_{CCAUX}		—	—	—	—	—	—	—	—	3	3
V_{CCIO}	Bank 0	—	—	—	—	—	—	—	—	3	3
	Bank 1	—	—	—	—	—	—	—	—	3	3
	Bank 2	—	—	—	—	—	—	—	—	3	3
	Bank 3	—	—	—	—	—	—	—	—	4	4
	Bank 4	—	—	—	—	—	—	—	—	0	4
	Bank 5	—	—	—	—	—	—	—	—	0	4
	Bank 6	—	—	—	—	—	—	—	—	0	4
	Bank 7	—	—	—	—	—	—	—	—	0	4
	Bank 8	—	—	—	—	—	—	—	—	4	4
	Bank 9	—	—	—	—	—	—	—	—	4	4
	Bank 10	—	—	—	—	—	—	—	—	4	4
	Bank 11	—	—	—	—	—	—	—	—	4	4
	Bank 12	—	—	—	—	—	—	—	—	0	3
	Bank 13	—	—	—	—	—	—	—	—	0	3
	Bank 14	—	—	—	—	—	—	—	—	0	3
Total Power Pins		—	—	—	—	—	—	—	—	59	86

Pin Information Summary		LAV-AT-200E			LAV-AT-300E				LAV-AT-500E		
		ASG324	LBG484	LFG676	CSG484	LBG484	LFG676	LFG1156	CSG676	LFG676	LFG1156
GND and NC Pins											
Vss		—	—	—	—	—	—	—	—	229	379
NC		—	—	—	—	—	—	—	—	69	119
Dedicated Misc Pins											
JTAG (TDI, TDO, TCK, TMS)		—	—	—	—	—	—	—	—	4	4
PROGRAMN		—	—	—	—	—	—	—	—	1	1
CFGMODE		—	—	—	—	—	—	—	—	1	1
DONE		—	—	—	—	—	—	—	—	1	1
INITN		—	—	—	—	—	—	—	—	1	1
Total Dedicated Pins		—	—	—	—	—	—	—	—	8	8
Shared Pins											
Shared Configuration Pins	Bank 1	—	—	—	—	—	—	—	—	13	13
	Bank 2	—	—	—	—	—	—	—	—	12	12
Shared PCLK Pins	Bank 0	—	—	—	—	—	—	—	—	4	4
	Bank 1	—	—	—	—	—	—	—	—	1	1
	Bank 2	—	—	—	—	—	—	—	—	1	1
	Bank 3	—	—	—	—	—	—	—	—	10	10
	Bank 4	—	—	—	—	—	—	—	—	0	10
	Bank 5	—	—	—	—	—	—	—	—	0	10
	Bank 6	—	—	—	—	—	—	—	—	0	10
	Bank 7	—	—	—	—	—	—	—	—	0	10
	Bank 8	—	—	—	—	—	—	—	—	10	10
	Bank 9	—	—	—	—	—	—	—	—	10	10
	Bank 10	—	—	—	—	—	—	—	—	10	10
	Bank 11	—	—	—	—	—	—	—	—	10	10
	Bank 12	—	—	—	—	—	—	—	—	0	4
	Bank 13	—	—	—	—	—	—	—	—	0	1
	Bank 14	—	—	—	—	—	—	—	—	0	1
Shared Reference Pins	Bank 0	—	—	—	—	—	—	—	—	0	0
	Bank 1	—	—	—	—	—	—	—	—	0	0
	Bank 2	—	—	—	—	—	—	—	—	0	0
	Bank 3	—	—	—	—	—	—	—	—	2	2
	Bank 4	—	—	—	—	—	—	—	—	0	2
	Bank 5	—	—	—	—	—	—	—	—	0	2
	Bank 6	—	—	—	—	—	—	—	—	0	2
	Bank 7	—	—	—	—	—	—	—	—	0	2
	Bank 8	—	—	—	—	—	—	—	—	2	2
	Bank 9	—	—	—	—	—	—	—	—	2	2
	Bank 10	—	—	—	—	—	—	—	—	2	2
	Bank 11	—	—	—	—	—	—	—	—	2	2
	Bank 12	—	—	—	—	—	—	—	—	0	0
	Bank 13	—	—	—	—	—	—	—	—	0	0
	Bank 14	—	—	—	—	—	—	—	—	0	0

4. Ordering Information

Lattice provides a wide variety of services for its products including custom marking, factory programming, known good die, and application specific testing. Contact the local sales representatives for more details.

4.1. Avant Part Number Description



4.2. Ordering Part Numbers

4.2.1. Commercial

Part Number	Speed	Package	Pins	Temp.	Logic Cells (k)
LAV-AT-500E-1LFG676C	1	LFG676	676	Commercial	477
LAV-AT-500E-2LFG676C	2	LFG676	676	Commercial	477
LAV-AT-500E-3LFG676C	3	LFG676	676	Commercial	477
LAV-AT-500E-1CSG676C	1	CSG676	676	Commercial	477
LAV-AT-500E-2CSG676C	2	CSG676	676	Commercial	477
LAV-AT-500E-3CSG676C	3	CSG676	676	Commercial	477
LAV-AT-500E-1LFG1156C	1	LFG1156	1156	Commercial	477
LAV-AT-500E-2LFG1156C	2	LFG1156	1156	Commercial	477
LAV-AT-500E-3LFG1156C	3	LFG1156	1156	Commercial	477
LAV-AT-300E-1LBG484C	1	LBG484	484	Commercial	306
LAV-AT-300E-2LBG484C	2	LBG484	484	Commercial	306
LAV-AT-300E-3LBG484C	3	LBG484	484	Commercial	306
LAV-AT-300E-1CSG484C	1	CSG484	484	Commercial	306
LAV-AT-300E-2CSG484C	2	CSG484	484	Commercial	306
LAV-AT-300E-3CSG484C	3	CSG484	484	Commercial	306
LAV-AT-300E-1LFG676C	1	LFG676	676	Commercial	306
LAV-AT-300E-2LFG676C	2	LFG676	676	Commercial	306
LAV-AT-300E-3LFG676C	3	LFG676	676	Commercial	306
LAV-AT-300E-1LFG1156C	1	LFG1156	1156	Commercial	306
LAV-AT-300E-2LFG1156C	2	LFG1156	1156	Commercial	306
LAV-AT-300E-3LFG1156C	3	LFG1156	1156	Commercial	306
LAV-AT-200E-1ASG324C	1	ASG324	324	Commercial	196
LAV-AT-200E-2ASG324C	2	ASG324	324	Commercial	196
LAV-AT-200E-3ASG324C	3	ASG324	324	Commercial	196
LAV-AT-200E-1LBG484C	1	LBG484	484	Commercial	196
LAV-AT-200E-2LBG484C	2	LBG484	484	Commercial	196
LAV-AT-200E-3LBG484C	3	LBG484	484	Commercial	196
LAV-AT-200E-1LFG676C	1	LFG676	676	Commercial	196
LAV-AT-200E-2LFG676C	2	LFG676	676	Commercial	196
LAV-AT-200E-3LFG676C	3	LFG676	676	Commercial	196

4.2.2. Industrial

Part Number	Speed	Package	Pins	Temp.	Logic Cells (k)
LAV-AT-500E-1LFG676I	1	LFG676	676	Industrial	477
LAV-AT-500E-2LFG676I	2	LFG676	676	Industrial	477
LAV-AT-500E-3LFG676I	3	LFG676	676	Industrial	477
LAV-AT-500E-1CSG676I	1	CSG676	676	Industrial	477
LAV-AT-500E-2CSG676I	2	CSG676	676	Industrial	477
LAV-AT-500E-3CSG676I	3	CSG676	676	Industrial	477
LAV-AT-500E-1LFG1156I	1	LFG1156	1156	Industrial	477
LAV-AT-500E-2LFG1156I	2	LFG1156	1156	Industrial	477
LAV-AT-500E-3LFG1156I	3	LFG1156	1156	Industrial	477
LAV-AT-300E-1LBG484I	1	LBG484	484	Industrial	306
LAV-AT-300E-2LBG484I	2	LBG484	484	Industrial	306
LAV-AT-300E-3LBG484I	3	LBG484	484	Industrial	306
LAV-AT-300E-1CSG484I	1	CSG484	484	Industrial	306
LAV-AT-300E-2CSG484I	2	CSG484	484	Industrial	306
LAV-AT-300E-3CSG484I	3	CSG484	484	Industrial	306
LAV-AT-300E-1LFG676I	1	LFG676	676	Industrial	306
LAV-AT-300E-2LFG676I	2	LFG676	676	Industrial	306
LAV-AT-300E-3LFG676I	3	LFG676	676	Industrial	306
LAV-AT-300E-1LFG1156I	1	LFG1156	1156	Industrial	306
LAV-AT-300E-2LFG1156I	2	LFG1156	1156	Industrial	306
LAV-AT-300E-3LFG1156I	3	LFG1156	1156	Industrial	306
LAV-AT-200E-1ASG324I	1	ASG324	324	Industrial	306
LAV-AT-200E-2ASG324I	2	ASG324	324	Industrial	306
LAV-AT-200E-3ASG324I	3	ASG324	324	Industrial	306
LAV-AT-200E-1LBG484I	1	LBG484	484	Industrial	306
LAV-AT-200E-2LBG484I	2	LBG484	484	Industrial	306
LAV-AT-200E-3LBG484I	3	LBG484	484	Industrial	306
LAV-AT-200E-1LFG676I	1	LFG676	676	Industrial	306
LAV-AT-200E-2LFG676I	2	LFG676	676	Industrial	306
LAV-AT-200E-3LFG676I	3	LFG676	676	Industrial	306

Supplemental Information

For Further Information

A variety of technical notes for the Avant family are available.

- sub-LVDS Signaling Using Lattice Devices (FPGA-TN-02028)
- Thermal Management (FPGA-TN-02044)
- Lattice Avant sysI/O User Guide (FPGA-TN-02297)
- Lattice Avant Power User Guide (FPGA-TN-02291)
- Using TraceID (FPGA-TN-02084)
- Lattice Avant Embedded Memory User Guide (FPGA-TN-02289)
- Lattice Avant sysCLOCK PLL Design and User Guide (FPGA-TN-02298)
- Lattice Avant sysDSP User Guide (FPGA-TN-02293)
- Lattice Avant High-Speed I/O and External Memory Interface (FPGA-TN-02300)
- Lattice Avant sysCONFIG User Guide (FPGA-TN-02299)
- High-Speed PCB Design Considerations (FPGA-TN-02178)
- Lattice Avant Hardware Checklist (FPGA-TN-02317)
- Lattice Memory Mapped Interface and Lattice Interrupt Interface User Guide (FPGA-UG-02039)

For more information on Avant-related IP, reference designs, and board documents, refer to the following pages:

- IP and Reference Designs for Avant at www.latticesemi.com
- Development Kits and Boards for Avant at www.latticesemi.com

For further information on interface standards refer to the following websites:

- JEDEC Standards (LVTTL, LVCMOS, SSTL) – www.jedec.org
- PCI – www.pcisig.com

Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at www.latticesemi.com/Support/AnswerDatabase.

Revision History

Revision 0.73, March 2023

Section	Change Summary
All	Minor adjustments in formatting across the document.
Architecture	Updated Table 2.4. Single-Ended I/O Standards Supported on Various Sides to change Output and Bi-directional values for LVCMOS10 and LVCMOS09 to Yes.
Supplemental Information	Added reference links for the IP, Reference Design, and Boards web page.

Revision 0.72, February 2023

Section	Change Summary
Acronyms in This Table	Updated DDRPHY definition and added LPDDR definition.

General Description	• Updated DDRS and LPDDR4 to DDR5, DDR4/LPDDR4, and DDR3L in the General Description section.
	• Updated the following in Table 1.1. Avant Platform Key Features:
	  • Changed DDR5 value to 2133 Mbps; added footnote and reference to footnote 1.
	  • Changed DDR4 and LPDDR4 value to 2400 Mbps; added footnote and reference to footnote 2.
	  • Added DDR3L value.
	• Updated Table 1.2. Avant Families to rearrange LPDDR4/DDR4 to DDR4/LPDDR4.

Architecture	• Changed DDR3L/4/5, LPDDR2/3/4 to DDR5, DDR4/LPDDR4, and DDR3L in Overview section.
	• Changed the following in Programmable I/O (PIO) section:
	  • Reorder top bullet items to DDR5, DDR4/LPDDR4, and DDR3L.
	  • Changed DDR5 value to 2133 Mbps, added footnote reference 1, and updated footnote 1.
	  • Added footnote 2 and footnote reference to DDR4/LPDDR4.
	  • Removed LPDDR2 and LPDDR3.
	• Changed DDR5, LPDDR4, DDR4 to DDR5 and DDR4/LPDDR4 in sysI/O Banking Scheme section.
	• Changed the following in DDR Memory Support:
	  • Changed DDR3L/DDR4/DDR5 and LPDDR2/LPDDR3/LPDDR4 to DDR5, DDR4/LPDDR4, and DDR3L.
	  • Updated Table 2.6. Summary of DDR Standards and Max Rates to reorder standards and remove LPDDR2 and LPDDR3.

Revision 0.71, December 2022

Section	Change Summary
All	• Updated document to include Avant-E information only. • Adjustments in formatting across the document.
Acronyms in This Document	Added description for DDLDEL, DDRPHY, GCLK, PIO, MPPCS, MPPHY, and RCLK.

Introduction	• Updated section content including the following:
	  • Changed smallest package size to 11 x 9 mm in Table 1.1. Avant Platform Key Features.
	  • Updated Table 1.2. Avant Families to include only Avant-E and Future Avant Families information, and updated Security row to Security/Hardened Crypto.
	  • Updated the following in Table 1.3. Avant-E Family Selection Guide:
	  • Added CSG484 and CSG676 packages.
	  • Changed package LFG672 to LFG676.
	  • Added type in the packages.
	  • Updated Total I/O values in the table.
	  • Added table note 2 to include reference to the Ordering Information section.
	  • Removed LFG900 package.
	  • Removed WRPLL and HPPLL references.

Section	Change Summary

Architecture	• Changed WRPLL and HPPLL references to PLL (WRIO) and PLL (HPIO), and CIBCLK to Fabric_CLK across this section.
	• Updated section names of DLL Delay (DLLDEL), Multi-Protocol PCS (MPPCS), and Multi-Protocol PHY (MPPHY) Integration.
	• Updated sysI/O buffer information in the Overview section.
	• Updated Figure 2.1. High-level Device Floorplan (LAV-AT-200E Device), Figure 2.2. High-level Device Floorplan (LAV-AT-300E Device), Figure 2.3. High-level Device Floorplan (LAV-AT-500E Device), Figure 2.4. High-Level View of Clock Networks and Elements (LAV-AT-500E Device), Figure 2.6. Multi-Region Clock Formation, and Figure 2.11. sysI/O Banking to include Avant-E information only.
	• Updated slice input to 16 in Slices section.
	• Updated user clock frequency to 400 or 320 MHz in On-Chip Oscillator section.
	• Updated Integer Feedback divider values, Spreading depth, and Glitchless Dynamic output bullet points and Figure 2.5. Avant PLL Block Diagram in PLL section.
	• Updated Figure 2.8. High-Level Implementation of DLLDEL and Code Control to change HPPLL_PHYCLK to PLL(HPIO)_PHYCLK.
	• Updated Table 2.2 sysMEM Block Configurations to remove 512 x 72.
	• Updated Figure 2.9. Memory Core Reset to update Port A and B to [35:0].
	• Updated Figure 2.10. DSP Functional Block.
	• Changed programmable drive strength to 4 to 12 mA in Programmable I/O (PIO) section.
	• Updated Figure 2.12. Group of Two High Performance Programmable I/O Cells and Figure 2.13. Wide Range Programmable I/O Cells to add bounding box.
	• Updated Table 2.6. Summary of DDR Standards and Max Rates to change DDR5 max speed to 2133 Mbps, including the table note.
	• Updated Device Configuration section content to reword INIT/DONE information and added note for Octal SPI.
	• Updated the following in SerDes and PCS:
	  • Added note that the SerDes feature is note supported in Avant-E.
	  • Updated Figure 2.14. SerDes Overview Diagram to make the lines more visible and updated Quad color to blue and Multi-Channel to orange.
	  • Updated Table 2.7. SerDes/PCS Supported Protocols to correct 10G Ethernet, 25G Ethernet, CPRI, eCPRI, ROE, and SyncE protocols, update table note reference, and change information in the table note to Avant platform.
	  • Updated Table 2.8. Avant SerDes Protocol Width Support to change Rate (Gbps) x Width Example values for Ethernet, CPRI, eCPRI, ROE, and SyncE.
	  • Updated Figure 2.17. PCIe Soft IP Wrapper to add TLP native and AXI-4 Lite.
	• Added note in Security Engine section that this feature is note supported in Avant-E.
	• Added note in System Monitor/Anti-Tamper Monitor section that this feature is note supported in Avant-E.

Pinout Information	• Removed nominal value for V_{CCA_MPQx} and V_{CCH_MPQx} in Signal Descriptions. • Updated Pin Information Summary section to include Avant-E information only, added packages for CSG484 and CSG676, change LFG672 to LFG676, and removed 900 package.
Ordering Information	Updated Ordering Information to include only Avant-E information, change LFG672 to LFG676, Family Code to Platform Code, and Variant Code to Family Code, and add CSG484 and CSG676 packages.

Revision 0.70, May 2022

Section	Change Summary
All	Advance release.

www.latticesemi.com