# Low $V_{IN}$, 10A Step-Down µModule Regulator

## FEATURES

- **10A DC Output Current**
- **Input Voltage Range: 2.375V to 5.5V**
- **Output Voltage Range: 0.6V to 5V**
- **No Heat Sink or Current Derating Up to 85°C Ambient Temperature**
- **±1.5% Maximum Total DC Output Error**
- **Multiphase Operation with Current Sharing**
- **Remote Sense Amplifier**
- Built-In Temperature Monitor
- Selectable Pulse-Skipping Mode/Burst Mode® Operation for High Efficiency at Light Load
- Soft-Start/Voltage Tracking
- Protection: Output Overvoltage and Overcurrent Foldback
- See LTM4649 for Up to 16$V_{IN}$ Operation
- 9mm × 15mm × 4.92mm BGA Package

## APPLICATIONS

- Telecom, Networking and Industrial Equipment
- Point of Load Regulation

## DESCRIPTION

The LTM®4648 is a 10A low $V_{IN}$ step-down DC/DC µModule® (micromodule) regulator. Included in the package are the switching controller, power FETs, inductor and all support components. Operating over an input voltage range of 2.375V to 5.5V, the LTM4648 supports an output voltage range of 0.6V to 5V, set by a single external resistor. This high efficiency design delivers up to 10A continuous current. Only bulk input and output capacitors are needed.

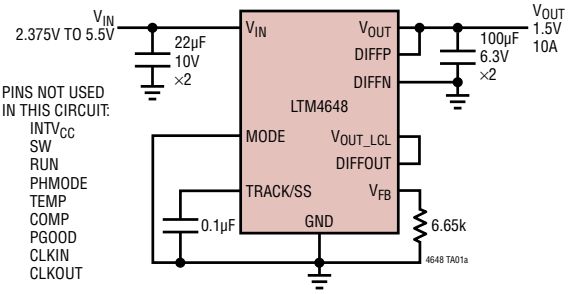
High switching frequency and a current mode architecture enable a very fast transient response to line and load changes without sacrificing stability. The device supports frequency synchronization, programmable multiphase operation and output voltage tracking for supply rail sequencing.

Fault protection features include overvoltage protection, overcurrent protection and thermal shutdown. The LTM4648 is offered in a small 9mm × 15mm × 4.92mm BGA package available with SnPb or RoHS compliant terminal finish. For up to 16$V_{IN}$ operation, see the LTM4649.

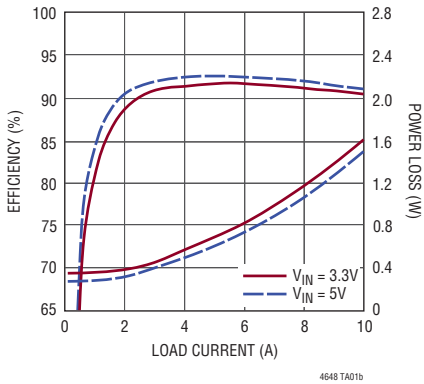


## TYPICAL APPLICATION

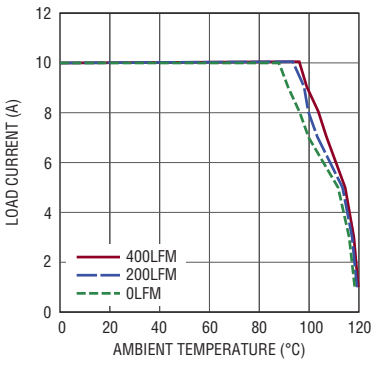
**2.375V to 5.5V Input, 1.5V Output DC/DC µModule Regulator**




**Efficiency and Power Loss at 5V and 3.3V Input**




**Current Derating, 5V to 1.5$V_{OUT}$ with No Heat Sink**

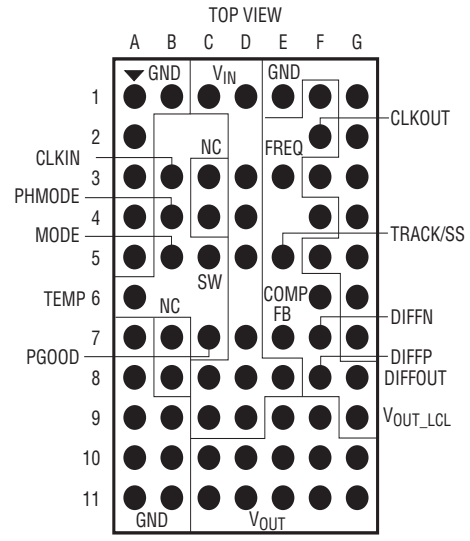


## ABSOLUTE MAXIMUM RATINGS

**(Note 1)**

$V_{IN}$ ..... –0.3V to 6V
$V_{OUT}$, $INTV_{CC}$, PGOOD, RUN (Note 5) ..... –0.3V to 6V
MODE, CLKIN, TRACK/SS, DIFFP, DIFFN,
DIFFOUT, PHASMD ..... –0.3V to $INTV_{CC}$
$V_{FB}$ ..... –0.3V to 2.7V
COMP (Note 6) ..... –0.3V to 2.7V
$INTV_{CC}$ Peak Output Current (Note 6) ..... 100mA
Internal Operating Temperature Range
(Note 2) ..... –55°C to 125°C
Storage Temperature Range ..... –55°C to 125°C
Peak Solder Reflow Body Temperature ..... 245°C

## PIN CONFIGURATION




BGA PACKAGE
68-LEAD (9mm × 15mm × 4.92mm)
$T_{JMAX}$ = 125°C, $\theta_{JA}$ = 14°C/W, $\theta_{JCbottom}$ = 5°C/W, $\theta_{JCtop}$ = 20°C/W
WEIGHT = 1.0g

## ORDER INFORMATION

| PART NUMBER | PAD OR BALL FINISH | PART MARKING* | | PACKAGE TYPE | MSL RATING | TEMPERATURE RANGE (SEE NOTE 2) |
|---|---|---|---|---|---|---|
| | | DEVICE | FINISH CODE | | | |
| LTM4648EY#PBF | SAC305 (RoHS) | LTM4648Y | e1 | BGA | 3 | –40°C to 125°C |
| LTM4648IY#PBF | | LTM4648Y | | | | |
| LTM4648IY | SnPb (63/37) | LTM4648Y | e0 | | | |

- Device temperature grade is indicated by a label on the shipping container.
- Pad or ball finish code is per IPC/JEDEC J-STD-609.
- BGA Package and Tray Drawings
- This product is not recommended for second side reflow. This product is moisture sensitive. For more information, go to Recommended BGA PCB Assembly and Manufacturing Procedures.

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at $T_A$ = 25°C (Note 2). $V_{IN}$ = 5V per typical application.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| $V_{IN}$ | Input DC Voltage | | ● | 2.375 | | 5.5 | V |
| $V_{OUT(RANGE)}$ | Output Voltage Range | | ● | 0.6 | | 5 | V |
| $V_{OUT(DC)}$ | Output Voltage, Total Variation with Line and Load | $C_{IN}$ = 10µF × 1,$C_{OUT}$ = 100µF Ceramic, 100µF POSCAP, $R_{FB}$ = 6.65k, MODE = GND, $V_{IN}$ = 2.375V to 5.5V, $I_{OUT}$ = 0A to 10A | ● | 1.477 | 1.50 | 1.523 | V |
| **Input Specifications** | | | | | | | |
| $V_{RUN}$ | RUN Pin On Threshold | $V_{RUN}$ Rising | | 1.1 | 1.25 | 1.4 | V |
| $V_{RUN(HYS)}$ | RUN Pin On Hysteresis | | | | 150 | | mV |
| $I_{Q(VIN)}$ | Input Supply Bias Current | $V_{IN}$ = 5V, $V_{OUT}$ = 1.5V, Burst Mode Operation<br>$V_{IN}$ = 5V, $V_{OUT}$ = 1.5V, Pulse-Skipping Mode<br>$V_{IN}$ = 5V, $V_{OUT}$ = 1.5V, Switching Continuous<br>Shutdown, RUN = 0, $V_{IN}$ = 5V | | | 5.5<br>25<br>100<br>2.5 | | mA<br>mA<br>mA<br>mA |
| $I_{S(VIN)}$ | Input Supply Current | $V_{IN}$ = 5.5V, $V_{OUT}$ = 1.5V, $I_{OUT}$ = 10A | | | 3.3 | | A |
| **Output Specifications** | | | | | | | |
| $I_{OUT(DC)}$ | Output Continuous Current Range | $V_{IN}$ = 5V, $V_{OUT}$ = 1.5V (Note 4) | | 0 | | 10 | A |
| $\frac{\Delta V_{OUT(LINE)}}{V_{OUT}}$ | Line Regulation Accuracy | $V_{OUT}$ = 1.5V, $V_{IN}$ from 2.375V to 5.5V $I_{OUT}$ = 0A | ● | | 0.010 | 0.04 | %/V |
| $\frac{\Delta V_{OUT(LOAD)}}{V_{OUT}}$ | Load Regulation Accuracy | $V_{OUT}$ = 1.5V, $I_{OUT}$ = 0A to 10A, $V_{IN}$ = 5V (Note 4) | ● | | 0.15 | 0.5 | % |
| $V_{OUT(AC)}$ | Output Ripple Voltage | $I_{OUT}$ = 0A, $C_{OUT}$ = 100µF Ceramic, 100µF POSCAP, $V_{IN}$ = 5V, $V_{OUT}$ = 1.5V | | | 15 | | mV |
| $\Delta V_{OUT(START)}$ | Turn-On Overshoot | $C_{OUT}$ = 100µF Ceramic, 100µF POSCAP, $V_{OUT}$ = 1.5V, $I_{OUT}$ = 0A, $V_{IN}$ = 5V | | | 20 | | mV |
| $t_{START}$ | Turn-On Time | $C_{OUT}$ = 100µF Ceramic, 100µF POSCAP, No Load, TRACK/SS = 0.01µF, $V_{IN}$ = 5V | | | 5 | | ms |
| $\Delta V_{OUTLS}$ | Peak Deviation for Dynamic Load | Load: 0% to 50% to 0% of Full Load, $C_{OUT}$ = 100µF Ceramic, 100µF POSCAP, $V_{IN}$ = 5V, $V_{OUT}$ = 1.5V | | | 60 | | mV |
| $t_{SETTLE}$ | Settling Time for Dynamic Load Step | Load: 0% to 50% to 0% of Full Load, $C_{OUT}$ = 100µF Ceramic, 100µF POSCAP, $V_{IN}$ = 5V, $V_{OUT}$=1.5V | | | 20 | | µs |
| $I_{OUTPK}$ | Output Current Limit | $V_{IN}$ = 5V, $V_{OUT}$ = 1.5V (Note 4) | | 11 | | | A |
| **Control Specifications** | | | | | | | |
| $V_{FB}$ | Voltage at $V_{FB}$ Pin | $I_{OUT}$ = 0A, $V_{OUT}$ = 1.5V | ● | 0.593 | 0.60 | 0.607 | V |
| $I_{FB}$ | Current at $V_{FB}$ Pin | | | | –12 | –25 | nA |
| $V_{OVL}$ | Feedback Overvoltage Lockout | | ● | 0.64 | 0.66 | 0.68 | V |
| $I_{TRACK/SS}$ | Track Pin Soft-Start Pull-Up Current | TRACK/SS = 0V | | 1.0 | 1.2 | 1.4 | µA |
| $t_{ON(MIN)}$ | Minimum On-Time | (Note 3) | | | 90 | | ns |
| $R_{FBHI}$ | Resistor Between $V_{OUT\_LCL}$ and $V_{FB}$ Pins | | | 9.90 | 10 | 10.10 | kΩ |
| DIFFP, DIFFN CM RANGE | Common Mode Input Range | $V_{IN}$ = 5V, Run > 1.4V | | 0 | | 3.6 | V |
| $V_{DIFFOUT(MAX)}$ | Maximum DIFFOUT Voltage | $I_{DIFFOUT}$ = 300µA | | $INTV_{CC}$ – 1.4 | | | V |
| $V_{OS}$ | Input Offset Voltage | $V_{OSNS}$+ = $V_{DIFFOUT}$ = 1.5V, $I_{DIFFOUT}$ = 100µA | | | | 4 | mV |
| $A_V$ | Differential Gain | | | | 1 | | V/V |
| SR | Slew Rate | | | | 2 | | V/µs |

## ELECTRICAL CHARACTERISTICS

**The ● denotes the specifications which apply over the full internal operating temperature range, otherwise specifications are at $T_A$ = 25°C (Note 2). $V_{IN}$ = 5V per typical application.**

| SYMBOL | PARAMETER | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| GBP | Gain Bandwidth Product | | | | 3 | | MHz |
| CMRR | Common Mode Rejection | (Note 6) | | | 60 | | dB |
| $I_{DIFFOUT}$ | DIFFOUT Current | Sourcing | | 2 | | | mA |
| $R_{IN}$ | Input Resistance | $V_{OSNS}$+ to GND | | | 80 | | kΩ |
| $V_{PGOOD}$ | PGOOD Trip Level | $V_{FB}$ With Respect to Set Output<br>$V_{FB}$ Ramping Negative<br>$V_{FB}$ Ramping Positive | | | <br>–10<br>10 | | <br>%<br>% |
| $V_{PGL}$ | PGOOD Voltage Low | $I_{PGOOD}$ = 2mA | | | 0.1 | 0.3 | V |
| **$INTV_{CC}$ Linear Regulator** | | | | | | | |
| $V_{INTVCC}$ | Internal $V_{CC}$ Voltage | 2.375V ≤ $V_{IN}$ ≤ 5V<br>$V_{IN}$ = 5.5V | | 4.8<br>5.15 | 5<br>5.25 | 5.2<br>5.35 | V<br>V |
| $V_{INTVCC}$ Load Reg | $INTV_{CC}$ Load Regulation | $I_{CC}$ = 0mA to 50mA | | | 0.5 | | % |
| **Oscillator and Phase-Locked Loop** | | | | | | | |
| $f_{SYNC}$ | SYNC Capture Range | | | 250 | | 650 | kHz |
| $f_S$ | Nominal Switching Frequency | | | 400 | 450 | 500 | kHz |
| $R_{MODE}$ | Mode Input Resistance | | | | 250 | | kΩ |
| $V_{IH\_CLKIN}$ | Clock Input Level High | | | 2.0 | | | V |
| $V_{IL\_CLKIN}$ | Clock Input Level Low | | | | | 0.8 | V |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime. Notes are automatically numbered when you apply the note style.

**Note 2:** The LTM4648 is tested under pulsed load conditions such that $T_J \approx T_A$. The LTM4648E is guaranteed to meet performance specifications over the 0°C to 125°C internal operating temperature range. Specifications over the –40°C to 125°C internal operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4648I is guaranteed to meet specifications over the –40°C to 125°C internal operating temperature range. Note that the maximum ambient temperature consistent with these specifications is determined by specific operating conditions in conjunction with board layout, the rated package thermal resistance and other environmental factors.

**Note 3:** The minimum on-time condition is tested at wafer sort.

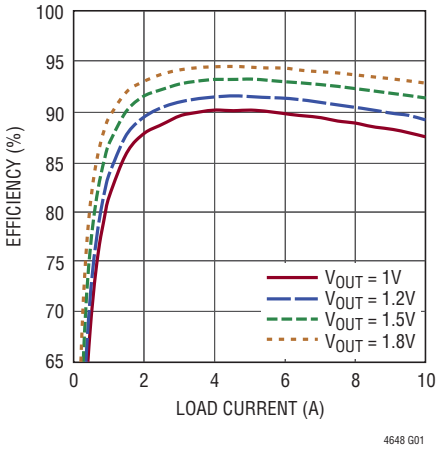
**Note 4:** See output current derating curves for different $V_{IN}$, $V_{OUT}$ and $T_A$.

**Note 5:** Guaranteed by design.

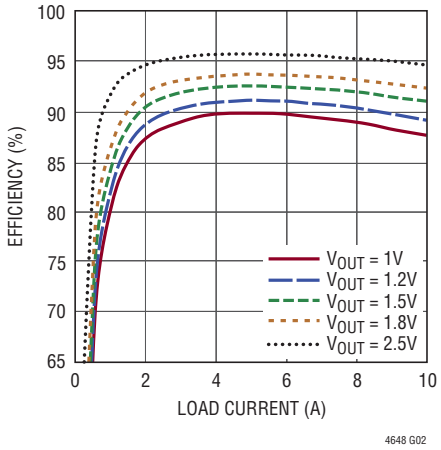
**Note 6:** 100% tested at wafer level.

# TYPICAL PERFORMANCE CHARACTERISTICS

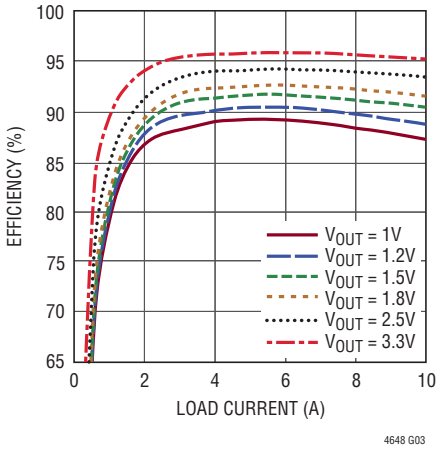
### 2.5$V_{IN}$ Efficiency



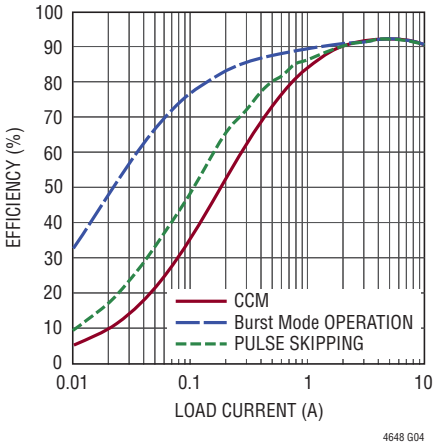

### 3.3$V_{IN}$ Efficiency



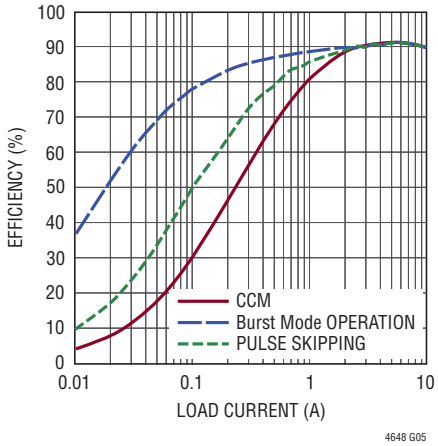

### 5$V_{IN}$ Efficiency



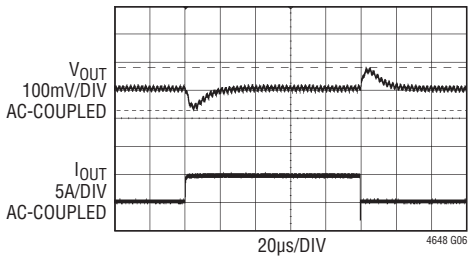

### CCM, Burst Mode and Pulse-Skipping Mode Efficiency ($V_{IN}$ = 3.3V, $V_{OUT}$ = 1.5V)




### CCM, Burst Mode and Pulse-Skipping Mode Efficiency ($V_{IN}$ = 5V, $V_{OUT}$ = 1.5V)

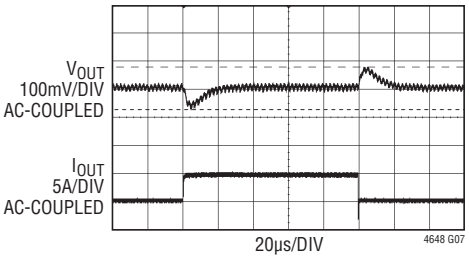



### 3.3$V_{IN}$, 1$V_{OUT}$ Load Transient



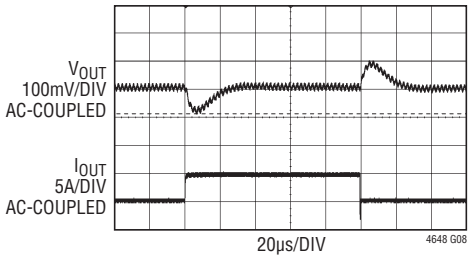

3.3$V_{IN}$, 1$V_{OUT}$, 5A TO 10A LOAD STEP, 5A/µs
$C_{OUT}$ = 1 • 22µF, 6.3V, 1210 + 2 • 100µF 1210 CERAMIC CAPACITORS
NO $C_{FF}$ CAPACITOR

### 5$V_{IN}$, 1$V_{OUT}$ Load Transient



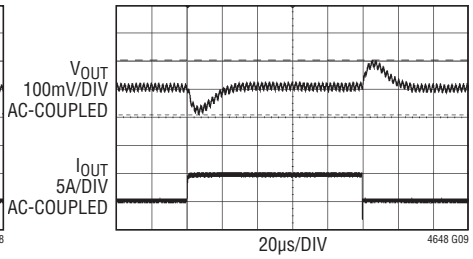

5$V_{IN}$, 1$V_{OUT}$, 5A TO 10A LOAD STEP, 5A/µs
$C_{OUT}$ = 1 • 22µF, 6.3V, 1210 + 2 • 100µF 6.3V 1210 CERAMIC CAPACITORS
NO $C_{FF}$ CAPACITOR

### 3.3$V_{IN}$, 1.5$V_{OUT}$ Load Transient




3.3$V_{IN}$, 1.5$V_{OUT}$, 5A TO 10A LOAD STEP, 5A/µs
$C_{OUT}$ = 1 • 22µF, 6.3V, 1210 + 2 • 100µF 6.3V 1210 CERAMIC CAPACITORS
NO $C_{FF}$ CAPACITOR

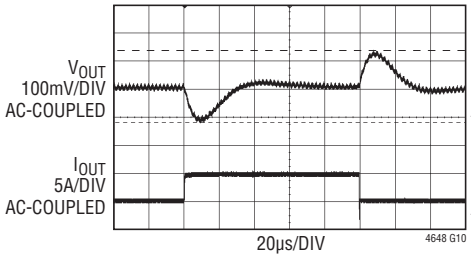
### 5$V_{IN}$, 1.5$V_{OUT}$ Load Transient




5$V_{IN}$, 1.5$V_{OUT}$, 5A TO 10A LOAD STEP, 5A/µs
$C_{OUT}$ = 1 • 22µF, 6.3V, 1210 + 2 • 100µF 6.3V 1210 CERAMIC CAPACITORS
NO $C_{FF}$ CAPACITOR

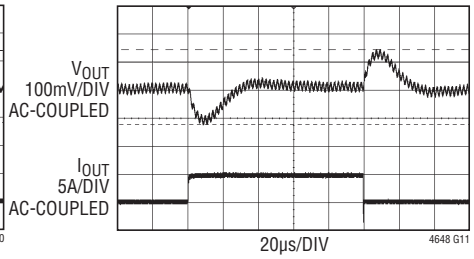
## TYPICAL PERFORMANCE CHARACTERISTICS

### $3.3V_{IN}$, $2.5V_{OUT}$ Load Transient



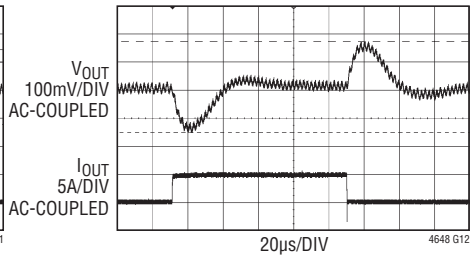

$3.3V_{IN}$, $2.5V_{OUT}$, 5A TO 10A LOAD STEP, 5A/µs
$C_{OUT}$ = 1 • 22µF, 6.3V, 1210 + 2 • 100µF 6.3V
1210 CERAMIC CAPACITORS
NO $C_{FF}$ CAPACITOR

### $5V_{IN}$, $2.5V_{OUT}$ Load Transient



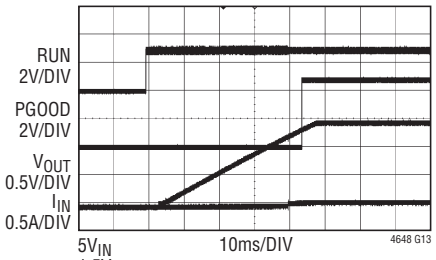

$5V_{IN}$, $2.5V_{OUT}$, 5A TO 10A LOAD STEP, 5A/µs
$C_{OUT}$ = 1 • 22µF, 6.3V, 1210 + 2 • 100µF 6.3V
1210 CERAMIC CAPACITORS
NO $C_{FF}$ CAPACITOR

### $5V_{IN}$, $3.3V_{OUT}$ Load Transient



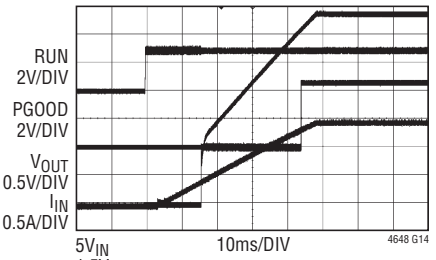

$5V_{IN}$, $3.3V_{OUT}$, 5A TO 10A LOAD STEP, 5A/µs
$C_{OUT}$ = 1 • 22µF, 6.3V, 1210 + 2 • 100µF 6.3V
1210 CERAMIC CAPACITORS
NO $C_{FF}$ CAPACITOR

### Output Start-Up



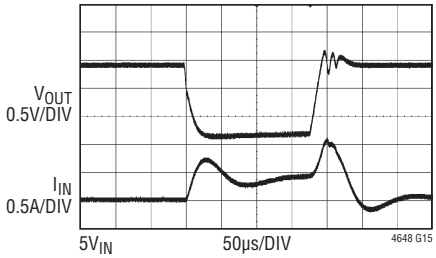

$5V_{IN}$
$1.5V_{OUT}$
$I_O$ = 0A START-UP
$C_{SS}$ = 0.1µF

### Output Start-Up



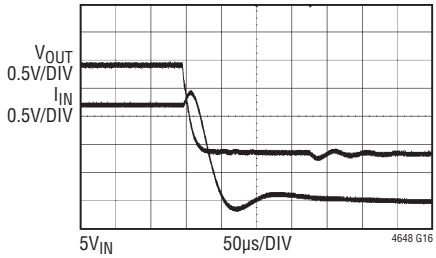

$5V_{IN}$
$1.5V_{OUT}$
$I_O$ = 10A START-UP
$C_{SS}$ = 0.1µF

### Output Short Circuit




$5V_{IN}$
$1.5V_{OUT}$
$I_{OUT}$ = 0A

### Output Short Circuit




$5V_{IN}$
$1.5V_{OUT}$
$I_{OUT}$ = 10A

## PIN FUNCTIONS

**PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.**

**GND (A1-A5, A7-A11, B1, B9-B11, E1, F3, F5, G1-G7):** Ground Pins for Both Input and Output Returns. All ground pins need to connect with large copper areas underneath the unit.

**TEMP (A6):** Onboard Temperature Diode for Monitoring the VBE Junction Voltage Change with Temperature. See the Applications Information section.

**CLKIN (B3):** External Synchronization Input to Phase Detector Pin. A clock on this pin will enable synchronization with forced continuous operation. See the Applications Information section.

**PHMODE (B4):** This pin can be tied to GND, tied to $INTV_{CC}$ or left floating. This pin determines the relative phases between the internal controllers and the phasing of the CLKOUT signal. See Table 2 in the Operation section.

**MODE (B5):** Mode Select Input. Connect this pin to $INTV_{CC}$ to enable Burst Mode operation. Connect to ground to enable forced continuous mode of operation. Floating this pin will enable pulse-skipping mode of operation.

**NC (B7-B8, C3-C4):** No Connection Pins. Either float these pins or connect them to GND for thermal purpose.

**$V_{IN}$ (C1, C8, C9, D1, D3-D5, D7-D9 and E8):** Power Input Pins. Apply input voltage between these pins and GND pins. Recommend placing input decoupling capacitance directly between $V_{IN}$ pins and GND pins.

**$V_{OUT}$ (C10-C11, D10-D11, E9-E11, F9-F11, G10-G11):** Power Output Pins. Apply output load between these pins and GND pins. Recommend placing output decoupling capacitance directly between these pins and GND pins. See Table 1.

**SW (C5):** Switching Node of the Circuit. This pin is used to check the switching frequency. Leave pin floating. A resistor-capacitor snubber can be placed from SW to PGND to eliminate high frequency switch node ringing. See the Applications Information section.

**PGOOD (C7):** Output Voltage Power Good Indicator. Open-drain logic output that is pulled to ground when the output voltage is not within ±10% of the regulation point.

**$V_{OUT\_LCL}$ (G9):** This pin is connected to the top of the internal top feedback resistor for the output. When the remote sense amplifier is used in the LTM4648, connect the remote sense amplifier output DIFFOUT to $V_{OUT\_LCL}$ to drive the 10k top feedback resistor. When the remote sense amplifier is not used in the LTM4648, connect $V_{OUT\_LCL}$ to $V_{OUT}$ directly.

**FREQ (E3):** Frequency Set Pin. A 10µA current is sourced from this pin. A resistor from this pin to ground sets a voltage, that in turn, programs the operating frequency. Alternatively, this pin can be driven with a DC voltage that can set the operating frequency. See the AApplications Information section. The LTM4648 has an internal resistor to program frequency to 450kHz.

**TRACK/SS (E5):** Output Voltage Tracking Pin and Soft-Start Inputs. The pin has a 1.2µA pull-up current source. A capacitor from this pin to ground will set a soft-start ramp rate. In tracking, the regulator output can be tracked to a different voltage. The different voltage is applied to a voltage divider then the slave output's track pin. This voltage divider is equal to the slave output's feedback divider for coincidental tracking. See the Applications Information section.

**FB (E7):** The Negative Input of the Error Amplifier. Internally, this pin is connected to $V_{OUT\_LCL}$ with a 10k precision resistor. Different output voltages can be programmed with an additional resistor between $V_{FB}$ and ground pins. In PolyPhase operation, tying the $V_{FB}$ pins together allows for parallel operation. See the Applications Information section for details.

**RUN (F1):** Run Control Pin. A voltage above 1.4V will turn on the module. The RUN pin has a 1µA pull-up current, once the RUN pin reaches 1.2V an additional 4.5µA pull-up current is added to this pin.

**CLKOUT (F2):** Output Clock Signal for PolyPhase Operation. The phase of CLKOUT is determined by the state of the PHMODE pin.

**$INTV_{CC}$ (F4):** Internal 5V LDO for Driving the Control Circuitry and the Power MOSFET Drivers. The 5V LDO has a 100mA current limit.

## PIN FUNCTIONS

**COMP (F6):** Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. Tie all COMP pins together in parallel operation.

**DIFFN (F7):** Input to the Remote Sense Amplifier. This pin connects to the ground remote sense point. Connect to GND when not used.

**DIFFP (F8):** Input to the Remote Sense Amplifier. This pin connects to the output remote sense point. Connect to GND when not used.

**DIFFOUT (G8):** Output of the Remote Sense Amplifier. This pin connects to the $V_{OUT\_LCL}$ pin for remote sense applications. Otherwise float when not used.

## BLOCK DIAGRAM

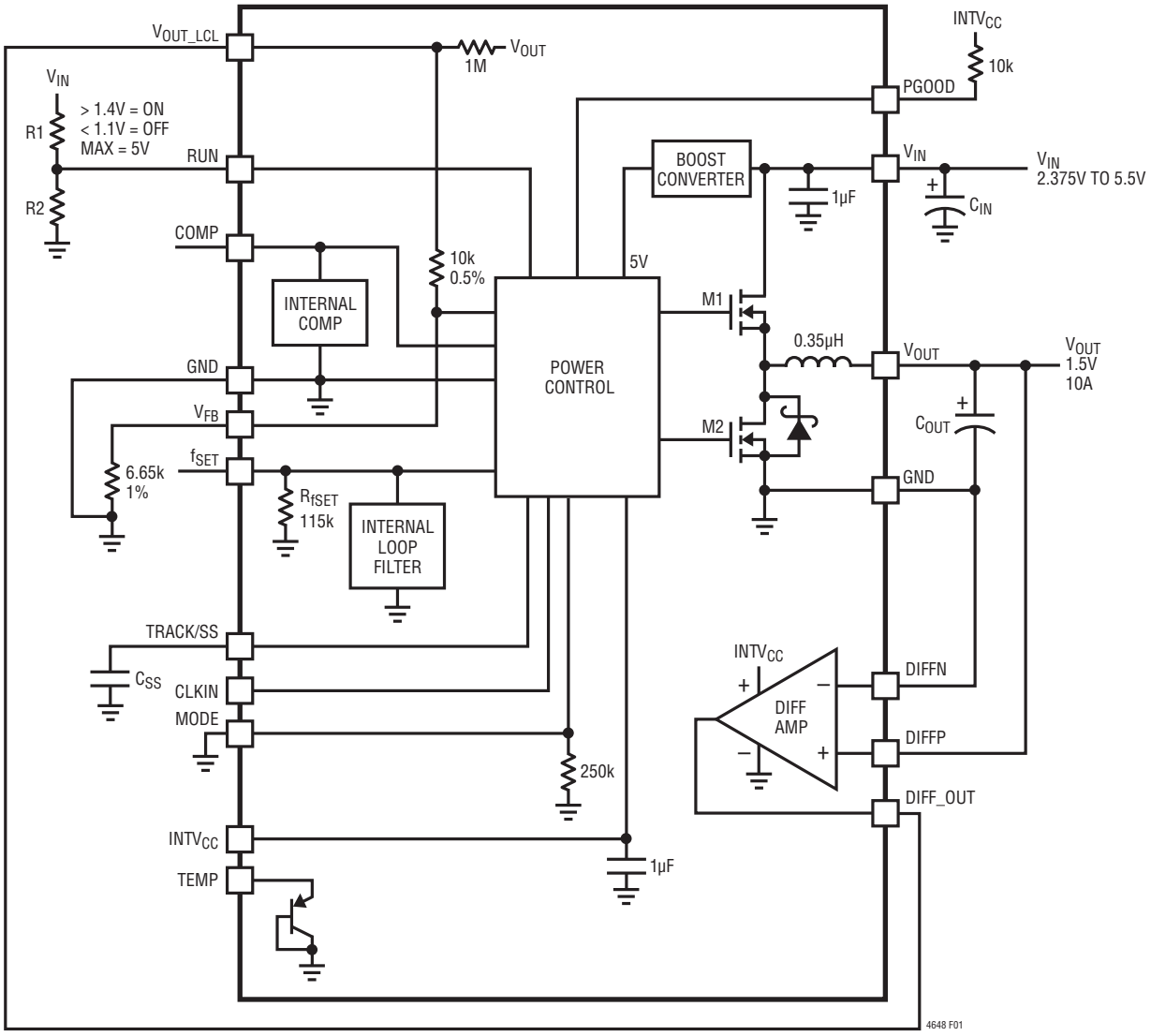



**Figure 1. Simplified LTM4648 Block Diagram**

## OPERATION

### Power Module Description

The LTM4648 is a high performance single output standalone nonisolated switching mode DC/DC power supply. It can provide up to 10A output current with few external input and output capacitors. This module provides precisely regulated output voltage programmable via an external resistor from 0.6VDC to 5VDC over a 2.375V to 5.5V input range. The typical application schematic is shown in Figure 18.

The LTM4648 has an integrated constant-frequency current mode regulator, power MOSFETs, inductor, and other supporting discrete components. The typical switching frequency is 450kHz. For switching noise-sensitive applications, it can be externally synchronized from 350kHz to 650kHz. See the Applications Information section.

With current mode control and internal feedback loop compensation, the LTM4648 module has sufficient stability margins and good transient performance with a wide range of output capacitors, especially with all ceramic output capacitors.

Current mode control provides cycle-by-cycle fast current limit in an overcurrent condition. An internal overvoltage monitor protects the output voltage in the event of an overvoltage >10%. The top MOSFET is turned off and the bottom MOSFET is turned on until the output is cleared.

Pulling the RUN pin below 1.1V forces the regulator into a shutdown state. The TRACK/SS pin is used for programming the output voltage ramp and voltage tracking during start-up. See the Applications Information section.

The LTM4648 is internally compensated to be stable over all operating conditions. Table 3 provides a guideline for input and output capacitances for several operating conditions. The Analog Devices µModule Power Design Tool will be provided for transient and stability analysis. The $V_{FB}$ pin is used to program the output voltage with a single external resistor to ground.

A remote sense amplifier is provided in the LTM4648 for accurately sensing output voltages ≤3.3V at the load point.

Multiphase operation can be easily employed with the synchronization inputs using an external clock source. See application examples.

High efficiency at light loads can be accomplished with selectable Burst Mode operation using the MODE pin. These light load features will accommodate battery operation. Efficiency graphs are provided for light load operation in the Typical Performance Characteristics section.

A diode connected PNP transistor with base and collector grounded is included in the module as a general purpose single-ended temperature monitor. The temperature monitor is intended to be used as a general temperature monitor, see Applications Information section

The switching node pins are available for functional operation monitoring and a resistor-capacitor snubber circuit can be careful placed on the switching node pin to ground to dampen any high frequency ringing on the transition edges. See the Applications Information section for details.

## APPLICATIONS INFORMATION

The typical LTM4648 application circuit is shown in Figure 18. External component selection is primarily determined by the maximum load current and output voltage. Refer to Table 3 for specific external capacitor requirements for particular applications.

### $V_{IN}$ to $V_{OUT}$ Step-Down Ratios

There are restrictions in the $V_{IN}$ to $V_{OUT}$ step-down ratio that can be achieved for a given input voltage. The $V_{IN}$ to $V_{OUT}$ minimum dropout is a function of load current and at very low input voltage and high duty cycle applications output power may be limited as the internal top power MOSFET is not rated for 10A operation at higher ambient temperatures. At very low duty cycles the minimum 90ns on-time must be maintained. See the Frequency Adjustment section and temperature derating curves.

### Output Voltage Programming

The PWM controller has an internal 0.6V ±1% reference voltage. As shown in the Block Diagram, a 10k 0.5% internal feedback resistor connects the $V_{OUT\_LCL}$ and $V_{FB}$ pins together. When the remote sense amplifier is used, then DIFFOUT is connected to the $V_{OUT\_LCL}$ pin. If the remote sense amplifier is not used, then $V_{OUT\_LCL}$ connects to $V_{OUT}$. The output voltage will default to 0.6V with no feedback resistor. Adding a resistor $R_{FB}$ from $V_{FB}$ to ground programs the output voltage:

$$V_{OUT} = 0.6V \bullet \frac{10k + R_{FB}}{R_{FB}}$$

**Table 1. $V_{FB}$ Resistor Table vs Various Output Voltages**

| $V_{OUT}$(V) | 0.6 | 1.0 | 1.2 | 1.5 | 1.8 | 2.5 | 3.3 | 5.0 |
|---|---|---|---|---|---|---|---|---|
| $R_{FB}$(k) | OPEN | 15 | 10 | 6.65 | 4.99 | 3.09 | 2.21 | 1.37 |

For parallel operation of N LTM4648, the following equation can be used to solve for $R_{FB}$:

$$R_{FB} = \frac{\frac{10k}{N}}{\frac{V_{OUT}}{0.6} - 1}$$

In parallel operation the $V_{FB}$ pins have an $I_{FB}$ current of 20nA maximum each channel. To reduce output voltage error due to this current, an additional $V_{OUT\_LCL}$ pin can be tied to $V_{OUT}$, and an additional $R_{FB}$ resistor can be used to lower the total Thevenin equivalent resistance seen by this current.

### Input Capacitors

The LTM4648 module should be connected to a low AC impedance DC source. Additional input capacitors are needed for the RMS input ripple current rating. The $I_{CIN(RMS)}$ equation which follows can be used to calculate the input capacitor requirement. Typically 22µF X7R ceramics are a good choice with RMS ripple current ratings of ~2A each. A 47µF to 100µF surface mount aluminum electrolytic bulk capacitor can be used for more input bulk capacitance. This bulk input capacitor is only needed if the input source impedance is compromised by long inductive leads, traces or not enough source capacitance. If low impedance power planes are used, then this bulk capacitor is not needed.

For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor ripple current, for each output, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1 - D)}$$

In the previous equation, $\eta\%$ is the estimated efficiency of the power module. The bulk capacitor can be a switcher-rated electrolytic aluminum capacitor or a Polymer capacitor.

### Output Capacitors

The LTM4648 is designed for low output voltage ripple noise. The bulk output capacitors defined as $C_{OUT}$ are chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. $C_{OUT}$ can be a low ESR tantalum capacitor, low ESR Polymer capacitor or ceramic capacitors. The typical output capacitance range is from 200µF to 470µF. Additional

## APPLICATIONS INFORMATION

output filtering may be required by the system designer if further reduction of output ripple or dynamic transient spikes is required. Table 3 shows a matrix of different output voltages and output capacitors to minimize the voltage droop and overshoot during a 5A/µs transient. The table optimizes total equivalent ESR and total bulk capacitance to optimize the transient performance. Stability criteria are considered in the Table 3 matrix, and the Analog Devices µModule Power Design Tool will be provided for stability analysis. Multiphase operation will reduce effective output ripple as a function of the number of phases. Application Note 77 discusses this noise reduction versus output ripple current cancellation, but the output capacitance should be considered carefully as a function of stability and transient response. The Analog Devices µModule Power Design Tool can calculate the output ripple reduction as the number of implemented phase's increases by N times.

### Burst Mode Operation

The LTM4648 is capable of Burst Mode operation in which the power MOSFETs operate intermittently based on load demand, thus saving quiescent current. For applications where maximizing the efficiency at very light loads is a high priority, Burst Mode operation should be applied. To enable Burst Mode operation, simply tie the MODE pin to $INTV_{CC}$. During Burst Mode operation, the peak current of the inductor is set to approximately 30% of the maximum peak current value in normal operation even though the voltage at the COMP pin indicates a lower value. The voltage at the COMP pin drops when the inductor's average current is greater than the load requirement. As the COMP voltage drops below 0.5V, the burst comparator trips, causing the internal sleep line to go high and turn off both power MOSFETs.

In sleep mode, the internal circuitry is partially turned off, reducing the quiescent current. The load current is now being supplied from the output capacitors. When the output voltage drops, causing COMP to rise, the internal sleep line goes low, and the LTM4648 resumes normal operation. The next oscillator cycle will turn on the top power MOSFET and the switching cycle repeats.

### Pulse-Skipping Mode Operation

In applications where low output ripple and high efficiency at intermediate currents are desired, pulse-skipping mode should be used. Pulse-skipping operation allows the LTM4648 to skip cycles at low output loads, thus increasing efficiency by reducing switching loss. Floating the MODE pin enables pulse-skipping operation. With pulse-skipping mode at light load, the internal current comparator may remain tripped for several cycles, thus skipping operation cycles. This mode has lower ripple than Burst Mode operation and maintains a higher frequency operation than Burst Mode operation.

### Forced Continuous Operation

In applications where fixed frequency operation is more critical than low current efficiency, and where the lowest output ripple is desired, forced continuous operation should be used. Forced continuous operation can be enabled by tying the MODE pin to ground. In this mode, inductor current is allowed to reverse during low output loads, the COMP voltage is in control of the current comparator threshold throughout, and the top MOSFET always turns on with each oscillator pulse. During start-up, forced continuous mode is disabled and inductor current is prevented from reversing until the LTM4648's output voltage is in regulation.

### Frequency Selection

The LTM4648 device is internally programmed to 450kHz switching frequency to improve power conversion efficiency. It is recommended for all of the application.

If desired, a resistor can be connected from the FREQ pin to $INTV_{CC}$ to adjust the FREQ pin DC voltage to increase the switching frequency between default 450kHz and maximum 650kHz. Figure 2 shows a graph of frequency setting verses FREQ pin DC voltage. Figure 18 shows an example of frequency programmed to 650kHz. Please be aware FREQ pin has an accurate 10µA current sourced from this pin when calculate the resistor value.

## APPLICATIONS INFORMATION

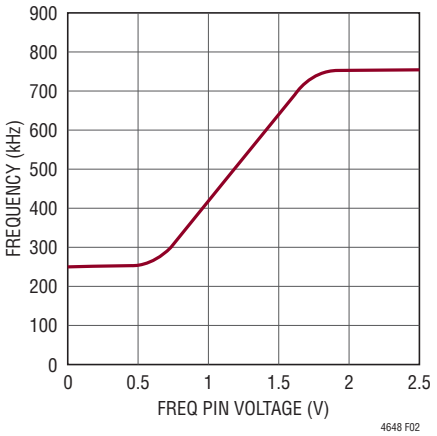



**Figure 2. Operating Frequency vs FREQ Pin Voltage**

### PLL and Frequency Synchronization

The LTM4648 device operates over a range of frequencies to improve power conversion efficiency. The nominal switching frequency is 450kHz. It can also be synchronized from 350kHz to 650kHz with an input clock that has a high level above 2V and a low level below 0.8V at the CLKIN pin. Once the LTM4648 is synchronizing to an external clock frequency, it will always running in Forced Continuous Operation. The 350kHz low end operation frequency limit is put in place to limit inductor ripple current.

### Multiphase Operation

For outputs that demand more than 10A of load current, multiple LTM4648 devices can be paralleled to provide more output current and reduced input and output voltage ripple.

The CLKOUT signal together with CLKIN pin can be used to cascade additional power stages to achieve the multiphase power supply solution. Tying the PHMODE pin to $INTV_{CC}$, GND, or (floating) generates a phase difference (between MODE/PLLIN and CLKOUT) of 180°, 120°, or 90° respectively as shown in Table 2. A total of 4 phases can be cascaded to run simultaneously with respect to each other by programming the PHMODE pin of each LTM4648 channel to different levels. Figure 3 shows a 3-phase design and 4-phase design example for clock phasing with the PHASMD table.

**Table 2. PHASEMD and CLKOUT Signal Relationship**

| PHASEMD | GND | FLOAT | $INTV_{CC}$ |
|---|---|---|---|
| CLKOUT | 120° | 90° | 180° |

The LTM4648 device is an inherently current mode controlled device, so parallel modules will have good current sharing. This will balance the thermals in the design. Tie the COMP, $V_{FB}$, TRACK/SS and RUN pins of each LTM4648 together to share the current evenly. Figure 20 and Figure 21 show a schematic of the parallel design.

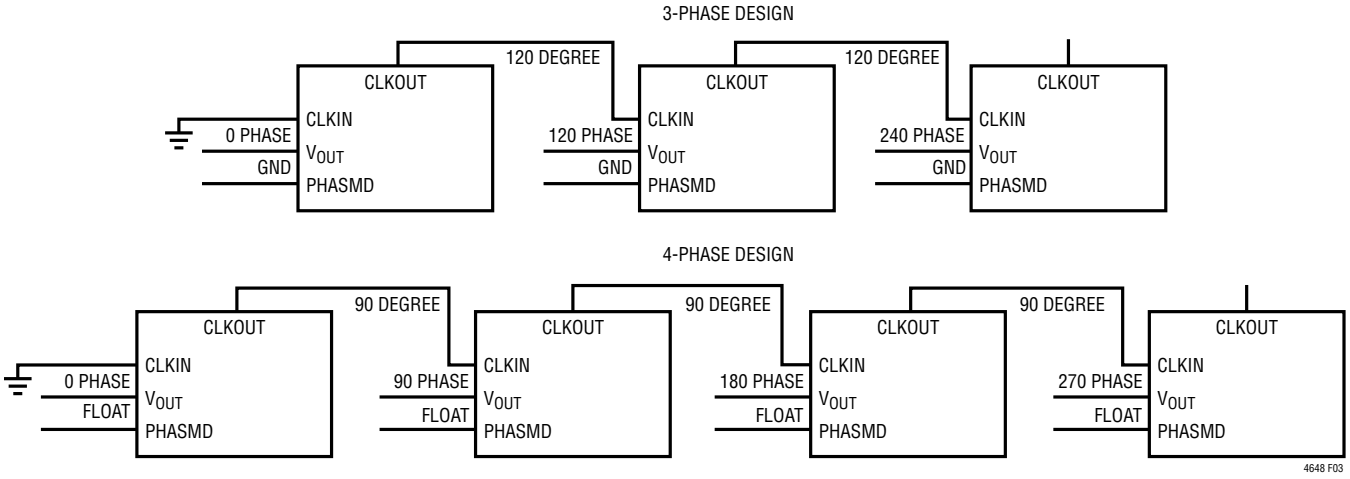



**Figure 3. Examples of 3-Phase, 4-Phase Operation with PHASMD Table**

## APPLICATIONS INFORMATION

A multiphase power supply could significantly reduce the amount of ripple current in both the input and output capacitors. The RMS input ripple current is reduced by, and the effective ripple frequency is multiplied by, the number of phases used (assuming that the input voltage is greater than the number of phases used times the output voltage). The output ripple amplitude is also reduced by the number of phases used.

### Input RMS Ripple Current Cancellation

Application Note 77 provides a detailed explanation of multiphase operation. The input RMS ripple current cancellation mathematical derivations are presented, and a graph is displayed representing the RMS ripple current reduction as a function of the number of interleaved phases (see Figure 4).

### Minimum On-Time

Minimum on-time $t_{ON}$ is the smallest time duration that the LTM4648 is capable of turning on the top MOSFET. It is determined by internal timing delays, and the gate charge required turning on the top MOSFET. Low duty cycle applications may approach this minimum on-time limit and care should be taken to ensure that:

$$\frac{V_{OUT}}{V_{IN} \bullet FREQ} > t_{ON(MIN)}$$

If the duty cycle falls below what can be accommodated by the minimum on-time, the controller will begin to skip cycles. The output voltage will continue to be regulated, but the output ripple and current will increase. The minimum on-time can be increased by lowering the switching frequency. A good rule of thumb is to use an 110ns on-time.

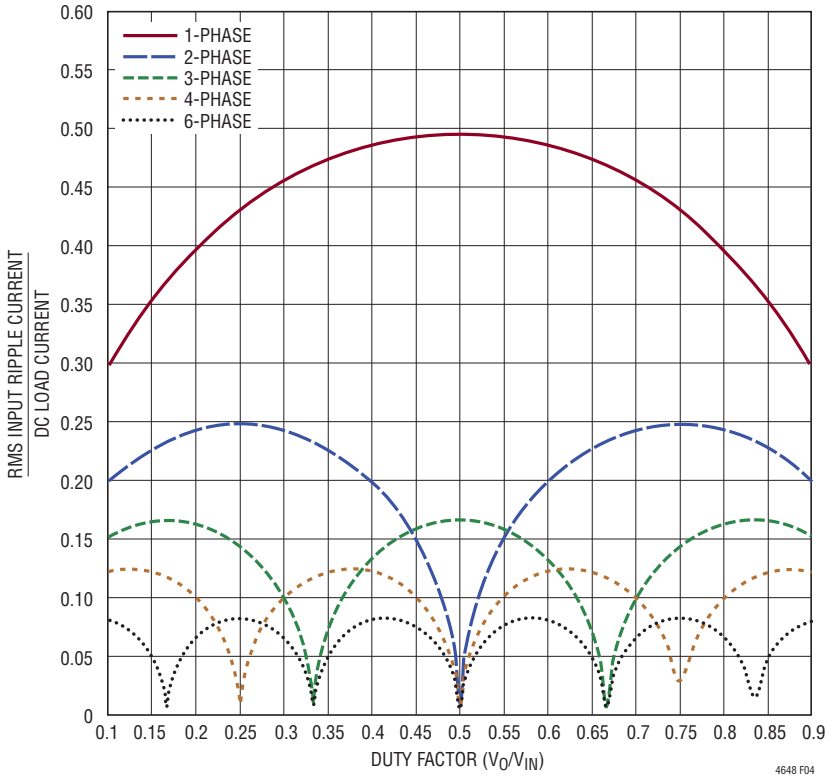



**Figure 4. Input RMS Current Ratios to DC Load Current as a Function of Duty Cycle**

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### Soft-Start

The TRACK/SS pin of the master can be controlled by a capacitor placed on the master regulator TRACK/SS pin to ground. A 1.2µA current source will charge the TRACK/SS pin up to the reference voltage and then proceed up to $INTV_{CC}$. After the 0.6V ramp, the TRACK/SS pin will no longer be in control, and the internal voltage reference will control output regulation from the feedback divider. Foldback current limit is disabled during this sequence of turn-on during tracking or soft-starting. The TRACK/SS pins are pulled low when the RUN pin is below 1.2V. The total soft-start time can be calculated as:

$$t_{SS} = \left( \frac{C_{SS}}{1.2\mu A} \right) \bullet 0.6$$

Regardless of the mode selected by the MODE pin, the regulator channels will always start in pulse-skipping mode up to TRACK/SS = 0.5V. Between TRACK/SS = 0.5V and 0.54V, it will operate in forced continuous mode and revert to the selected mode once TRACK/SS > 0.54V. In order to track with another channel once in steady state operation, the LTM4648 is forced into continuous mode operation as soon as $V_{FB}$ is below 0.54V regardless of the setting on the MODE pin.

### Output Voltage Tracking

Output voltage tracking can be programmed externally using the TRACK/SS pins. The output can be tracked up and down with another regulator. The master regulator's output is divided down with an external resistor divider that is the same as the slave regulator's feedback divider to implement coincident tracking. The LTM4648 uses an accurate 60.4k resistor internally for the top feedback resistor for each channel. Figure 6 shows an example of coincident tracking. Equations:

$$V_{SLAVE} = \left( 1 + \frac{10k}{R_{TA}} \right) \bullet V_{TRACK}$$

$V_{TRACK}$ is the track ramp applied to the slave's track pin. $V_{TRACK}$ has a control range of 0V to 0.6V, or the internal reference voltage. When the master's output is divided down with the same resistor values used to set the slave's output, then the slave will coincident track with the master until it reaches its final value. The master will continue to its final value from the slave's regulation point. Voltage tracking is disabled when $V_{TRACK}$ is more than 0.6V. RTA in Figure 5 will be equal to the $R_{FB}$ for coincident tracking. Figure 6 shows the coincident tracking waveforms.

Ratiometric tracking can be achieved by a few simple calculations and the slew rate value applied to the master's TRACK/SS pin. As mentioned above, the TRACK/SS pin has a control range from 0V to 0.6V. The master's TRACK/SS pin slew rate is directly equal to the master's output slew rate in Volts/Time. The equation:

$$\frac{MR}{SR} \bullet 10k = R_{TB}$$

where MR is the master's output slew rate and SR is the slave's output slew rate in Volts/Time. When coincident tracking is desired, then MR and SR are equal, thus $R_{TB}$ is equal the 10k. $R_{TA}$ is derived from equation:

$$R_{TA} = \frac{0.6V}{\frac{V_{FB}}{10k} + \frac{V_{FB}}{R_{FB}} - \frac{V_{TRACK}}{R_{TB}}}$$

where $V_{FB}$ is the feedback voltage reference of the regulator, and $V_{TRACK}$ is 0.6V. Since $R_{TB}$ is equal to the 10k top feedback resistor of the slave regulator in equal slew rate or coincident tracking, then $R_{TA}$ is equal to $R_{FB}$ with $V_{FB} = V_{TRACK}$. Therefore $R_{TB}$ = 10k, and $R_{TA}$ = 10k in Figure 4.

In ratiometric tracking, a different slew rate maybe desired for the slave regulator. $R_{TB}$ can be solved for when SR is slower than MR. Make sure that the slave supply slew rate is chosen to be fast enough so that the slave output voltage will reach it final value before the master output.

Each of the TRACK/SS pins will have the 1.2µA current source on when a resistive divider is used to implement tracking on that specific channel. This will impose an offset on the TRACK/SS pin input. Smaller values resistors with the same ratios as the resistor values calculated from the above equation can be used. For example, where the 10k is used then a 1.0k can be used to reduce the TRACK/SS pin offset to a negligible value.

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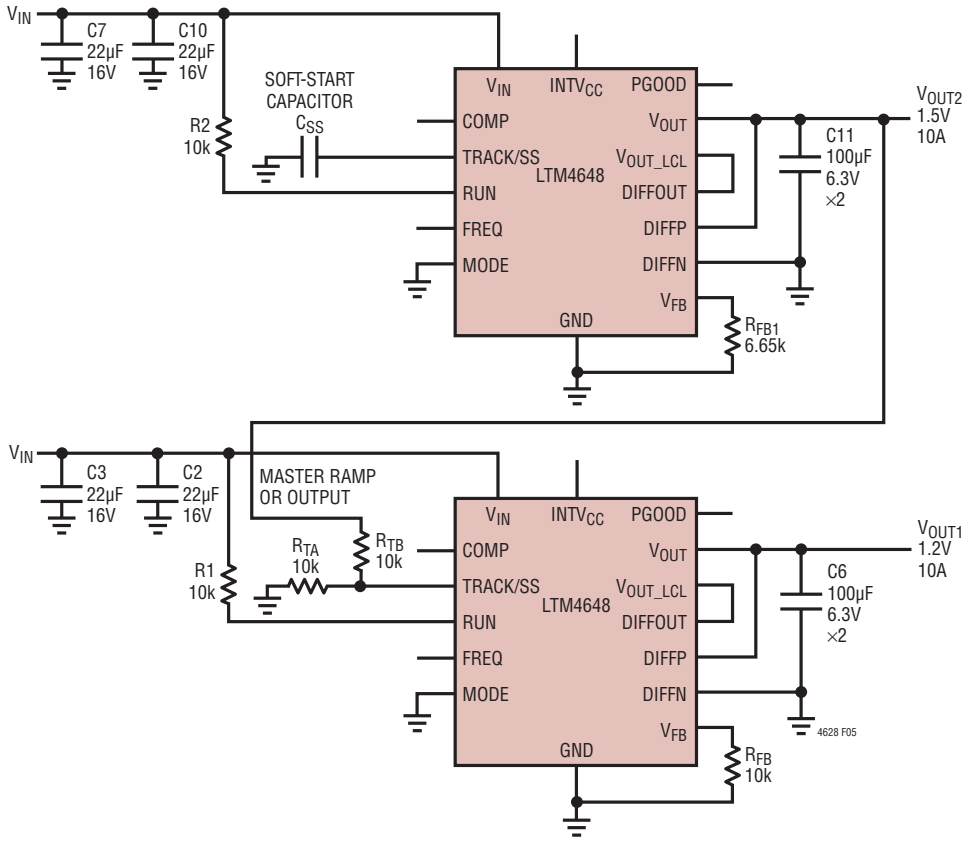


**Figure 5. Dual Outputs (1.5V and 1.2V) with Tracking**

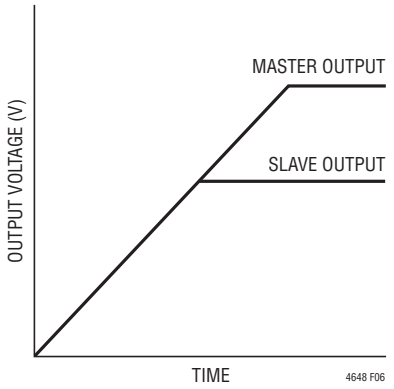


**Figure 6. Output Coincident Tracking Waveform**

### Power Good

The PGOOD pins are open-drain pins that can be used to monitor valid output voltage regulation. This pin monitors a ±7.5% window around the regulation point. A resistor can be pulled up to a particular supply voltage no greater than 6V maximum for monitoring.

### Stability Compensation

The module has already been internally compensated for all output voltages. Table 3 is provided for most application requirements. The Analog Devices µModule Power Design Tool will be provided for other control loop optimization.

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### Run Enable

The RUN pin has an enable threshold of 1.40V maximum, typically 1.25V with 150mV of hysteresis. It controls the turn-on of the µModule. The RUN pin can be pulled up to $V_{IN}$ for 5V operation, or a 5V Zener diode can be placed on the pin and a 10k to 100k resistor can be placed up to higher than 5V input for enabling the µModule. The RUN pin can also be used for output voltage sequencing.

In parallel operation the RUN pins can be tied together and controlled from a single control. See the Typical Application circuits in Figure 20 and Figure 21. The RUN pin can also be left floating. The RUN pin has a 1µA pull-up current source that increases to 4.5µA during ramp-up.

### Differential Remote Sense Amplifier

An accurate differential remote sense amplifier is provided in the LTM4648 to sense low output voltages accurately at the remote load points. This is especially true for high current loads. It is very important that the DIFFP and DIFFN are connected properly at the output, and DIFFOUT is connected to $V_{OUT\_LCL}$. Review the parallel schematics in Figure 20 and Figure 21.

### SW Pins

The SW pin is generally for testing purposes by monitoring the pin. The SW pin can also be used to dampen out switch node ringing caused by LC parasitic in the switched current path. Usually a series R-C combination is used called a snubber circuit. The resistor will dampen the resonance and the capacitor is chosen to only affect the high frequency ringing across the resistor.

If the stray inductance or capacitance can be measured or approximated then a somewhat analytical technique can be used to select the snubber values. The inductance is usually easier to predict. It combines the power path board inductance in combination with the MOSFET interconnect bond wire inductance.

First the SW pin can be monitored with a wide bandwidth scope with a high frequency scope probe. The ring frequency can be measured for its value. The impedance Z can be calculated:

$$Z_L = 2\pi \bullet f \bullet L$$

where f is the resonant frequency of the ring, and L is the total parasitic inductance in the switch path. If a resistor is selected that is equal to Z, then the ringing should be dampened. The snubber capacitor value is chosen so that its impedance is equal to the resistor at the ring frequency. Calculated by:

$$Z_C = \frac{1}{2\pi \bullet f \bullet C}$$

These values are a good place to start with. Modification to these components should be made to attenuate the ringing with the least amount the power loss.

### Temperature Monitoring

Measuring the absolute temperature of a diode is possible due to the relationship between current, voltage and temperature described by the classic diode equation:

$$I_D = I_S \bullet e^{\left(\frac{V_D}{\eta \bullet V_T}\right)}$$

or

$$V_D = \eta \bullet V_T \bullet \ln\frac{I_D}{I_S}$$

where $I_D$ is the diode current, $V_D$ is the diode voltage, $\eta$ is the ideality factor (typically close to 1.0) and $I_S$ (saturation current) is a process dependent parameter. $V_T$ can be broken out to:

$$V_T = \frac{k \bullet T}{q}$$

where T is the diode junction temperature in Kelvin, q is the electron charge and k is Boltzmann's constant. $V_T$ is approximately 26mV at room temperature (298K) and scales linearly with Kelvin temperature. It is this linear temperature relationship that makes diodes suitable temperature sensors. The $I_S$ term in the equation above is the extrapolated current through a diode junction when the diode has zero volts across the terminals. The $I_S$ term varies from process to process, varies with temperature, and by definition must always be less than $I_D$. Combining all of the constants into one term:

$$K_D = \frac{\eta \bullet k}{q}$$

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where $K_D = 8.62^{-5}$, and knowing $\ln(I_D/I_S)$ is always positive because $I_D$ is always greater than $I_S$, leaves us with the equation that:

$$V_D = T(KELVIN) \bullet K_D \bullet \ln\frac{I_D}{I_S}$$

where $V_D$ appears to increase with temperature. It is common knowledge that a silicon diode biased with a current source has an approximately –2mV/°C temperature relationship (Figure 7), which is at odds with the equation. In fact, the $I_S$ term increases with temperature, reducing the $\ln(I_D/I_S)$ absolute value yielding an approximately –2mV/°C composite diode voltage slope.

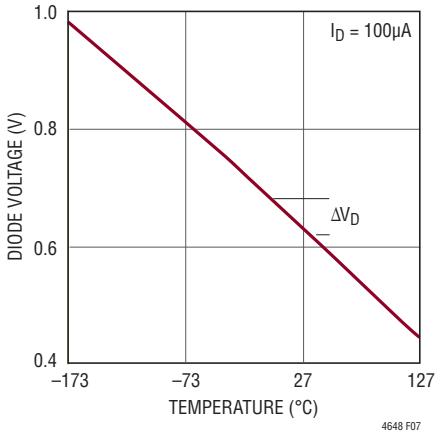



**Figure 7. Diode Voltage, $V_D$, vs Temperature T (°C) for Different Bias Currents**

An external diode connected PNP transistor can be pulled up to $V_{IN}$ with a resistor to set the current to 100µA for using this diode connected transistor as a general temperature monitor by monitoring the diode voltage drop with temperature, or a specific temperature monitor can be used that injects two currents that are at a 10:1 ratio for very accurate temperature monitoring. See Figure 22 for an example.

### Thermal Considerations and Output Current Derating

The thermal resistances reported in the Pin Configuration section of the data sheet are consistent with those parameters defined by JESD51-9 and are intended for use with finite element analysis (FEA) software modeling tools that leverage the outcome of thermal modeling, simulation, and correlation to hardware evaluation performed on a µModule package mounted to a hardware test board—also defined by JESD51-9 ("Test Boards for Area Array Surface Mount Package Thermal Measurements"). The motivation for providing these thermal coefficients in found in JESD51-12 ("Guidelines for Reporting and Using Electronic Package Thermal Information").

Many designers may opt to use laboratory equipment and a test vehicle such as the demo board to anticipate the µModule regulator's thermal performance in their application at various electrical and environmental operating conditions to compliment any FEA activities. Without FEA software, the thermal resistances reported in the Pin Configuration section are in-and-of themselves not relevant to providing guidance of thermal performance; instead, the derating curves provided in the data sheet can be used in a manner that yields insight and guidance pertaining to one's application usage, and can be adapted to correlate thermal performance to one's own application.

The Pin Configuration section typically gives four thermal coefficients explicitly defined in JESD51-12; these coefficients are quoted or paraphrased below:

1. $\theta_{JA}$: the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.

## APPLICATIONS INFORMATION

2. $\theta_{JCbottom}$: the thermal resistance from junction to ambient, is the natural convection junction-to-ambient air thermal resistance measured in a one cubic foot sealed enclosure. This environment is sometimes referred to as "still air" although natural convection causes the air to move. This value is determined with the part mounted to a JESD51-9 defined test board, which does not reflect an actual application or viable operating condition.

3. $\theta_{JCtop}$: the thermal resistance from junction to top of the product case, is determined with nearly all of the component power dissipation flowing through the top of the package. As the electrical connections of the typical µModule are on the bottom of the package, it is rare for an application to operate such that most of the heat flows from the junction to the top of the part. As in the case of $\theta_{JCbottom}$, this value may be useful for comparing packages but the test conditions don't generally match the user's application.

4. $\theta_{JB}$: the thermal resistance from junction to the printed circuit board, is the junction-to-board thermal resistance where almost all of the heat flows through the bottom of the µModule and into the board, and is really the sum of the $\theta_{JCbottom}$ and the thermal resistance of the bottom of the part through the solder joints and through a portion of the board. The board temperature is measured a specified distance from the package, using a two sided, two layer board. This board is described in JESD51-9.

A graphical representation of the aforementioned thermal resistances is given in Figure 8; blue resistances are contained within the µModule regulator, whereas green resistances are external to the µModule.

As a practical matter, it should be clear to the reader that no individual or sub-group of the four thermal resistance parameters defined by JESD51-12 or provided in the Pin Configuration section replicates or conveys normal operating conditions of a µModule. For example, in normal board-mounted applications, never does 100% of the device's total power loss (heat) thermally conduct exclusively through the top or exclusively through bottom of the µModule—as the standard defines for $\theta_{JCtop}$ and $\theta_{JCbottom}$, respectively. In practice, power loss is thermally dissipated in both directions away from the package—granted, in the absence of a heat sink and airflow, a majority of the heat flow is into the board.

Within a SIP (system-in-package) module, be aware there are multiple power devices and components dissipating power, with a consequence that the thermal resistances relative to different junctions of components or die are not exactly linear with respect to total package power loss. To reconcile this complication without sacrificing modeling simplicity—but also, not ignoring practical realities—an approach has been taken using FEA software modeling along with laboratory testing in a controlled-environment chamber to reasonably define and correlate the thermal

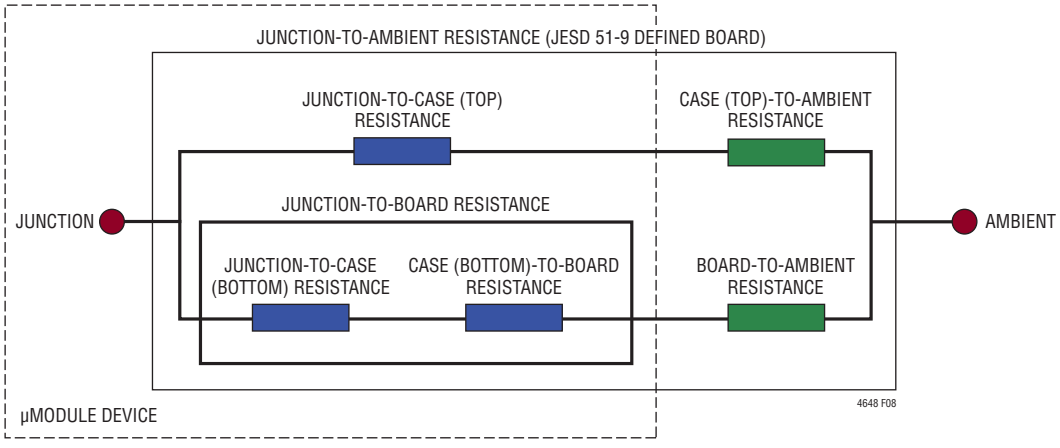



**Figure 8. Graphical Representation of JESD51-12 Thermal Coefficients**

## APPLICATIONS INFORMATION

resistance values supplied in this data sheet: (1) Initially, FEA software is used to accurately build the mechanical geometry of the µModule and the specified PCB with all of the correct material coefficients along with accurate power loss source definitions; (2) this model simulates a software-defined JEDEC environment consistent with JESD51-9 to predict power loss heat flow and temperature readings at different interfaces that enable the calculation of the JEDEC-defined thermal resistance values; (3) the model and FEA software is used to evaluate the µModule with heat sink and airflow; (4) having solved for and analyzed these thermal resistance values and simulated various operating conditions in the software model, a thorough laboratory evaluation replicates the simulated conditions with thermocouples within a controlled-environment chamber while operating the device at the same power loss as that which was simulated. An outcome of this process and due-diligence yields a set of derating curves provided in other sections of this data sheet. After these laboratory test have been performed and correlated to the µModule model, then the $\theta_{JB}$ and $\theta_{BA}$ are summed together to correlate quite well with the µModule model with no airflow or heat sinking in a properly define chamber. This $\theta_{JB} + \theta_{BA}$ value is shown in the Pin Configuration section and should accurately equal the $\theta_{JA}$ value because approximately 100% of power loss flows from the junction through the board into ambient with no airflow or top mounted heat sink.

The 1.5V, 2.5V and 3.3V power loss curves in Figure 9 and Figure 10 can be used in coordination with the load current derating curves in Figure 11 to Figure 15 for calculating an approximate $\theta_{JA}$ thermal resistance for the LTM4648 with various heat sinking and airflow conditions. The power loss curves are taken at room temperature, and are increased with a multiplicative factor according to the ambient temperature. This approximate factor is: 1.4 for 120°C. The derating curves are plotted with the output current starting at 10A and the ambient temperature at 40°C. The output voltages are 1.5V, 2.5V and 3.3V. These are chosen to include the lower and higher output voltage ranges for correlating the thermal resistance. Thermal models are derived from several temperature measurements in a controlled temperature chamber along with thermal modeling analysis. The junction temperatures are monitored while ambient temperature is increased with and without airflow. The power loss increase with ambient temperature change is factored into the derating

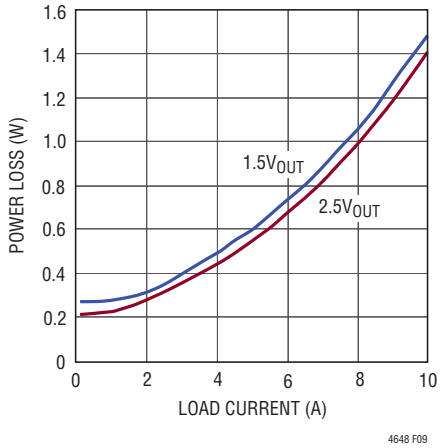



**Figure 9. $3.3V_{IN}$ to $2.5V_{OUT}$ and $1.5V_{OUT}$ Power Loss**

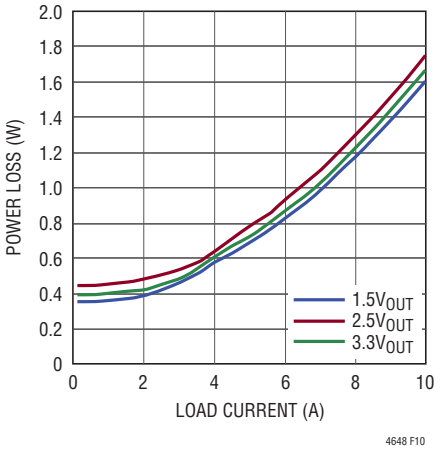



**Figure 10. $5V_{IN}$ to $3.3V_{OUT}$, $2.5V_{OUT}$ and $1.5V_{OUT}$ Power Loss**

## APPLICATIONS INFORMATION

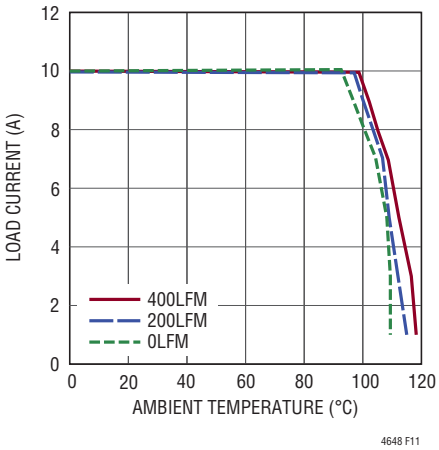



**Figure 11. No Heat Sink with $3.3V_{IN}$ to $1.5V_{OUT}$**

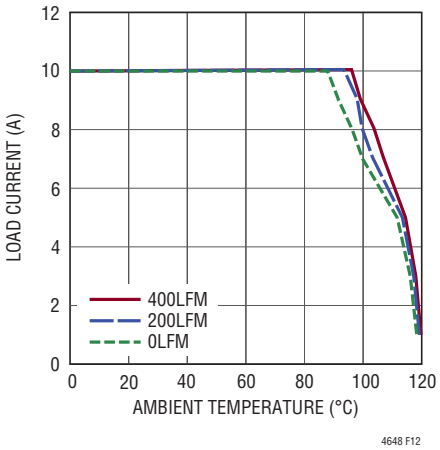



**Figure 12. No Heat Sink with $5V_{IN}$ to $1.5V_{OUT}$**

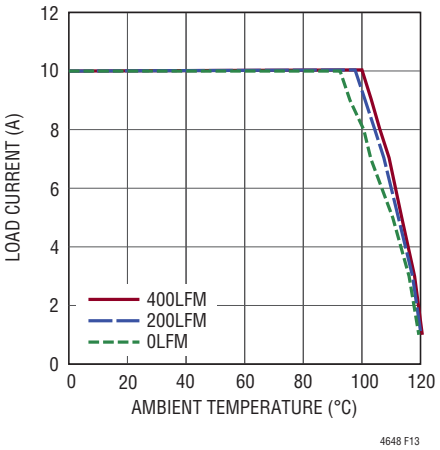



**Figure 13. No Heat Sink with $3.3V_{IN}$ to $2.5V_{OUT}$**

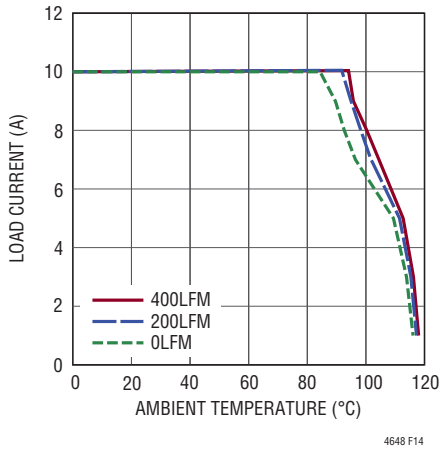



**Figure 14. No Heat Sink with $5V_{IN}$ to $2.5V_{OUT}$**

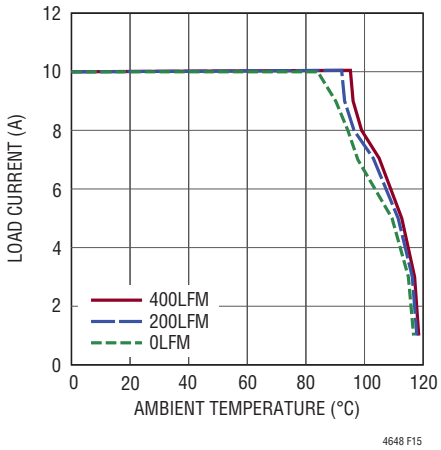



**Figure 15. No Heat Sink with $5V_{IN}$ to $3.3V_{OUT}$**

curves. The junctions are maintained at 120°C maximum while lowering output current or power with increasing ambient temperature. The decreased output current will decrease the internal module loss as ambient temperature is increased. The monitored junction temperature of 120°C minus the ambient operating temperature specifies how much module temperature rise can be allowed. As an example in Figure 12 the load current is derated to ~8A at ~95°C with no air or heat sink and the power loss for the 5V to 1.5V at 8A output is about 1.68W. The 1.68W loss is calculated with the ~1.2W room temperature loss from the 5V to 1.5V power loss curve at 8A, and the 1.4 multiplying factor at 120°C junction. If the 95°C ambient temperature is subtracted from the 120°C junction temperature, then the difference of 25°C divided by 1.68W equals a 15°C/W $\theta_{JA}$ thermal resistance. Table 4 specifies a 14°C/W value which is very close. Table 4, Table 5 and Table 6 provide equivalent thermal resistances for 1.5V, 2.5V and 3.3V outputs with and without airflow. The derived thermal resistances in Table 4, Table 5 and Table 6 for the various conditions can be multiplied by the calculated power loss as a function of ambient temperature to derive temperature rise above ambient, thus maximum junction temperature. Room temperature power loss can be derived from the efficiency curves in the Typical Performance Characteristics

## APPLICATIONS INFORMATION

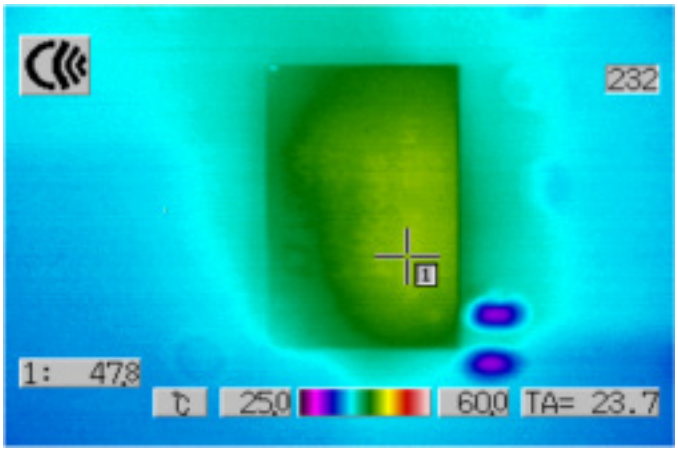



**Figure 16. Thermal Image $5V_{IN}$ to $1.5V_{OUT}$ at 10A (No Heat Sink, No Air Flow and Room Temperature)**

section and adjusted with the above ambient temperature multiplicative factors. The printed circuit board is a 1.6mm thick four layer board with two ounce copper for the two outer layers and one ounce copper for the two inner layers. The PCB dimensions are 95mm × 76mm.

### Safety Considerations

The LTM4648 module does not provide isolation from $V_{IN}$ to $V_{OUT}$. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current needs to be provided to protect each unit from catastrophic failure.

### Layout Checklist/Example

The high integration of LTM4648 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including $V_{IN}$, GND and $V_{OUT}$. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the $V_{IN}$, GND and $V_{OUT}$ pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on the pads, unless they are capped.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to GND underneath the unit.

Figure 17 gives a good example of the recommended layout.

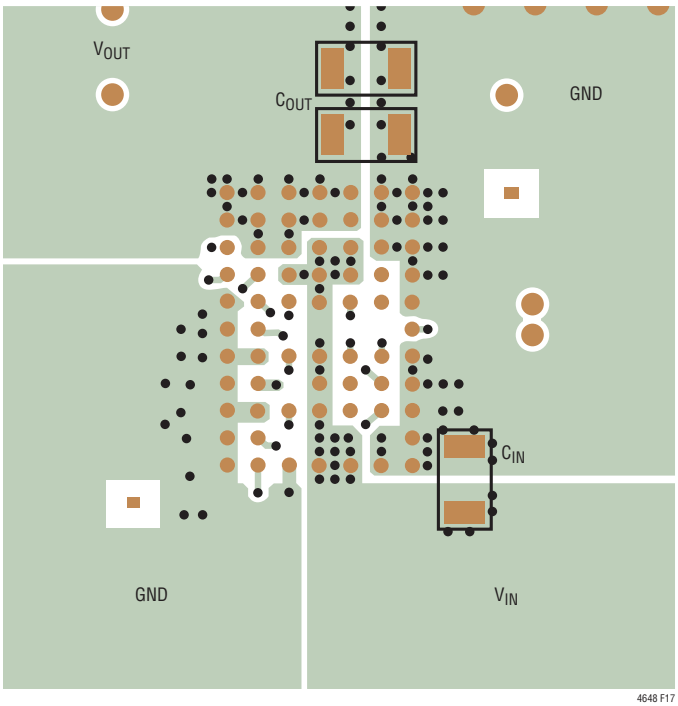



**Figure 17. Recommended PCB Layout**

## APPLICATIONS INFORMATION

**Table 3. Output Voltage Response vs Component Matrix (Refer to Figure 18) 0A to 5A Load Step Typical Measured Values**

| $C_{IN}$ (BULK)* | VENDORS | PART NUMBER | $C_{IN}$ (CERAMIC) | VENDORS | PART NUMBER | $C_{OUT}$ (CERAMIC) | VENDORS | PART NUMBER |
|---|---|---|---|---|---|---|---|---|
| 150µF, 16V | SANYO OSCON | 25HVH150MT | 22µF, 16V | MURATA | GRM32ER71C226KE18L | 100µF, 6.3V | MURATA | GRM32ER60J107ME20L |
| | | | | | | | AVX | 12106D107MAT |

| $V_{OUT}$ | $V_{IN}$ | $C_{IN}$ (BULK)* | $C_{IN}$ (CERAMIC) | $C_{OUT}$ (CERAMIC) | $C_{FF}$ (pF) | $V_{DROOP}$ | $V_{P-P}$ | RECOVERY TIME | LOAD STEP SPEED | $R_{FB}$ | FREQ |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1V | 2.375V, 3.3, 5V | 120µF* | 22µF × 3 | 100µF × 3 | None | 65mV | 130mV | 25µs | 5A/µs | 15kΩ | 450kHz |
| 1.2V | 2.375V, 3.3V, 5V | 120µF* | 22µF × 3 | 100µF × 3 | None | 70mV | 140mv | 25µs | 5A/µs | 10kΩ | 450kHz |
| 1.5V | 3.3V, 5V | 120µF* | 22µF × 3 | 100µF × 3 | None | 80mV | 160mV | 30µs | 5A/µs | 6.65kΩ | 450kHz |
| 2.5V | 3.3V, 5V | 120µF* | 22µF × 3 | 100µF × 3 | None | 110mV | 230mV | 40µs | 5A/µs | 3.09kΩ | 450kHz |
| 3.3V | 5V | 120µF* | 22µF × 3 | 100µF × 3 | None | 140mV | 290mV | 40µs | 5A/µs | 2.21kΩ | 450kHz |

*Bulk capacitor is optional if $V_{IN}$ has very low input impedance.

**Table 4. 1.5V Output**

| DERATING CURVE | $V_{IN}$ (V) | POWER LOSS CURVE | AIR FLOW (LFM) | HEAT SINK | $\theta_{JA}$ (°C/W) |
|---|---|---|---|---|---|
| Figures 11, 12 | 3.3, 5 | Figures 9, 10 | 0 | None | 14 |
| Figures 11, 12 | 3.3, 5 | Figures 9, 10 | 200 | None | 12 |
| Figures 11, 12 | 3.3, 5 | Figures 9, 10 | 400 | None | 10 |

**Table 5. 2.5V Output**

| DERATING CURVE | $V_{IN}$ (V) | POWER LOSS CURVE | AIR FLOW (LFM) | HEAT SINK | $\theta_{JA}$ (°C/W) |
|---|---|---|---|---|---|
| Figure 13, 14 | 3.3, 5 | Figures 9, 10 | 0 | None | 14 |
| Figure 13, 14 | 3.3, 5 | Figures 9, 10 | 200 | None | 12 |
| Figure 13, 14 | 3.3, 5 | Figures 9, 10 | 400 | None | 10 |

**Table 6. 3.3V Output**

| DERATING CURVE | $V_{IN}$ (V) | POWER LOSS CURVE | AIR FLOW (LFM) | HEAT SINK | $\theta_{JA}$ (°C/W) |
|---|---|---|---|---|---|
| Figure 15 | 5 | Figure 10 | 0 | None | 14 |
| Figure 15 | 5 | Figure 10 | 200 | None | 12 |
| Figure 15 | 5 | Figure 10 | 400 | None | 10 |

## TYPICAL APPLICATIONS

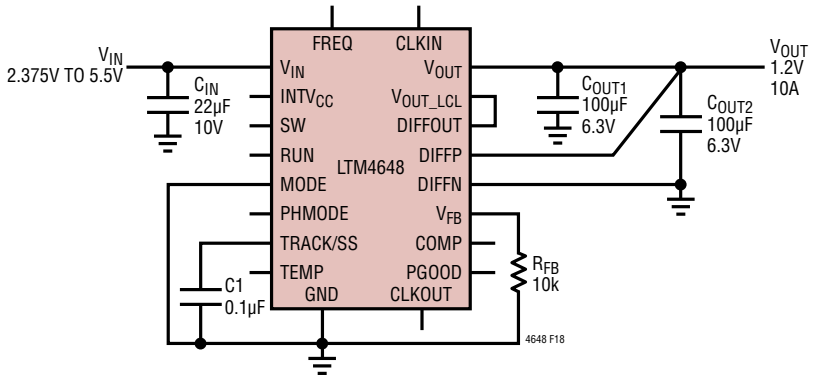



**Figure 18. 2.375V to 5.5$V_{IN}$, 1.2V at 10A Design**

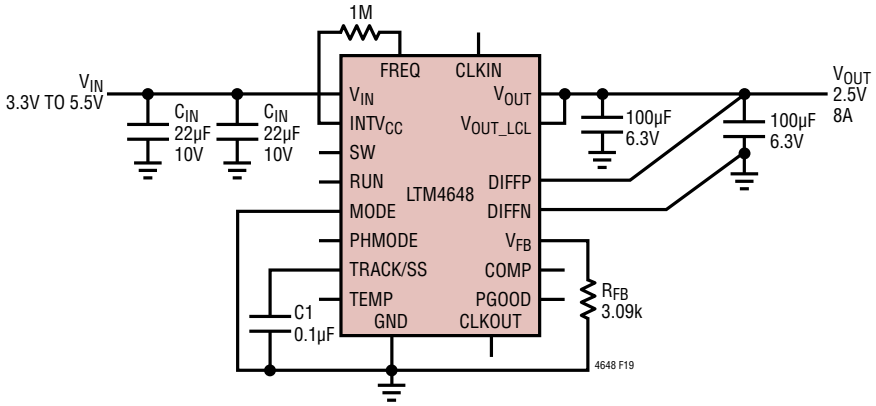



**Figure 19. 3.3V to 5V $V_{IN}$, 2.5$V_{OUT}$ at 8A Design with Increased 650kHz Frequency**

## TYPICAL APPLICATIONS

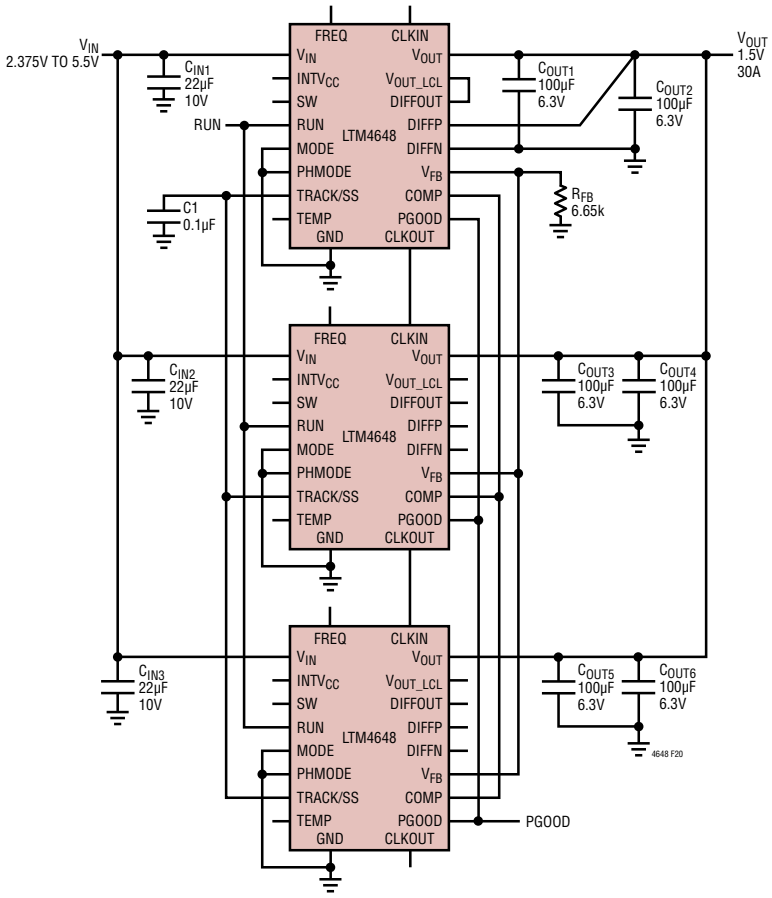



**Figure 20. Three LTM4648 in Parallel, 1.5V at 30A Design**

## TYPICAL APPLICATIONS

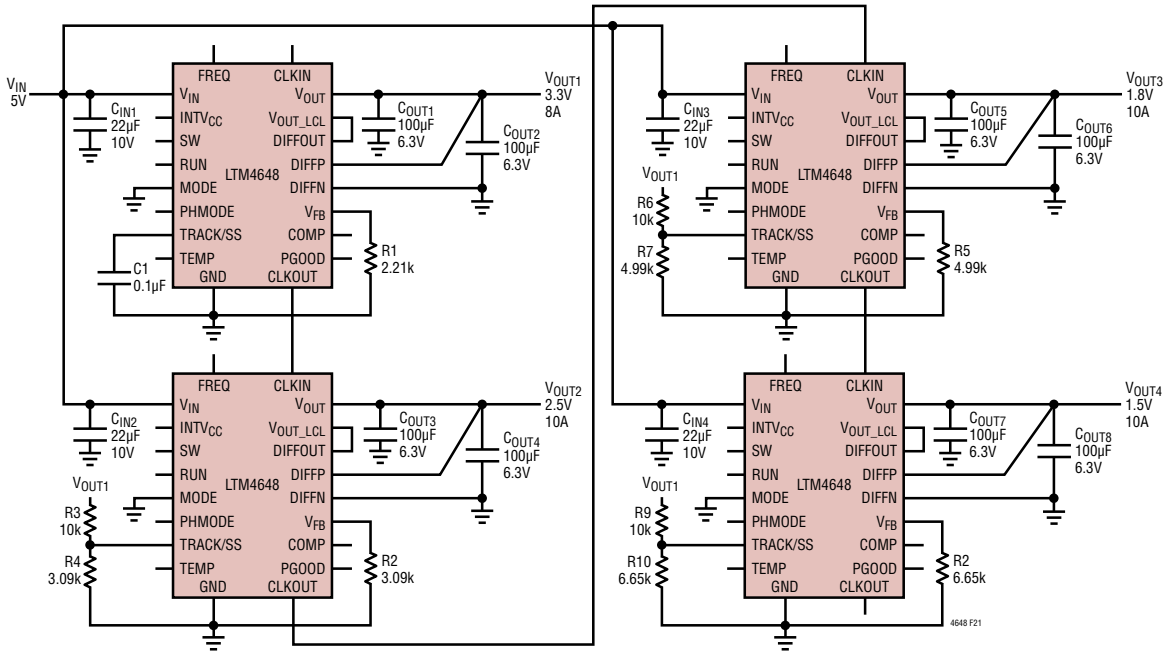



**Figure 21. Quad Outputs 4-Phase LTM4648 Regulator with Tracking Function**

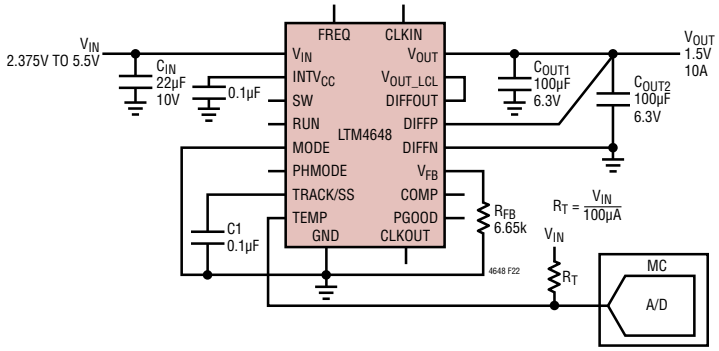



**Figure 22. Single LTM4648 10A Design with Temperature Monitoring**

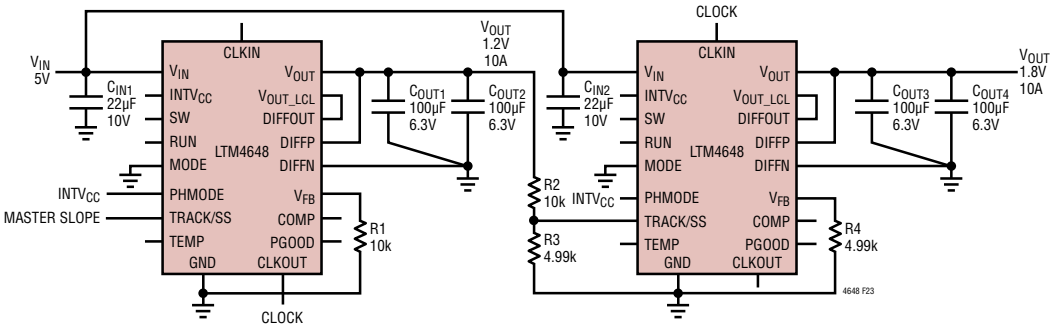
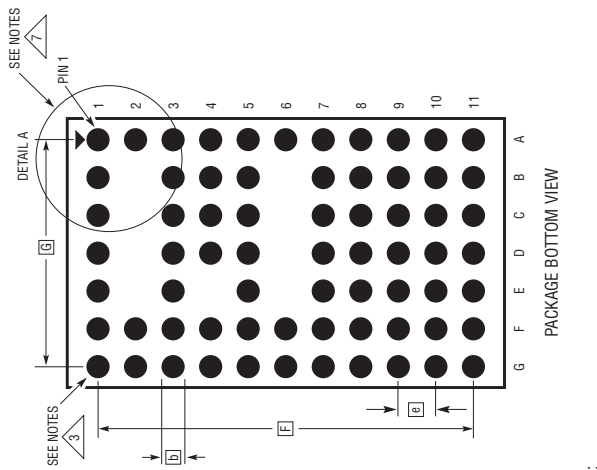


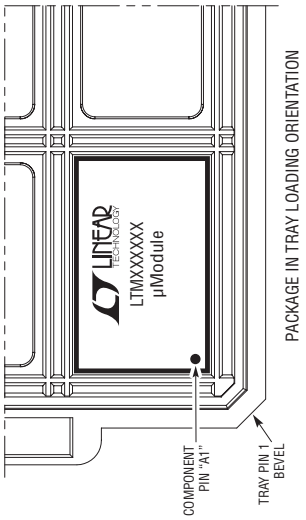

**Figure 23. Dual Outputs 2-Phase LTM4648 Regulator with Tracking Function**

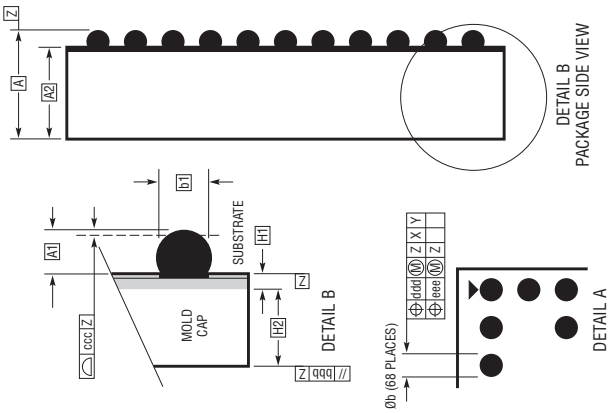
# PACKAGE DESCRIPTION

**BGA Package**
**68-Lead (15.00mm × 9.00mm × 4.92mm)**
(Reference LTC DWG# 05-08-1892 Rev A)

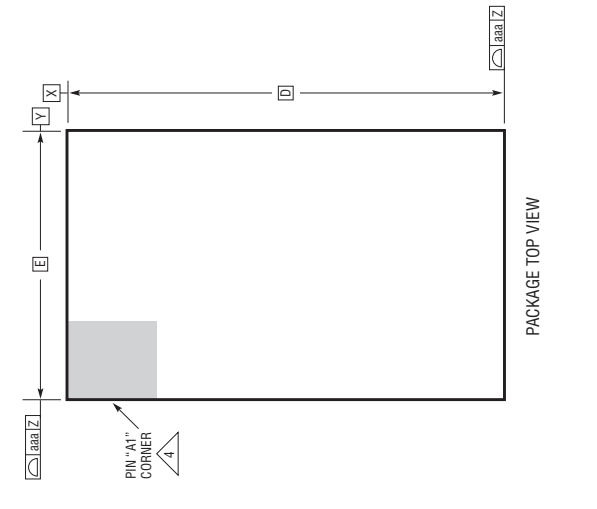


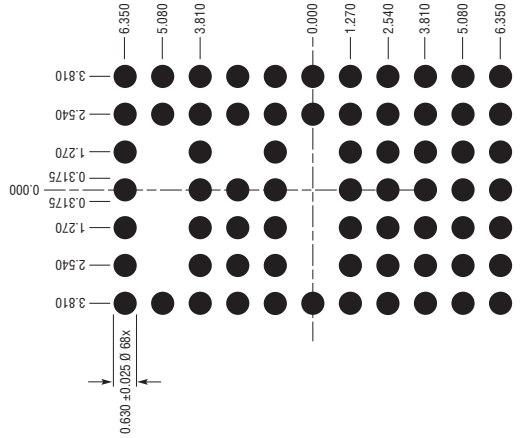

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. ALL DIMENSIONS ARE IN MILLIMETERS
3. BALL DESIGNATION PER JESD MS-028 AND JEP95
4. DETAILS OF PIN #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PIN #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE
5. PRIMARY DATUM -Z- IS SEATING PLANE
6. SOLDER BALL COMPOSITION CAN BE 96.5% Sn/3.0% Ag/0.5% Cu OR Sn Pb EUTECTIC
7. PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY




| DIMENSIONS | | | | |
|---|---|---|---|---|
| SYMBOL | MIN | NOM | MAX | NOTES |
| A | 4.72 | 4.92 | 5.12 | |
| A1 | 0.50 | 0.60 | 0.70 | |
| A2 | 4.22 | 4.32 | 4.42 | |
| b | 0.60 | 0.75 | 0.90 | |
| b1 | 0.60 | 0.63 | 0.66 | |
| D | | 15.00 | | |
| E | | 9.00 | | |
| e | | 1.27 | | |
| F | | 12.70 | | |
| G | | 7.62 | | |
| H1 | 0.27 | 0.32 | 0.37 | |
| H2 | 3.95 | 4.00 | 4.05 | |
| aaa | | | 0.15 | |
| bbb | | | 0.10 | |
| ccc | | | 0.20 | |
| ddd | | | 0.30 | |
| eee | | | 0.15 | |
| TOTAL NUMBER OF BALLS: 68 | | | | |



# PACKAGE DESCRIPTION

**PACKAGE ROW AND COLUMN LABELING MAY VARY AMONG µModule PRODUCTS. REVIEW EACH PACKAGE LAYOUT CAREFULLY.**

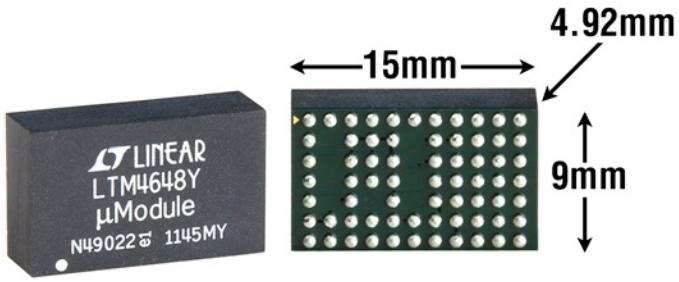
**LTM4648 Component BGA Pinout**

| PIN ID | FUNCTION | PIN ID | FUNCTION | PIN ID | FUNCTION | PIN ID | FUNCTION | PIN ID | FUNCTION | PIN ID | FUNCTION | PIN ID | FUNCTION |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A1 | GND | B1 | GND | C1 | $V_{IN}$ | D1 | $V_{IN}$ | E1 | GND | F1 | RUN | G1 | GND |
| A2 | GND | B2 | – | C2 | – | D2 | – | E2 | – | F2 | CLCKOUT | G2 | GND |
| A3 | GND | B3 | CLKIN | C3 | NC | D3 | $V_{IN}$ | E3 | FREQ | F3 | GND | G3 | GND |
| A4 | GND | B4 | PHMODE | C4 | NC | D4 | $V_{IN}$ | E4 | – | F4 | INTVCC | G4 | GND |
| A5 | GND | B5 | MODE | C5 | SW | D5 | $V_{IN}$ | E5 | TRACK/SS | F5 | GND | G5 | GND |
| A6 | TEMP | B6 | – | C6 | – | D6 | – | E6 | – | F6 | COMP | G6 | GND |
| A7 | GND | B7 | NC | C7 | PGOOD | D7 | $V_{IN}$ | E7 | FB | F7 | DIFFN | G7 | GND |
| A8 | GND | B8 | NC | C8 | $V_{IN}$ | D8 | $V_{IN}$ | E8 | $V_{IN}$ | F8 | DIFFP | G8 | DIFFOUT |
| A9 | GND | B9 | GND | C9 | $V_{IN}$ | D9 | $V_{IN}$ | E9 | $V_{OUT}$ | F9 | $V_{OUT}$ | G9 | $V_{OUT\_LCL}$ |
| A10 | GND | B10 | GND | C10 | $V_{OUT}$ | D10 | $V_{OUT}$ | E10 | $V_{OUT}$ | F10 | $V_{OUT}$ | G10 | $V_{OUT}$ |
| A11 | GND | B11 | GND | C11 | $V_{OUT}$ | D11 | $V_{OUT}$ | E11 | $V_{OUT}$ | F11 | $V_{OUT}$ | G11 | $V_{OUT}$ |

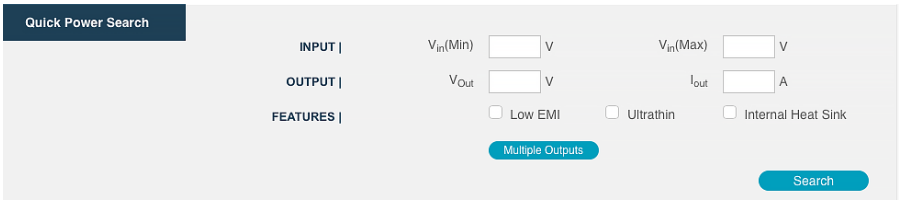
# REVISION HISTORY

| REV | DATE | DESCRIPTION | PAGE NUMBER |
|---|---|---|---|
| A | 6/18 | Added module line for LTM4648IY<br>Added Pin 1 mark on POD<br>Added SnPB as an option description<br>Added SnPB as an option in the Ordering Information | 2<br>2<br>1<br>2 |

## TYPICAL APPLICATION




## DESIGN RESOURCES

| SUBJECT | DESCRIPTION | |
|---|---|---|
| µModule Design and Manufacturing Resources | Design:<br>• Selector Guides<br>• Demo Boards and Gerber Files<br>• Free Simulation Tools | Manufacturing:<br>• Quick Start Guide<br>• PCB Design, Assembly and Manufacturing Guidelines<br>• Package and Board Level Reliability |
| µModule Regulator Products Search | 1. Sort table of products by parameters and download the result as a spread sheet.<br>2. Search using the Quick Power Search parametric table.<br>  | |
| Digital Power System Management | Analog Devices' family of digital power supply management ICs are highly integrated solutions that offer essential functions, including power supply monitoring, supervision, margining and sequencing, and feature EEPROM for storing user configurations and fault logging. | |



## RELATED PARTS

| PART NUMBER | DESCRIPTION | COMMENTS |
|---|---|---|
| LTM4627 | 20V, 15A Step-Down µModule Regulator | $4.5V \le V_{IN} \le 20V$, $0.6V \le V_{OUT} \le 5V$, PLL input, Remote Sense Amplifier, $V_{OUT}$ Tracking, 15mm × 15mm × 4.3mm LGA and 15mm × 15mm × 4.9mm BGA |
| LTM4620A | Dual 16V, 13A or Single 26A Step-Down µModule Regulator | $4.5V \le V_{IN} \le 16V$, $0.6V \le V_{OUT} \le 5.3V$, PLL Input, Remote Sense Amplifier, $V_{OUT}$ Tracking, 15mm × 15mm × 4.41mm LGA |
| LTM4613 | $36V_{IN}$, 8A EN55022 Class B Certified DC/DC Step-Down µModule Regulator | $5V \le V_{IN} \le 36V$, $3.3V \le V_{OUT} \le 15V$, PLL Input, $V_{OUT}$ Tracking and Margining, 15mm × 15mm × 4.32mm LGA |
| LTM4608A | Low $V_{IN}$, 8A Step-Down µModule | $2.7V \le V_{IN} \le 5.5V$, $0.6V \le V_{OUT} \le 5V$, $V_{OUT}$ Tracking, CLKIN 9mm × 15mm × 2.82mm LGA |
| LTM4649 | 16V, 10A Step-Down µModule Regulator | $4.5V \le V_{IN} \le 16V$, $0.6V \le V_{OUT} \le 3.3V$, PLL Input, Remote Sense Amplifier, $V_{OUT}$ Tracking, 9mm × 15mm × 4.92mm BGA |
| LTC2974 | Quad Digital Power Supply Manager with EEPROM | $I^2C$/PMBus Interface, Configuration EEPROM, Fault Logging, Per Channel Voltage, Current and Temperature Measurements |