LND150/LND250

N-Channel Depletion-Mode DMOS FETs

Features

- Free from Secondary Breakdown
- Low-Power Drive Requirement
- Ease of Paralleling
- Excellent Thermal Stability
- Integral Source-Drain Diode
- High Input Impedance and Low C_{ISS}
- ESD Gate Protection

Applications

- Solid-State Relays
- Normally-On Switches
- Converters
- Power Supply Circuits
- Constant-Current Sources
- Input Protection Circuits

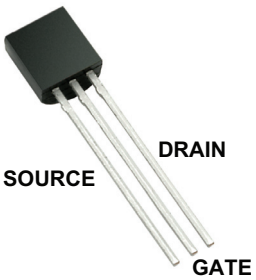
General Description

The LND150 and LND250 are high-voltage N-channel Depletion-mode (normally-on) transistors utilizing lateral DMOS technology. The gate is ESD protected.

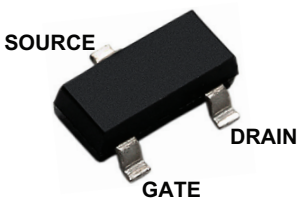
The LND150/LND250 are ideal for high-voltage applications, such as normally-on switches, precision constant-current sources, voltage-ramp generation and amplification.

Package Types

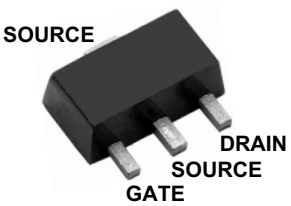
3-lead TO-92
(Top view)



3-lead SOT-23
(Top view)



3-lead SOT-89
(Top view)



See Table 3-1, Table 3-2 and Table 3-3 for pin information.

1.0 ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS†

Drain-to-Source Voltage ..... BV_{DSX}
Drain-to-Gate Voltage ..... BV_{DGX}
Gate-to-Source Voltage ..... ±20V
Operating Ambient Temperature, T_A ..... –55°C to 150°C
Storage Temperature, T_S ..... –55°C to 150°C

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. All DC parameters are 100% tested at 25°C unless otherwise stated. Pulse test: 300 µs pulse, 2% duty cycle

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Drain-to-Source Breakdown Voltage	BV_{DSX}	500	—	—	V	V_{GS} = –10V, I_D = 1 mA
Gate-to-Source Off Voltage	$V_{GS(OFF)}$	–1	—	–3	V	V_{GS} = 25V, I_D = 100 nA
Change in $V_{GS(OFF)}$ with Temperature	$\Delta V_{GS(OFF)}$	—	—	5	mV/°C	V_{GS} = 25V, I_D = 100 nA (**Note 1**)
Gate Body Leakage Current	I_{GSS}	—	—	100	nA	V_{GS} = ±20V, V_{DS} = 0V
Drain-to-Source Leakage Current	$I_{D(OFF)}$	—	—	100	nA	V_{GS} = –10V, V_{DS} = 450V
		—	—	100	µA	V_{DS} = 0.8V Maximum rating, V_{GS} = –10V, T_A= 125°C (**Note 1**)
Saturated Drain-to-Source Current	I_{DSS}	1	—	3	mA	V_{GS} = 0V, V_{DS} = 25V
Static Drain-to-Source On-State Resistance	$R_{DS(ON)}$	—	850	1000	Ω	V_{GS} = 0V, I_D = 0.5 mA
Change in $R_{DS(ON)}$ with Temperature	$\Delta R_{DS(ON)}$	—	—	1.2	%/°C	V_{GS} = 0V, I_D = 0.5 mA (**Note 1**)

Note 1: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: T_A = 25°C unless otherwise specified. Specification is obtained by characterization and is not 100% tested.

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
Forward Transconductance	G_{FS}	1	2	—	mmho	V_{DS} = 0V, I_D = 1 mA
Input Capacitance	C_{ISS}	—	7.5	10	pF	V_{GS} = –10V, V_{DS} = 25V, f = 1 MHz
Common Source Output Capacitance	C_{OSS}	—	2	3.5	pF	
Reverse Transfer Capacitance	C_{RSS}	—	0.5	1	pF	
Turn-On Delay Time	$t_{d(ON)}$	—	0.09	—	ns	V_{DD} = 25V, I_D = 1 mA, R_{GEN} = 25Ω
Rise Time	t_r	—	0.45	—	ns	
Turn-Off Delay Time	$t_{d(OFF)}$	—	0.1	—	ns	
Fall Time	t_f	—	1.3	—	ns	
DIODE PARAMETER						
Diode Forward Voltage Drop	V_{SD}	—	—	0.9	V	V_{GS} = –10V, I_{SD} = 1 mA (**Note 1**)
Reverse Recovery Time	t_{rr}	—	200	—	ns	V_{GS} = –10V, I_{SD} = 1 mA

Note 1: Unless otherwise stated, all DC parameters are 100% tested at +25°C. Pulse test: 300 µs pulse, 2% duty cycle.

TEMPERATURE SPECIFICATIONS

Parameter	Sym.	Min.	Typ.	Max.	Unit	Conditions
TEMPERATURE RANGE						
Operating Ambient Temperature	T_A	–55	—	+150	°C	
Storage Temperature	T_S	–55	—	+150	°C	
PACKAGE THERMAL RESISTANCE						
3-lead TO-92	θ_{JA}	—	132	—	°C/W	
3-lead SOT-23	θ_{JA}	—	203	—	°C/W	
3-lead SOT-89	θ_{JA}	—	133	—	°C/W	

THERMAL CHARACTERISTICS

Package	I_D (**Note 1**) (Continuous) (mA)	I_D (Pulsed) (A)	Power Dissipation at T_A = 25°C (W)	I_{DR} (mA)	I_{DRM} (**Note 1**) (A)
3-lead TO-92	30	30	0.74	30	30
3-lead SOT-23	13	30	0.36	13	30
3-lead SOT-89	30	30	1.6 (**Note 2**)	30	30

Note 1: I_D (continuous) is limited by maximum rated T_J.

2: T_A = 25°C. Mounted on an FR4 Board, 25 mm x 25 mm x 1.57 mm.

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

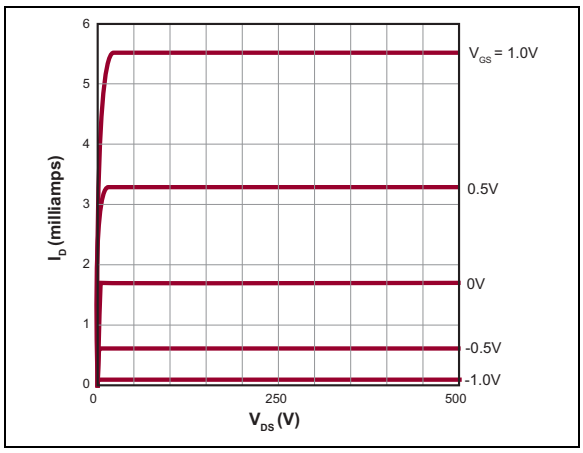


FIGURE 2-1: *Output Characteristics.*

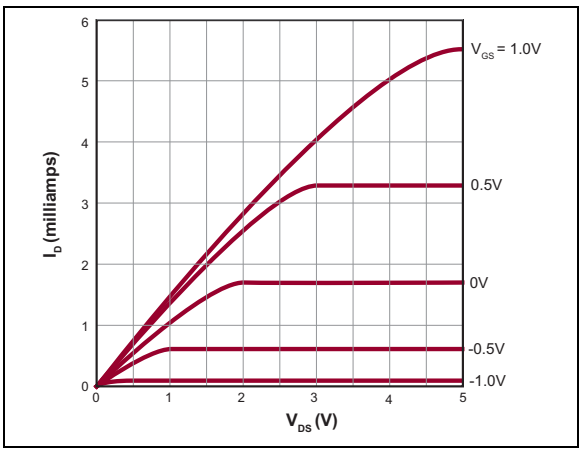


FIGURE 2-4: *Saturation Characteristics.*

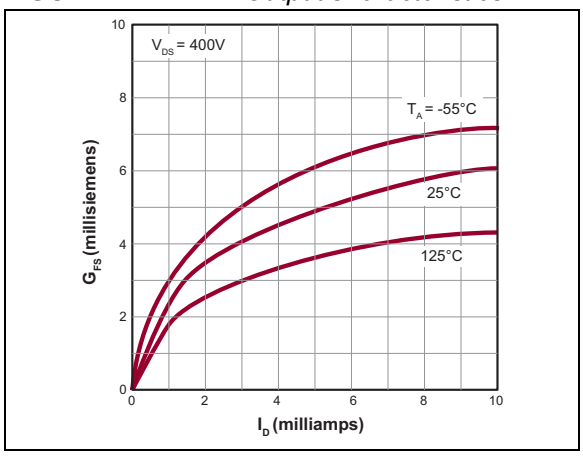


FIGURE 2-2: *Transconductance vs. Drain Current.*

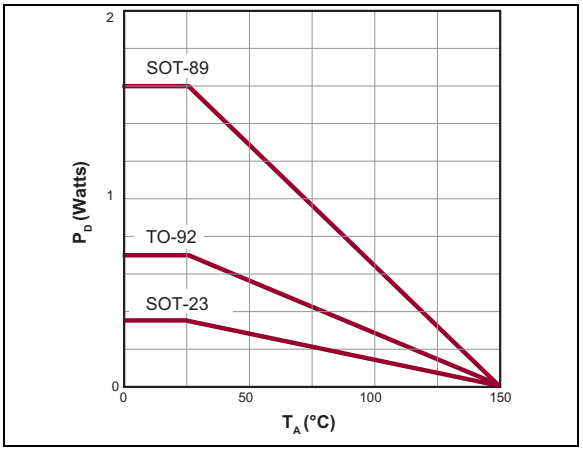


FIGURE 2-5: *Power Dissipation vs. Ambient Temperature.*

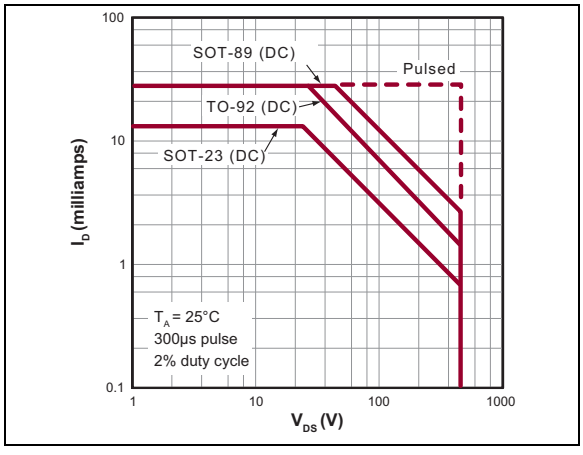


FIGURE 2-3: *Maximum Rated Safe Operating Area.*

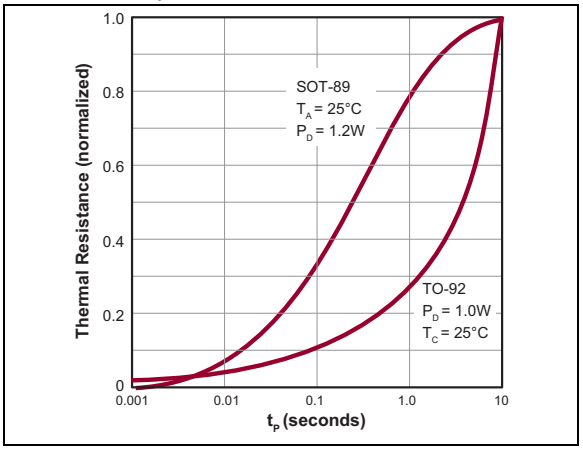


FIGURE 2-6: *Thermal Response Characteristics.*

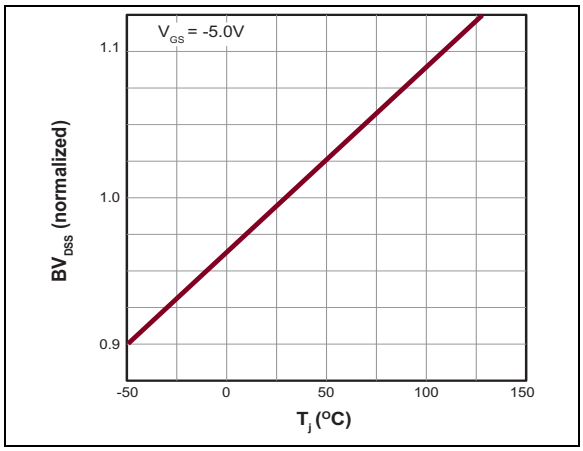


FIGURE 2-7: *BV_{DSS} Variation with Temperature.*

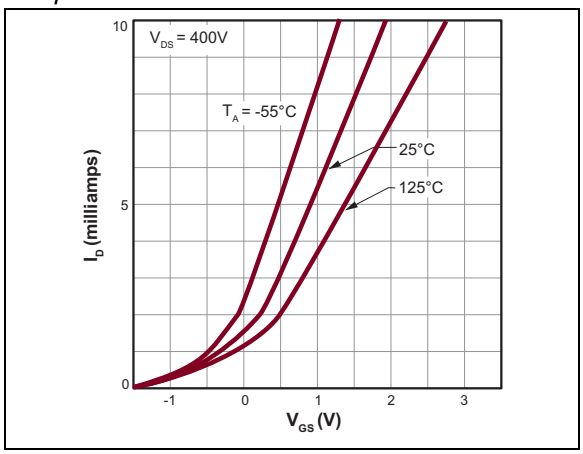


FIGURE 2-8: *Transfer Characteristics.*

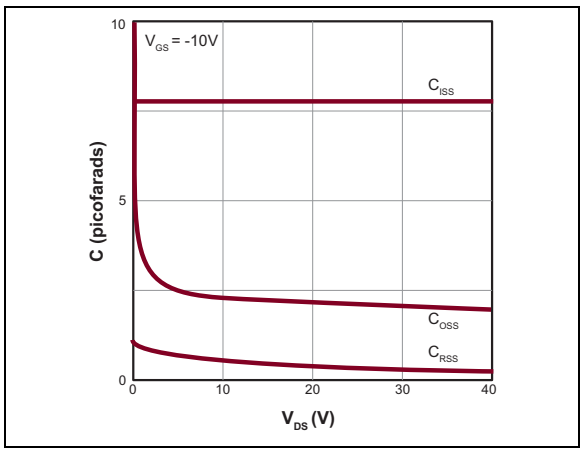


FIGURE 2-9: *Capacitance vs. Drain-to-Source Voltage.*

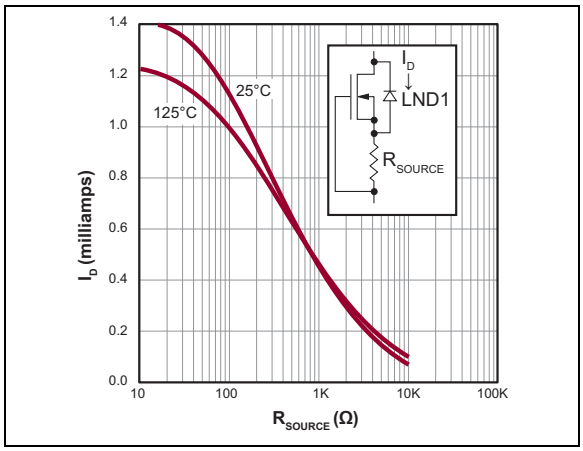


FIGURE 2-10: *Drain Current vs. R_{SOURCE}.*

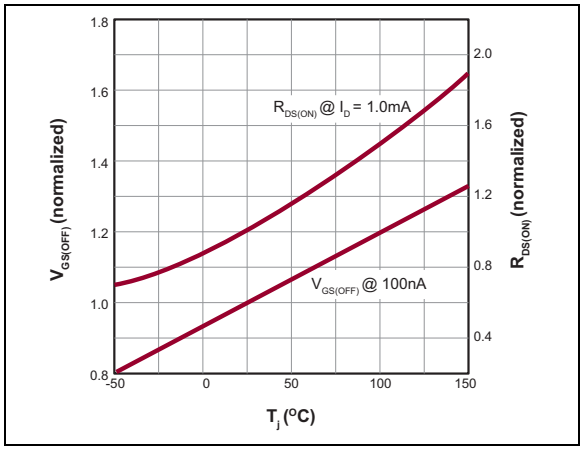


FIGURE 2-11: *$V_{GS(OFF)}$ and R_{DS} Variation with Temperature.*

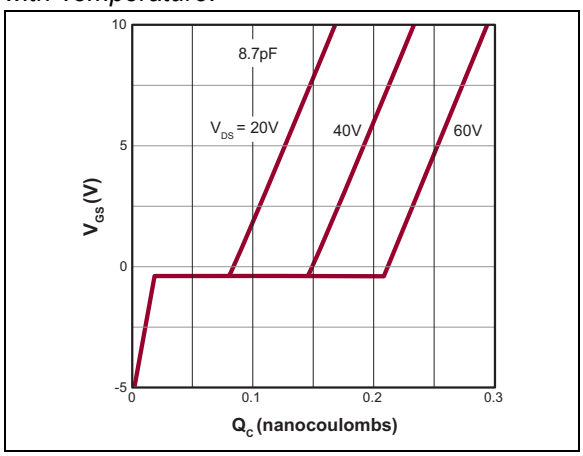


FIGURE 2-12: *Gate Drive Dynamic Characteristics.*

3.0 PIN DESCRIPTION

The details on the pins of LND150/LND250 are listed on Table 3-1, Table 3-2 and Table 3-3. Refer to **Package Types** for the location of pins.

TABLE 3-1: TO-92 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	SOURCE	SOURCE
2	GATE	GATE
3	DRAIN	DRAIN

TABLE 3-2: SOT-23 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	GATE	GATE
2	DRAIN	DRAIN
3	SOURCE	SOURCE

TABLE 3-3: SOT-89 PIN FUNCTION TABLE

Pin Number	Pin Name	Description
1	GATE	GATE
2, 4	SOURCE	SOURCE
3	DRAIN	DRAIN

4.0 FUNCTIONAL DESCRIPTION

Figure 4-1 illustrates the switching waveforms and test circuit for LND150/LND250.

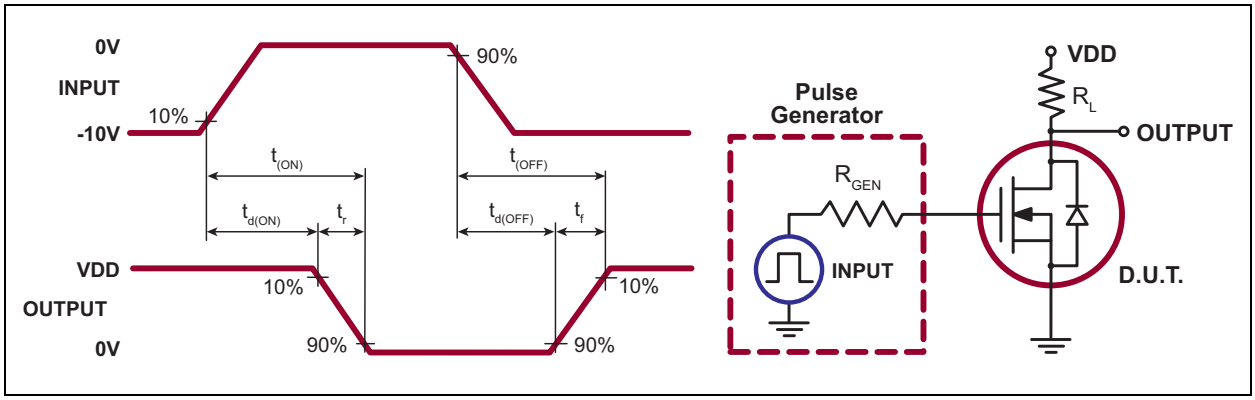


FIGURE 4-1: *Switching Waveforms and Test Circuit.*

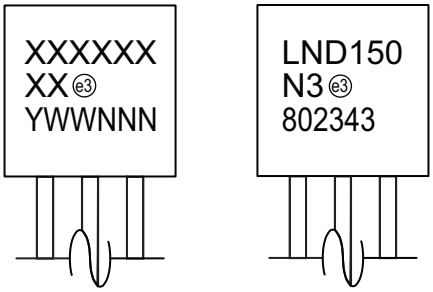
TABLE 4-1: PRODUCT SUMMARY

BV_{DSX}/BV_{DGX} (V)	$R_{DS(ON)}$ (Maximum) (Ω)	$I_{DSS(ON)}$ (Minimum) (mA)
500	1000	1

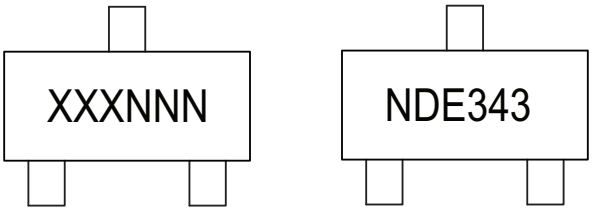
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

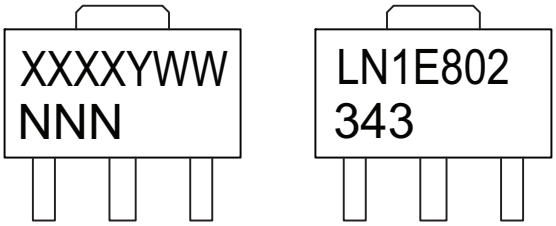
3-lead TO-92 Example



3-lead SOT-23 Example



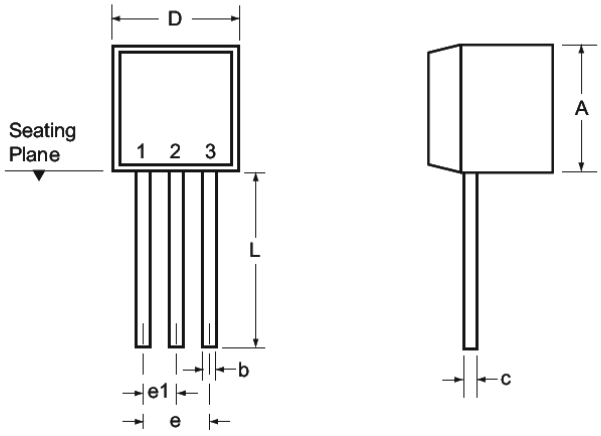
3-lead SOT-89 Example

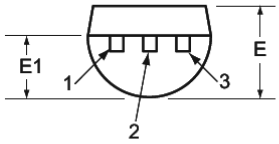


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

3-Lead TO-92 Package Outline (L/LL/N3)





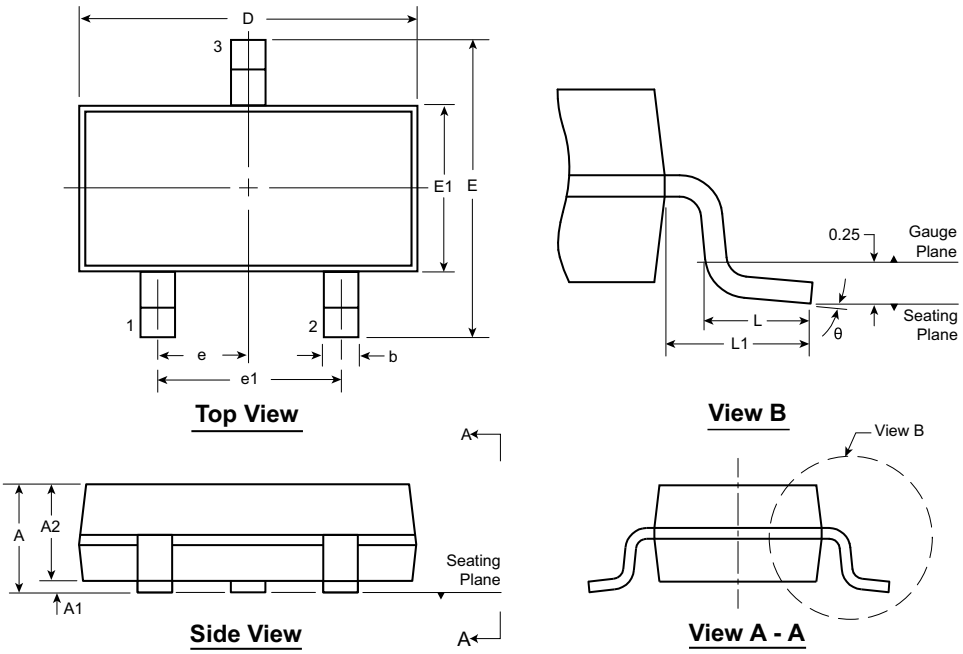
Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	c	D	E	E1	e	e1	L
Dimensions (inches)	MIN	.170	.014†	.014†	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022†	.022†	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.
** This dimension is not specified in the JEDEC drawing.*
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

3-Lead TO-236AB (SOT-23) Package Outline (K1/T)

2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch

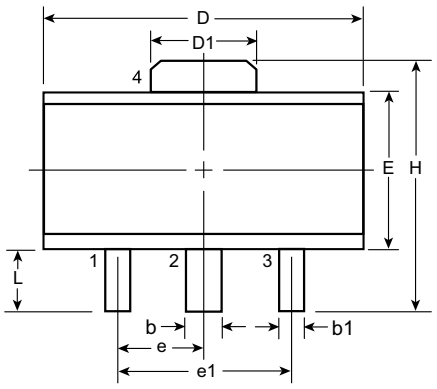


Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

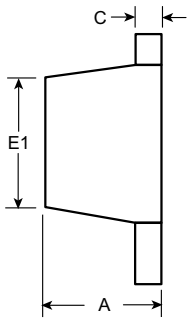
Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	θ
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20†	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.
† This dimension differs from the JEDEC drawing.
Drawings not to scale.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Top View



Side View

Note: For the most current package drawings, see the Microchip Packaging Specification at www.microchip.com/packaging.

Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00†	1.50 BSC	3.00 BSC	3.94	0.73†
	NOM	-	-	-	-	-	-	-	-			-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.
† This dimension differs from the JEDEC drawing
***Drawings not to scale**.*

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (August 2018)

- Converted and merged Supertex Doc#s DSFP-LND150 and DSFP-LND250 to Microchip DS20005454
- Changed the package marking format
- Removed the TO-92 N3 P005 media type
- Added some sections to comply with the standard Microchip Technology Inc. documentation format
- Made minor text changes throughout the document

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	XX	-	X	-	X
Device	Package Options		Environmental		Media Type

Devices:	LND150	= N-Channel Depletion-Mode DMOS FET
	LND250	= N-Channel Depletion-Mode DMOS FET
Packages:	N3	= 3-lead TO-92
	K1	= 3-lead SOT-23
	N8	= 3-lead SOT-89
Environmental:	G	= Lead (Pb)-free/ROHS-compliant package
Media Types:	(blank)	= 1000/Bag for an N3 package = 3000/Reel for a K1 package = 2000/Reel for an N8 package
	P002	= 2000/Reel for an N3 package
	P003	= 2000/Reel for an N3 package
	P013	= 2000/AMMO Pack for an N3 package
	P014	= 2000/AMMO Pack for an N3 package

Note: LND250 is only offered in 3-lead SOT-23 package.

Examples:

a) LND150N3-G:	N-Channel Depletion-Mode DMOS FET, 3-lead TO-92, 1000/Bag
b) LND150K1-G:	N-Channel Depletion-Mode DMOS FET, 3-lead SOT-23, 3000/Reel
c) LND150N8-G:	N-Channel Depletion-Mode DMOS FET, 3-lead TO-92, 2000/Reel
d) LND150N3-G-P002:	N-Channel Depletion-Mode DMOS FET, 3-lead TO-92, 2000/Reel

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
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- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

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Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.

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