

AN-2175 LM21305 POL Demonstration Module and Reference Design

1 Introduction

This LM21305 synchronous buck switching regulator board-mounted module is a complete, easy-to-use DC-DC point-of-load (POL) solution capable of driving up to 5A of load current with excellent conversion efficiency, output voltage accuracy, load and line regulation. The POL module can accept an input voltage between 3V and 18V and deliver an adjustable and accurate output voltage as low as 0.598V. The module has been designed to balance overall solution size with regulator efficiency while showcasing high current density. The power stage has been optimized for an input voltage of 12V and a switching frequency of 500 kHz. While the output voltage setpoint is nominally 1.8V, it can be easily re-defined by modifying one of the feedback resistors. Moreover, by attaching a resistor between the TRIM pin and GND or VOUT, the output voltage can be adjusted up or down, respectively. For fast load transient response and stable operation over the entire input voltage range, the compensation of the current-mode control loop has been designed to provide a loop bandwidth of 50 kHz and phase margin of 60°. The Enable (EN) and Power Good (PGOOD) pins can be applied to easily configure the LM21305 in power systems architected with multiple voltage rails and explicit sequencing requirements.

2 POL Module Features

- Output current range of 0A to 5A
- Input voltage range of 3V to 18V (no external bias supply required)
- All ceramic capacitor design
- Programmable input under-voltage lock-out (UVLO) via precision enable
- Default output voltage of 1.8V. For other VOUT setpoints, see [Table 2](#). VOUT can also be adjusted using a resistor connected to the module's TRIM pin
- 90% efficiency at 3.3V/5A, 85% efficiency at 1.8V/5A
- Fixed switching frequency for predictable EMI characteristic and easy filtering
- 500 kHz default switching frequency; adjusted using the SYNC pin
- Optional AVIN external bias input if system level 5V is available

3 POL Module Package Highlights

- 0.9" x 0.7" (22.8 mm x 17.8 mm) reduced size form factor
- 0.04" diameter pins (with intrinsic standoffs) for PVIN, VOUT, GND, TRIM, SYNC, EN, PGOOD, and AVIN
- 4 layer construction standard FR4 laminate PCB
- Top and bottom PCBs layers and the two inner layers are all 2oz/ft² (70 µm) copper weight
- 62 mil (0.062", 1.6 mm) overall PCB thickness

4 LM21305 Regulator IC Features

- Integrated, low $R_{DS(on)}$, low Q_G high- and low-side power MOSFETs (44 m Ω and 22 m Ω , respectively)
- Optimized MOSFET gate drivers enable low switch deadtimes for efficient high frequency operation
- True monotonic startup into pre-biased loads
- $\pm 1.6\%$ feedback (FB) voltage accuracy over full junction temperature range $T_J = -40^\circ\text{C}$ to 125°C
- Peak current-mode control with cycle-by-cycle current limiting
- Output power good flag
- Resistor adjustable switching frequency from 300 kHz to 1.5 MHz
- Frequency synchronization
- Diode emulation mode at light loads
- Precision enable with hysteresis
- Output over-voltage protection (OVP)
- 5 mm x 5 mm WQFN-28 package with an exposed die attach pad (DAP)

5 POL Module Design Concept

This POL module has been designed to mount on a system motherboard as close as possible to the point-of-load. While it can operate on a standalone basis for bench measurements and the like, the module has demonstrably improved thermal characteristics when solder connected into a motherboard. Most of the conductive heat transfer associated with the module's thermal dissipation is achieved through its VIN, VOUT and GND connection terminals. Leveraging the copper polygons and planes that are typically available in the motherboard PCB stack-up, the module effective thermal impedance and, hence, the LM21305 regulator IC junction temperature rise are reduced. Note that if the module is operated as a standalone entity, adequate airflow should be available to mitigate excessive temperature rise. Furthermore, extra passive components to facilitate additional functionality can be located on the motherboard, for example, TRIM resistors to margin or adjust VOUT, any components tied to EN or PGOOD for particular startup sequencing or delay requirements, and so forth. Additional input and output filter capacitors can also be connected, if required. The power and signal terminal pins of the module are manufactured by Mill-Max. The pin employed has 0.04" (1 mm) diameter and the recommended motherboard PCB hole to accommodate such a pin is 0.043" (1.1 mm) diameter. The standoff inherent in the pin design dictates that the bottom of the module PCB will be 0.17" (4.3 mm) above the top of the motherboard, providing adequate clearance for airflow to the bottom side components.

6 Additional Component Footprints

A component footprint on the module is provided for a bootstrap diode in SOD523 package. The LM21305 has an internal boot diode. At low input voltages, however, it may be advantageous to connect an external Schottky diode to maximize the available gate drive voltage for the integrated high-side MOSFET.

7 Typical Applications

- POL conversions from 3.3V, 5V and 12V intermediate bus rails.
- Communications infrastructure, for example, optical networking, data centers, servers, base stations, storage systems
- Space constrained applications, industrial controls and factory automation
- Radio, medical, test, and data acquisition systems (where the switching frequency is tuned to avoid interference with other circuitry)

10 Module Circuit Schematic

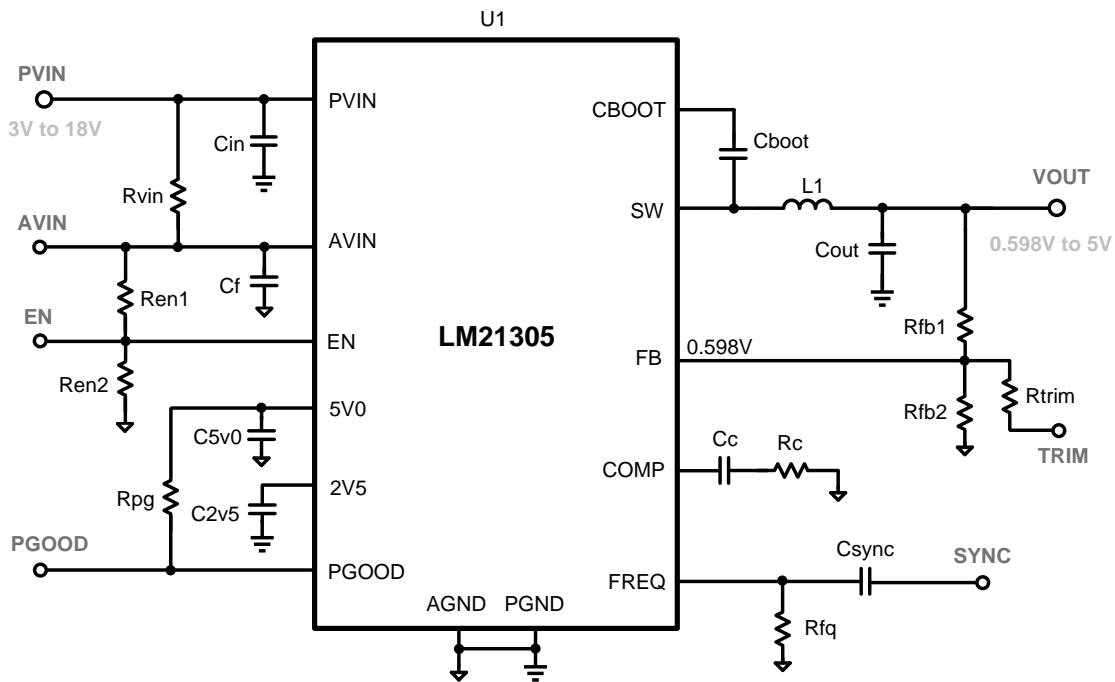


Figure 3. LM21305 POL Module Schematic

11 Bill of Materials (BOM)

Table 1. Bill of Materials (BOM) for LM21305 POL Module, $V_{IN} = 3V$ to $18V$, $V_{OUT} = 1.8V$

Quantity	Reference Designator	Description	Manufacturer	Manufacturer Part Number
1	PCB1	Printed Circuit Board		
3	C2v5, Cboot, Cf	CAP, CERM, 0.1 μ F, 25V, \pm 5%, X7R, 0603	AVX	06033C104JAT2A
1	C5v0	CAP, CERM, 1 μ F, 10V, \pm 10%, X5R, 0603	AVX	0603ZD105KAT2A
1	Cc	CAP, CERM, 4700 pF, 50V, \pm 10%, X7R, 0603	AVX	06035C472KAT2A
1	Cin	CAP, CERM, 22 μ F, 25V, \pm 10%, X5R, 1210	TDK	C3225X5R1E226M
1	Cout	CAP, CERM, 100 μ F, 6.3V, \pm 20%, X5R, 1210	MuRata	GRM32ER60J107ME20L
1	Csync	CAP, CERM, 100 pF, 16V, \pm 10%, X7R, 0603	AVX	0603YC101KAT2A
0	Dboot	N/A	Infineon	BAT64-02W
8	VIN, VOUT, GND, TRIM, SYNC, EN, PGOOD, AVIN	Circuit pin prntd 0.170", 0.082"	Mill-Max	3125-2-00-34-00-00-08-0
1	L1	Inductor, 1.5 μ H, 11A, 9.7 m Ω , SMD	TDK	SPM6530T-1R5M100
1	Rc	RES, 3.3 k Ω , 1%, 0.1W, 0603	Vishay-Dale	CRCW06033K30FKEA
1	Ren1	RES, 27.4 k Ω , 1%, 0.1W, 0603	Vishay-Dale	CRCW060327K4FKEA
2	Ren2, Rfq	RES, 100 k Ω , 1%, 0.1W, 0603	Vishay-Dale	CRCW0603100KFKEA
2	Rfb1, Rtrim	RES, 20.0 k Ω , 1%, 0.1W, 0603	Vishay-Dale	CRCW060320K0FKEA
2	Rfb2, Rpg	RES, 10.0 k Ω , 1%, 0.1W, 0603	Vishay-Dale	CRCW060310K0FKEA
1	Rvin	RES, 1 Ω , 1%, 0.1W, 0603	Vishay-Dale	CRCW06031R00FKEA
1	U1	LM21305 Buck Regulator IC, WQFN-28	Texas Instruments	LM21305

12 Adjusting the Output Voltage - Feedback Resistors

While the output voltage setpoint is nominally 1.8V, it can be easily changed by modifying one of the feedback resistors as shown in [Table 2](#).

Table 2. Output Voltage Setting (Rfb2 = 10 kΩ)

VOUT	Rfb1
5.0V	73.3 kΩ
3.3V	45.3 kΩ
2.5V	31.6 kΩ
1.8V	20 kΩ (default)
1.5V	15 kΩ
1.2V	10 kΩ
0.9V	5 kΩ
0.8V	3.4 kΩ
0.7V	1.7 kΩ
0.598V	0Ω

13 Adjusting the Output Voltage - Trim Functionality

The output voltage can also be adjusted above or below the nominal setpoint by attaching a resistor to the module's TRIM pin. The resistor between the LM21305's feedback (FB) node and the TRIM pin (R_{trim}) determines the output voltage adjustable range. To increase the output voltage, a resistor needs to be attached between the TRIM pin and GND (R_{trim_up} in [Figure 4](#)). Conversely, to decrease the output voltage, a resistor needs to be attached between the TRIM pin and the VOUT pin (R_{trim_down} in [Figure 4](#)).

A value of R_{trim} = 20 kΩ is recommended to adjust the output voltage from 1.2V to 2.4V (±33% of nominal) while retaining an acceptable control loop behavior. With R_{trim} = 20 kΩ, an output voltage of 2.4V can be achieved simply by shorting the TRIM pin to GND, and an output voltage of 1.2V can be achieved by shorting the TRIM pin to VOUT. Selecting R_{trim_down} = 40 kΩ gives an output voltage of 1.5V. To retain the nominal output voltage setpoint of 1.8V, the TRIM pin should be left open.

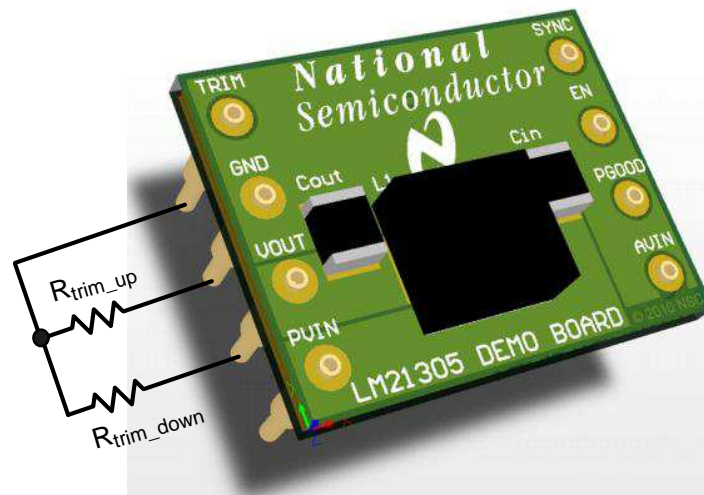


Figure 4. Output Voltage Trim and Adjustment

The resistor values required to trim the output voltage up or down are given, respectively, as follows:

$$R_{\text{trim_up}} = \frac{V_{\text{ref}}}{\frac{V_{\text{OUT}} - V_{\text{ref}}}{R_{\text{fb1}}} - \frac{V_{\text{ref}}}{R_{\text{fb2}}}} - R_{\text{trim}} \quad (1)$$

$$R_{\text{trim_down}} = \frac{V_{\text{OUT}} - V_{\text{ref}}}{\frac{V_{\text{ref}}}{R_{\text{fb2}}} - \frac{V_{\text{OUT}} - V_{\text{ref}}}{R_{\text{fb1}}}} - R_{\text{trim}} \quad (2)$$

Thus, given the resistor values from [Table 1](#), a nominal output voltage of 1.8V, $V_{\text{ref}} = 0.6\text{V}$, it follows that:

$$R_{\text{trim_up}} = \frac{120}{10(V_{\text{OUT}} - 0.598\text{V}) - 12} - 20 \quad (3)$$

$$R_{\text{trim_down}} = \frac{200(V_{\text{OUT}} - 0.598\text{V})}{12 - 10(V_{\text{OUT}} - 0.598\text{V})} - 20 \quad (4)$$

NOTE: Resistor values are in $\text{k}\Omega$ and V_{OUT} represents the desired output voltage. The accuracy of the output voltage adjustment is subject to the tolerances of the respective resistors. The resistor values for a desired output voltage can also be found using the curves provided in [Figure 5](#).

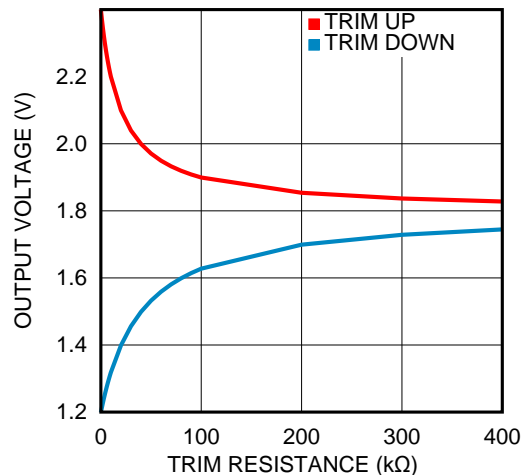


Figure 5. Trim Curve for Output Voltage Trim, Margining and Adjustment

14 Loop Compensation

Note that a change in output voltage directly affects the gain from V_{OUT} to the FB pin of the LM21305 and, hence, the overall loop gain. Loop gain is highest when the output voltage is trimmed down to its minimum. Operation at higher output voltage (with comparatively lower loop gain) may call for re-compensation of the control loop if optimal transient performance is desired. For example, the crossover frequency reduces to 40 kHz when the output voltage is trimmed to its maximum level of 2.4V. You are encouraged to avail of the LM21305 quick-start calculator to derive appropriate compensation components to maximize performance of the loop for a given output voltage.

15 Programmable UVLO With Hysteresis

There is a resistive divider implemented on the module that can be used to establish a precision UVLO level, this is currently set below the minimum input operating voltage so that the module turns on at $V_{\text{IN}} = 2.93\text{V}$ (typical). A common user change to this circuit is to adjust the values of R_{en1} and/or R_{en2} to vary the UVLO level to suit the target application. For calculation, see the *LM21305 5A Adjustable Frequency Synchronous Buck Regulator Data Sheet* ([SNVS639](#)). The EN pin can be pulled low to shutdown the module.

16 External Bias Supply

By removing resistor R_f , an external bias supply rail (5V) can be connected to the AVIN pin. This allows increased gate drive level at low input voltages and alleviates the LM21305 LDO bias supply power dissipation at high input voltages. Note that the LM21305 UVLO is referenced to the voltage at AVIN; to achieve a valid soft-start, PVIN should come up before AVIN.

17 Test Connections

The module should be connected to a power supply and load as portrayed in Figure 6. The relevant voltmeters and ammeters for measuring efficiency are also shown. A tip and barrel scope probe setup should be used to measure output voltage ripple and load transient response.

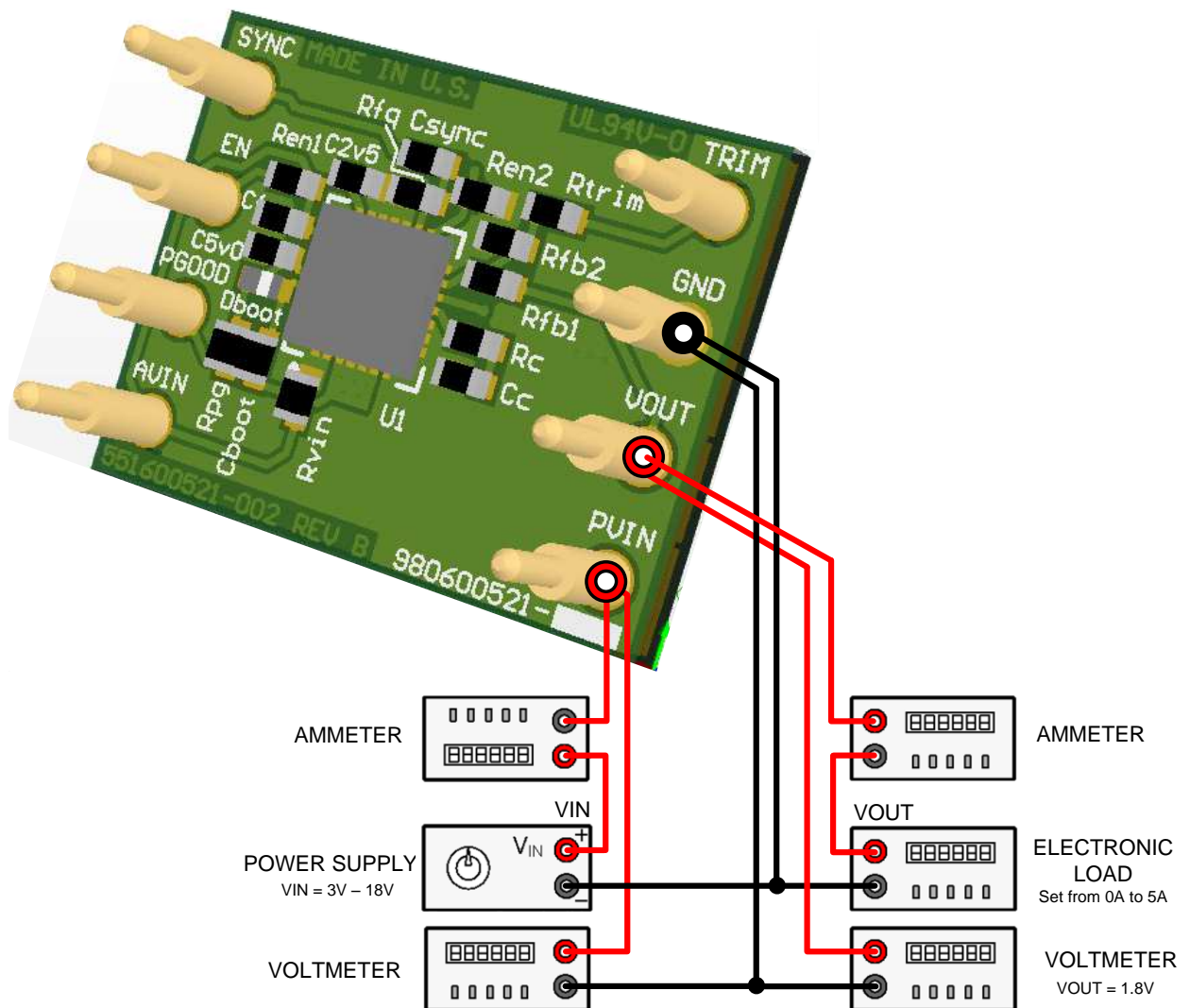
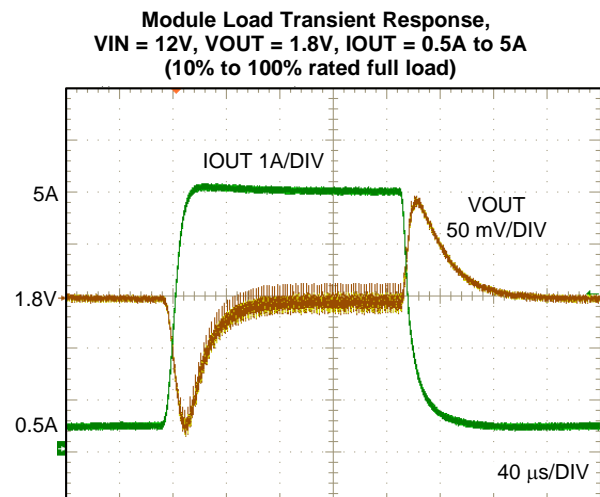
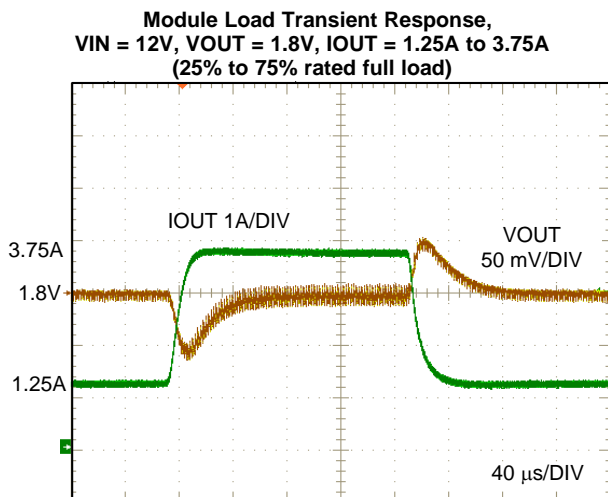
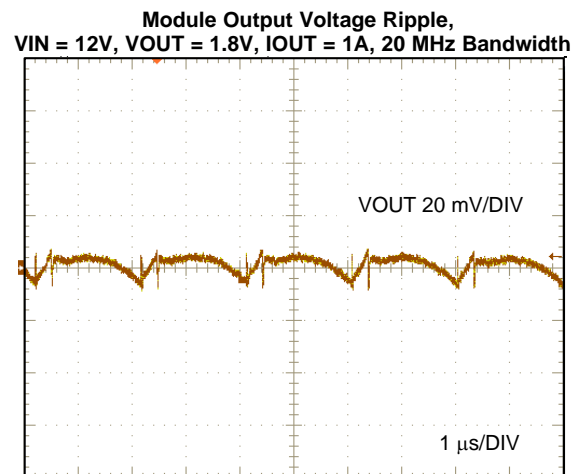
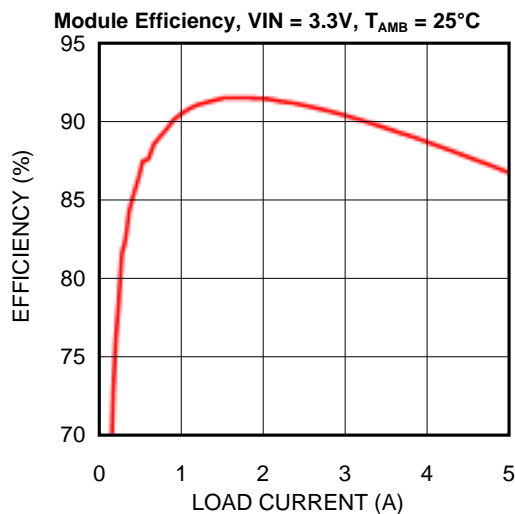
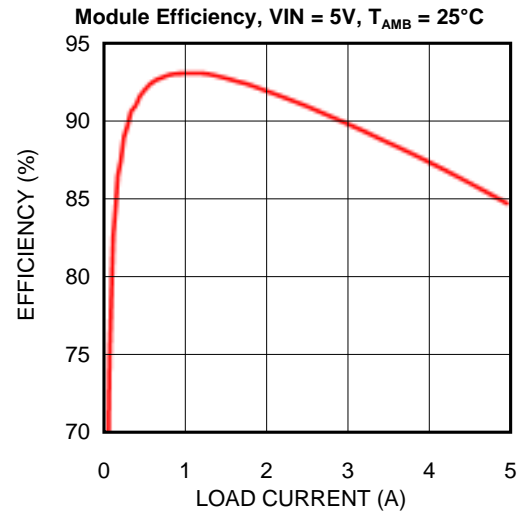
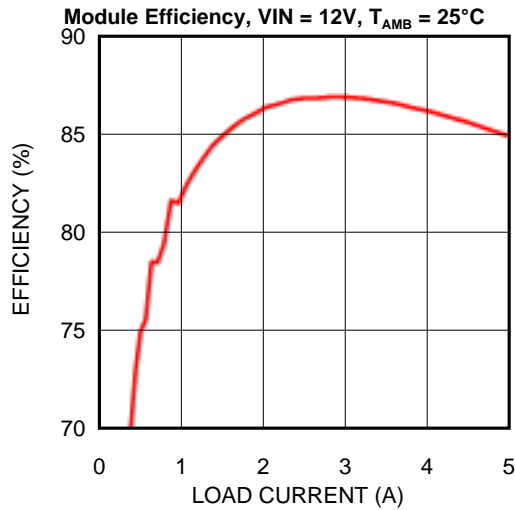
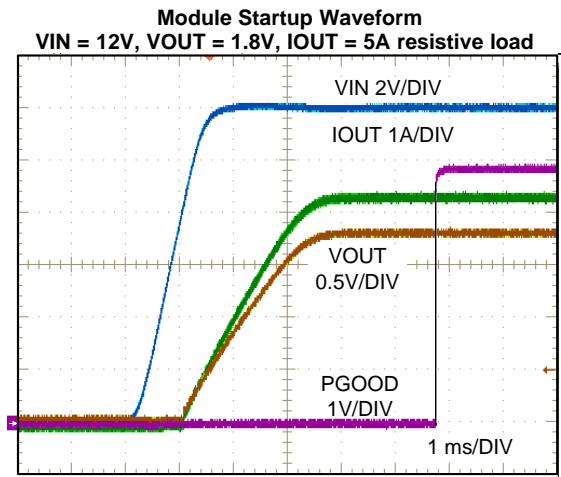
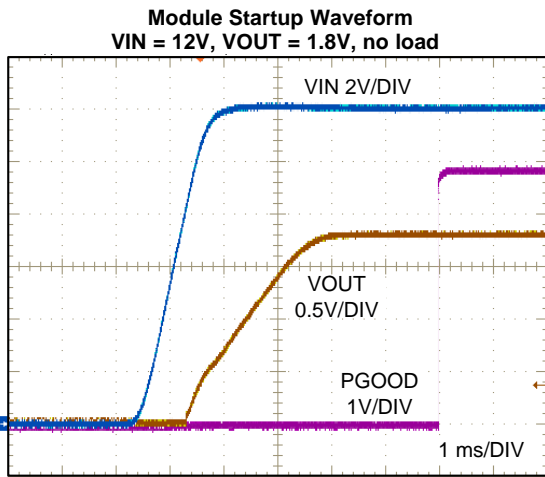


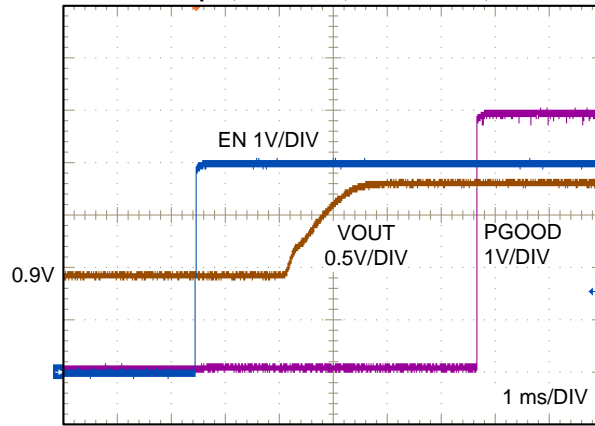
Figure 6. Module Efficiency Measurement Setup

18 Typical Performance Characteristics





Module Enable Waveform with 0.9V Pre-Biased Output, VIN = 12V, VOUT = 1.8V, no load



19 Module PCB View and Layout Diagrams

The associated gerber and CAD files can be downloaded from the LM21305 product folder.

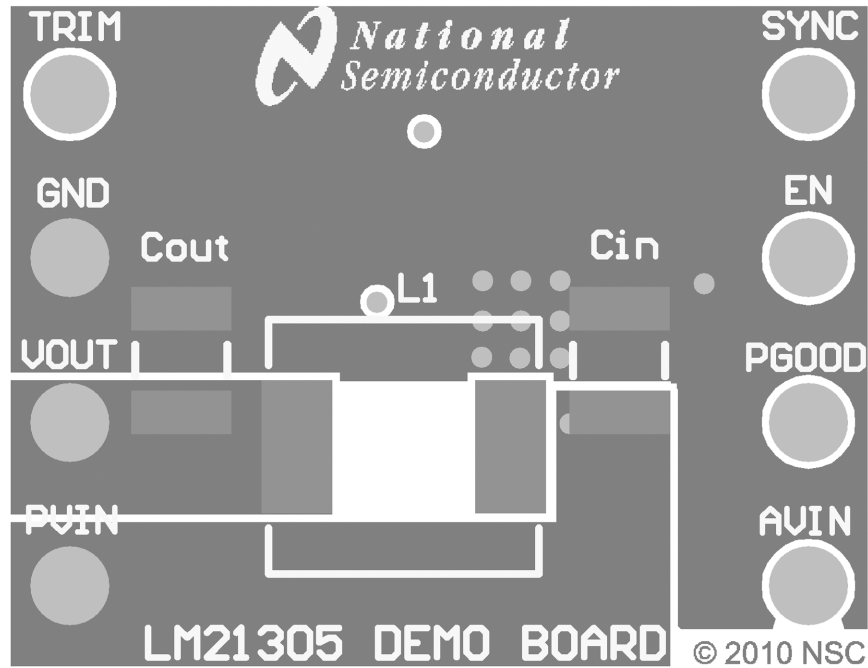


Figure 7. Top Layer and Assembly

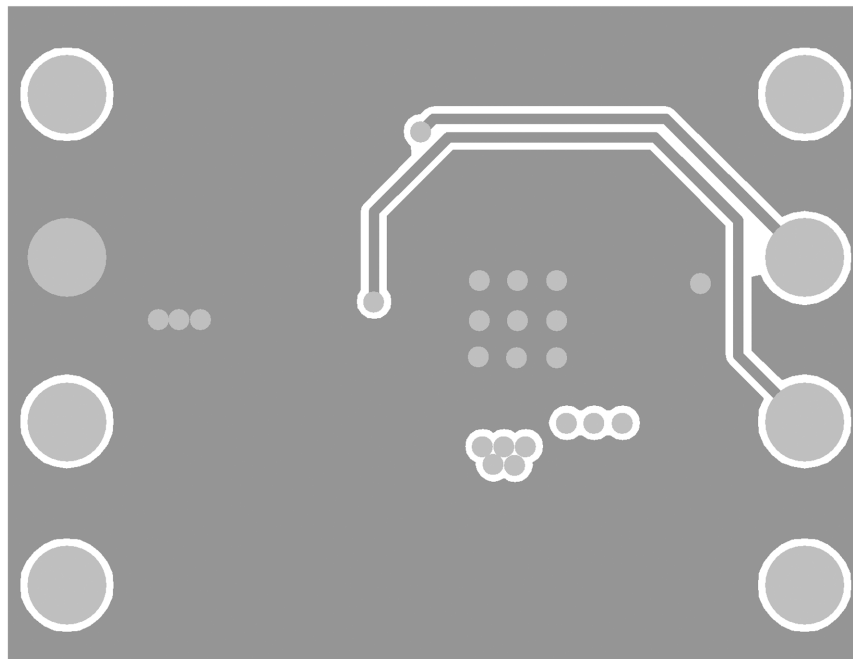


Figure 8. Internal Layer I (Ground)
Heat Sinking Layer

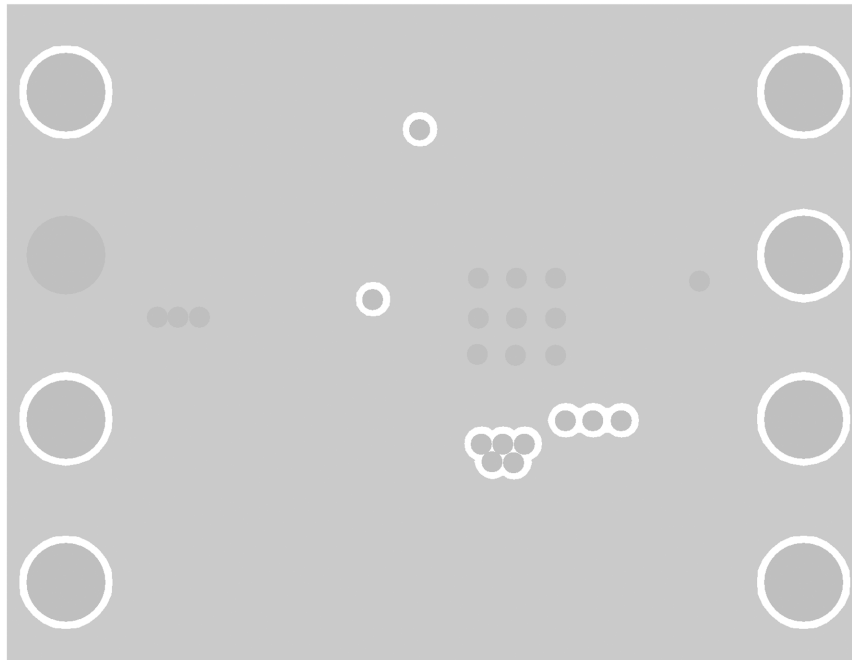


Figure 9. Internal Layer II (Ground) Heat Sinking Layer

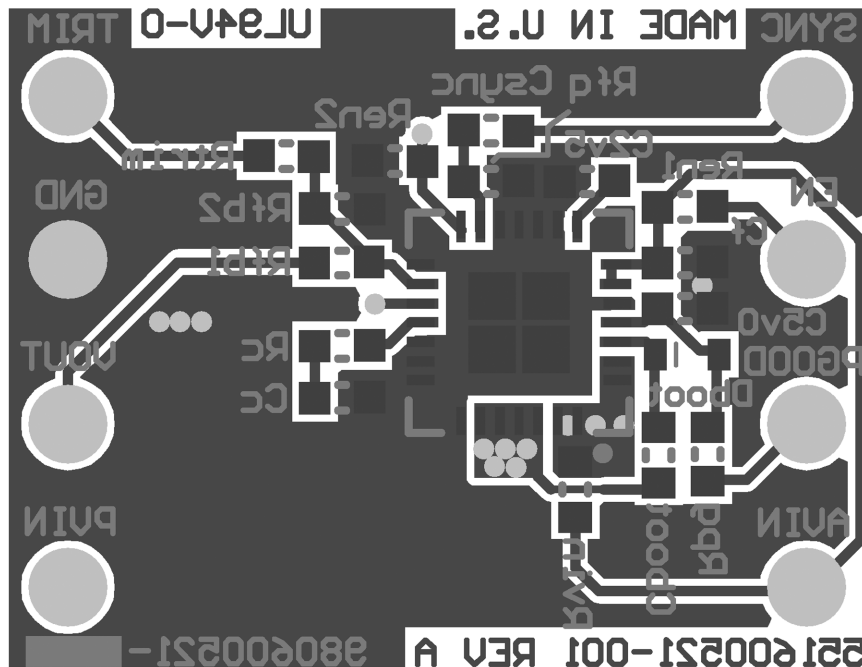


Figure 10. Bottom Layer and Assembly (viewed from top side)

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