AN-2080 LM10500 Evaluation Board

1 LM10500 Overview

The LM10500 is a 5 A Energy Management Unit (EMU) that actively reduces system level power consumption by utilizing a continuous, real-time, closed-loop Adaptive Voltage Scaling (AVS) scheme. The LM10500 operates cooperatively with PowerWise® AVS compatible ASICs, SoCs, and processors to optimize supply voltages adaptively over process and temperature variations. The device is controlled via PWI 1.0 or PWI 2.0 high-speed serial interface.

A typical power saving of 40% can be achieved when LM10500 is used with AVS compatible ASICs, SoCs, and processors.

2 Adaptive Voltage Scaling Technology

PowerWise Adaptive Voltage Scaling (AVS) technology is an advanced closed-loop technology for reducing active and standby energy consumption of digital processing engines and ASICs. Hardware Performance Monitor (HPM) is designed into the digital engine together with an Advanced Power Controller (APC) to monitor the performance of the silicon based on process and temperature variation. Information is fed back to an Energy Management Unit (EMU) which then sets the voltage precisely according to the processor's needs. The AVS technology enables optimum power delivery to the processors, ASICs, and SoCs, which maximizes overall system energy savings. AVS technology is process and architecture independent.

3 Features

- Closed-loop Adaptive Voltage Scaling (AVS)
- PWI 1.0 / PWI 2.0 compatible
- Resistor-programmable switching frequency
- Frequency synchronization
- Precision enable
- Internal soft-start to reduce in-rush current
- Power Good (PWROK)
- Under-Voltage Lock Out (UVLO)
- Over-Voltage Protection (OVP)
- Cycle-by-cycle current limiting (OCP)
- Thermal shutdown

4 Applications

- Point-of-Load Regulation
- Servers and Networking Cards
- Storage Devices
- Set-Top-Box Processors
- Medical and Industrial Processors

5 Evaluation Kit Overview

The LM10500 Evaluation Boards can operate standalone, communicate to a USB2PWI interface board, or to an external AVS master. The USB2PWI interface board and a Graphic User Interface (GUI) are included in the evaluation kit to easily evaluate the LM10500 AVS functionality from a PC. The evaluation kit is consist of:

- LM10500 Evaluation board, as shown in Figure 1
- USB2PWI interface board, as shown in Figure 2
- 5-pin mini USB cable
- A CD, including:
  - LM10500 evaluation GUI;
  - LM10500 data sheet;
  - LM10500 evaluation board application note (this document).

There are two versions of LM10500 Evaluation board: LM10500SQ-0.8EV and LM10500-1.0EV. The differences of the two versions are summarized in the table below.

Evaluation Board ID	LM10500SQ-0.8EV	LM10500SQ-1.0EV
Device ID	LM10500SQ-0.8	LM10500SQ-1.0
Board Default Output Voltage V_{OUT}	0.8 V	1.2 V
Feedback Node Default Voltage V_{FB}	0.8 V	1.0 V

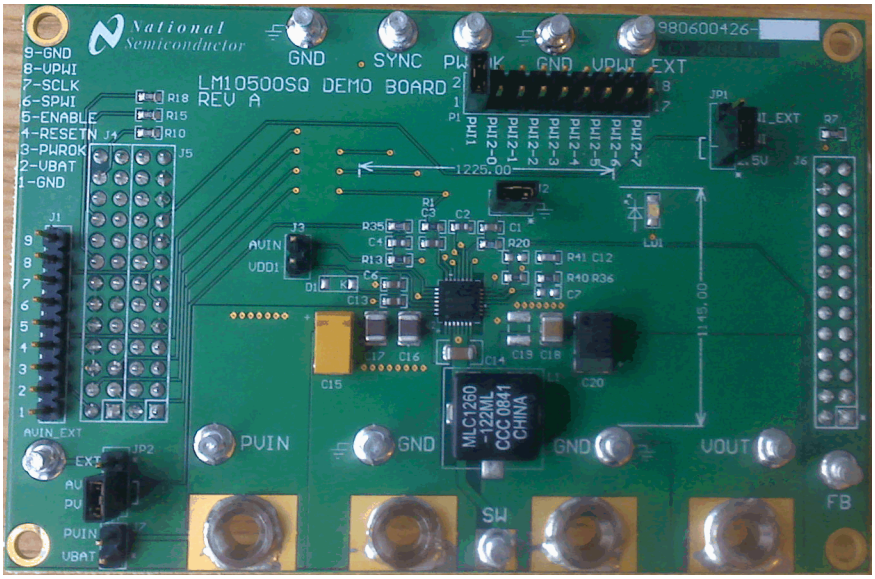


Figure 1. LM10500 Evaluation Board

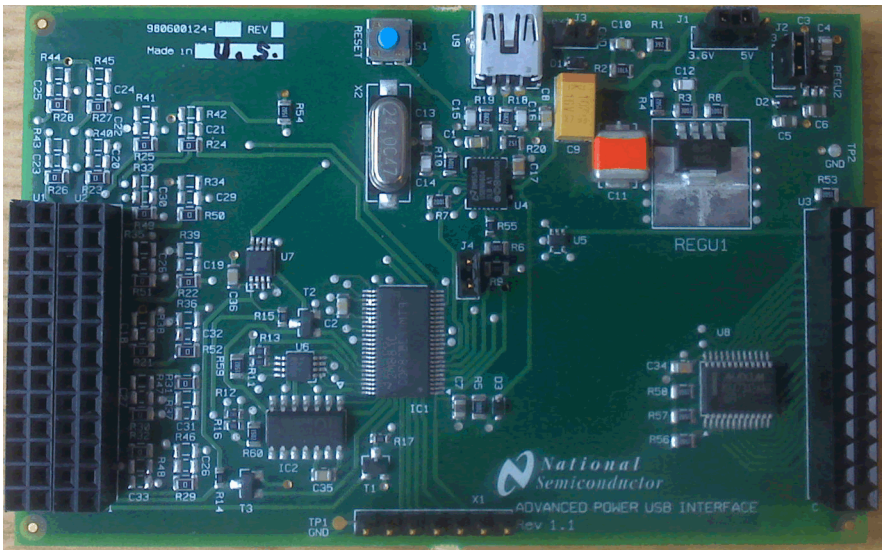


Figure 2. USB2PWI Interface Board

6 Typical Application Circuit

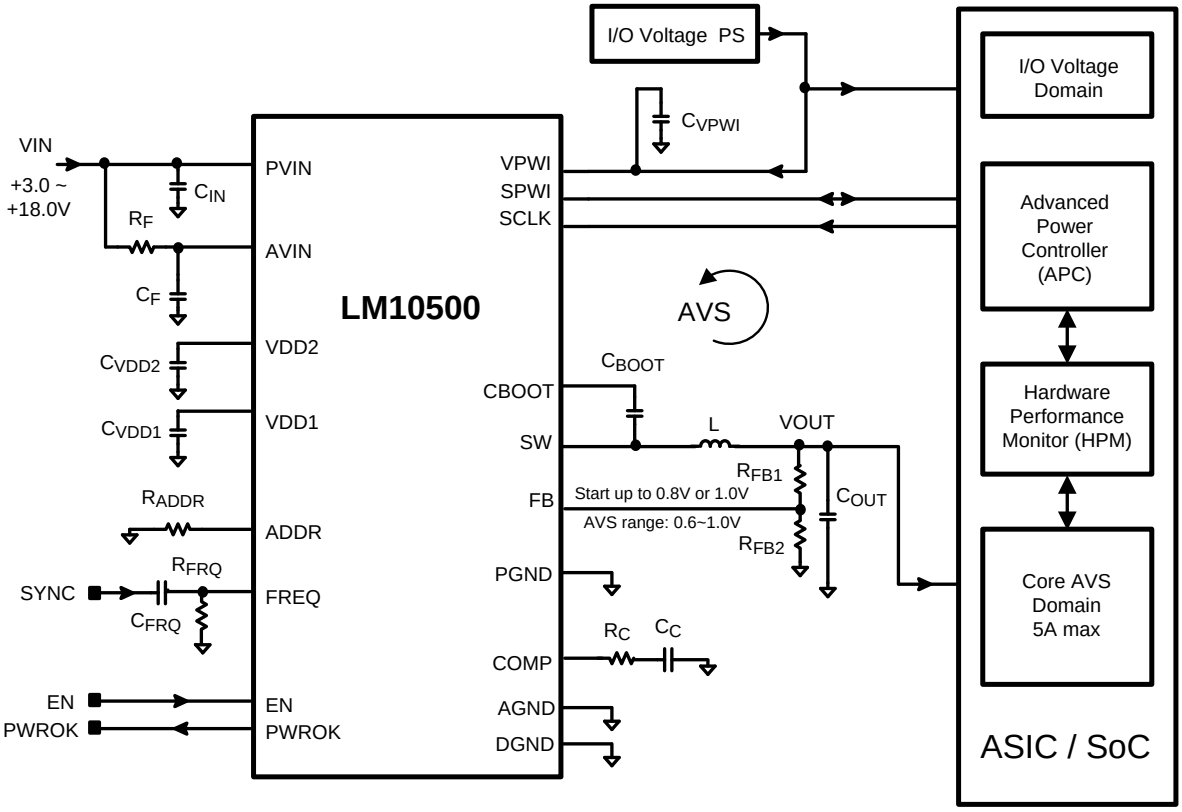


Figure 3. Typical Application Circuit

7 Connection Guide

7.1 Default Setting and Operation Options

The designed default condition and operating range for the LM10500 Evaluation Board are shown in the following table.

Parameter	Default Setting	Operation Range and Options
PVIN	J7 open Connect to External Supply = 12V	J7 open, connect PVIN to external supply. Voltage range is between 3 V and 18 V.
		J7 closed, PVIN is connected to V_{BAT} = 3.6 V. V_{BAT} is generated by the USB2PWI board. To protect the USB2PWI board, do not connect PVIN to an external power supply with J7 closed. Loading capability of V_{BAT} is very limited.
AVIN	= PVIN by JP2	On JP2, connect AVIN to PVIN. AVIN follows PVIN voltage.
		On JP2, connect AVIN to AVIN_EXT. AVIN_EXT can be connected to an external supply. Voltage range is between 3 V and 18 V, regardless of PVIN voltage. Note that AVIN = 5 V provides optimal efficiency.
V_{OUT}	1.2 V @LM10500SQ-1.0EV	0.6 V to 5 V (with resistor divider and PWI programming)
	0.8 V @LM10500SQ-0.8EV	
VPWI	2.5 V	On JP1, connect VPWI to 2.5 V. VPWI is powered by on-board LDO.
		On JP1, connect VPWI to VPWI_EXT. VPWI is powered by external supply (1.8 V - 10% to 3.3 V + 10%).
Switching Frequency	300 kHz	J2 close, frequency range is from 300 kHz to 1.5 MHz, programmed by R20.
		J2 open, switch node can be synchronized to an external clock. Note that R20 should also be selected to provide the same frequency as the external clock. Please refer to the LM10500 data sheet for more details.
I_{OUT}		0 A to 5 A
No. of PCB Layers	4	
Max Temp	85°C	

7.2 Terminal Descriptions

Terminals	Description
PVIN	Connect the power supply between this terminal and the GND terminal beside it. The device is rated between 3 V to 18 V. The absolute maximum voltage rating is 22 V.
GND	The GND terminals are meant to provide close return paths to the power and signal terminals besides them. They are all connected together on board.
SW	SW is connected to the switch node of the power stage. It can be used to monitor the switch node waveform by a scope.
VOUT	VOUT terminal is connected to the output capacitor on the board and should be connected to the load
FB	FB terminal is connected to the FB pin of the LM10500. It can be used to monitor the AVS voltage command programmed by PWI. Careful not to add any noise to the FB terminal or load it by any means.
AVIN_EXT	External AVIN supply. Connect AVIN to AVIN_EXT on JP2 to power AVIN externally.
SYNC	Synchronizing clock input. When J2 is Closed, switching frequency is controlled by the on board resistor R20. When J2 is Open, the switch node waveform will be synchronized to the clock source connected to SYNC terminal.
PWROK	This terminal connects to the PWROK pin of the LM10500. PWROK is pulled up to 2.5V via a 10 kΩ resistor.
VPWI_EXT	External VPWI supply. Connect VPWI to VPWI_EXT on JP2 to power VPWI externally
J4 J5 J6	Connectors to the USB2PWI board shown in Figure 4see Section 8.2.
J1	Connector to monitor AVS signal or to an external controller, see Section 8.3.

7.3 Jumper Settings

Jumpers	Description
JP1	VPWI selection, default VPWI = 2.5 V
JP2	AVIN selection, default AVIN = PVIN
J2	Default Closed: switching frequency is controlled by R20 (300 kHz default)
	When Open: switching frequency is synchronized to clock source connected to SYNC terminal
J3	Default OPEN
	Should only be connected when AVIN ≤ 5 V. When AVIN ≤ 5 V, connecting J3 can improve efficiency. Caution: if AVIN > 5.5 V, connecting J3 could damage the LM10500 device.
J7	Default OPEN
	Should only be connected when no voltage supply is connected to PVIN and AVIN. Intended for easy demonstration of the board by powering PVIN and AVIN by VBAT = 3.6 V. Caution: if PVIN is higher than 5.5 V, connecting J7 could damage the USB2PWI board. VBAT can not support large load current.
P1	PWI version and address selection. Note that the LM10500 supports PWI1, PWI2-0, PWI2-1, PWI2-2, and PWI2-3. The USB2PWI board supports PWI1 and PWI2-0.

8 Operation Guide

8.1 Standalone Operation

LM10500 evaluation board can operate standalone without PWI interface connected. It is a full-featured high performance 5 A synchronous buck regulator optimized for solution size, flexibility, and high conversion efficiency. It also features monolithic integration of the high-side and low-side power MOSFETs, resistor programmable switching frequency, frequency synchronization, internal soft start, precision enable, power good (PWROK) indicator, input under voltage lock-out, over voltage protection, over current protection and thermal shutdown.

8.2 PWI Communication Using USB2PWI Board

The unique feature of the LM10500 is close-loop Adaptive Voltage Scaling (AVS) capability. The LM10500 operates cooperatively with PowerWise® AVS compatible ASICs, SoCs, and processors to optimize supply voltages adaptively over process and temperature variations. To simplify the evaluation of the AVS functions in the LM10500, the evaluation board is designed to operate with the USB2PWI interface board (included in the evaluation kit). With the USB2PWI board, PWI registers and LM10500 operating states can be controlled by a PC via a simple register-based Graphical User Interface (GUI). Connect the LM10500 evaluation board on top of the USB2PWI board by J4, J5 and J6, as shown in Figure 4, then connect the USB2PWI board to a PC with a 5-pin mini USB cable (included in the evaluation kit).

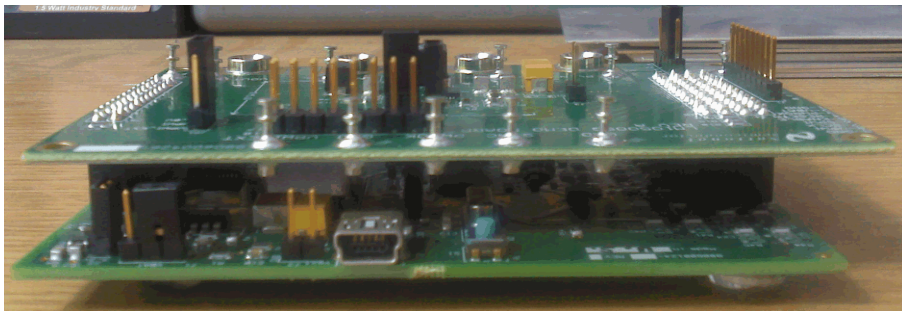


Figure 4. Connecting the LM10500 Evaluation Board to the USB2PWI Interface Board

The USB2PWI board is powered by the USB port. It generates a 3.6 V voltage: V_{BAT}. V_{BAT} is used on the evaluation board to provide the on board 2.5 V, which can be used to power VPWI. V_{BAT} can also be connected to PVIN to power the LM10500 when no other power supply is available. But the loading capability is limited on V_{BAT}. If available, PVIN should be powered by a bench supply with sufficient voltage and current ranges.

8.3 PWI Communication Using 9-Pin Connector J1

The LM10500 evaluation board can also interface to an AVS compatible master controller using J1. All signals related to the PWI signaling environment are available on this 1x9 header on the edge of the board. Although primarily intended for signal inspection, this header also allows external control of the PWI communication. This connector allows the LM10500 to be tested in a closed AVS loop with a master, such as AVS compatible ASICs, SoCs, and processors.

The pin list of J1 is shown in the table below.

Pin	Label	Type	Description
1	GND	GND	Ground
2	VBAT	Power	VBAT or sense
3	PWROK	Output	PWROK
4	RESETN	Input	1: Active 0: Reset
5	ENABLE	Input	1: Enabled 0: Disabled
6	SPWI	Input/Output	PWI data
7	SCLK	Input	PWI clock
8	VPWI	Power	VPWI-EXT or sense
9	GND	GND	Ground

The pins are spaced at 100-mil intervals. They can also be used as a sensing pin to determine the drive level for the PWI interface pins: SCLK, SPWI, PWROK, ENABLE and RESETN. VBAT and VPWI should be used as the control voltage input when the USB2PWI board is not connected. SPWI and SCLK are PWI communication data pin and clock pin, respectively. ENABLE is connected to the EN pin of the device. It is pulled up to AVIN via a 10 kΩ resistor on the board. This pin also can be used to enable / disable the device externally. If driven externally, a voltage typically greater than 1.2 V will enable the device. VPWI is for powering VPWI pin externally or monitoring the VPWI pin. VPWI range is from (1.8 V-10%) to (3.3 V+10%).

9 User's GUI for LM10500 Evaluation Board

A user's GUI is provided to control LM10500 evaluation boards via USB connection. The GUI for LM10500 is shown in Figure 5. It is compatible with both PWI1.0 and PWI2.0. The GUI supports PWI1.0 and PWI2.0 address 0. The LM10500 device supports PWI1.0 and PWI2.0 address 0, 1, 2, and 3. The GUI can read and write LM10500 registers to control and monitor the output voltage and operation mode. The GUI can also enable, reset the LM10500, and control the operation states, such as sleep, wake up, shutdown and reset, by generating PWI commands. All AVS functions of the LM10500 can be tested easily through the GUI.

9.1 Quick Start Guide

1. Connect the LM10500 Evaluation Board to the USB2PWI Interface Board (as in Figure 4) and plug the USB2PWI board to a PC using a USB cable. Apply PVIN and AVIN power to the LM10500 Evaluation Board. Part is enabled by default. Press the reset button on the SUB2PWI board. The reset button is the blue button located right next to the USB connector.
2. Run the GUI by double clicking 'Evaluation.exe', with 'Evaluation.ini' and 'usblptio.dll' in the same folder, from the PC. The default state of the GUI is shown in Figure 5.

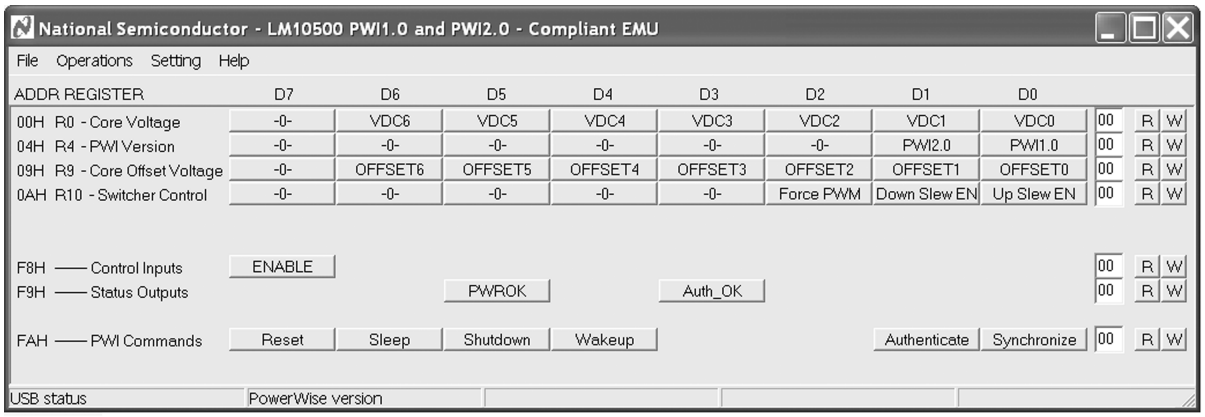


Figure 5. User's GUI For The LM10500 Evaluation Board

3. (optional) Check authentication by clicking the 'Authenticate' button on the bottom right of the GUI. Then click 'R' on the right of the 'Auth_OK' button to read back the authentication result. If 'PWROK' and "Auth_OK' are both '1' (in their depressed positions), then authentication is succeeded and the GUI is ready to control the LM10500 evaluation board.
4. CTRL+R, or from the menu 'Operations', select 'Read all', the default register values will be read from the LM10500 and shown in the GUI, as in Figure 6. If the default register setting does not show, press reset button on the USB2PWI board and repeat this step.

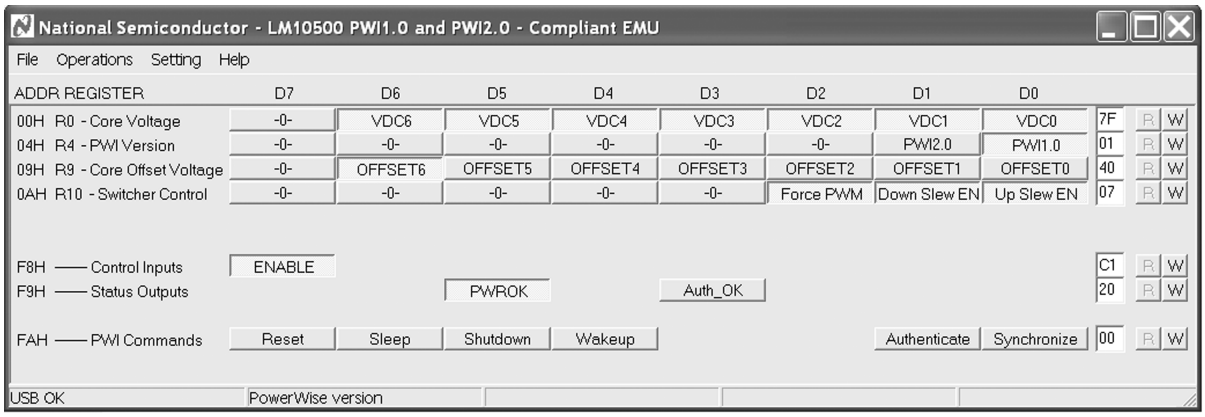


Figure 6. The LM10500 GUI With Default Register Values And Status (LM10500SQ-0.8)

NOTE: Note that picture shows the default values for LM10500SQ-0.8 with PWI1.0. For LM10500SQ-1.0, R9 is 0H. For PWI2.0 protocol, R4 is 02H,

9.2 GUI Layout and Conventions

Buttons in their depressed position mean that the corresponding bits are equal to 1, logic high, and in the raised position show the corresponding bits are equal to 0, logic low. '-0-' on a button means the bit is not used. Reading from unused bits returns '0' and writing to unused bits are ignored.

The top 4 lines of the GUI are the PWI registers of the LM10500. R0 controls the core voltage, ranging from 00h to 7Fh. R4 shows the PWI version: 01h means PWI1.0 and 02h means PWI2.0. R9 is the core voltage offset and the default value differs in LM10500SQ-0.8 and LM10500SQ-1.0. The default value of R9 is 00h in LM10500SQ-1.0 and 40h in LM10500SQ-0.8. The actual core voltage code is determined by the resulting code of (R0-R9) if (R0-R9) is above zero, otherwise, the core voltage code is zero. R10 enables and disables FPWM and stepping controls. Please refer to the LM10500 datasheet for more details.

The 'ENABLE' button controls the hardware enable if it is connected to LM10500.

The PWROK and Auth_OK are read-only bits, indicating the LM10500 has proper output voltage and successful Authentication, respectively.

The PWI commands buttons send out commands to alter the operating state of the PWI slave: the LM10500, authenticate and synchronize. Please refer to PowerWise Interface Specification for the details of PWI standard at pwistandard.com.

A summary of the operation state is shown in Figure 7.

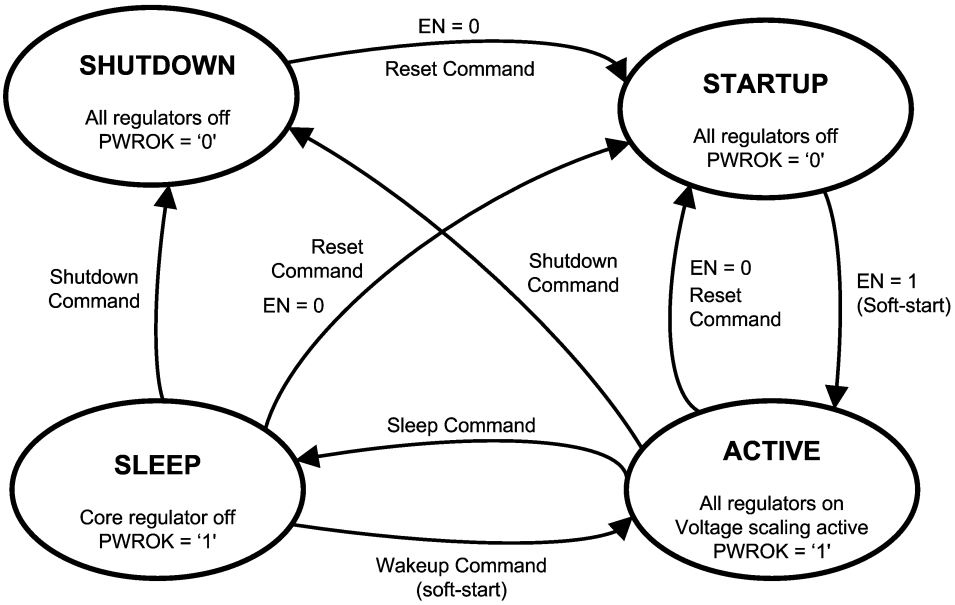


Figure 7. PWI Slave Operation States Diagram

9.3 Register Read and Register Write

There are a few ways to read and write to the registers through the GUI.

Register Read

- Click button 'R' at the right end of a register to read in the value of this register from the LM10500.
- Click menu Operations, then select Read all (Ctrl+R), to read in all the register values.
- Click menu Settings, select 'Register Polling', set 'polling time' to be non zero, as shown in Figure 8, then all registers are read in once every 'polling time'.
- Click menu Operations, then select Direct access, to read in a register by providing its address, as shown in Figure 9.

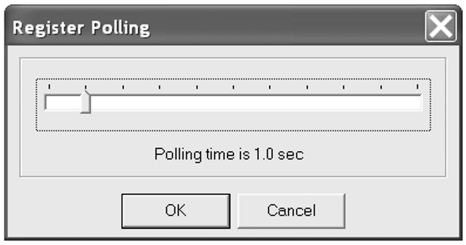


Figure 8. Register Polling Setting In The GUI

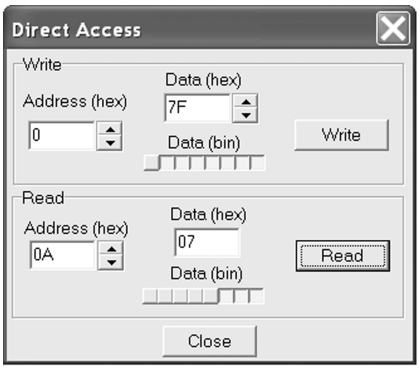


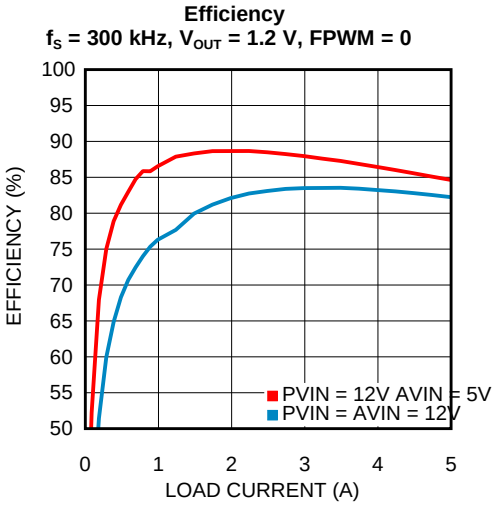
Figure 9. Direct Access Read / Write In The GUI

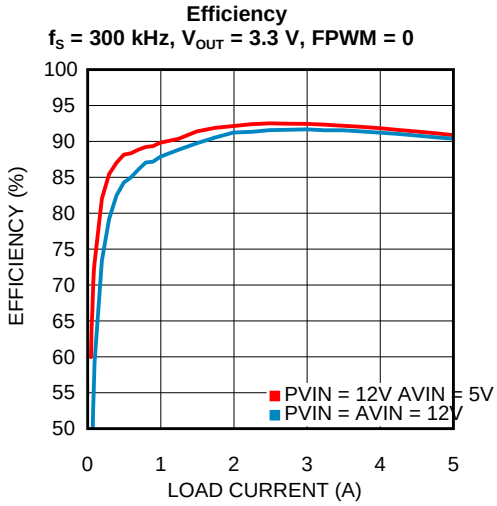
Register Write

- Click button 'W' at the right end of a register to write this register to the LM10500.
- Click menu Operations, then select Write all (Ctrl+W), to write the current values in the GUI to all registers in the LM10500.
- Click menu Settings, then select Update immediately, when checked, registers in LM10500 are written whenever the buttons in the GUI are updated.
- Click menu Operations, then select Direct access, to write to a register by providing its address and value, as shown in Figure 9.

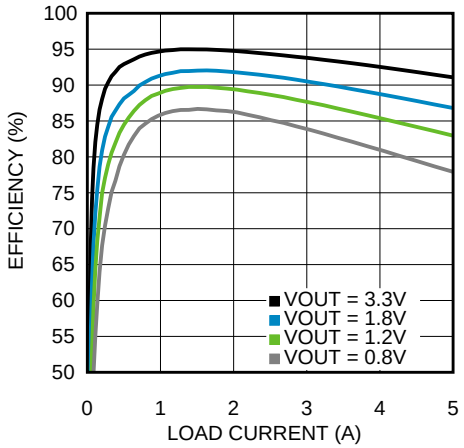
10 Typical Performance Characteristics

Unless otherwise specified: PVIN = AVIN = 12 V, V_{OUT} = 1.2 V, L = 2.2 µH, C_{OUT} = 220 µF, fs = 300 kHz.

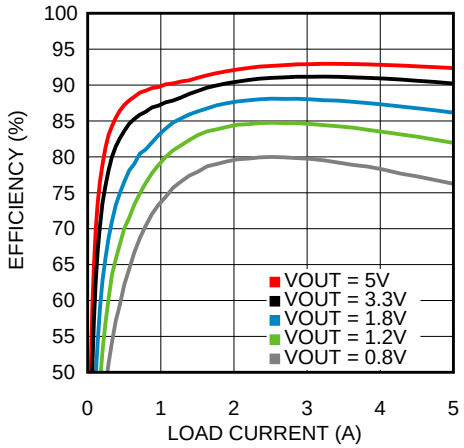




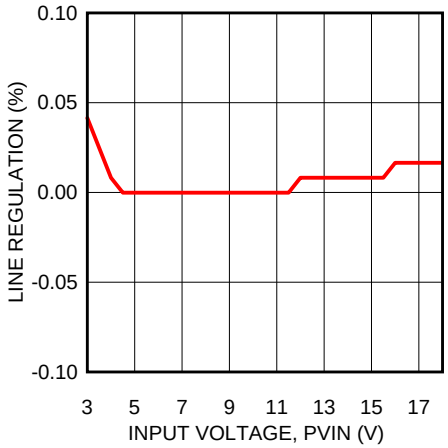
Efficiency
f_S = 300 kHz, AVIN = PVIN = 5 V, FPWM = 0



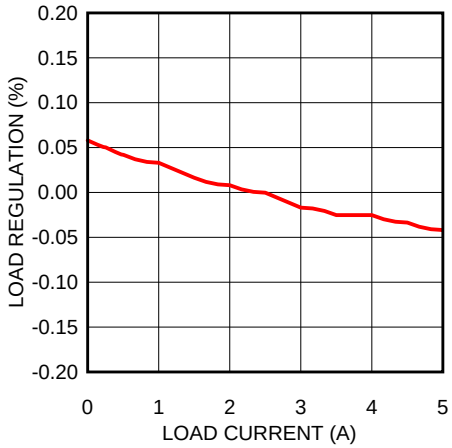
Efficiency
f_S = 300 kHz, AVIN = PVIN = 12V, FPWM = 0



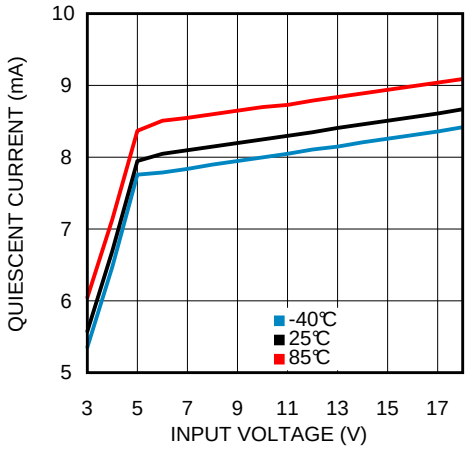
Line Regulation (%)



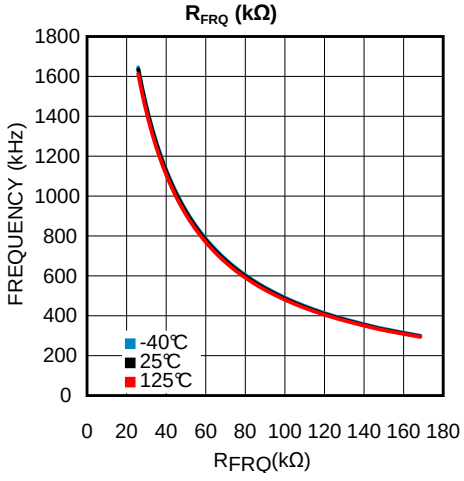
Load Regulation (%)



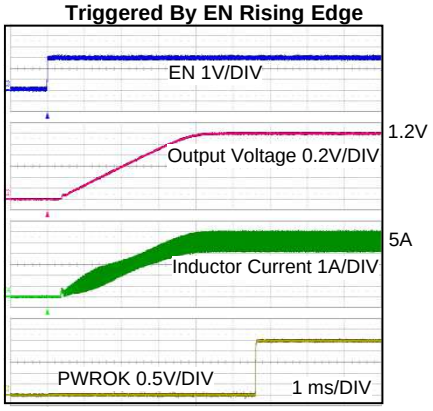
I_Q When EN = 1, I_{OUT} = 0, FPWM = 0



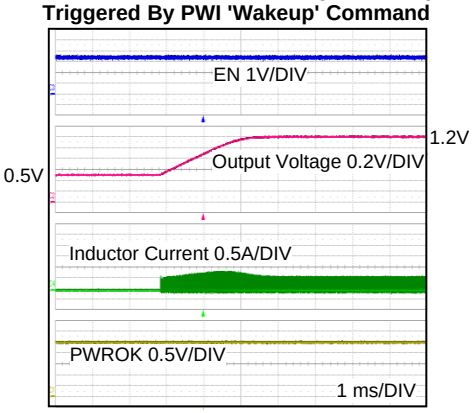
Switching Frequency (kHz)
vs.
R_{FRQ} (kΩ)



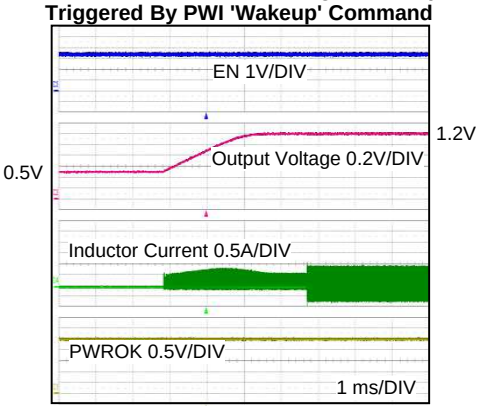
Soft Start With 5 A Load, Triggered By EN Rising Edge



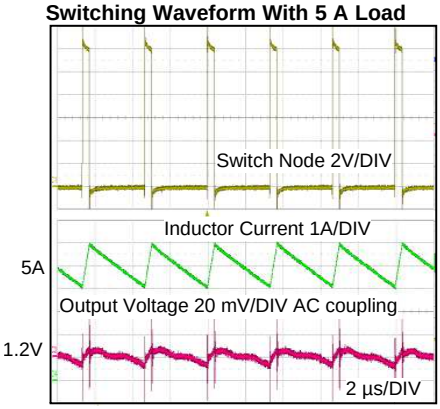
Soft Start With 0.5V Pre-bias Voltage, DCM Operation, Triggered By PWI 'Wakeup' Command



Soft Start With 0.5V Pre-bias Voltage, CCM Operation, Triggered By PWI 'Wakeup' Command



Switching Waveform With 5 A Load



11 Evaluation Board Schematic

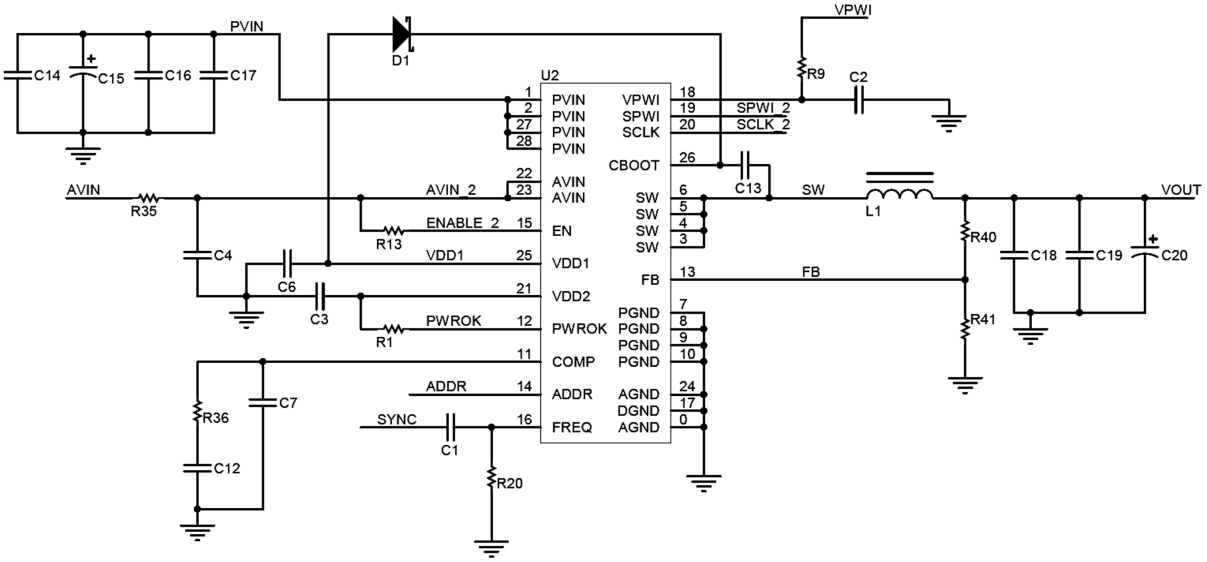


Figure 10. LM10500 Evaluation Board Schematic (Part I)

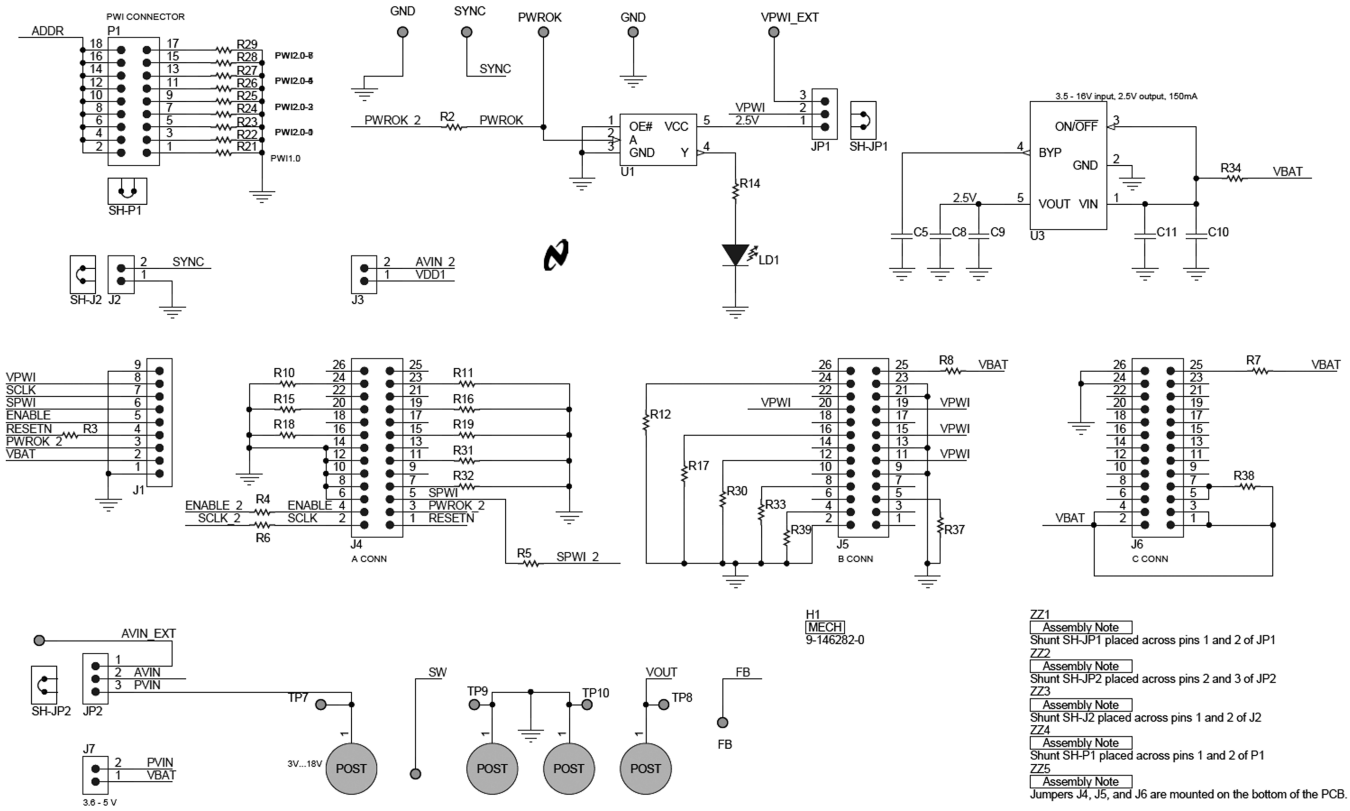


Figure 11. LM10500 Evaluation Board Schematic (Part II)

12 Evaluation Board Bill of Materials[(1)]

(1) The BOM shows the Bill of Materials for both LM10500SQ-0.8EV and LM10500SQ-1.0EV. All components are the same except U1, L1, R36, R40 and R41. Components for LM10500SQ-0.8EV are marked by *, while those for LM10500SQ-1.0EV are marked by **.

Designator(s)	Part Description	Part Number	Footprint	Mfg
U1	IC BUF NON-INV	NC7SZ125M5X	SOT23-5	FAIRCHILD
U2	AVS compatible EMU	LM10500 *	28 WQFN	Texas Instruments
	AVS compatible EMU	LM10500 **	28 WQFN	Texas Instruments
U3	IC REG LDO MICROPOWER	LP2985AIM5-2.5	SOT23-5	Texas Instruments
C1	CERAMIC 100 pF 100V	ECJ-1VC2A101J	603	PANASONIC
C2, C4, C8, C11, C14	CERAMIC 1.0 µF 35V X5R	GMK107BJ105KA	603	TAIYO YUDEN
C3, C6, C13	CERAMIC 0.1 µF 50V X7R	UMK107B7104KA-T	603	TAIYO YUDEN
C5, C12	CERAMIC 10000 pF 25V	C1608C0G1E103J	603	TDK
C7, C19	NL	NL	NL	NL
C9, C10	CER 10 µF 10V X7R 20% 1206	C3216X7R1A106M	1206	TDK
C15	TANT 47 µF 25V	T495X476K025ATE150	CASE D	KEMET
C16, C17	CERAMIC 10 µF 50V	UMK325C7106MM-T	1210	TAIYO YUDEN
C18	CERAMIC 47 µF X5R	GRM32ER61A476KE20L	1210	MURATA
C20	220 µF POLYMER 6.3V	EEF-UE0J221LR	CASE D	PANASONIC
D1	NL	NL		NL
L1	1.2 µH SMD INDUCTOR *	MLC1260-122ML		COILCRAFT
	2.2 µH SMD INDUCTOR **	SER1052-222ML		COILCRAFT
LD1	LED GREEN 2.1V 0805	CMDA5CG7D1Z	805	CML
R1, R13	10.0 KΩ 0603 1%	RC0603FR-710KL	603	YAGEO
R2, R3, R4, R5, R6	33Ω 0603 1%	RC0603FR-0733RL	603	YAGEO
R7, R8	1.5 KΩ 0603 1%	RC0603FR-071K5L	603	YAGEO
R9, R34, R35, R38	1Ω 0603 1%	RC0603FR-071RL	603	YAGEO
R10, R11, R12, R15, R16, R17, R18, R19, R30, R31, R32, R33, R37, R39	1KΩ 0603 1%	RC0603FR-071KL	603	YAGEO
R14	249Ω 0603 1%	RC0603FR-07249RL	603	YAGEO
R20	169 KΩ 0603 1%	RC0603FR-07169KL	603	YAGEO
R21	0.00Ω 0603 1%	CRCW06030000Z0EA	603	VISHAY/DALE
R22	40.2 KΩ 0603 1%	RC0603FR-0740K2L	603	YAGEO
R23	60.4 KΩ 0603 1%	RC0603FR-0760K4L	603	YAGEO
R24	80.6 KΩ 0603 1%	RC0603FR-0780K6L	603	YAGEO
R25	100 KΩ 0603 1%	RC0603FR-07100KL	603	YAGEO
R26	120 KΩ 0603 1%	RC0603FR-07120KL	603	YAGEO
R27	140 KΩ 0603 1%	RC0603FR-07140KL	603	YAGEO
R28	160 KΩ 0603 1%	RC0603FR-07160KL	603	YAGEO
R29	180 KΩ 0603 1%	RC0603FR-07180KL	603	YAGEO
R36	1.74 KΩ 603 1% *	RC0603FR-071K74KL	603	YAGEO
	2KΩ 0603 1% **	RC0603FR-072KL	603	YAGEO
R40	0.00Ω 0603 1% *	CRCW06030000Z0EA	603	VISHAY/DALE
	2KΩ 0603 1% **	RC0603FR-072KL	603	YAGEO
R41	NL *			
	10 KΩ 0603 1% **	RC0603FR-710KL	603	YAGEO

13 Evaluation Board Layout

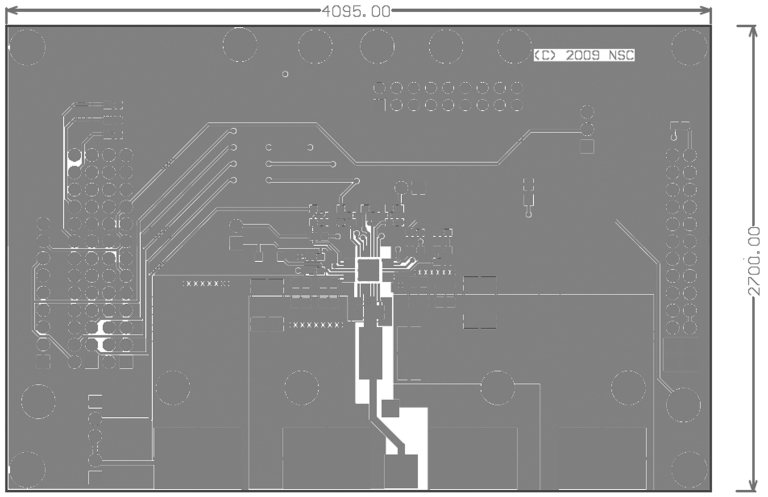


Figure 12. Top Layer

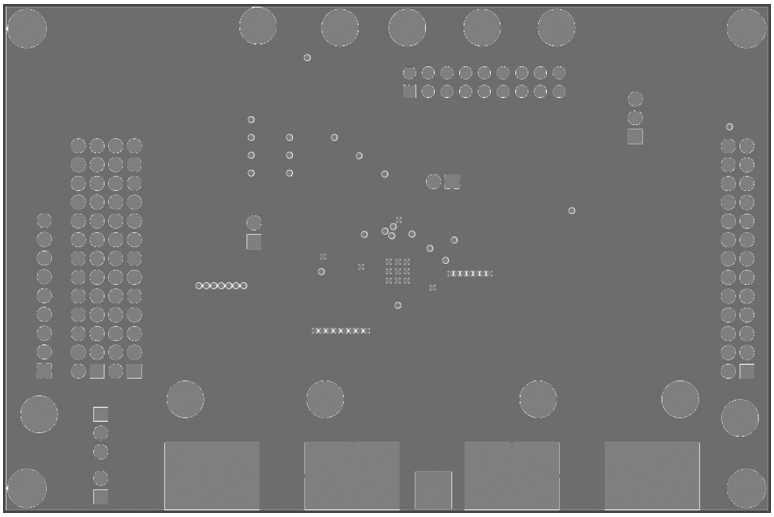


Figure 13. Middle Layer 1

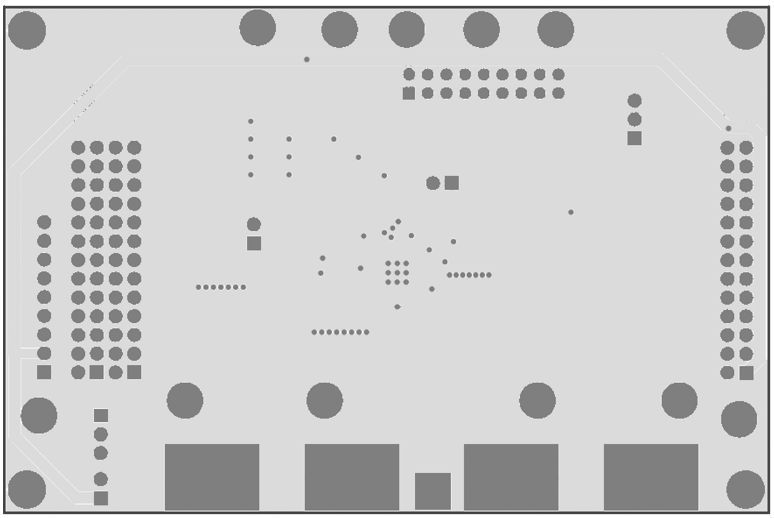


Figure 14. Middle Layer 2

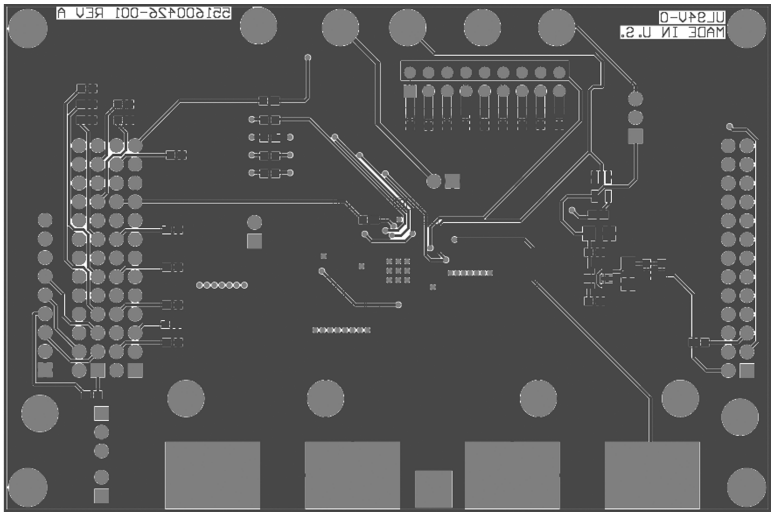


Figure 15. Bottom Layer

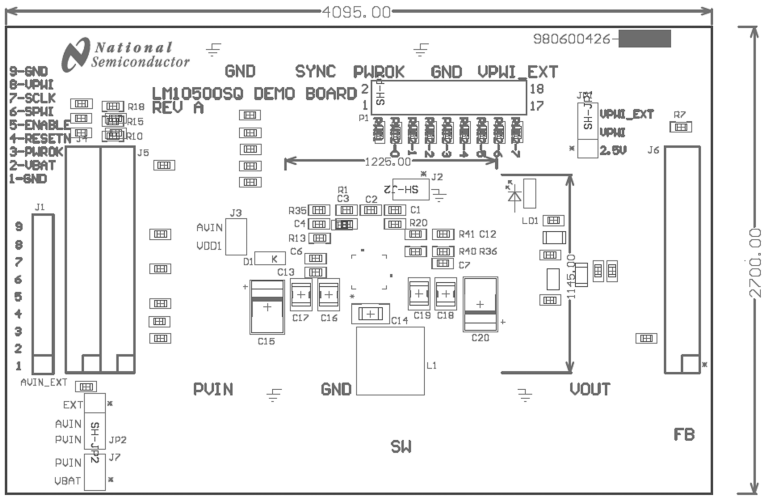


Figure 16. Top Overlay

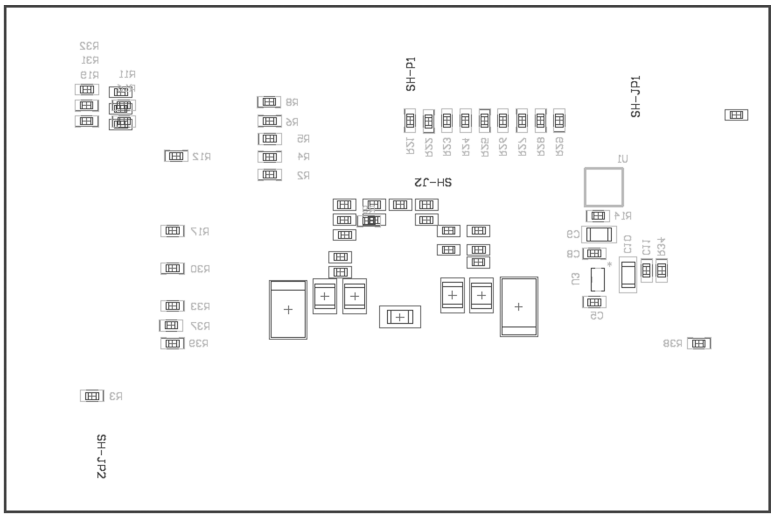


Figure 17. Bottom Overlay

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