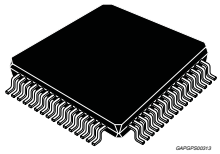
L9678
L9678-S

User configurable airbag IC

Datasheet - production data



LQFP64 (10x10x1.4mm)

Features

- Energy reserve voltage power supply
  - High frequency boost regulator, 1.882 MHz
  - Output voltage user selectable, 23 V or 33 V ±5%
- User configurable linear power supplies
  - 5.0 V and 7.2 V ±4% output voltages
  - External pass transistor
- Fully integrated 3.3 V ±4% linear regulator
- Battery voltage monitor and shutdown control with wake-up control
- System voltage diagnostics with integrated ADC
- Crossover switch
  - Crossover performance, max 3 Ω, 600 mA max.
- Squib deployment drivers
  - 4 channel HSD/LSD
  - 25 V maximum deployment voltage
  - 1.2 A @ 2 ms and 1.75 A @ 0.5/0.7 ms deployment profiles
  - Integrated safing FET linear regulator, 20 V/25 V nominal
  - Current monitoring
  - Rmeasure, STB, STG and leakage diagnostics
  - High and low side driver FET tests
  - Safing FET test
- User customizable safing logic
- Two channel PSI-5 remote sensor interface (asynchronous mode), [only for L9678-S version]
- Four channel hall-effect, resistive or switch sensor interface
- ISO9141 transceiver
- Dual channel configurable high-side/low-side LED driver
- Watchdog timer
- Two integrated oscillators: 7.5/16 MHz
- Temperature sensor
- 32 bit SPI communications
- Minimum operating voltage = 6 V
- Operating temperature, -40 °C to 95 °C
- Packaging - 64 pin

Table 1. Device summary

Order code	Package	Packing	Remote sensor interface
L9678	LQFP64 (10 x 10 x 1.4 mm)	Tray	No
L9678-S	LQFP64 (10 x 10 x 1.4 mm)	Tray	Yes

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1 Description

The L9678 IC is a system chip solution targeted for emerging market applications. Base system designs can be completed with the L9678, SPC560Px microcontroller and an on-board acceleration sensor or PSI5 sensor.

Energy reserve voltage is derived through a cost effective high frequency boost regulator. High frequency operation allows the user to pick up low value and cheap inductance. The voltage is programmable to 23 V or 33 V nominal.

Battery voltage is sensed through the VBATMON pin providing start-up and shutdown control for the system. Once battery voltage drops below the minimum operating voltage, the device enables the integrated crossover switch to permit orderly shutdown.

L9678 offers two linear regulators (5 V with external pass transistor and fully integrated 3.3 V). User can use one of these regulators to supply µC. Input/output pins are compatible with both ranges by dedicated supply pin VDDQ. External pass transistor gives the flexibility to easily address different current loads in case of different micro-controllers.

One optional 7.2 V linear regulator with external pass transistor can be used to supply remote sensor interface.

External acceleration data is received through the PSI-5 remote sensor interface. Both channels have independent decoders. Sensor data and diagnostics are available via SPI.

The safing logic monitors inertial sensors (remote sensors via PSI-5 or on-board sensors via SPI) to determine if a crash event is in progress, thereby enabling deployment to occur. Parameters for sensor configuration and thresholds are user programmable.

Squib deployment uses four independent high and low side drivers, capable of deploying at 25 V max. Diagnostic data control is provided through the SPI interface.

The Hall-effect, resistive or switch sensor interface can be used to determine the state of external switch devices, such as buckle switches, seat track position sensors, weight sensors, deactivation switches.

The integrated clock module provides a fixed clock signal for the microcontroller. The clock module provides the user the option of deleting the commonly used resonator or crystal.

2 Absolute and operative maximum ratings

2.1 Absolute maximum ratings

Warning: **This part may be irreparably damaged if taken outside the specified absolute maximum ratings. Operation above the absolute maximum ratings may also cause a decrease in reliability.**

Table 2. Absolute maximum ratings

Pin #	Pin name	Pin function	Min.	Max.	Unit
1	RESET	Reset output	-0.3	VDDQ+0.3 ≤6.5	V
2	SPI_MISO	SPI interface data out / Safing sensor data in	-0.3	VDDQ+0.3 ≤6.5	V
3	SPI_MOSI	SPI interface data in	-0.3	VDDQ+0.3 ≤6.5	V
4	SPI_SCK	SPI interface clock	-0.3	VDDQ+0.3 ≤6.5	V
5	SPI_CS	SPI interface chip select	-0.3	VDDQ+0.3 ≤6.5	V
6	WDT/TM	Watchdog disable (Not for application)	-0.3	20	V
7	VDD3V3	3.3 V regulator output	-0.3	4.6	V
8	NC	Not connected (1)	-	-	-
9	CVDD	Internal 3.3 V regulator output	-0.3	4.6	V
10	GNDD	Digital ground	-0.3	0.3	V
11	SR0	Squib 0 low-side pin	-0.3	40	V
12	SF0	Squib 0 high-side pin	-1.0	40	V
13	SG01	Squib 0 & 1 deployment ground pin	-0.3	0.3	V
14	SS01	Squib 0 & 1 deployment supply pin	-0.3	40	V
15	SF1	Squib 1 high-side pin	-1.0	40	V
16	SR1	Squib 1 low-side pin	-0.3	40	V
17	DCS3	Sensor switch interface channel 3	-1.0	40	V
18	DCS2	Sensor switch interface channel 2	-1.0	40	V
19	DCS1	Sensor switch interface channel 1	-1.0	40	V
20	DCS0	Sensor switch interface channel 0	-1.0	40	V
21	VRESDIAG	Reserve voltage diagnostic input	-0.3	40	V
22	RSU0/NC	PSI-5 Ch. 0 remote sensor output (only L9678-S), NC on L9678	-1.0	40	V
23	RSU1/NC	PSI-5 Ch. 1 remote sensor output (only L9678-S), NC on L9678	-1.0	40	V
24	VSUP/NC	Remote sensor power supply (only L9678-S), NC(1) on L9678	-0.3	40	V

Table 2. Absolute maximum ratings (continued)

Pin #	Pin name	Pin function	Min.	Max.	Unit
25	BVSUP/NC	VSUP external transistor control (only L9678-S), NC(1) on L9678	-0.3	40	V
26	GPOD0	GPO driver 1 drain output pin	-1.0	40	V
27	GPOS0	GPO driver 1 source output pin	-1.0	40	V
28	GPOS1	GPO driver 0 source output pin	-1.0	40	V
29	GPOD1	GPO driver 0 drain output pin	-1.0	40	V
30	NC	Not connected (1)	-	-	-
31	ISOK	ISO9141 bus pin (K-LINE)	-18.0	40	V
32	GNDSUB1	Substrate ground	-0.3	0.3	V
33	SR3	Squib 3 low-side pin	-0.3	40	V
34	SF3	Squib 3 high-side pin	-1.0	40	V
35	SS23	Squib 2 & 3 deployment supply pin	-0.3	40	V
36	SG23	Squib 2 & 3 deployment ground pin	-0.3	0.3	V
37	SF2	Squib 2 high-side pin	-1.0	40	V
38	SR2	Squib 2 low-side pin	-0.3	40	V
39	GNDA	Analog ground	-0.3	0.3	V
40	ISORX	ISO9141 receiver pin	-0.3	VDDQ+0.3 ≤6.5	V
41	ISOTX	ISO9141 transmit pin	-0.3	VDDQ+0.3 ≤6.5	V
42	FENL	LS driver FET control input	-0.3	VDDQ+0.3 ≤6.5	V
43	FENH	HS driver FET control input	-0.3	VDDQ+0.3 ≤6.5	V
44	SAF_CS0	SPI interface safing sensor chip select	-0.3	VDDQ+0.3 ≤6.5	V
45	SAF_CS1	SPI interface safing sensor chip select	-0.3	VDDQ+0.3 ≤6.5	V
46	NC	Not connected (1)	-	-	-
47	WAKEUP	Wake-up control input	-0.3	40	V
48	VBATMON	Battery line voltage monitor	-18	40	V
49	VSF	Safing regulator supply output	-0.3	ERBOOST+0.3 ≤40	V
50	VIN	Battery connection	-0.3	40	V
51	VER	Reserve voltage	-0.3	40	V
52	ERBOOST	Energy reserve regulator output	-0.3	40	V
53	ERBSTSW	Boost switching output	-0.3	40	V
54	NC	Not connected (1)	-	-	-
55	BSTGND	Boost regulator ground	-0.3	0.3	V
56	ACL	EOL disposal control input	-0.3	40	V
57	BVDD5	VDD5 external transistor control	-0.3	40	V
58	NC	Not connected	-	-	-
59	VDD5	5V regulator output	-0.3	6.5	V
60	NC	Not connected (1)	-	-	-

Table 2. Absolute maximum ratings (continued)

Pin #	Pin name	Pin function	Min.	Max.	Unit
61	COVRACT	External crossover switch control	-0.3	VDDQ+0.3 ≤6.5	V
62	VDDQ	I/O supply	-0.3	6.5	V
63	ARM	Arming Output	-0.3	VDDQ+0.3 ≤6.5	V
64	GNDSUB2	Substrate ground	-0.3	0.3	V

1. Not connected internally, should be connected to GND externally.

2.2 Operative maximum ratings

Within the operative ratings the part operates as specified and without parameter deviations Once taken beyond the operative ratings and returned back within, the part will recover with no damage or degradation.

Additional supply-voltage and temperature conditions are given separately at the beginning of each specification table.

Table 3. Operative maximum ratings

Pin #	Pin name	Pin function	Min.	Max.	Unit
1	RESET	Reset output	-0.1	VDDQ+0.1 ≤5.5	V
2	SPI_MISO	SPI interface data out / Safing sensor data in	-0.1	VDDQ+0.1 ≤5.5	V
3	SPI_MOSI	SPI interface data in	-0.1	VDDQ+0.1 ≤5.5	V
4	SPI_SCK	SPI interface clock	-0.1	VDDQ+0.1 ≤5.5	V
5	SPI_CS	SPI interface chip select	-0.1	VDDQ+0.1 ≤5.5	V
6	WDT/TM	Watchdog disable	-0.1	20	V
7	VDD3V3	3.3V regulator output	-0.1	3.6	V
8	NC	Not connected(1)	-	-	-
9	CVDD	Internal 3.3V regulator output	-0.1	3.6	V
10	GNDD	Digital ground	-0.1	0.1	V
11	SR0	Squib 0 low-side pin	-0.1	VER	V
12	SF0	Squib 0 high-side pin	-1.0	VER	V
13	SG01	Squib 0 & 1 deployment ground pin	-0.1	0.1	V
14	SS01	Squib 0 & 1 deployment supply pin	-0.1	40	V
15	SF1	Squib 1 high-side pin	-1.0	VER	V
16	SR1	Squib 1 low-side pin	-0.1	VER	V
17	DCS3	Sensor switch interface channel 3	-1.0	V_{DCS_L}	V
18	DCS2	Sensor switch interface channel 2	-1.0	V_{DCS_L}	V
19	DCS1	Sensor switch interface channel 1	-1.0	V_{DCS_L}	V
20	DCS0	Sensor switch interface channel 0	-1.0	V_{DCS_L}	V
21	VRESDIAG	Reserve voltage diagnostic input	-0.1	35	V
22	RSU0/NC	PSI-5 Ch. 0 remote sensor output (only L9678-S), NC on L9678	-1.0	VSUP	V

Table 3. Operative maximum ratings (continued)

Pin #	Pin name	Pin function	Min.	Max.	Unit
23	RSU1/NC	PSI-5 Ch. 1 remote sensor output (only L9678-S), NC on L9678	-1.0	VSUP	V
24	VSUP/NC	Remote sensor power supply (only L9678-S, NC(1) on L9678)	-0.1	VIN	V
25	BVSUP/NC	VSUP external transistor control (only L9678-S, NC(1) on L9678)	-0.1	VIN	V
26	GPOD0	GPO driver 1 drain output pin	-0.1	40	V
27	GPOS0	GPO driver 1 source output pin	-1.0	VIN	V
28	GPOS1	GPO driver 0 source output pin	-1.0	VIN	V
29	GPOD1	GPO driver 0 drain output pin	-0.1	40	V
30	NC	Not connected (1)	-	-	-
31	ISOK	ISO9141 bus pin	-1.0	40	V
32	GNDSUB1	Substrate ground	-0.1	0.1	V
33	SR3	Squib 3 low-side pin	-0.1	VER	V
34	SF3	Squib 3 high-side pin	-1.0	VER	V
35	SS23	Squib 2 & 3 deployment supply pin	-0.1	40	V
36	SG23	Squib 2 & 3 deployment ground pin	-0.1	0.1	V
37	SF2	Squib 2 high-side pin	-1.0	VER	V
38	SR2	Squib 2 low-side pin	-0.1	VER	V
39	GNDA	Analog ground	-0.1	0.1	V
40	ISORX	ISO9141 receiver pin	-0.1	VDDQ+0.1 ≤ 5.5	V
41	ISOTX	ISO9141 transmit pin	-0.1	VDDQ+0.1 ≤ 5.5	V
42	FENL	LS driver FET control input	-0.1	VDDQ+0.1 ≤ 5.5	V
43	FENH	HS driver FET control input	-0.1	VDDQ+0.1 ≤ 5.5	V
44	SAF_CS0	SPI interface safing sensor chip select	-0.1	VDDQ+0.1 ≤ 5.5	V
45	SAF_CS1	SPI interface safing sensor chip select	-0.1	VDDQ+0.1 ≤ 5.5	V
46	NC	Not connected (1)	-	-	-
47	WAKEUP	Wake-up control input	-0.1	VIN	V
48	VBATMON	Battery line voltage monitor	-0.1	18	V
49	VSF	Safing regulator supply output	-0.1	27	V
50	VIN	Battery connection	-0.1	35	V
51	VER	Reserve voltage	-0.1	35	V
52	ERBOOST	Energy reserve regulator output	-0.1	35	V
53	ERBSTSW	Boost switching output	-0.1	ERBOOST+1	V
54	NC	Not connected (1)	-	-	-
55	BSTGND	Boost regulator ground	-0.1	0.1	V
56	ACL	EOL disposal control input	--0.1	40	V
57	BVDD5	VDD5 external transistor control	-0.1	VIN	V

Table 3. Operative maximum ratings (continued)

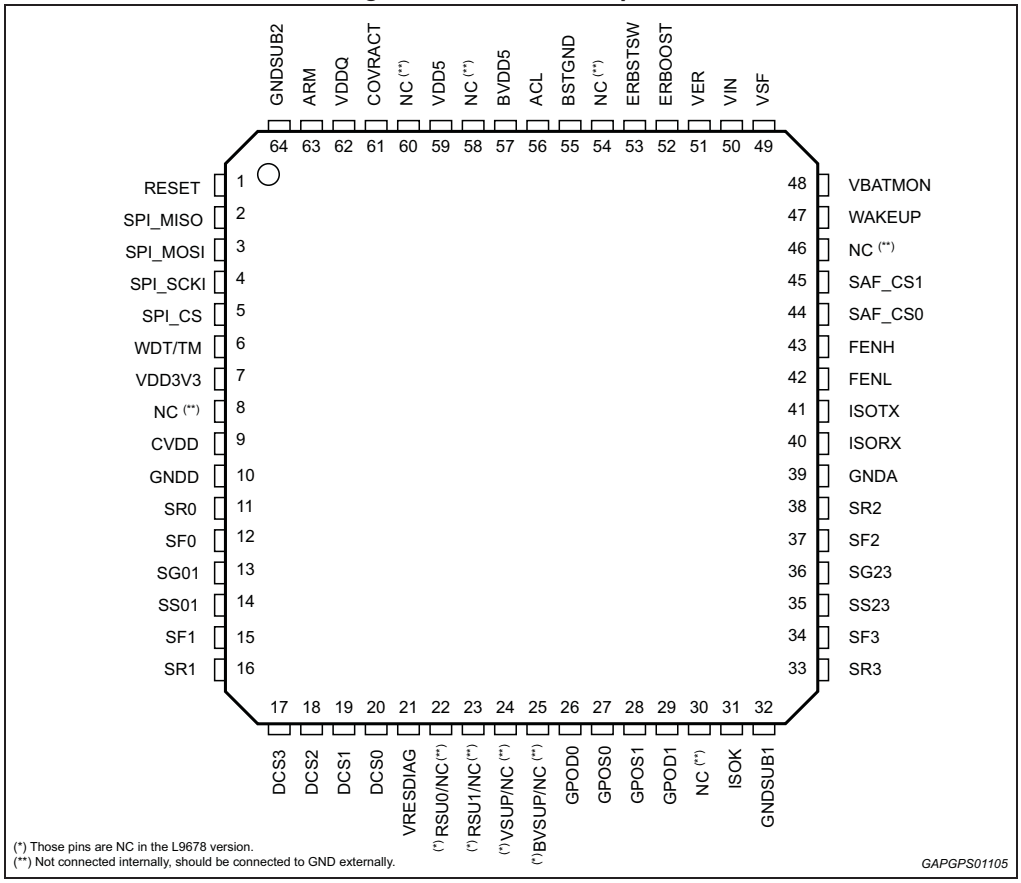
Pin #	Pin name	Pin function	Min.	Max.	Unit
58	NC	Not connected (1)	-	-	-
59	VDD5	5V regulator output	-0.1	5.5	V
60	NC	Not connected (1)	-	-	-
61	COVRACT	External crossover switch control	-0.1	VDDQ+0.1 ≤ 5.5	V
62	VDDQ	I/O supply	-0.1	5.5	V
63	ARM	Arming Output	-0.1	VDDQ+0.1 ≤ 5.5	V
64	GNDSUB2	Substrate ground	-0.1	0.1	V

1. Not connected internally, should be connected to GND externally.

2.3 Pin-out description

The L9678-S/L9678 pin-out is shown below. The package is a LQFP 64-pin full plastic package.

Figure 1. Pin-out description

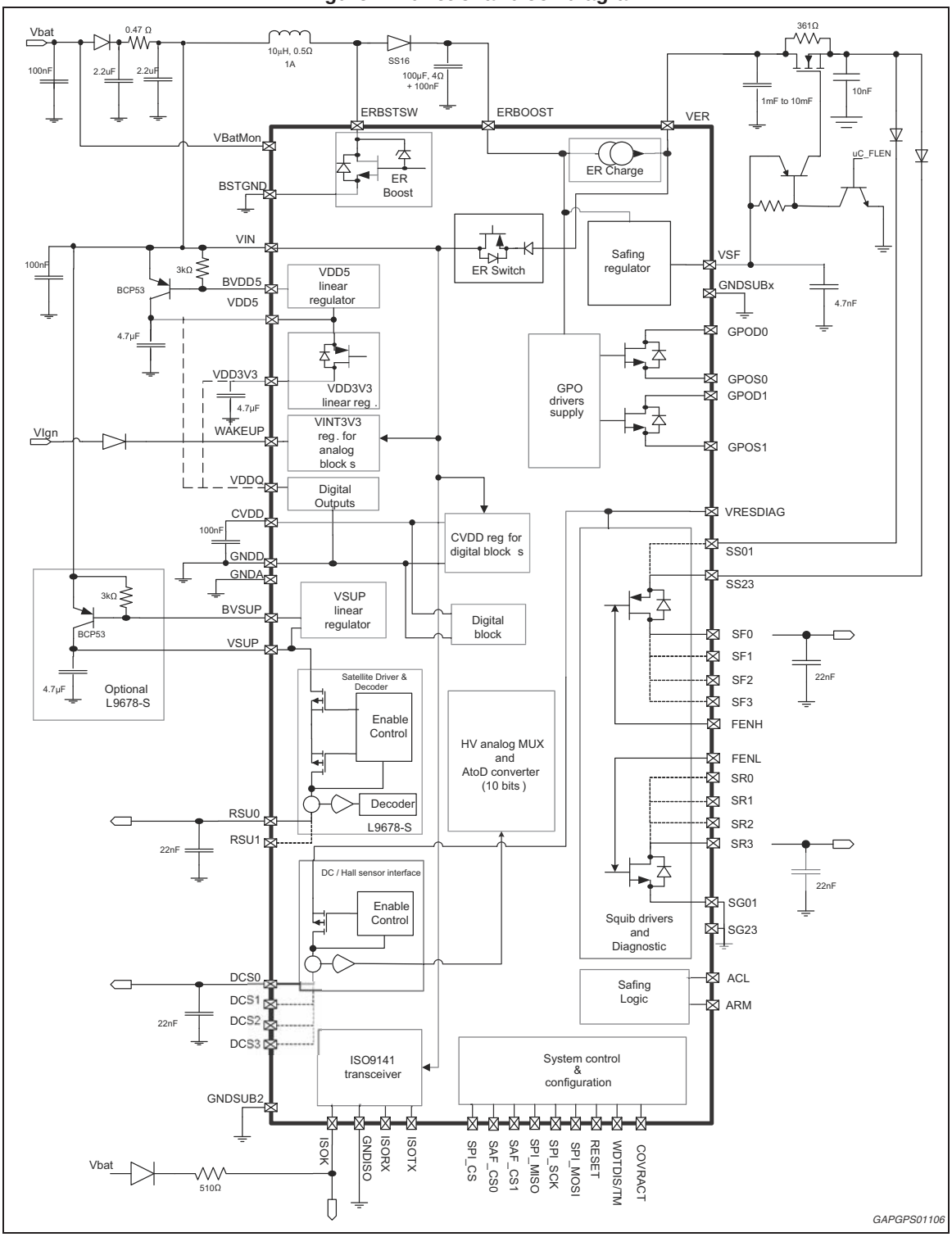


3 Overview and block diagram

The L9678 is a unique solution specifically targeted for entry level airbag systems while permitting the system designer significant flexibility in configuring the system power and management block. The configurable methodology allows cost versus performance trade-off without changing devices or circuit board designs. The L9678 contains the base functionality required for entry level systems and can complete a system design with a microcontroller and acceleration sensor. The high level block diagram is shown below *Figure 2*.

Basic features include a configurable power supply & management block, 4 channel squib drivers, 2 channel HS/LS GPO drivers, 4 channel sensor interface, safing logic, watchdog timer, ISO9141 communications and temperature sensor. The L9678-S device is pin compatible to the L9678 and includes two PSI-5 remote sensor interface channels and a dedicated regulator for remote sensor.

Figure 2. Functional block diagram



4 Start-up power control

4.1 Power supply overview

The L9678 IC contains a complete power management system able to provide all necessary voltages for an entry level airbag application. Moreover L9678 power supply is user configurable allowing the design engineer to balance cost and performance per their particular application. The power supply block contains the following features:

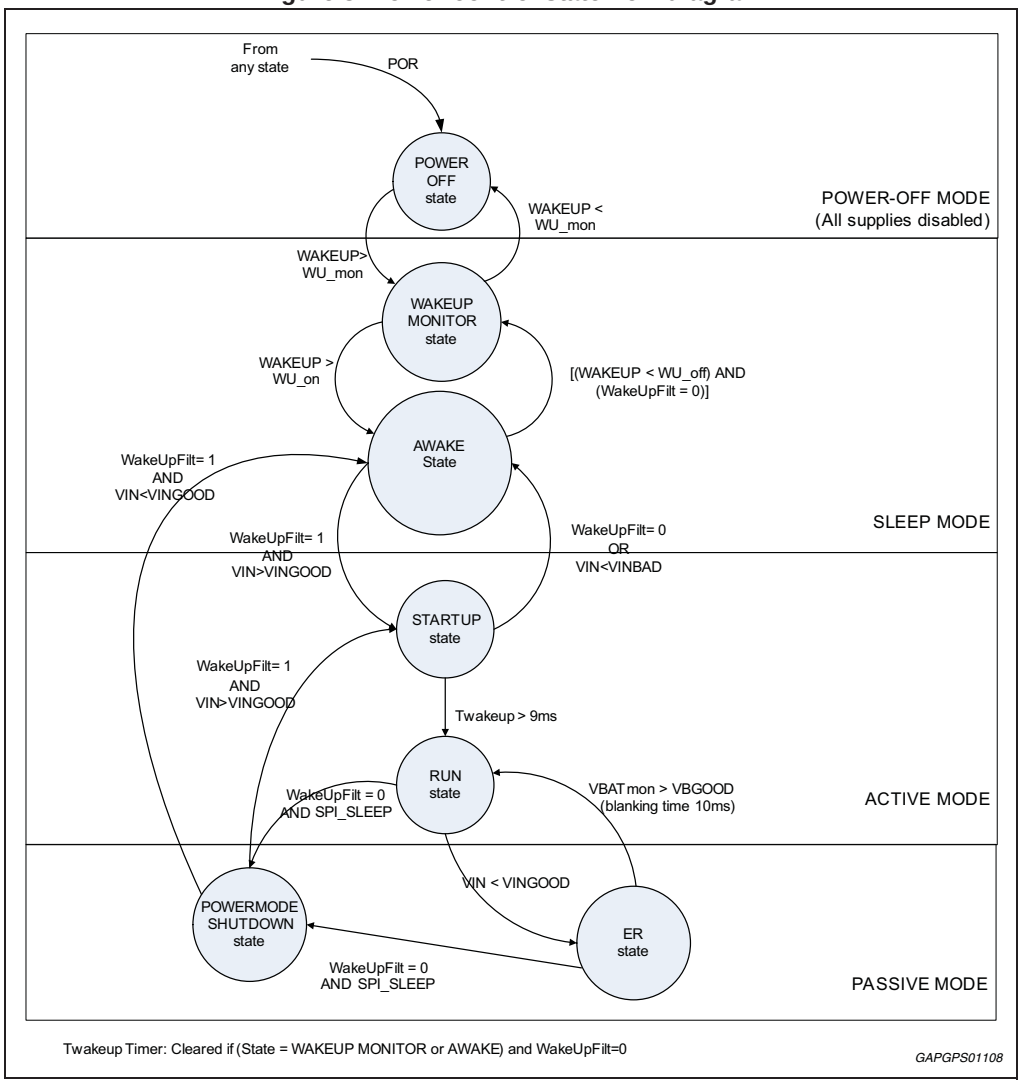
- Two 3.3 V internal regulators for operating internal logic (CVDD) and analog circuits (VINT3V3). An external CVDD pin is used to provide filtering capacitance to digital section supply rail.
- Energy reserve supply (ERBOOST) achieved through an integrated switching boost regulator. The design of this boost regulator is intended to be a cost effective solution with respect to traditional boost regulators because it makes use of a low value inductor with an operative frequency of 1.882 MHz. Switching output is ERBSTSW pin, while voltage feedback input pin is ERBOOST. The output voltage could be set to either 23 V±5% or 33 V±5%.
- Energy reserve capacitor connected to VER pin. To control in-rush current, a dedicated current generator is implemented between ERBOOST pin and VER pin.
- Capability to drive an external safing FET (n-ch type) by means of an internal voltage regulator on VSF pin, where a 20 V level is given (configurable to 25V via SPI command).
- The integrated current limited ER switch requires no external components. This switch is controlled through the integrated power control state machine and is enabled either once a loss of battery is detected or a shutdown command is received. Under the same conditions also the discrete digital pin COVRACT is activated allowing the control of an external optional cross-over switch.
- One linear regulator VDD5 (5 V nominal, ±4% tolerance) requiring external power transistor and capacitors. VDD5 is used as micro-controller supply (in case of 5 V family controllers) and, in any case, as supply for VDD3V3 rail.
- One integrated linear regulator VDD3V3 (3.3 V nominal, ±4% tolerance) requiring external capacitors. VDD3V3 is used as micro-controller supply (in case of 3.3 V family controllers).
- VDDQ pin to provide output voltage rail reference. VDDQ could be connected to either VDD5 or VDD3V3 to enable 5 V or 3.3 V digital communication between device and micro-controller.
- Capability to drive an external power transistor connected to VIN to provide a 7.2 V rail on VSUP pin. This voltage rail could be used to supply PSI-5 remote sensor.
- Battery voltage sense input comparator with hysteresis connected to VBATMON pin. Power-up and operation states are carefully handled with respect to the battery level to provide the most effective power supply configuration.
- All voltage rails (VIN, ERBOOST, VER, VRESDIAG, VDD5, VDD3V3, VSUP and VSF) can be monitored through internal ADC diagnostics.

4.2 Power mode control

Start-up and power down of the L9678 are controlled by the WAKEUP pin, VBATMON pin, VIN pin device status and the SPI interface. There are four main power modes: power-off, sleep, active and passive mode.

Each power mode is described below and represented in the state flow diagram shown in *Figure 3*. The descriptions include references to conditions and sometimes nominal values. The absolute values for each condition are listed in the electrical specifications section.

Figure 3. Power control state flow diagram



4.2.1 Power_off mode

During the Power-off mode all supplies are disabled keeping the system in a quiescent state with very low current draw from battery. As soon as WAKEUP > WU_mon the IC will move to Sleep mode.

4.2.2 Sleep mode

During the Sleep mode the VINT3V3 and CVDD internal regulators are turned on and the IC is ready for full activation of all the other supplies. As soon as battery voltage is over a minimum threshold, all the other supplies are turned on and the IC enters the Active mode.

4.2.3 Active mode

This is the normal operating mode for the system.

All power supplies are enabled and the energy reserve boost converter starts to increase the voltage at ERBOOST. Likewise, the VDD5 regulator is turned on. Once the VDD5 has reached a good value, the VDD3V3 regulator starts up. Once the VDD3V3 regulator is in regulation, RESET is released allowing the system microcontroller and other components to begin their power-on sequence. Among these, also the ER charge current generator can be enabled by the microcontroller via a dedicated SPI command.

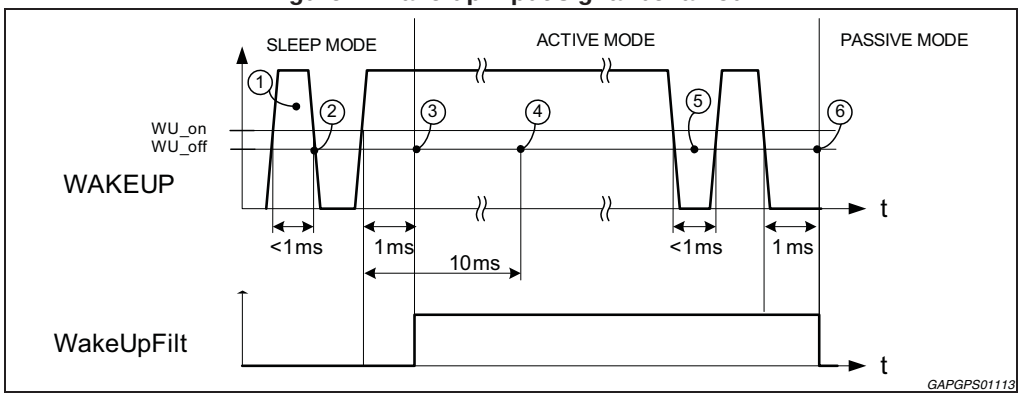
The active mode can be left when either WAKEUP pin or VIN voltage drop down. For the very first 9 ms after having entered the active mode, the WAKEUP pin low would immediately cause the IC to switch back to sleep mode. After that time, WAKEUP pin low must be first confirmed by a MCUSPI_SLEEP command prior to cause the system to switch to passive mode. Passive mode is also entered in case of VIN voltage low.

4.2.4 Passive mode

In this state, the energy reserve charge current is disabled and the ERBOOST boost converter is disabled only if the SYS_CFG(KEEP_ERBST_ON)=0. When in passive mode the device automatically activates both the COVRACT output pin and the integrated ER switch to allow VIN to be connected to the ER capacitor. In this time, VIN is supposed to be increased up to almost VER level and the system operation relies on energy from the ER capacitor. Two scenarios are possible: high or low battery. If VIN < VINGOOD, the device moved from RUN state in ACTIVE mode to the ER state. Here, the ER capacitor is depleted while supplying all the regulators until the POR on internal regulator occurs. The threshold to decide the ER switch activation is based on VIN, because VIN is the supply voltage rail for all regulators. If the device has still a good battery level, it entered the POWERMODE SHUTDOWN thanks to WAKEUP pin and MCU command to switch off. In this case, the VER node will be discharged down to approximately VIN level, which then will be supplied out of the battery line. System will continue to run up to a dedicated SPI command which will lead the device to enter the POWEROFF state.

The wake-up pin is filtered to suppress undesired state changes resulting from transients or glitches. Typical conditions are shown in the chart below and summarized by state.

Figure 4. Wake-up input signal behaviour



Condition summary:

1. No change of sleep mode state but current consumption may exceed specification for sleep mode.
2. The sleep mode current returns within the specified limits.
3. Power supply exits sleep mode. Switchers start operating if applicable voltages exceed under voltage lockouts. As T_{wakeup} time-out is not elapsed, a low level at WAKEUP instantaneously sends the system back to sleep.
4. Sleep Reset is released and the entire system starts operating. A SPI command to enter sleep state would be ignored.
5. No change in system status, a SPI command to enter sleep state would be ignored.
6. No change in system status, but a SPI command to turn off switchers would be accepted and turn the system off.

With the below table, all the functionalities of the device are shown with respect of the power states. When one function is flagged, the related circuitry cannot be activated on that state.

Table 4. Functions disabling by state

Function	Power Off	Wake-up monitor	Awake	Start-up	Run	Power mode shutdown	ER
Wakeup detector	X	-	-	-	-	-	-
Internal regulator	X	X	-	-	-	-	-
ERBOOST regulator	X	X	X	-	-	X	X
VSUP regulator (L9678-S only)	X	X	X	-	-	-	-
ER CAP charge current source	X	X	X	-	-	X	X
ER switch	X	X	X	X	X	-	-
COVRACT Output	X	X	X	X	X	-	-
VDD5 regulator	X	X	X	-	-	-	-
VDD3V3 regulator	X	X	X	-	-	-	-
Deployment drivers	X	X	X	-	-	-	-
VSF safing FET regulator	X	X	X	-	-	-	-
Remote sensor interfaces (L9678-S only)	X	X	X	-	-	-	-

Table 4. Functions disabling by state (continued)

Function	Power Off	Wake-up monitor	Awake	Start-up	Run	Power mode shutdown	ER
Watchdog	X	X	X	-	-	-	-
Diagnostics	X	X	X	-	-	-	-
DC sensor interface	X	X	X	-	-	-	-
GPO drivers	X	X	X	-	-	-	-
Safing logic	X	X	X	-	-	-	-
ISO9141	X	X	X	-	-	-	-

4.2.5 Power-up and power-down sequence

The behavior of the IC during normal power-up and power-down is shown in *Figure 5* to *Figure 8*. The following sequences represent just a subset of all possible power-up and power-down scenarios.

In *Figure 5* a normal IC power-up controlled by the state of the WAKEUP pin is shown.

Figure 5. Normal power-up sequence - WAKEUP controlled

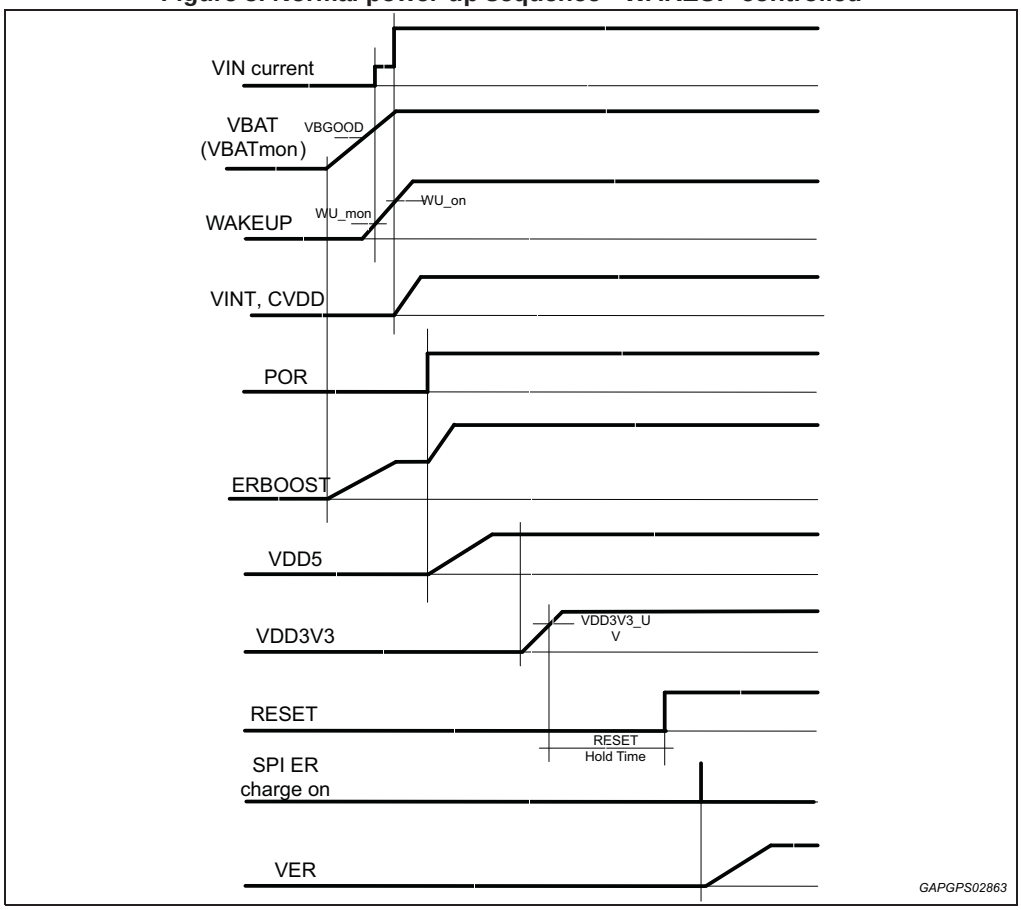
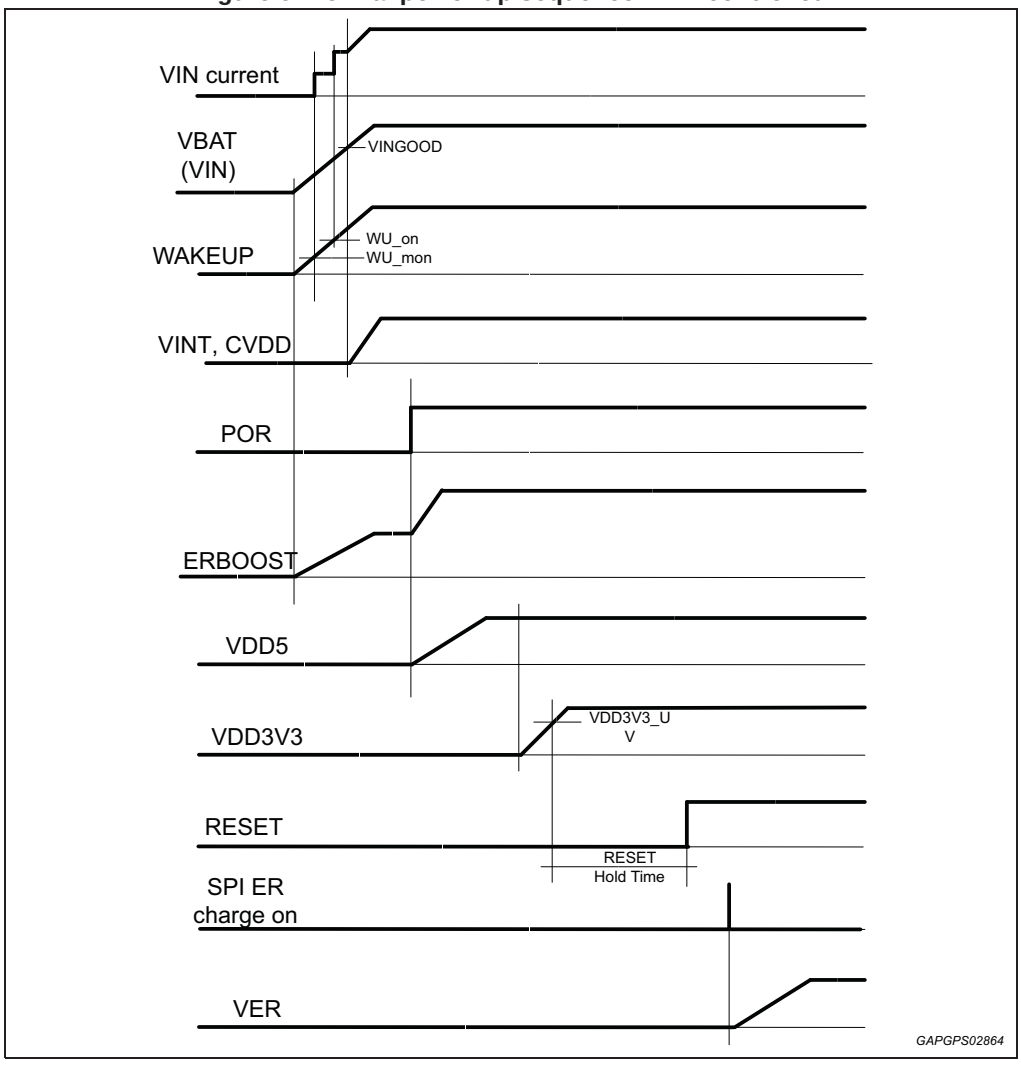


Figure 6. Normal power-up sequence - VIN controlled



Two different scenarios for power-down of the IC are here below shown. *Figure 7* describes the powering down for the case when WAKEUP pin is released. As soon as a SPI_SLEEP command is received by the MCU the System will immediately move to the energy reserve (PASSIVE mode). In *Figure 8*, VIN release begins the shutdown process.

Figure 7. Normal power down sequence - WAKEUP and SPI controlled

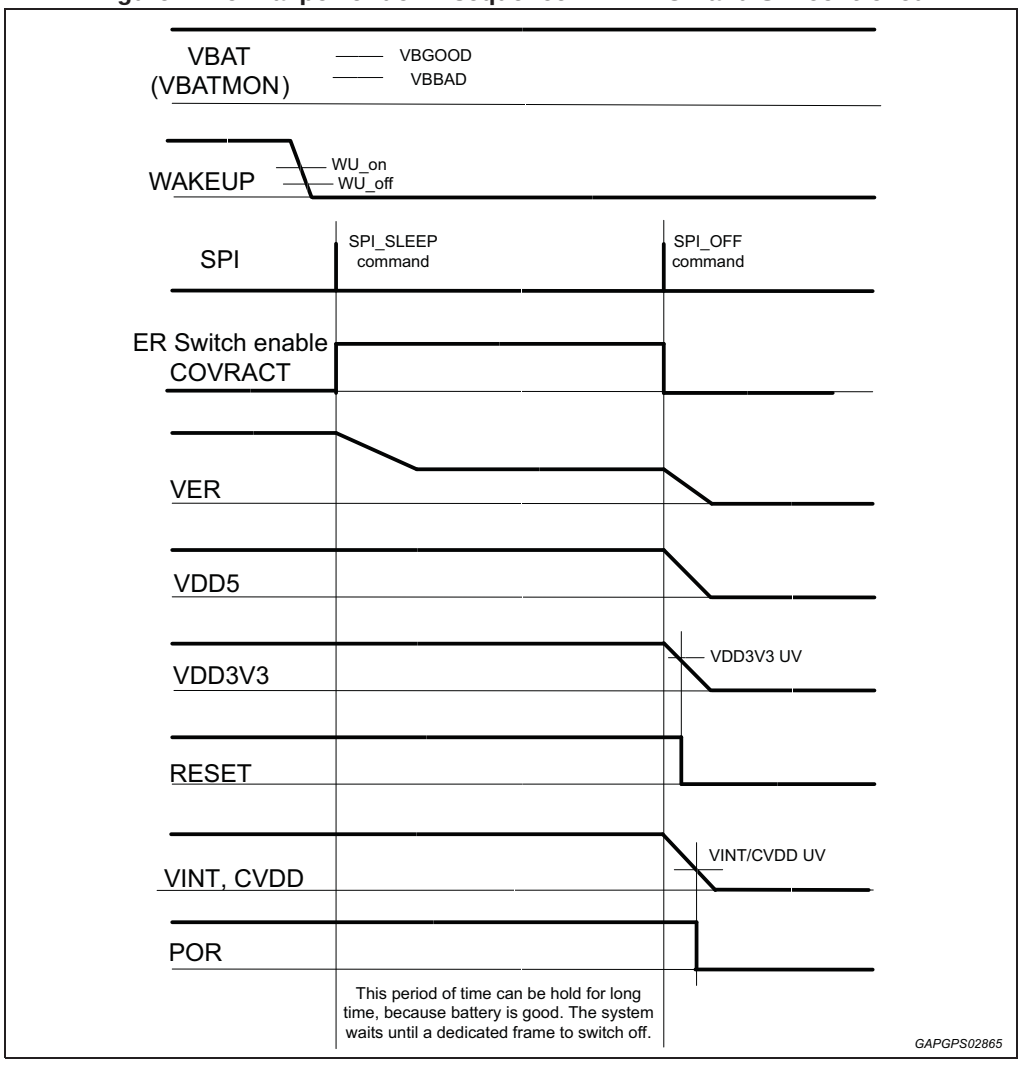
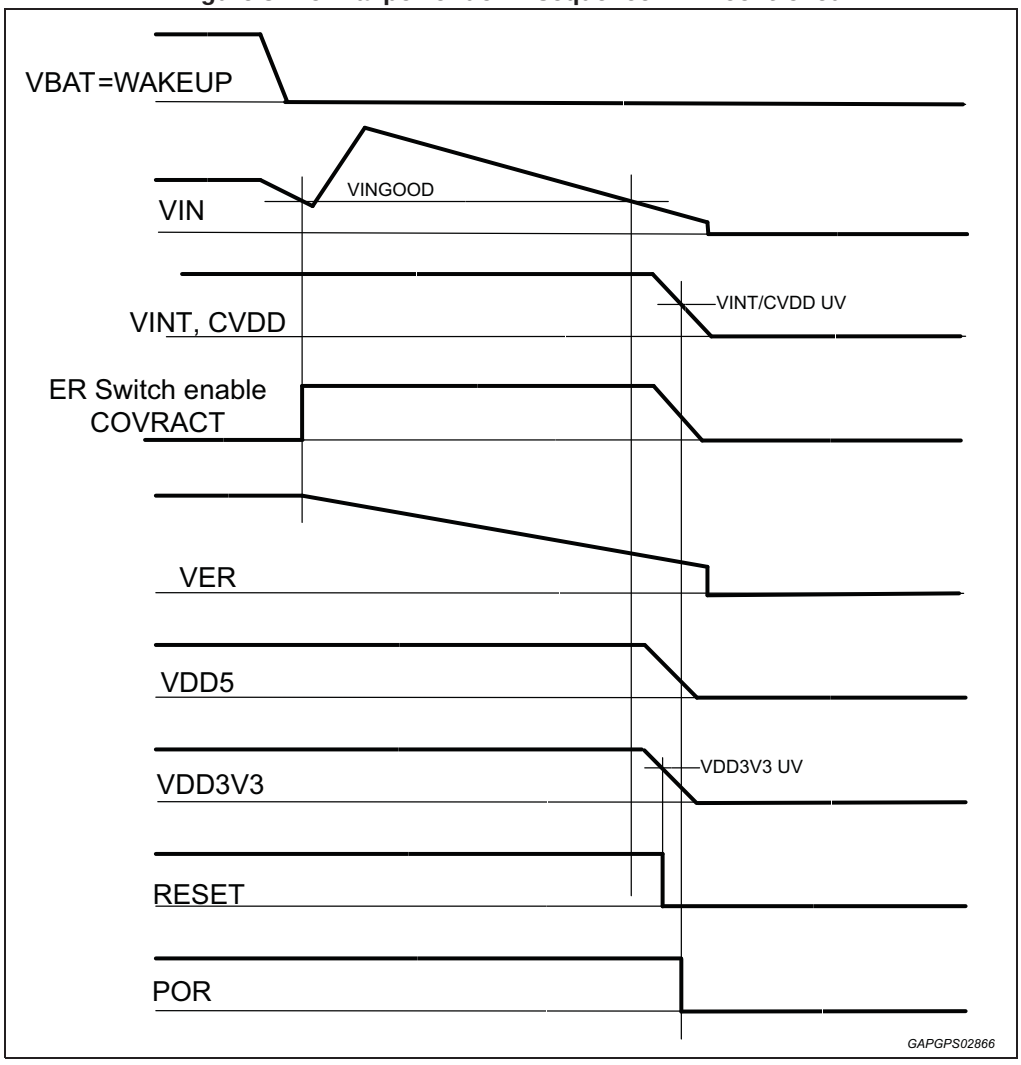


Figure 8. Normal power down sequence - VIN controlled



4.2.6 Operating states

Different states can be identified while operating the device. These states allow safe and predictable initialization, test, operation and end of line disposal of the part (scrapping).

As soon as the RESET signal is de-asserted at the beginning of the ACTIVE mode, the microcontroller powers up. At this stage, L9678 is in the Init state: during this state the device must be initialized by the controller. In particular, the watchdog timer window can be programmed during this state.

When the watchdog service begins (upon the first successful watchdog feed), the device switches to Diag state for diagnostics purposes. The remaining configuration of the device is allowed in this state, in particular for safing records and deployment masks. Several tests are also enabled while in this state and all these tests are mutually exclusive to one another. HS and LS switch tests of the squib drivers can only be processed during this diag state. Also high side safing FET can only be run during this state. When not in diag state, any

commands for squib driver switch tests will be ignored. Other checks are also performed: on the arming output to check for non stuck-at conditions on the pin and for the configured firing time. The SSM remains in this state until commanded to transition into the Safing state or Scrap state via the dedicated SPI commands.

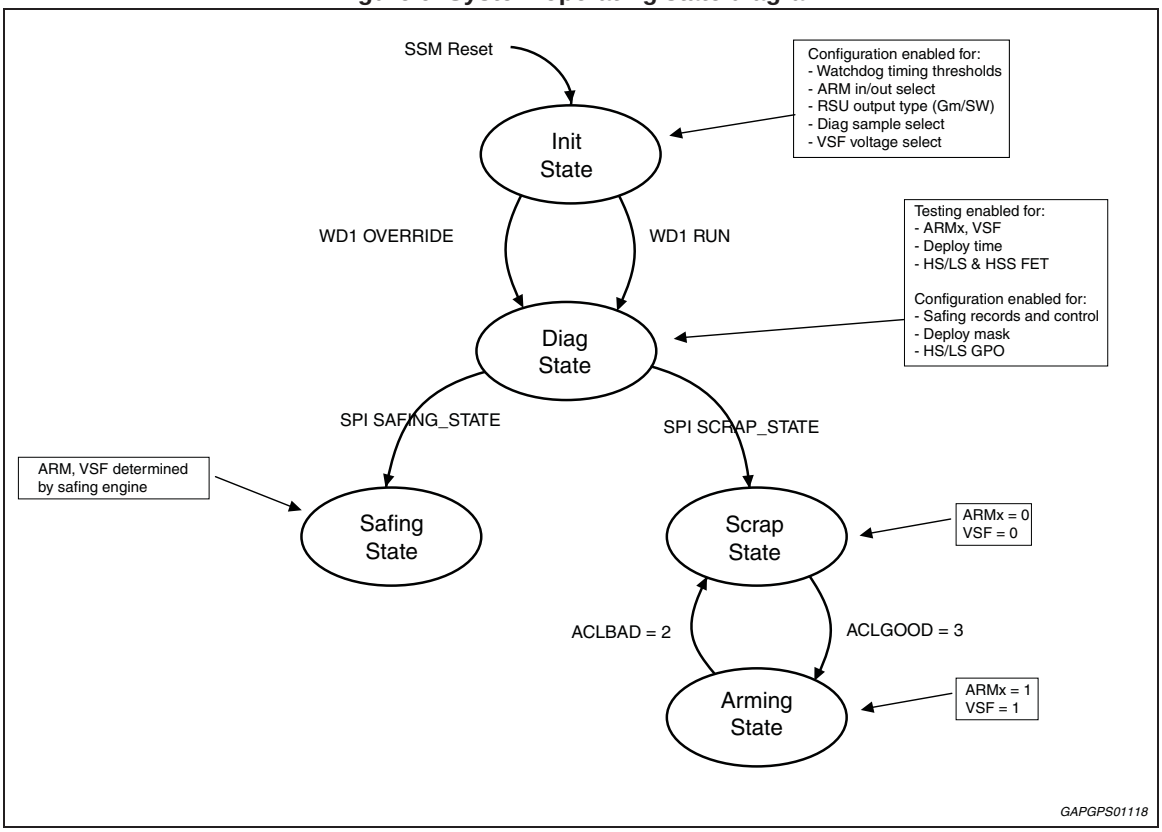
Upon reception of the SAFING_STATE command while in Diag state, the device enters Safing state. This is the primary run-time state for normal operation, and the logic performs the safing function, including monitoring of sensor data and setting of the ARM signal. The only means of exiting Safing state is by the assertion of the SSM_Reset signal.

The Scrap state is entered upon reception of the SCRAP_STATE command while in Diag state. While in Scrap state, the part allows the main microcontroller to initiate a transition to Arming state, and monitoring of the Remote Sensor SPI interface (in L9678-S) and the safing logic is disabled. From Scrap state, the device can transition to Arming state only, and the only means of moving back to Init state is through an SSM_Reset.

In order to protect from inadvertent entry into Arming state, and to prevent undesired activation of the safing signals, a dedicated mechanism is used to control entry into, and exit from Arming state. This mechanism is described further in *Section 10.7: Additional communication line*. While in Arming state, the arming output is asserted. Exit from Arming state occurs when the time-out is reached without a correct ACL signal or when SSM_Reset is asserted. Upon exit, the device re-enters Scrap state, except for the case of SSM_Reset, which results in entry into Init state.

System Operating states are shown in *Figure 9*.

Figure 9. System operating state diagram



4.3 Configurable system power control

The overall operating voltage requirements of the device are different considering the L9678 device (without VSUP regulator and remote sensor interface) or the L9678-S device (with VSUP regulator and remote sensor interface). Performance for the L9678-S device is influenced by the PSI-5 remote sensor interfaces. This function requires a minimum voltage at the channel's input (VSUP) to ensure a proper functionality for the sensor.

An integrated current generator (30 mA nominal) is used to charge the external energy reserve capacitor connected to VER pin. Any system load (regulators, interfaces, squib driver diagnostics) operate directly from battery until battery is lost. Upon detecting low or loss of battery, the crossover switch enables operation from energy reserve.

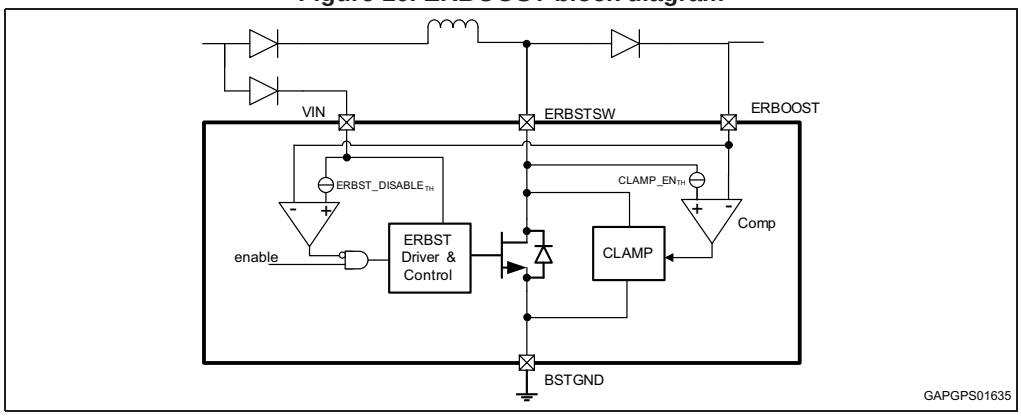
4.3.1 ERBOOST switching regulator

The L9678 IC uses an advanced energy reserve switching regulator operating at 1.882 MHz nominal. The higher switching frequency enables the user to select smaller less expensive inductors and moves the operating frequency to permit easier compliance with system emissions.

The energy reserve boost regulator charges the external system tank capacitor through an integrated fixed current source significantly reducing in-rush currents typical of large energy reserve capacitors. The boost circuit provides energy for the reserve capacitor with assumed run time load of less than 20 mA and to the VSF regulator. Once system shutdown is initiated or a loss of battery condition is diagnosed, the boost regulator is disabled so that system power can be taken from the energy reserve capacitor.

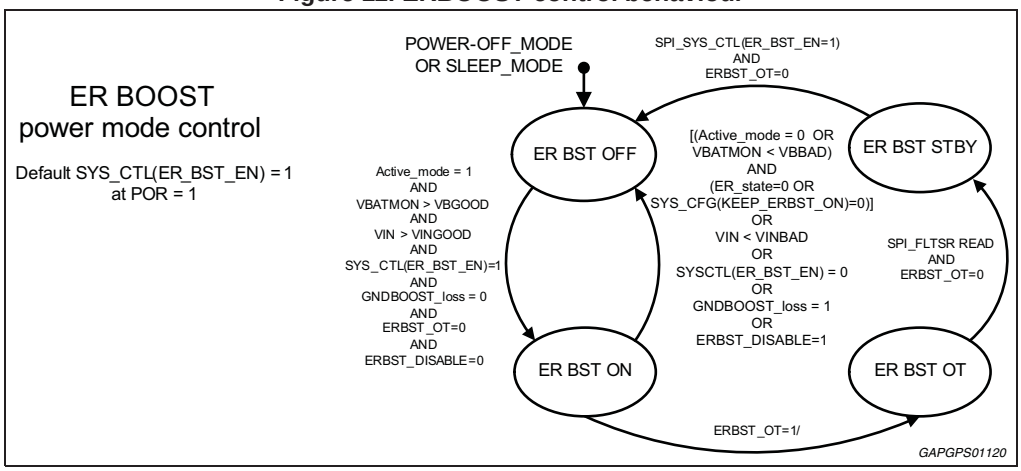
The energy reserve boost regulator defaults to 23 V at power-on and can be set to 33 V nominal by the user through an SPI command. The boost converter can also be disabled by the user through an SPI command. Enabling, disabling and setting the boost output voltage is done through the System Control (SYS_CTL) register. Boost converter diagnostics include over voltage and under voltage. The under voltage condition is reported by the ER_BST_NOK bit in the POWER_STATE register. The integrated FET featuring the boost switch is protected against short to battery by means of a thermal shutdown circuit. When thermal fault is detected the FET is switched off and latched in this state until the related fault flag ERBST_OT in the FLTSR register is read. In case of loss of ground the FET is switched off and automatically reactivated as soon as ground connection is restored. Over-voltage protection from load dump and inductive flyback is provided via an active clamp and an ER_Boost disable circuitry, see *Figure 10*.

Figure 10. ERBOOST block diagram



Normal run time power for the system is provided directly from the battery input, not from the boost. Boost energy is available to the system through the energy reserve crossover switch once battery is lost or a commanded system shutdown is initiated. By default, the ERBoost regulator is switched off once enetered in passive mode. To keep active the ERBoost also in passive mode the SPI bit SYS_CFG(KEEP_ERBST_ON) must be set to 1.

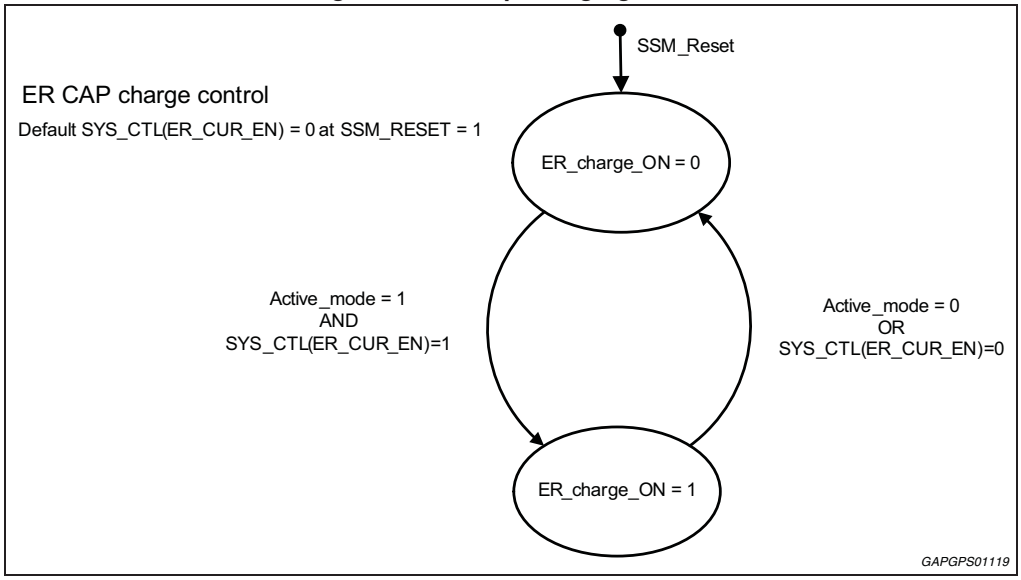
Figure 11. ERBOOST control behaviour



4.3.2 Energy reserve capacitor charging circuit

The energy reserve capacitor connected to VER pin can be charged in an efficient way by means of a current generator. Its capability is 30 mA nominal, so that for example a 2.2 mF capacitor can be charged in approximately 2 s to 24 V. The current generator is activated or deactivated by SPI command only while in ACTIVE mode. When not in ACTIVE mode, the generator is always switched off in order to decouple ERBOOST node voltage from VER reserve voltage.

Figure 12. ER cap charging circuit

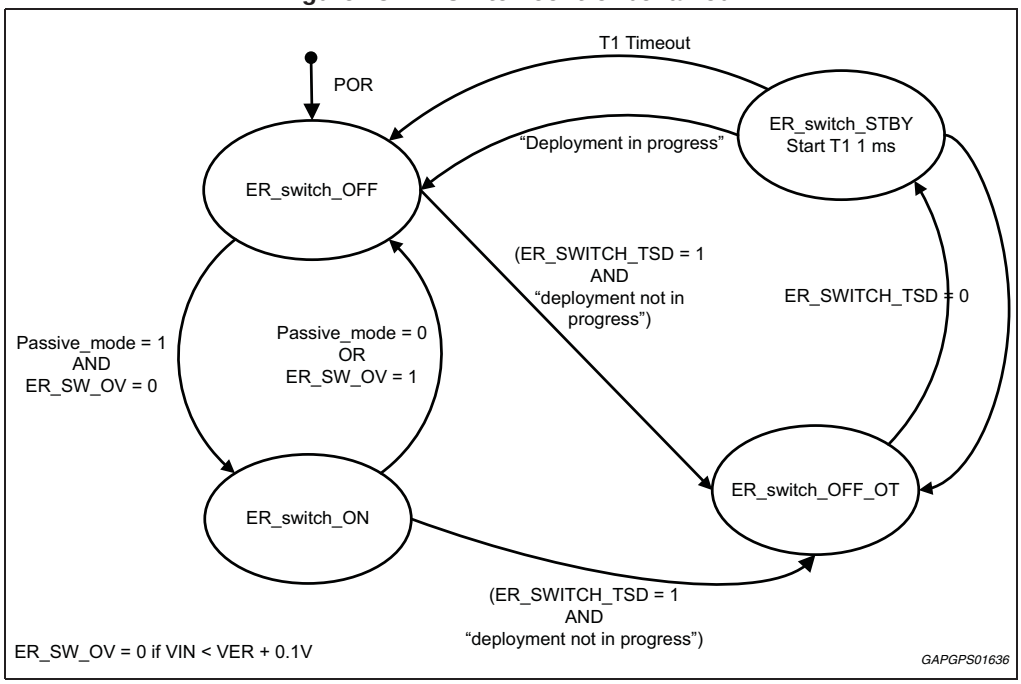


4.3.3 ER switch and COVRACT pin

L9678 has an integrated circuit that can operate as a crossover switch with $R_{ds(on)}$ = 1.5 Ω nominal. The ER switch is automatically activated upon entering the PASSIVE mode.

Voltage difference between VIN and VER is monitored in order to prevent VER back-feeding when VIN exceeds VER by 0.1V max. The ER switch is automatically deactivated upon the above mentioned overvoltage detection. The ER control implements a thermal protection and a current limitation guard to avoid in-rush charge current at ER switch enabling or at fault condition for short to ground. During PASSIVE mode the discrete digital output pin COVRACT is activated to allow for external optional cross-over switch control.

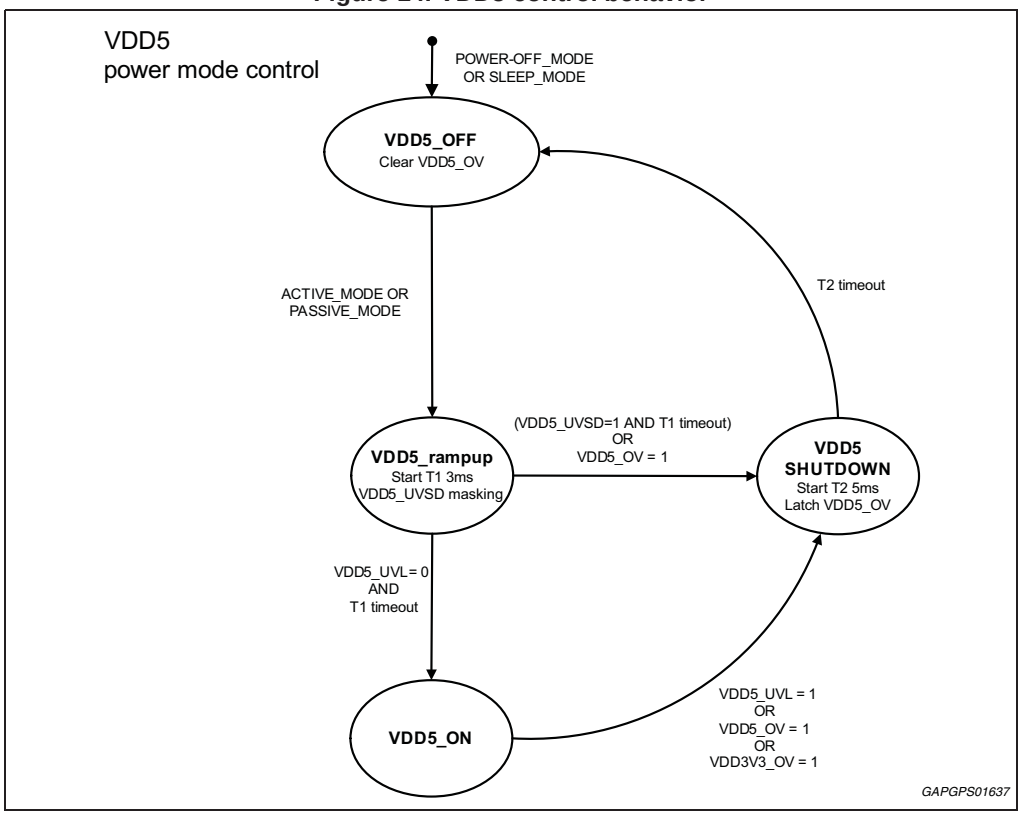
Figure 13. ER switch control behaviour



4.3.4 VDD5 linear regulator

The VDD5 linear regulator provides 5 V system voltage derived directly from battery line with an external power transistor to reduce integrated circuit power dissipation. This voltage rail is used in case a 5 V micro-controller is adopted. The stability of the regulation loop is guaranteed by use of a small external capacitor. Current limitation is provided by means of controlling output current on BVDD5 pin. The external pass transistor gives the flexibility to easily address different current loads in case of different micro-controllers. The VDD5 regulator is enabled in the ACTIVE mode and continues operation in the PASSIVE mode using power from energy reserve. VDD5 supply is monitored for system reset (see Power On Reset and Reset); voltage monitoring is based on a second redundant bandgap voltage reference.

Figure 14. VDD5 control behavior

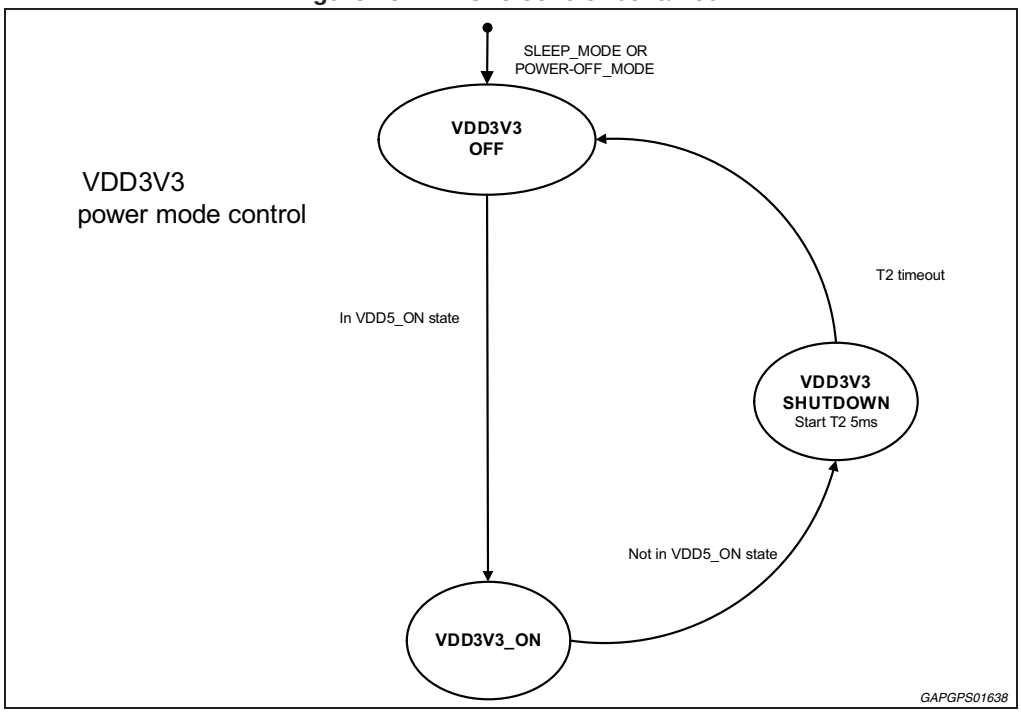


4.3.5 VDD3V3 linear regulator

The fully integrated VDD3V3 linear regulator provides 3.3 V system voltage derived directly from VDD5. This voltage rail is used in case a 3.3 V micro-controller is adopted. The stability of the regulation loop is guaranteed by use of a small external capacitor. Current limitation is implemented and its maximum current capability on VDD3V3 is 125 mA. The VDD3V3 regulator is enabled in the ACTIVE mode and continues operation in the PASSIVE mode using power from energy reserve. VDD3V3 supply is monitored for system reset (see Power On Reset and Reset); voltage monitoring is based on a second redundant bandgap voltage reference.

Note that if the VDDQ pin (digital outputs supply) is connected to the VDD3V3, and any of the digital output pins are connected to 5 V logic, there is no internal blocking diode to prevent back-feeding this 3.3 V supply.

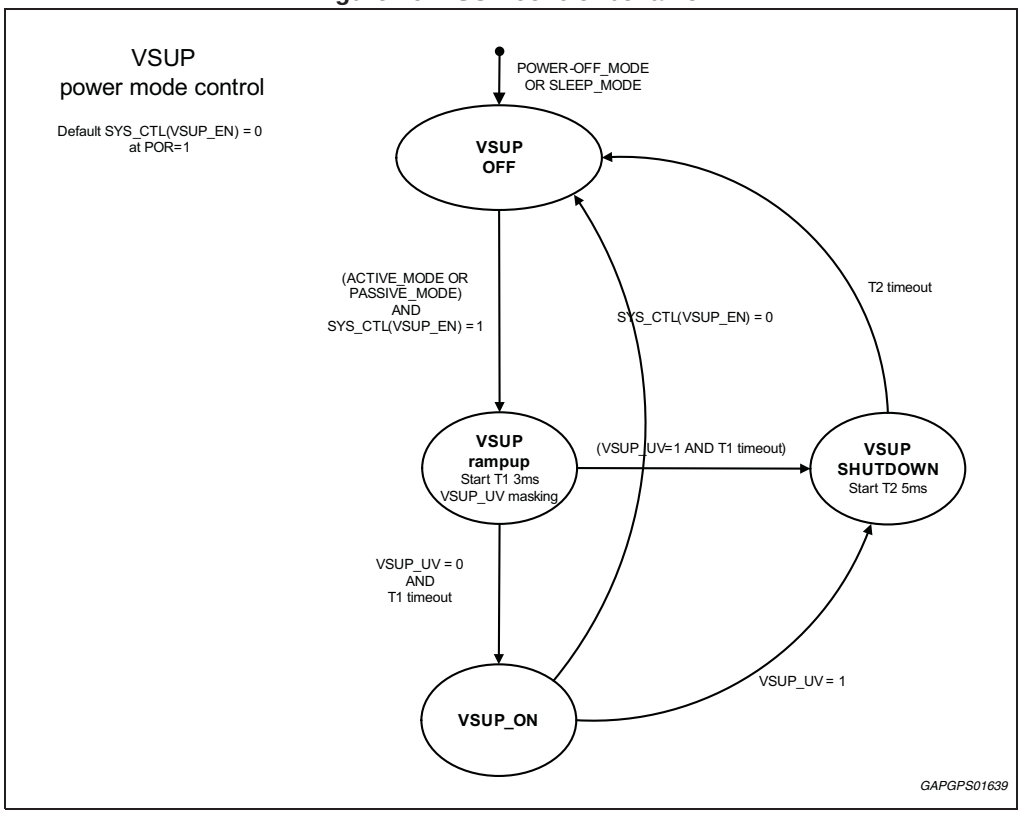
Figure 15. VDD3V3 control behaviour



4.3.6 VSUP linear regulator (optional)

The VSUP linear regulator can be used to provide 7 V derived directly from battery line with an external power transistor. This voltage rail can be used mainly to supply PSI-5 remote sensor interface. The stability of the regulation loop is guaranteed by use of a small external capacitor. Current limitation is provided by means of controlling output current on BVSUP pin. The external pass transistor gives the flexibility to easily address different current loads. The VSUP regulator is enabled in the ACTIVE mode and continues operation in the PASSIVE mode using power from energy reserve. In the case of L9678 (no remote sensor interfaces), VSUP can be externally connected to ground.

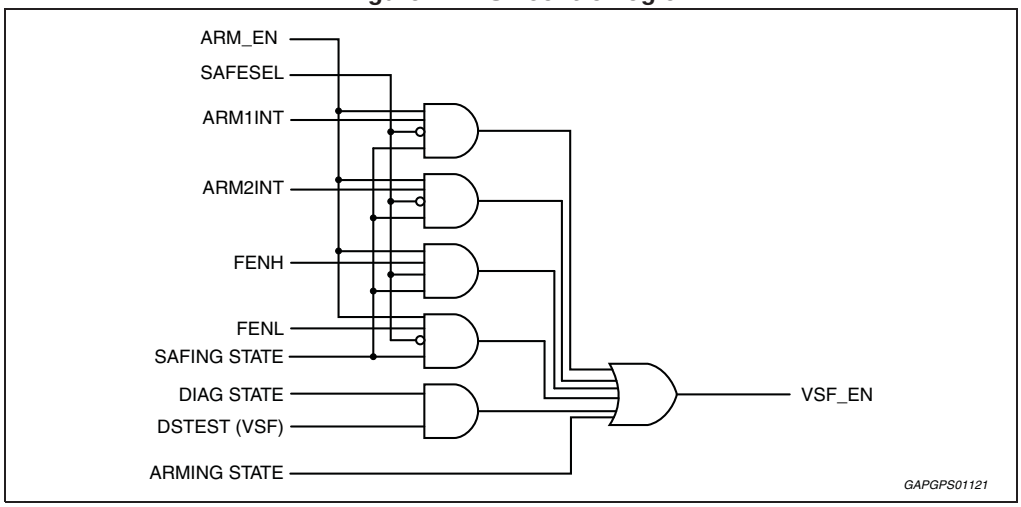
Figure 16. VSUP control behavior



4.3.7 VSF linear regulator

The fully integrated VSF linear regulator provides a 20V voltage nominal (configurable to 25V via SPI command) derived directly from ERBOOST. This voltage rail is used in case an external n-ch safing FET has to be used. The stability of the regulation loop is guaranteed by use of a small external capacitor. Current limitation is implemented. A minimum drop-out of 2V between ERBOOST and VSF is needed. VSF is enabled by the assertion of any ARMxINT signal, or by the assertion of (FENH and not (FENL)), as shown in *Figure 17*

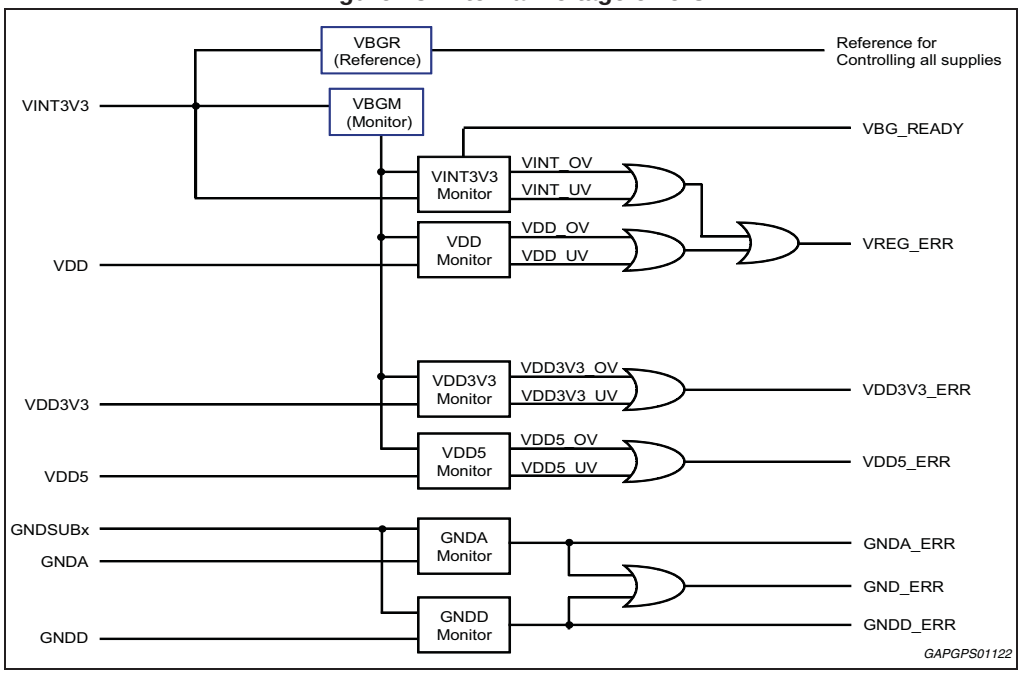
Figure 17. VSF control logic



4.4 Reset functions

The device provides reset logic to safely control system operation in the event of internal ECU failures. Several internal reset signals are generated depending on the type of failure detected. In the following figure, the voltage monitoring diagram is shown. BG_ERR reports error on the bandgap reference voltage, VREG_ERR reports errors on any of the internal regulators (VINT3V3 for 3.3 V analog circuitry, CVDD for 3.3 V digital circuitry), VDD3V3_ERR and VDD5_ERR report errors on VDD3V3 and VDD5 regulators, respectively.

Figure 18. Internal voltage errors



An active low pin output (RESET pin) is driven from the L9678 to allow resetting of external devices such as the microcontroller, sensors, and other ICs within the ECU.

Three internal reset signals are generated by the device:

- POR

  Power On Reset - This reset is asserted when a failure is detected in the internal supplies or bandgap circuits. When active, all other resets are asserted.

- WSM_RESET

  Watchdog State Machine Reset - This reset is generated when the POR is active.

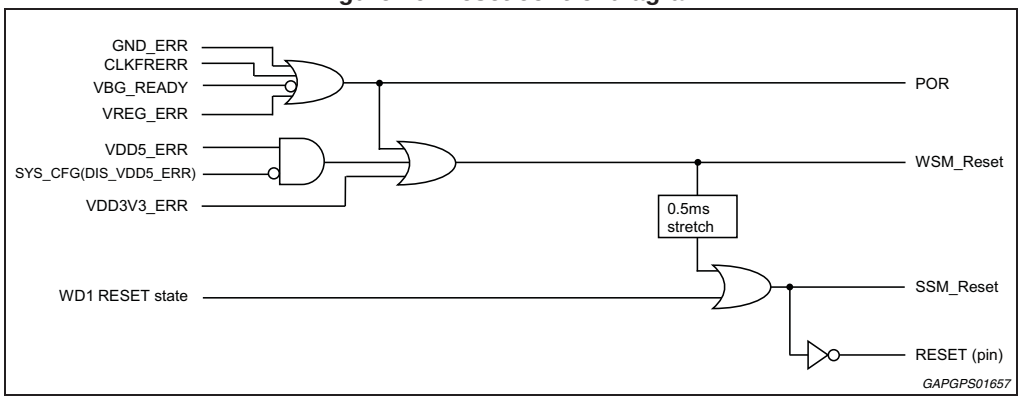
- SSM_RESET

  System State Machine Reset - This reset is asserted when the POR or the WSM_RESET are active, or when a failure is detected in either Watchdog state machine.

The RESET pin is the active-low signal driven on the output pin, and is an inverted form of SSM_RESET. The cause of a RESET activation is latched and reported into the Fault Status Register FLTSR and cleared on SPI reading.

The reset logic shall be controlled as shown in the diagram below:

Figure 19. Reset control diagram



GND_ERR is a general fault signal with the purpose of driving the device into POR when either GNDA or GNDD are shifted more than 300 mV nominal with respect to the reference ground pins GNDSUB.

5 SPI interface

The L9678 system solution device has many user selectable features controlled through serial communications by the integrated microcontroller. The SPI interface provides configuration, control and status functions for the device. The global SPI interface consists of an input shift register, output shift register and four control signals. SPI_MOSI is the data input to the input shift register. SPI_MISO is the data output from the output shift register. SPI_SCK is the clock source input while SPI_CS is the active-low chip select input.
All SPI communications are executed in exact 32 bit increments. The general format of the 32 bit transmission is shown in *Table 5*.

Data to the IC (i.e. SPI_MOSI) consists of a target read register ID (RID), a target write register ID (WID), write data parity (WPAR) and 16 bits of data (WRITE). WRITE data is the data to be written to the target write register indicated by WID. Data returned from the IC (i.e. SPI_MISO) consists of a global status word (GSW), read data parity (RPAR) and 20 bits of data (READ). READ data will be the contents of the target read register as indicated by the RID bits. The parity bits WPAR and RPAR cover all the 32 bits of the MOSI and MISO frames, respectively. Odd parity type is used.

Table 5. SPI register R/W

SPI register R/W																
	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
SPI_MOSI	GID	RID[6:0]							WID[6:0]							WPAR
SPI_MISO	GSW[10:0]											RPAR	READ[19:16]			
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SPI_MOSI	WRITE[15:0]															
SPI_MISO	READ[15:0]															

The communications is controlled through SPI_CS, enabling and disabling communication. When SPI_CS is at logic high, all SPI communication I/O is tri-stated and no data is accepted. When SPI_CS is low, data is latched on the rising edge of SPI_SCK and data is shifted on the falling edge. The SPI_MOSI pin receives serial data from the master with MSB first. Likewise for SPI_MISO, data is read MSB first, LSB last.

The L9678 IC contains a data validation method through the SPI_SCK input to keep transmissions with not exactly 32 bits from being written to the device. The SPI_SCK input counts the number of received clocks and should the clock counter exceed or count fewer than 32 clocks, the received message is discarded and a SPI_FLT bit is flagged in the Global Status Word (GSW). The SPI_FLT bit is also set in case of parity error detected on the MOSI frame. Any attempt access to a register with a forbidden access mode (read or write) is not leading to changes to the internal registers but the SPI_FLT bit is not set in this case.

The SPI interface consists of several 32-bit registers to allow for configuration, control and status of the IC as well as special manufacturing test modes. The register definition is defined by the read register ID (RID) and the write register ID (WID) as shown in Table 5 - Global SPI Register Table. Global ID bit (GID) is used to extend available register addresses, but it is shared between RID and WID; only RID and WID with the same GID value can be addressed within the same SPI word. The operating states here show in which states the SPI write command is processed.

The L9678 checks the validity of the received WID and RID fields in the SPI_MOSI frame. Should a SPI write command with WID matching a writeable register be received in an illegal operating state, the command will be discarded and the ERR_WID bit will be flagged in the next Global Status Word GSW. The ERR_WID flag is not set in case WID is addressing a read/only register. Should a SPI read command be received containing an unused RID address, the command will be discarded and the ERR_RID bit will be flagged in the current GSW.

Table 6. Global SPI register map

GID	RID / WID							Hex	R/W	Name	Description	Operating State(1)				
												Init	Diag	Ssafing	Scrap	Arming
0	0	0	0	0	0	0	0	$00	R	FLTSR	Global fault status register					
0	0	0	0	0	0	0	1	$01	R/W	SYS_CFG	Power supply configuration (regulators' output voltage selection, enable internal safing engine)	X				
0	0	0	0	0	0	1	0	$02	R/W	SYS_CTL	Register to control the power management (enable for tests in diag state, enable for power mode control bits)	X	X	X	X	X
0	0	0	0	0	0	1	1	$03	W	SPI_SLEEP	Sleep Mode command	X	X	X	X	X
0	0	0	0	0	1	0	0	$04	R	SYS_STATE	Read register to report in which state the power control state machine is and also in which Operating state we are.					
0	0	0	0	0	1	0	1	$05	R	POWER_STATE	Power state register (feedback on regulators' status and voltage thresholds)					
0	0	0	0	0	1	1	0	$06	R/W	DCR_0	Deployment configuration register		X	X	X	X
0	0	0	0	0	1	1	1	$07	R/W	DCR_1			X	X	X	X
0	0	0	0	1	0	0	0	$08	R/W	DCR_2			X	X	X	X
0	0	0	0	1	0	0	1	$09	R/W	DCR_3			X	X	X	X
0	0	0	0	1	0	1	0	$0A								
0	0	0	0	1	0	1	1	$0B								
0	0	0	0	1	1	0	0	$0C								
0	0	0	0	1	1	0	1	$0D								
0	0	0	0	1	1	1	0	$0E								
0	0	0	0	1	1	1	1	$0F								
0	0	0	1	0	0	0	0	$10								
0	0	0	1	0	0	0	1	$11								
0	0	0	1	0	0	1	0	$12	R/W	DEPCOM	Deployment command register			X		X

Table 6. Global SPI register map (continued)

GID	RID / WID								Hex	R/W	Name	Description	Operating State[1]				
													Init	Diag	Ssafing	Scrap	Arming
0	0	0	1	0	0	1	1		$13	R	DSR_0	Deployment status register					
0	0	0	1	0	1	0	0		$14	R	DSR_1						
0	0	0	1	0	1	0	1		$15	R	DSR_2						
0	0	0	1	0	1	1	0		$16	R	DSR_3						
0	0	0	1	0	1	1	1		$17								
0	0	0	1	1	0	0	0		$18								
0	0	0	1	1	0	0	1		$19								
0	0	0	1	1	0	1	0		$1A								
0	0	0	1	1	0	1	1		$1B								
0	0	0	1	1	1	0	0		$1C								
0	0	0	1	1	1	0	1		$1D								
0	0	0	1	1	1	1	0		$1E								
0	0	0	1	1	1	1	1		$1F	R	DCMTS01	Deployment current monitor register					
0	0	1	0	0	0	0	0		$20	R	DCMTS23						
0	0	1	0	0	0	0	1		$21								
0	0	1	0	0	0	1	0		$22								
0	0	1	0	0	0	1	1		$23								
0	0	1	0	0	1	0	0		$24								
0	0	1	0	0	1	0	1		$25	R/W	SPIDEPEN	Lock/Unlock command			X		X
0	0	1	0	0	1	1	0		$26	R	LP_GNDLOSS	Loss of ground fault for squib loops					
0	0	1	0	0	1	1	1		$27	R	VERSION_ID	Device version					
0	0	1	0	1	0	0	0		$28	R/W	WD_RETRY_CONF	Watchdog Retry Configuration	X				
0	0	1	0	1	0	0	1		$29								
0	0	1	0	1	0	1	0		$2A	R/W	WDTCR	Watchdog timer configuration	X				
0	0	1	0	1	0	1	1		$2B	R/W	WD1T	Watchdog key transmission & Test mode	X	X	X	X	X

Table 6. Global SPI register map (continued)

GID	RID / WID								Hex	R/W	Name	Description	Operating State[1]				
													Init	Diag	Ssafing	Scrap	Arming
0	0	1	0	1	1	0	0		$2C	R	WD_STATE	Watchdog state					
0	0	1	0	1	1	0	1		$2D	R/W	CLK_CONF	Clock Configuration	X				
0	0	1	0	1	1	1	0		$2E								
0	0	1	0	1	1	1	1		$2F								
0	0	1	1	0	0	0	0		$30	W	SCRAP_STATE	Scrap State command		X			
0	0	1	1	0	0	0	1		$31	W	SAFING_STATE	Safing State command		X			
0	0	1	1	0	0	1	0		$32								
0	0	1	1	0	0	1	1		$33								
0	0	1	1	0	1	0	0		$34								
0	0	1	1	0	1	0	1		$35	W	WD_TEST	Watchdog first and second level test	X	X	X	X	X
0	0	1	1	0	1	1	0		$36	R/W	SYSDIAGREQ	Diagnostic command for system safing		X			
0	0	1	1	0	1	1	1		$37	R	LPDIAGSTAT	Diagnostic results register for deployment loops					
0	0	1	1	1	0	0	0		$38	R/W	LPDIAGREQ	Diagnostic configuration command for deployment loops		X	X	X	X
0	0	1	1	1	0	0	1		$39	R/W	SWCTRL	DC sensor diagnostic configuration		X	X	X	X
0	0	1	1	1	0	1	0		$3A	R/W	DIAGCTRL_A	In WID is AtoD converter control register A. In RID is AtoD result A request.		X	X	X	X
0	0	1	1	1	0	1	1		$3B	R/W	DIAGCTRL_B	In WID is AtoD converter control register B. In RID is AtoD result B request.		X	X	X	X
0	0	1	1	1	1	0	0		$3C	R/W	DIAGCTRL_C	In WID is AtoD converter control register C. In RID is AtoD result C request.		X	X	X	X
0	0	1	1	1	1	0	1		$3D	R/W	DIAGCTRL_D	In WID is AtoD converter control register D. In RID is AtoD result D request.		X	X	X	X
0	0	1	1	1	1	1	0		$3E								
0	0	1	1	1	1	1	1		$3F								
0	1	0	0	0	0	0	0		$40								

Table 6. Global SPI register map (continued)

GID	RID / WID							Hex	R/W	Name	Description	Operating State(1)				
												Init	Diag	Ssafing	Scrap	Arming
0	1	0	0	0	0	0	1	$41								
0	1	0	0	0	0	1	0	$42	R/W	GPOCR	General Purpose Output configuration	X	X			
0	1	0	0	0	0	1	1	$43	R/W	GPOCTRL0	General Purpose Output control register	X	X	X	X	X
0	1	0	0	0	1	0	0	$44	R/W	GPOCTRL1	General Purpose Output control register	X	X	X	X	X
0	1	0	0	0	1	0	1	$45								
0	1	0	0	0	1	1	0	$46	R	GPOFLTSR	General Purpose Output fault status register					
0	1	0	0	0	1	1	1	$47	R	ISOFLTSR	ISO9141 fault status register					
0	1	0	0	1	0	0	0	$48								
0	1	0	0	1	0	0	1	$49								
0	1	0	0	1	0	1	0	$4A	R/W	RSCR1	PSI5 configuration register		X			
0	1	0	0	1	0	1	1	$4B	R/W	RSCR2			X			
0	1	0	0	1	1	0	0	$4C								
0	1	0	0	1	1	0	1	$4D								
0	1	0	0	1	1	1	0	$4E	R/W	RSCTRL	Remote sensor control register		X	X	X	X
0	1	0	0	1	1	1	1	$4F								
0	1	0	1	0	0	0	0	$50	R	RSDR1	Remote sensor data and fault flag registers					
0	1	0	1	0	0	0	1	$51	R	RSDR2						
0	1	0	1	0	0	1	0	$52								
0	1	0	1	0	0	1	1	$53								
0	1	0	1	0	1	0	0	$54								
0	1	0	1	0	1	0	1	$55								
0	1	0	1	0	1	1	0	$56								
0	1	0	1	0	1	1	1	$57								
0	1	0	1	1	0	0	0	$58								
0	1	0	1	1	0	0	1	$59								

Table 6. Global SPI register map (continued)

GID	RID / WID							Hex	R/W	Name	Description	Operating State[1]				
												Init	Diag	Ssafing	Scrap	Arming
0	1	0	1	1	0	1	0	$5A								
0	1	0	1	1	0	1	1	$5B								
0	1	0	1	1	1	0	0	$5C								
0	1	0	1	1	1	0	1	$5D								
0	1	0	1	1	1	1	0	$5E								
0	1	0	1	1	1	1	1	$5F								
0	1	1	0	0	0	0	0	$60								
0	1	1	0	0	0	0	1	$61								
0	1	1	0	0	0	1	0	$62								
0	1	1	0	0	0	1	1	$63								
0	1	1	0	0	1	0	0	$64								
0	1	1	0	0	1	0	1	$65								
0	1	1	0	0	1	1	0	$66	R/W	SAF_ALGO_CONF	Safing Algorithm configuration register		X			
0	1	1	0	0	1	1	1	$67								
0	1	1	0	1	0	0	0	$68								
0	1	1	0	1	0	0	1	$69								
0	1	1	0	1	0	1	0	$6A	R	ARM_STATE	Status of internal arming signals FENH, FENL, ARMx					
0	1	1	0	1	0	1	1	$6B								
0	1	1	0	1	1	0	0	$6C								
0	1	1	0	1	1	0	1	$6D								
0	1	1	0	1	1	1	0	$6E	R/W	LOOP_MATRIX_ARM1	Assignment of ARM 1 pin to which LOOPS		X			
0	1	1	0	1	1	1	1	$6F	R/W	LOOP_MATRIX_ARM2	Assignment of ARM 2 pin to which LOOPS		X			
0	1	1	1	0	0	0	0	$70								
0	1	1	1	0	0	0	1	$71								

Table 6. Global SPI register map (continued)

GID	RID / WID							Hex	R/W	Name	Description	Operating State[1]				
												Init	Diag	Ssafing	Scrap	Arming
0	1	1	1	0	0	1	0	$72								
0	1	1	1	0	0	1	1	$73	R	AEPSTS_ARM1	Arming pulse stretch timer value					
0	1	1	1	0	1	0	0	$74	R	AEPSTS_ARM2						
0	1	1	1	0	1	0	1	$75								
0	1	1	1	0	1	1	0	$76								
0	1	1	1	0	1	1	1	$77								
0	1	1	1	1	0	0	0	$78								
0	1	1	1	1	0	0	1	$79								
0	1	1	1	1	0	1	0	$7A								
0	1	1	1	1	0	1	1	$7B								
0	1	1	1	1	1	0	0	$7C								
0	1	1	1	1	1	0	1	$7D								
0	1	1	1	1	1	1	0	$7E								
0	1	1	1	1	1	1	1	$7F	R/W	SAF_ENABLE	Safing record enable		X	X	X	X
1	0	0	0	0	0	0	0	$80	R/W	SAF_REQ_MASK_1	Safing record request mask		X			
1	0	0	0	0	0	0	1	$81	R/W	SAF_REQ_MASK_2			X			
1	0	0	0	0	0	1	0	$82	R/W	SAF_REQ_MASK_3			X			
1	0	0	0	0	0	1	1	$83	R/W	SAF_REQ_MASK_4			X			
1	0	0	0	0	1	0	0	$84								
1	0	0	0	0	1	0	1	$85								
1	0	0	0	0	1	1	0	$86								
1	0	0	0	0	1	1	1	$87								
1	0	0	0	1	0	0	0	$88								
1	0	0	0	1	0	0	1	$89								
1	0	0	0	1	0	1	0	$8A								

Table 6. Global SPI register map (continued)

GID	RID / WID							Hex	R/W	Name	Description	Operating State(1)				
												Init	Diag	Ssafing	Scrap	Arming
1	0	0	0	1	0	1	1	$8B			Safing record request mask					
1	0	0	0	1	1	0	0	$8C								
1	0	0	0	1	1	0	1	$8D								
1	0	0	0	1	1	1	0	$8E								
1	0	0	0	1	1	1	1	$8F								
1	0	0	1	0	0	0	0	$90								
1	0	0	1	0	0	0	1	$91								
1	0	0	1	0	0	1	0	$92								
1	0	0	1	0	0	1	1	$93	R/W	SAF_REQ_TARGET_1	Safing record request target		X			
1	0	0	1	0	1	0	0	$94	R/W	SAF_REQ_TARGET_2			X			
1	0	0	1	0	1	0	1	$95	R/W	SAF_REQ_TARGET_3			X			
1	0	0	1	0	1	1	0	$96	R/W	SAF_REQ_TARGET_4			X			
1	0	0	1	0	1	1	1	$97								
1	0	0	1	1	0	0	0	$98								
1	0	0	1	1	0	0	1	$99								
1	0	0	1	1	0	1	0	$9A								
1	0	0	1	1	0	1	1	$9B								
1	0	0	1	1	1	0	0	$9C								
1	0	0	1	1	1	0	1	$9D								
1	0	0	1	1	1	1	0	$9E								
1	0	0	1	1	1	1	1	$9F								
1	0	1	0	0	0	0	0	$A0								
1	0	1	0	0	0	0	1	$A1								
1	0	1	0	0	0	1	0	$A2								
1	0	1	0	0	0	1	1	$A3								

Table 6. Global SPI register map (continued)

GID	RID / WID								Hex	R/W	Name	Description	Operating State[1]				
													Init	Diag	Ssafing	Scrap	Arming
1	0	1	0	0	1	0	0	$A4				Safing record request target					
1	0	1	0	0	1	0	1	$A5									
1	0	1	0	0	1	1	0	$A6	R/W	SAF_RESP_MASK_1	Safing record response mask		X				
1	0	1	0	0	1	1	1	$A7	R/W	SAF_RESP_MASK_2			X				
1	0	1	0	1	0	0	0	$A8	R/W	SAF_RESP_MASK_3			X				
1	0	1	0	1	0	0	1	$A9	R/W	SAF_RESP_MASK_4			X				
1	0	1	0	1	0	1	0	$AA									
1	0	1	0	1	0	1	1	$AB									
1	0	1	0	1	1	0	0	$AC									
1	0	1	0	1	1	0	1	$AD									
1	0	1	0	1	1	1	0	$AE									
1	0	1	0	1	1	1	1	$AF									
1	0	1	1	0	0	0	0	$B0									
1	0	1	1	0	0	0	1	$B1									
1	0	1	1	0	0	1	0	$B2									
1	0	1	1	0	0	1	1	$B3									
1	0	1	1	0	1	0	0	$B4									
1	0	1	1	0	1	0	1	$B5									
1	0	1	1	0	1	1	0	$B6									
1	0	1	1	0	1	1	1	$B7									
1	0	1	1	1	0	0	0	$B8									
1	0	1	1	1	0	0	1	$B9	R/W	SAF_RESP_TARGET_1	Safing record response target		X				
1	0	1	1	1	0	1	0	$BA	R/W	SAF_RESP_TARGET_2			X				
1	0	1	1	1	0	1	1	$BB	R/W	SAF_RESP_TARGET_3			X				
1	0	1	1	1	1	0	0	$BC	R/W	SAF_RESP_TARGET_4			X				

Table 6. Global SPI register map (continued)

GID	RID / WID								Hex	R/W	Name	Description	Operating State[1]				
													Init	Diag	Ssafing	Scrap	Arming
1	0	1	1	1	1	0	1		$BD			Safing record response target					
1	0	1	1	1	1	1	0		$BE								
1	0	1	1	1	1	1	1		$BF								
1	1	0	0	0	0	0	0		$C0								
1	1	0	0	0	0	0	1		$C1								
1	1	0	0	0	0	1	0		$C2								
1	1	0	0	0	0	1	1		$C3								
1	1	0	0	0	1	0	0		$C4								
1	1	0	0	0	1	0	1		$C5								
1	1	0	0	0	1	1	0		$C6								
1	1	0	0	0	1	1	1		$C7								
1	1	0	0	1	0	0	0		$C8								
1	1	0	0	1	0	0	1		$C9								
1	1	0	0	1	0	1	0		$CA								
1	1	0	0	1	0	1	1		$CB								
1	1	0	0	1	1	0	0		$CC	R/W	SAF_DATA_MASK_1	Safing record data mask		X			
1	1	0	0	1	1	0	1		$CD	R/W	SAF_DATA_MASK_2			X			
1	1	0	0	1	1	1	0		$CE	R/W	SAF_DATA_MASK_3			X			
1	1	0	0	1	1	1	1		$CF	R/W	SAF_DATA_MASK_4			X			
1	1	0	1	0	0	0	0		$D0								
1	1	0	1	0	0	0	1		$D1								
1	1	0	1	0	0	1	0		$D2								
1	1	0	1	0	0	1	1		$D3								
1	1	0	1	0	1	0	0		$D4								
1	1	0	1	0	1	0	1		$D5								

Table 6. Global SPI register map (continued)

GID	RID / WID								Hex	R/W	Name	Description	Operating State(1)				
													Init	Diag	Ssafing	Scrap	Arming
1	1	0	1	0	1	1	0		$D6			Safing record data mask					
1	1	0	1	0	1	1	1		$D7								
1	1	0	1	1	0	0	0		$D8								
1	1	0	1	1	0	0	1		$D9								
1	1	0	1	1	0	1	0		$DA								
1	1	0	1	1	0	1	1		$DB								
1	1	0	1	1	1	0	0		$DC								
1	1	0	1	1	1	0	1		$DD								
1	1	0	1	1	1	1	0		$DE								
1	1	0	1	1	1	1	1		$DF	R/W	SAF_THRESHOLD_1	Safing record threshold		X			
1	1	1	0	0	0	0	0		$E0	R/W	SAF_THRESHOLD_2			X			
1	1	1	0	0	0	0	1		$E1	R/W	SAF_THRESHOLD_3			X			
1	1	1	0	0	0	1	0		$E2	R/W	SAF_THRESHOLD_4			X			
1	1	1	0	0	0	1	1		$E3								
1	1	1	0	0	1	0	0		$E4								
1	1	1	0	0	1	0	1		$E5								
1	1	1	0	0	1	1	0		$E6								
1	1	1	0	0	1	1	1		$E7								
1	1	1	0	1	0	0	0		$E8								
1	1	1	0	1	0	0	1		$E9								
1	1	1	0	1	0	1	0		$EA								
1	1	1	0	1	0	1	1		$EB								
1	1	1	0	1	1	0	0		$EC								
1	1	1	0	1	1	0	1		$ED								
1	1	1	0	1	1	1	0		$EE								

Table 6. Global SPI register map (continued)

GID	RID / WID							Hex	R/W	Name	Description	Operating State[1]				
												Init	Diag	Ssafing	Scrap	Arming
1	1	1	0	1	1	1	1	$EF	R/W	SAF_CONTROL_1	Safing record control		X			
1	1	1	1	0	0	0	0	$F0	R/W	SAF_CONTROL_2			X			
1	1	1	1	0	0	0	1	$F1	R/W	SAF_CONTROL_3			X			
1	1	1	1	0	0	1	0	$F2	R/W	SAF_CONTROL_4			X			
1	1	1	1	0	0	1	1	$F3								
1	1	1	1	0	1	0	0	$F4								
1	1	1	1	0	1	0	1	$F5								
1	1	1	1	0	1	1	0	$F6								
1	1	1	1	0	1	1	1	$F7								
1	1	1	1	1	0	0	0	$F8								
1	1	1	1	1	0	0	1	$F9								
1	1	1	1	1	0	1	0	$FA								
1	1	1	1	1	0	1	1	$FB								
1	1	1	1	1	1	0	0	$FC								
1	1	1	1	1	1	0	1	$FD								
1	1	1	1	1	1	1	0	$FE								
1	1	1	1	1	1	1	1	$FF	R	SAF_CC	Safing record compare complete					

1. A check mark indicates in which operating state a WRITE-command is valid.

5.1 Global SPI register

A summary of all the read/write registers contained within the SPI map are shown below and are further referenced throughout the specification as they apply. The SPI register tables also specify the effect of the internal reset signals assertion on each bit field (the symbol '-' is used to indicate that the register is not affected by the relevant reset signal).

Global status word

L9678 contains an 11-bit word that returns global status information. The GSW is the most significant 11 bits of SPI_MISO data.

ID	R/W/RW
-	R

Register name	Description
GSW	Global Status Word

MISO BIT	31	30	29	28	27	26	25	24	23	22	21
MISO	SPIFLT	DEPOK	RSFLT	WDTDIS_S	ERSTATE	POWERFLT	FLT	CONVRDY2	CONVRDY1	ERR_WID	ERR_RID
GSW BIT	10	9	8	7	6	5	4	3	2	1	0

Table 7. Global status word (GSW)

Bit	Name	POR	WSM	SSM	Description
10	SPIFLT	0	0	0	SPI Fault, set if previous SPI frame had wrong parity check or wrong number of bits, cleared upon read 0 No fault 1 Fault
9	DEPOK	0	0	0	General Deployment Successful Flag, logical OR of the corresponding CHxDS bits (bit 15) in DSRx Registers 0 All the DSRx-CHDS bits are 0 1 At least one of the DSRx-CHDS bits is 1
8	RSFLT	0	0	0	Remote Sensor Interface Fault Present, logical OR of the corresponding FLTBIT bits (bit 15) in RSDRx Registers 0 All the RSDRx-FLTBIT bits are 0 1 At least one of the RSDRx-FLTBIT bits is 1
7	WDTDIS_S	0	0	0	State of WDTDIS pin 0 WDTDIS = 0 1 WDTDIS = 1

Table 7. Global status word (GSW) (continued)

Bit	Name	POR	WSM	SSM	Description
6	ERSTATE	0	0	0	Set when Power mode state machine is in ER state 0 Power mode state machine is not in ER state 1 Power mode state machine is in ER state
5	POWERFLT	0	0	0	Fault present in Power State Register, logical OR between bits from 18 to 9 of POWER_STATE Register 0 All the bits from 18 to 9 in the POWER_STATE Registers are 0s 1 At least one of the bits from 18 to 9 in the POWER_STATE Registers is 1
4	FLT	1	1	1	Fault present in Fault Status Register (FLTSR), logical OR between all bits of FLTSR 0 All the bits in the Fault Status Register (FLTSR) are 0s 1 At least one of the bits in the Fault Status Register (FLTSR) is 1
3	CONVRDY2	0	0	0	ADC Conversion of request 3 or 4 has been completed so new results are available 0 No new data available 1 New data available
2	CONVRDY1	0	0	0	ADC Conversion of request 1 or 2 has been completed so new results are available 0 No new data available 1 New data available
1	ERR_WID	0	0	0	Write address of previous SPI frame is not permitted in current operating phase (INIT, DIAG, SAFING, SCRAP, ARMING) 0 No Error 1 Error
0	ERR_RID	0	0	0	Read address received in the actual SPI frame is unused so data in the response is don't care 0 No Error 1 Error

Read/write register

5.1.1 Fault status register (FLTSR)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	ERBST_OT	CLKFRERR	-	0	0	0	OTPCRC_ERR	0	0	0	WD1_LO	WD1_TM	WD1_WDR	0	WSMRST	SSMRST	0	POR

Address: 00

Type: R

Buffer: $0000

Reset: -

	POR	WSM	SSM	
EBST_OT	0	-	-	ER Boost over-temperature bit Set when over-temp condition detected, cleared on SPI read or POR=1 0 No Fault 1 Fault
CLKFRERR	0	-	-	Internal oscillator cross-check error bit Set when osc error detected, cleared on SPI read or POR=1 0 No Fault 1 Fault
OTPCRC_ERR	0	-	-	OTP CRC error bit Set when OTP error detected (tested at release of POR), cleared by POR=1 0 No Fault 1 Fault
WD1_LO	0	0	-	WD1 lockout - reflects WD1 lockout state Set and cleared per Watchdog Timer Flow Diagram 0 WD1 Lockout inactive 1 WD1 Lockout active
WD1_TM	0	0	0	WD1 test mode - reflects WD1TM signal state Set and cleared per Watchdog Timer Flow Diagram 0 WD1TM=0 1 WD1TM=1

WD1_WDR	0	0	-	WD1 reset latch Set and cleared per Watchdog Timer Flow Diagram 0 WD1_WDR signal = 0 1 WD1_WDR signal = 1
WSMRST	1	1	-	Watchdog state machine reset Set when WSM reset goes to '1', cleared upon SPI read 0 WSM reset has not occurred 1 WSM Reset has occurred
SSMRST	1	1	1	Safing state machine reset Set when SSM reset goes to '1', cleared upon SPI read 0 SSM reset has not occurred 1 SSM Reset has occurred
POR	1	-	-	Power on Reset Set when POR goes to '1', cleared upon SPI read 0 POR reset has not occurred 1 POR Reset has occurred

5.1.2 System configuration register (SYS_CFG)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				EN_AUTO_SWITCH_OFF	DIS_VDD5_ERR	X	KEEP_ERBST_ON	X	V_DIAG	-	SQMEAS		VMEAS		X	SAFESEL	VSF_V	X	WD1_TOVR
MISO	0	0	0	0	EN_AUTO_SWITCH_OFF	DIS_VDD5_ERR	0	KEEP_ERBST_ON	0	V_DIAG	-	SQMEAS		VMEAS		0	SAFESEL	VSF_V	0	WD1_TOVR

Address: 01

Type: RW

Buffer: $0100

Reset: $0002

	POR	WSM	SSM	
EN_AUTO_SWITCH_OFF	0	0	0	Enable auto switch off ISRC current source and DCS regulator after measurement completion 0 Auto switch off disabled 1 Auto switch off enabled
DIS_VDD5_ERR	0	0	-	Disable VDD5 OV/UV to generate reset 0 OV/UV generate reset 1 OV/UV don’t generate reset
KEEP_ERBST_ON	0	0	0	ER Boost behaviour during ER state 0 ER Boost is disabled 1 ER Boost stay enabled
HI_LEV_DIAG_TIME	0	0	0	Selection of duration of high level squib diagnostics 0 Short time (see high level diag diagram) 1 Long time (see high level diag diagram)
SQMEAS	00	00	00	Sample number in DC sensor, squib measurement and temperature conversions Updated by SSM_RESET or SPI write

0 8 samples
1 16 samples
10 4 samples
11 1 sample

VMEAS	00	00	00	Sample number in any other voltage measurement conversions Updated by SSM_RESET or SPI write Updated by SSM_RESET or SPI write 0 4 samples 1 16 samples 10 8 samples 11 1 sample
SAFESEL	1	1	1	Safing engine mode select Updated by SSM_RESET or SPI write 0 Internal safing engine 1 external safing engine
VSF_V	0	0	0	VSF voltage select Updated by SSM_RESET or SPI write 0 20V 1 25V
WD1_TOVR	0	0	-	Override of initial 500ms time-out of WD1 state machine Set and cleared per Watchdog Timer Flow Diagram 0 time-out is active 1 time-out is disabled

5.1.3 System control register (SYS_CTL)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	VIN_TH_SEL	VBATMON_TH_SEL		ER_BST_V	X	ER_CUR_EN	ER_BST_EN	VSUP_EN	SPI_OFF	X	X	X	X
MISO	0	0	0	0	-	0	0	VIN_TH_SEL	VBATMON_TH_SEL		ER_BST_V	0	ER_CUR_EN	ER_BST_EN	VSUP_EN	SPI_OFF	0	0	0	0

Address: 02

Type: RW

Buffer: $0200

Reset: $0004

	POR	WSM	SSM	
VIN_TH_SEL	0	0	0	VIN comparators threshold selector 0 5.5V 1 7.5V
VBATMON_TH_SEL	00	00	00	VBATMON comparators threshold selector 00 6V 01 6.8V 10 8V 11 8.8V
ER_BST_V	0	0	0	ER Boost voltage select Updated by SSM_RESET or SPI write 0 set 23V boost 1 set 33V boost
ER_CUR_EN	0	0	0	ER charge / discharge control Updated by SSM_RESET or SPI write 0 ER current source OFF request 1 ER current source ON request
ER_BST_EN	1	1	1	Boost enable Updated by SSM_RESET or SPI write

0 ER_BOOST OFF request
1 ER_BOOST ON request

VSUP_EN	0	0	0	Supplemental supply for satellites Updated by SSM_RESET or SPI write 0 VSUP commanded off 1 VSUP
SPI_OFF	0	0	0	Go to POWER OFF state from POWERMODE SHUTDOWN state Updated by SSM_RESET or SPI write while in POWERMODE SHUTDOWN state 0 no effect 1 transition to POWER OFF state

5.1.4 SPI Sleep command register (SPI_SLEEP)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				$3C95															
MISO	0	0	0	0	-	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address: 03

Type: W

Buffer: -

Reset: $0006

	POR	WSM	SSM	
SLEEP_MODE	N/A	N/A	N/A	Non-latched command that allows transition into POWERMODE_SHUTDOWN state according to the Power Control State Flow Diagram

5.1.5 System status register (SYS_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	OPER_CTL_STATE			0	0	0	0	0	POWER_CTL_STATE		

Address: 04

Type: R

Buffer: $0400

Reset: -

	POR	WSM	SSM	
OPER_CTL_STATE[2:0]	000	000	000	Reports Operating Control State Updated per Power Up Phases diagram 000 = INIT 001 = DIAG 010 = SAFING 011 = SCRAP 100 = ARMING 101 unused 110 unused 111 unused
POWER_CTL_STATE[2:0]	000	-	-	Reports Power Control State Updated per Power Control State Flow Diagram 000 = AWAKE 001 = STARTUP 010 = RUN 011 = ER 100 = POWER MODE SHUTDOWN 101 unused 110 unused 111 unused

5.1.6 Power state register (POWER_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	WAKEUP	VBBAD	NOT_VBGOOD	VINBAD	NOT_VINGOOD	VDD3V3_UV	VDD3V3_OV	ER_BST_NOK	VDD5_UV	VDD5_OV	VSUP_NOK	ER_BST_ON	ER_CHRG_ON	0	0	ER_SW_ON	VDD5_ACT	VSUP_ACT	VDD3V3_ACT	VSF_ACT

Address: 05

Type: R

Buffer: $0500

Reset: -

	POR	WSM	SSM	
WAKEUP	-	-	-	WAKEUP pin status Set and cleared based on voltage 0 WAKEUP pin < WU_off 1 WAKEUP pin > WU_on
VBBAD	-	-	-	VBATMON bad pin status Set and cleared based on voltage 1 VBATMON < VBBAD 0 VBATMON > VBBAD
NOT_VBGOOD	-	-	-	VBATMON good pin status Set and cleared based on voltage 1 VBATMON < VBGOOD 0 VBATMON > VBGOOD
VINBAD	-	-	-	VIN bad pin status Set and cleared based on voltage 0 VIN > VINBAD 1 VIN < VINBAD
NOT_VINGOOD	-	-	-	VIN good pin status Set and cleared based on voltage 0 VIN > VINGOOD 1 VIN < VINGOOD
VDD3V3_UV	-	-	-	VDD3V3 bad pin status

				Set based on voltage, cleared on SPI read 0 VDD3V3 > VDD3V3_UV 1 VDD3V3 < VDD3V3_UV
VDD3V3_OV	-	-	-	VDD3V3 bad pin status Set based on voltage, cleared on SPI read 0 VDD3V3 < VDD3V3_OV 1 VDD3V3 > VDD3V3_OV
ER_BST_NOK	-	-	-	ERBOOST pin status Set and cleared based on voltage 1 V_ERBOOST < ERBOOST_OK 0 V_ERBOOST > ERBOOST_OK
VDD5_UV	-	-	-	VDD5_UV status Set based on voltage, cleared on SPI read 0 VDD5 > VDD5_UV 1 VDD5 < VDD5_UV
VDD5_OV	-	-	-	VDD5_OV status Set based on voltage, cleared on SPI read 0 VDD5 < VDD5_OV 1 VDD5 > VDD5_OV
VSUP_NOK	-	-	-	VSUP status Set and cleared based on voltage 0 VSUP > VSUP_OK 1 VSUP < VSUP_OK
ER_BST_ON	0	-	-	ERBOOST_ON state Updated according to ER_BOOST Control Behavior diagram 0 RBOOST_OFF or ERBOOST_OT state or ER_BST_STBY state (boost not running) 1 ERBOOST_ON state (boost running)
ER_CHRG_ON	0	0	0	ERCHARGE_ON state Updated according to ER_CHARGE Power Mode Control diagram 0 ERCHARGE_ON = 0 1 ERCHARGE_ON = 1

ER_SW_ON	0	-	-	ER_SWITCH State Updated according to ER Switch state diagram 0 ER_SWITCH_OFF 1 ER_SWITCH_ON
VDD5_ACT	0	-	-	VDD5 Active state Updated according to VDD5 Power Mode Control state diagram 0 VDD5 supply in VDD5_OFF or VDD5_SHUTDOWN states 1 VDD5 supply in VDD5_RAMPUP or VDD5_ON states
VSUP_ACT	0	0	0	VSUP Active state Updated according to VSUP Power Mode Control state diagram 0 VSUP supply in VSUP_OFF or VSUP_SHUTDOWN states 1 VSUP supply in VSUP_RAMPUP or VSUP_ON states
VDD3V3_ACT	0	-	-	VDD3V3 Active state Updated according to VDD3V3 Power Mode Control state diagram 0 VDD3V3 supply in VDD3V3_OFF or VDD3V3_SHUTDOWN states 1 VDD3V3 supply in VSUP_ON state
VSF_ACT	0	0	0	VSF Active state Updated according to VSF Control Logic diagram 0 VSF_EN = 0 1 VSF_EN = 1

5.1.7 Deployment configuration registers (DCR_x)

Channel 0 (DCR_0)

Channel 1 (DCR_1)

Channel 2 (DCR_2)

Channel 3 (DCR_3)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	Deploy_Time		Dep_Current		Dep_expire_time		X	X
MISO	0	0	0	0	0	0	0	0	0	0	0	0	Deploy_Time		Dep_Current		Dep_expire_time		0	0

Address: 06 (DCR_0)
07 (DCR_1)
08 (DCR_2)
09 (DCR_3)

Type: RW

Buffer: $0600 (DCR_0)
$0700 (DCR_1)
$0800 (DCR_2)
$0900 (DCR_3)

Reset: $000C (DCR_0)
$000E (DCR_1)
$0010 (DCR_2)
$0012 (DCR_3)

	POR	WSM	SSM	
Deploy_Time[1:0]	00	00	00	Default deployment time select Updated by SSM_RESET or SPI write while in DIAG state 00 Unused (no deploy, 8 us pulse output on ARM1 pin during PULSE TEST) 01 0.5 ms 10 0.7 ms 11 2.0 ms
Dep_Current[1:0]	00	00	00	Deployment Current limit select Updated by SSM_RESET or SPI write while in DIAG state 00 Unused (no deploy)

01 1.75A min

10 1.2A min

11 Unused (no deploy)

Dep_expire_time[1:0]	00	00	00	Deploy command expiration timer select Updated by SSM_RESET or SPI write while in DIAG state 00 500ms 01 250ms 10 125ms 11 0ms

5.1.8 Deployment command (DEPCOM)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	CH3DEPREQ	CH2DEPREQ	CH1DEPREQ	CH0DEPREQ
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CH3DEP	CH2DEP	CH1DEP	CH0DEP

Address: 12

Type: RW

Buffer: $1200

Reset: $0024

	POR	WSM	SSM	
CHxDEPREQ	N/A	N/A	N/A	Channel x Deploy Request - non-latched channel-specific deploy request 0 No change to deployment control for channel x 1 Clear and start Expiration timer if in ARMING or SAFING state and in DEPLOY_ENABLED state
CHxDEP	0	0	0	Channel x deployment expiration timer enable Set when SPI_DEPCOM(CHxDEPREQ=1) AND in ARMING or SAFING state AND in DEP_ENABLED state Cleared on SSM_RESET OR when in DEP_DISABLED state OR when Deploy Expiration Timer x reaches time-out threshold 0 Expiration timer enabled - Deploy command still valid 1 Expiration Timer disabled - Deploy command no more valid

5.1.9 Deployment configuration registers (DSR_x)

Channel 0 (DSR_0)

Channel 1 (DSR_1)

Channel 2 (DSR_2)

Channel 3 (DSR_3)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
MISO	0	0	0	0	CHxDS	CHxSTAT	CHxDD	DCRxERR	0	0	0	0	0	0	DEP_CHx_ExpTimer					

Address: 13 (DSR_0)
14 (DSR_1)
15 (DSR_2)
16 (DSR_3)

Type: R

Buffer: $1300 (DSR_0)
$1400 (DSR_1)
$1500 (DSR_2)
$1600 (DSR_3)

Reset: -

	POR	WSM	SSM	
CHxDS	0	0	0	Channel x deployment successful Updated according to Deployment Driver Control Logic (set when deployment terminates on ch x due to deploy timer time-out, cleared on SSM_RESET OR when deployment starts on ch x) 0 Deployment not successful 1 Deployment successful
CHxSTAT	0	0	0	(set when deployment starts on ch x, cleared on SSM_RESET OR when deployment terminates due to deploy timer time-out, LS Over current OR GND Loss) 0 Deployment not in progress 1 Deployment in progress
CHxDD	0	0	0	Default Deploy Flag on Channel x Updated by SSM_RESET, or when the Deployment Configuration Register is written with an incorrect configuration

0 Correct Time/Current combination selected

1 Incorrect Time/Current combination selected (default time/current is set)

DCRxERR 0 0 0 Deployment configuration register err

0 Deploy configuration change accepted and stored in memory

1 Deploy configuration change rejected because deploy is in progress (or DEP_EXPIRE_TIME changed when in DEP_ENABLED state)

DEP_CHx_ExpTimer [5:0] 000000 000000 000000 Channel x Deployment Expiration Timer value 8ms/count

Updated according to Deployment Driver Control Logic

(Cleared on SSM_RESET OR when Exp Timer times out OR when SPI_DEPREQx is received while in DEP_ENABLED state AND in ARMING or SAFING states)

5.1.10 Deployment current monitor status registers (DCMTSxy)

Channels 0, 1 (DCMTS01)

Channels 2, 3 (DCMTS23)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	Current_Mon_Timer_y[7:0]								Current_Mon_Timer_x[7:0]							

Address: 1F (DCMTS01))
20 (DCMTS23)

Type: R

Buffer: $1F00 (DCMTS01)
$2000 (DCMTS23)

Reset: -

	POR	WSM	SSM	
Current_Mon_Timer_y[7:0]	$00	$00	$00	Channel y current monitor timer value corresponding to SPI command DCMTSxy. Set to default (cleared) on SSM_RESET or when a new deployment starts on channel y. Increments each 16µs while deployment current exceeds monitor threshold on channel y
Current_Mon_Timer_x[7:0]	$00	$00	$00	Channel x current monitor timer value corresponding to SPI command DCMTSxy. Set to default (cleared) on SSM_RESET or when a new deployment starts on channel x. Increments each 16µs while deployment current on channel x exceeds monitor threshold

5.1.11 Deploy enable register (SPIDEPEN)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				DEPEN_WR[15:0															
MISO	0	0	0	0	DEPEN_STATE[15:0]															

Address: 25

Type: RW

Buffer: $2500

Reset: $004A

	POR	WSM	SSM	
DEPEN_WR[15:0]	N/A	N/A	N/A	Non-latched encoded value for LOCK / UNLOCK command $0FF0 LOCK - enter DEP_DISABLED state $F00F UNLOCK - enter DEP_ENABLED state
DEPEN_STATE[15:0]	$0FF0	$0FF0	$0FF0	Deploy Enabled State Updated according to Global SPI Deployment Enable State Diagram $0FF0 In DEP_DISABLED state $F00F In DEP_ENABLED state

5.1.12 Squib ground loss register (LP_GNDLOSS)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GNDLOSS3	GNDLOSS2	GNDLOSS1	GNDLOSS0

Address: 26

Type: R

Buffer: $2600

Reset: -

	POR	WSM	SSM	
GNDLOSSx	0	0	0	Loop x Squib Ground loss

Cleared upon SSM_RESET or SPI read. Set when GND loss is detected during deployment or loop diag's (HS sw test, LS sw test, squib resistance)

0 Loss of ground not detected

1 Loss of ground detected

5.1.13 Device version register (VERSION_ID)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	DEVICE ID			0	0	VERSN					

Address: 27

Type: R

Buffer: $2700

Reset: -

	POR	WSM	SSM	
DEVICE ID	-	-	-	Identification of the device Static value - never updated 001 Low end 010 Medium end 011 High end
VERSN	-	-	-	Identification of the silicon version 000011 CB version other codes previous versions

5.1.14 Watchdog retry configuration register (WD_RETRY_CONF)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-																	WD1_RETRY_TH		
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	WD1_RETRY_TH		

Address: 28

Type: RW

Buffer: $2800

Reset: $0050

	POR	WSM	SSM	
WD1_RETRY_TH	7	7	-	WD1 retry counter threshold (number of WD errors permitted before latching WD1_LOCKOUT=1)

5.1.15 Watchdog timer configuration register (WDTCR)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	WD1_MODE	WDTMIN[6:0]							WDTDELTA[6:0]						
MISO	0	0	0	0	0	WD1_MODE	WDTMIN[6:0]							WDTDELTA[6:0]						

Address: 2A

Type: RW

Buffer: $2A00

Reset: $0054

	POR	WSM	SSM	
WD1_MODE	0	0	-	WD1 Mode Updated by WSM_RESET or SPI write while in WD1_INIT state 0 Fast WD1 mode - nominal 8µs timer resolution (2ms max value) 1 Slow WD1 mode - nominal 64µs timer resolution (16.3ms max value)
WDTMIN[6:0]	$32	$32	-	WD1 window minimum value - resolution according to WD1_MODE bit ($32 = 400µs in WD1 fast mode) Updated by WSM_RESET or SPI write while in WD1_INIT state
WDTDELTA[6:0]	$19	$19	-	WD1 window delta value - WDTMAX=WDTMIN+WDTDELTA - resolution according to WD1_MODE bit ($19 = 200µs in WD1 fast mode) Updated by WSM_RESET or SPI write while in WD1_INIT state

5.1.16 WD1 timer control register (WD1T)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	WD1CTL[1:0]	
MISO	0	0	0	0	WD1_TIMER								0	0	0	0	0	0	WD1CTL[1:0]	

Address: 2B

Type: W

Buffer: $2B00

Reset: $0056

	POR	WSM	SSM	
WD1CTL[1:0]	00	00	00	WD1 Control command Updated by SSM_RESET or SPI write 00 NOP 01 Code 'A' 10 Code 'B' 11 NOP
WD1_TIMER	$00	$00	$00	WD1 Window timer value Cleared by SSM_RESET or by WD1 refresh, incremented every 8µs or 64µs while in WD1_RUN or WD1_TEST states

5.1.17 WD1 state register (WDSTATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	WD1_ERR_CNT[3:0]				WD_STATE[2:0]			0	0	0	0	0	0	0	0

Address: 2C

Type: R

Buffer: $2C00

Reset: -

	POR	WSM	SSM	
WD1_ERR_CNT[3:0]	000	000	-	Watchdog error counter Updated according to Watchdog State Diagram
WD1_STATE[2:0]	000	000	-	Watchdog state Updated according to Watchdog State Diagram 000 INITIAL

001 RUN

010 TEST

011 RESET

100 OVERRIDE

5.1.18 Clock configuration register (CLK_CONF)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	AUX_SS_DIS	MAIN_SS_DIS	ERBST_F_SEL[1:0]	
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	AUX_SS_DIS	MAIN_SS_DIS	ERBST_F_SEL[1:0]	

Address: 2D

Type: RW

Buffer: $2D00

Reset: $005A

	POR	WSM	SSM	
AUX_SS_DIS	1	-	-	Auxiliary 3.75MHz oscillator Spread Spectrum disable Updated by POR or SPI write while in INIT state 0 Spread Spectrum enabled 1 Spread Spectrum disabled
MAIN_SS_DIS	0	-	-	Main 16MHz oscillator Spread Spectrum disable Updated by POR or SPI write while in INIT state 0 Spread Spectrum enabled 1 Spread Spectrum disabled
ERBST_F_SEL[1:0]	00	-	-	ER Boost switching frequency select Updated by POR or SPI write while in INIT state 00 1.88 MHz 01 2.13 MHz 10 2.00 MHz 11 2.00 MHz

5.1.19 Scrap state entry command register (SCRAP_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				$3535															
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address: 30

Type: W

Buffer: -

Reset: $0060

POR	WSM	SSM
N/A	N/A	N/A

Non-latched Scrap State entry command

Enter Scrap state from DIAG state

5.1.20 Safing state entry command register (SAFING_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				$ACAC															
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address: 31

Type: W

Buffer: -

Reset: $0062

POR	WSM	SSM
N/A	N/A	N/A

Non-latched Safing State entry command

Enter safing state from DIAG state and clear arming pulse stretch counter (if received in DIAG or SAFING state)

5.1.21 WD1 test command register (WD1_TEST)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				$3C								X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address: 35

Type: W

Buffer: -

Reset: $006A

	POR	WSM	SSM
	N/A	N/A	N/A

Non-latched WD1 Test Command

WD1_TEST SPI command as described in *Figure 36: Watchdog state diagram*.

5.1.22 System diagnostic register (SYSDIAGREQ)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	DSTEST[3:0]			
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DSTEST[3:0]			

Address: 36

Type: RW

Buffer: $3601

Reset: $006C

	POR	WSM	SSM	
DSTEST[3:0]	0000	0000	0000	Diagnostic State Test selection

Updated by SSM_RESET or SPI write while in DIAG state

0000 = all outputs inactive

0001 = ARM pin active

0010 = all outputs inactive

0011 = all outputs inactive

0100 = all outputs inactive

0101 = all outputs inactive

0110 = VSF regulator active

0111 = HS squib driver FET active

1000 = LS squib driver FET active

1001 = Output deployment timing pulses on ARM1 (separated by 8 ms)

1010 = ST reserved

1011 - 1111 = all outputs inactive

5.1.23 Diagnostic result register for deployment loops (LPDIAGSTAT)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	DIAG_LEVEL	TIP	0	FP	FETON	ST_reserved	HSR_HI	HSR_LO	RES_MEAS_CHSEL/ HIGH_LEV_DIAG_SELECTED				SBL	STG	STB	SQP	LEAK_CHSEL			

Address: 37

Type: R

Buffer: $3700

Reset: -

	POR	WSM	SSM	
DIAG_LEVEL	0	0	0	Diagnostic mode selector Not present for low level diagnostic Updated by SSM_RESET or SPI write to LPDIAGREQ 0 low level mode 1 high level mode
TIP	0	0	0	High level diagnostic test is running Updated by SSM_RESET or Loops diagnostic state machine 0 High level diagnostic test is not running 1 High level diagnostic test is running
FP	0	0	0	Fault present before requested diagnostic Updated by SSM_RESET or Loops diagnostic state machine 0 Fault not present before requested diagnostic 1 Fault present before requested diagnostic
FETON	0	0	0	FET activation during diagnostic

				Updated by SSM_RESET or Loops diagnostic state machine or when HS or LS FET is activated during DIAG state 0 FET is off during diagnostic 1 FET is on during diagnostic
ST_reserved	0	0	0	ST_reserved
HSR_HI	0	0	0	HSR Diagnostic - HIGH Range Updated by SSM_RESET or Loops diagnostic state machine or when squib resistance test is run 0 HSR measurement < HSR HIGH value 1 HSR measurement > HSR HIGH value
HSR_LO	0	0	0	HSR Diagnostic - Low Range Updated by SSM_RESET or Loops diagnostic state machine or when squib resistance test is run 1 HSR measurement< HSR LOW value 0 HSR measurement > HSR LOW value
RES_MEAS_CHSEL [3:0]	0000	0000	0000	Channel selected for resistance measurement Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib resistance channel selected 0000 = Ch 0 0001 = Ch 1 0010 = Ch 2 0011 = Ch 3 0100 - 1111 None Selected
HIGH_LEV_DIAG_ SELECTED[3:0]	0000	0000	0000	0000 No diagnostic selected 0001 VRCM CHECK 0010 Leakage CHECK 0011 Short Between Loops CHECK 0100 Unused 0101Squib resistance range CHECK 0110 Squib resistance measurement 0111 FET test 1000 - 1111 Unused

SBL	0	0	0	Short between loop state Updated by SSM_RESET or Loops diagnostic state machine 0 Short between squib loops is not present 1 Short between squib loops is present
STG	0	0	0	Short to Ground Test Status Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib leakage diagnostic 0 STG not detected 1 1 STG detected
STB	0	0	0	Short to Battery Test Status Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib leakage diagnostic 0 STB not detected 1 STB detected
SQP	0	0	0	Squib PIN where leakage test has been performed Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib leakage diagnostic 0 SRx 1 SFx
LEAK_CHSEL[3:0]	0000	0000	0000	Channel selected for leakage measurement Updated by SSM_RESET or Loops diagnostic state machine or as determined by squib leakage diagnostic 0000 = Ch 0 0001 = Ch 1 0010 = Ch 2 0011 = Ch 3 0100 - 1111 None Selected

5.1.24 Loops diagnostic configuration command register for low level diagnostic (LPDIAGREQ)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				DIAG_LEVEL	ISRC_CURR_SEL	PD_CURR	ISRC [1:0]		ISINK	VRCM[1:0]		RES_MEAS_CHSEL[3:0]				LEAK_CHSEL[3:0]			
MISO	0	0	0	0	DIAG_LEVEL	ISRC_CURR_SEL	PD_CURR	ISRC [1:0]		ISINK	VRCM[1:0]		RES_MEAS_CHSEL[3:0]				LEAK_CHSEL[3:0]			

Address: 38

Type: RW

Buffer: $3800

Reset: $0070

	POR	WSM	SSM	
DIAG_LEVEL	0	0	0	Diagnostic mode selector Updated by SSM_RESET or SPI write 0 low level mode 1 N/A - see description below
ISRC_CURR_SEL	0	0	0	Selection of ISRC current value 0 40mA 1 8mA
PD_CURR	0	0	0	Pull down current control Updated by SSM_RESET or SPI write 0 Request OFF only for channels connected to VRCM or ISINK or ISRC, ON for all other channels 1 Request OFF for all channels
ISRC [1:0]	00	00	00	High side current source for channel selected in RES_MEAS_CHSEL[3:0] Updated by SSM_RESET or SPI write 00 = OFF 01 = ON 40 mA current for channel selected in RES_MEAS_CHSEL, OFF on all other channels

10 = ON bypass current for channel selected in RES_MEAS_CHSEL, OFF ON all other channels

11 = OFF

ISINK	0	0	0	Low Side current sink control (max 50mA) Updated by SSM_RESET or SPI write 0 All channels OFF 1 ON for channel selected by RES_MEAS_CHSEL[3:0], OFF on all other channels
VRCM[1:0]	00	00	00	Voltage Regulator Current Monitor control Updated by SSM_RESET or SPI write 00 VRCM not connected 01 VRCM connected to SFx of channel selected by LEAK_CHSEL[3:0] 01 VRCM connected to SFx of channel selected by LEAK_CHSEL[3:0] and pull down current of the same channel disabled 10 VRCM connected to SRx of channel selected by LEAK_CHSEL[3:0] and pull down current of the same channel enabled (ISINK and ISRC must be switched
RES_MEAS_CHSEL[3:0]	0000	0000	0000	Squib Resistance Measurement Channel select - selects the channel and muxes for the resistance test, and the channel for HS driver test (full path fet test) activation Updated by SSM_RESET or SPI write 0000 Channel 0 0001 Channel 1 0010 Channel 2 0011 Channel 3 0100 - 1111 None Selected
LEAK_CHSEL[3:0]	0000	0000	0000	Squib Leakage Measurement Channel select - selects the channel and muxes for the leakage test, and the channel for HS/LS FET test activation. Updated by SSM_RESET or SPI write 0000 Channel 0 0001 Channel 1 0010 Channel 2 0011 Channel 3 0100 - 1111 None Selected

5.1.25 Loops diagnostic configuration command register for high level diagnostic (LPDIAGREQ)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				DIAG_LEVEL	X	X	X	X	X	X	X	HIGH_LEVEL_DIAG_SEL			SQP	LOOP_DIAG_CHSEL[3:0]		
MISO	0	0	0	0	DIAG_LEVEL	0	0	0	0	0	0	0	HIGH_LEVEL_DIAG_SEL			SQP	LOOP_DIAG_CHSEL[3:0]		

Address: 38

Type: RW

Buffer: $3800

Reset: $0070

	POR	WSM	SSM	
DIAG_LEVEL	0	0	0	Diagnostic mode selector 0 0 N/A - see description above 1 1 high level mode
HIGH_LEVEL_DIAG_SEL	000	000	000	Selection of high level squib diagnostic Updated by SSM_RESET or SPI write 000 No diagnostic selected 001 VRCM CHECK 010 Leakage CHECK 011 Short Between Loops CHECK 100 Unused 101 Squib resistance range CHECK 110 Squib resistance measurement 111 FET test
SQP	0	0	0	Squib pin select for all leakage diagnostic Updated by SSM_RESET or SPI write

				0 SRx 1 SFx
LOOP_DIAG_CHSEL[3:0]	0000	0000	0000	Channel select - selects the channel and muxes for all squib diagnostic. Updated by SSM_RESET or SPI write 0000 Channel 0 0001 Channel 1 0010 Channel 2 0011 Channel 3 0100 - 1111 None Selected

5.1.26 DC sensor diagnostic configuration command register (SWCTRL)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	DCS_PDCURR	SWOEN	X	X	CHID[3:0]			
MISO	0	0	0	0	0	0	0	0	0	0	0	0	DCS_PDCURR	SWOEN	0	0	CHID[3:0]			

Address: 39

Type: RW

Buffer: $3900

Reset: $0072

	POR	WSM	SSM	
DCS_PDCURR	0	0	0	Disable of all pull down current for DC sensor Updated by SSM_RESET or SPI write 0 OFF for channel under voltage or current measurement, ON for all other channels 1 OFF for all channels
SWOEN	0	0	0	Switch Output Enable Updated by SSM_RESET or SPI write 0 OFF 1 ON (40mA)
CHID[3:0]	0000	0000	0000	Channel ID - selects DC sensor channel for output activation Updated by SSM_RESET or SPI write 0000 Channel 0 0001 Channel 1 0010 Channel 2 0011 Channel 3 0100 - 1111 None Selected

5.1.27 ADC request and data registers (DIAGCTRL_x)

ADC A control command (DIAGCTRL_A)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	ADCREQ_A[6:0]						
MISO	NEWDATA_A	0	0	ADCREQ_A[6:0]							ADCRES_A[9:0]									

Address: 3A

Type: RW

Buffer: $3A00

Reset: $0074

ADC B control command (DIAGCTRL_B)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	ADCREQ_B[6:0]						
MISO	NEWDATA_B	0	0	ADCREQ_B[6:0]							ADCRES_B[9:0]									

Address: 3B

Type: RW

Buffer: $3B00

Reset: $0076

ADC C control command (DIAGCTRL_C)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	ADCREQ_C[6:0]						
MISO	NEWDATA_C	0	0	ADCREQ_C[6:0]							ADCRES_C[9:0]									

Address: 3C

Type: RW

Buffer: $3C00

Reset: $0078

ADC D control command (DIAGCTRL_D)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	ADCREQ_D[6:0]						
MISO	NEWDATA_D	0	0	ADCREQ_D[6:0]							ADCRES_D[9:0]									

Address: 3D

Type: RW

Buffer: $3D00

Reset: $007A

	POR	WSM	SSM	
NEWDATA_x	0	0	0	New data available from convertion Updated by SSM_RESET or ADC state machine 0 cleared on read 1 convertion finished
ADCREQ_x[6:0]	$00	$00	$00	ADC Request select command Updated by SSM_RESET or SPI write to DIAGCTRL_x Measurement $00 Unused $01 Ground Ref $02 Full scale Ref $030 DCSx voltage $04 DCSx current $05 DCSx resistance $06 Squib x resistance $07 Internal BG reference voltage (BGR) $080 Internal BG monitor voltage (BGM) $09 Unused $0A Temperature $0B DCS 0 voltage $0C DCS 1 voltage $0D DCS 2 voltage $0E DCS 3 voltage $20 VBATMON pin voltage $21 VIN pin voltage $22 Internal analog supply voltage (VINT) $23 Internal digital supply voltage (VDD)

$24 ERBOOST pin voltage
$25 Unused
$26 VER pin voltage
$27 VSUP voltage
$28 VDDQ voltage
$29 WAKEUP pin voltage
$2A VSF pin voltage
$2B WDTDIS pin voltage
$2C GPOD0 pin voltage
$2D GPOS0 pin voltage
$2E GPOD1 pin voltage
$2F GPOS1 pin voltage
$30 Unused
$31 Unused
$32 RSU0 pin Voltage
$33 RSU1 pin Voltage
$34 Unused
$35 Unused
$36 SS0 pin voltage
$37 SS1 pin voltage
$38 SS2 pin voltage
$39 SS3 pin voltage
$3A Unused
$3B Unused
$3C Unused
$3D Unused
$3E Unused
$3F Unused
$40 Unused
$41 Unused
$42 VRESDIAG voltage
$43 VDD5 voltage
$44 VDD3V3 voltage
$45 ISOK voltage
$46 SF0
$47 SF1
$48 SF2
$49 SF3
$4A - $7F Unused

ADCRES_x[9:0]	$000	$000	$000	10-bit ADC result value corresponding to ADCREQ_x request Updated by SSM_RESET or ADC state machine

5.1.28 GPO configuration register (GPOCR)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	GPO1LS	GPO0LS
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GPO1LS	GPO0LS

Address: 42

Type: RW

Buffer: $4200

Reset: $0084

	POR	WSM	SSM	
GPOxLS	0	0	0	GPO driver configuration bit Updated by SSM_RESET or SPI write 0 High-side Driver configuration for GPOx (ER_BOOST_OK is required to enable GPO as HS) 1 Low-side Driver configuration for GPOx (ER_BOOST_OK is not required to enable GPO as LS)

5.1.29 GPO configuration register (GPOCTRLx)

Channel 0 (GPOCTRL0)

Channel 1 (GPOCTRL1)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	GPOxPWM[5:0]					
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	GPOxPWM[5:0]					

Address: 43 (GPOCTRL0)
44 (GPOCTRL1)

Type: RW

Buffer: $4300 (GPOCTRL0)
$4400 (GPOCTRL1)

Reset: $0086 (GPOCTRL0)
$0088 (GPOCTRL1)

	POR	WSM	SSM	
GPOxPWM	000000	000000	000000	6 bit value for PWM% with scaling of 1.6% per count Updated by SSM_RESET or SPI write

5.1.30 GPO fault status register (GPOFLTSR)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	GPO1DISABLE	GPO0DISABLE	0	GPO_NOT_CONF	0	0	0	0	0	GPO1TEMP	GPO1LIM	GPO1OPN	0	0	GPO0TEMP	GPO0LIM	GPO0OPN	0	0

Address: 46

Type: R

Buffer: $4600

Reset: -

	POR	WSM	SSM	
GPO1DISABLE	1	1	1	GPO 1 disable state 0 GPO enable to work 1 GPO disabled due to thermal fault or configuration not received or ERBOOST not OK (only HS mode)
GPO0DISABLE	1	1	1	GPO 0 disable state 0 GPO enable to work 1 GPO disabled due to thermal fault or configuration not received or ERBOOST not OK (only HS mode)
GPO_NOT_CONF	1	1	1	GPO configuration status 0 GPO HS/LS configured (activation is permitted) 1 GPO not yet configured (activation is denied)
GPO1TEMP	0	0	0	GPO 1 Thermal Fault Cleared by SSM_RESET or SPI read, set by detection circuit 0 Fault not detected 1 Fault detected
GPO1LIM	0	0	0	GPO 1 Current Limit Flag Cleared by SSM_RESET or SPI read, set by detection circuit while ON 0 Fault not detected 1 Fault detected
GPO1OPN	0	0	0	GPO 1 Open Detection Cleared by SSM_RESET or SPI read, set by detection circuit while ON 0 Fault not detected

1 Fault detected

GPO0TEMP 0 0 0 GPO 0 Thermal Fault

Cleared by SSM_RESET or SPI read, set by detection circuit

0 Fault not detected

1 Fault detected

GPO0LIM 0 0 0 GPO 0 Current Limit Flag

OK Cleared by SSM_RESET or SPI read, set by detection circuit while ON

0 Fault not detected

1 Fault detected

GPO0OPN 0 0 0 GPO 0 Open Detection

OK Cleared by SSM_RESET or SPI read, set by detection circuit while ON

0 Fault not detected

1 Fault detected

5.1.31 ISO fault status register (ISOFLTSR)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ISOTEMP	ISOLIM

Address: 47

Type: R

Buffer: $4700

Reset: -

	POR	WSM	SSM	
ISOTEMP	0	0	0	ISO Thermal Fault

Cleared by SSM_RESET or SPI read, set by detection circuit

0 Fault not detected

1 Fault detected

ISOLIM 0 0 0 ISO Current Limit Flag

Cleared by SSM_RESET or SPI read, set by detection circuit while ON (ISOK=0)

0 Fault not detected

1 Fault detected

5.1.32 Remote sensor configuration register (RSCRx)

Remote sensor configuration register 1 (RSCR1)

Remote sensor configuration register 2 (RSCR2)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	SLOWTRACK	STARTbitsMEAS_DISABLE	X	X	BLKTxSEL	X	X	X	X	X	X	STSx[3:0]			
MISO	0	0	0	0	0	SLOWTRACK	STARTbitsMEAS_DISABLE	0	0	BLKTxSEL	0	0	0	0	0	0	STSx[3:0]			

Address: 4A (RSCR1)
4B (RSCR2)

Type: RW

Buffer: $4A00 (RSCR1)
$4B00 (RSCR2)

Reset: $0094 (RSCR1)
$0096 (RSCR2)

	POR	WSM	SSM	
SLOWTRACK	0	0	0	Reduce frequency of base current tracking 0 8µs/1µs 1 16µs/2µs
STARTbitsMEAS_DISABLE	0	0	0	Disable of start bits period measure to decode data bits 0 Period of start bits used to decode following data bits 1 Period of start bits not used to decode following data bits
BLKTxSEL	0	0	0	Current limiting blanking time select for channel x Updated by SSM_RESET or SPI write 0 Blanking time = 5ms 1 Blanking time = 10ms

	POR	WSM	SSM	
STSx[3:0]	0000	0000	0000	Remote sensor type select Updated by SSM_RESET or SPI write 0000 Async PSI5, parity, 8-bit, 125k (A8P-228/1L) 0001 Async PSI5, parity, 8-bit, 189k (A8P-228/1H) 0010 Async PSI5, parity, 10-bit, 125k (A10P-228/1L) 0011 Async PSI5, parity, 10-bit, 189k (A10P-228/1H) 0100-1111 Async PSI5, parity, 10-bit, 189k (A10P-228/1H)

5.1.33 Remote sensor control register (RSCTRL)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	CH1EN	X	CH0EN	X
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CH1EN	0	CH0EN	0

Address: 4E

Type: R/W

Buffer: $4E00

Reset: $009C

	POR	WSM	SSM	
CHxEN	0	0	0	Channel x Output enable Updated by SSM_RESET or SPI write 0 Off 1 On

5.1.34 Remote sensor data/fault registers w/o fault (RSDRx)

Remote sensor 0 data and fault flag register (RSDR0)

Remote sensor 1 data and fault flag register (RSDR1)

Note: The value in Bit15 (FLT) will re-define the use of the other bits, hence the informations below are divided into two groups.

Bit 15 = 0 NO FAULT condition

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	CRC			0	FLT=0	On/Off	LCID [3:0]				DATA [9:0]									

Address: 50 (RSDR0)
51 (RSDR1)

Type: R

Buffer: $5000 (RSDR0)
$5100 (RSDR1)

Reset: -

	POR	WSM	SSM	
CRC[2:0]	000	000	000	CRC based on bits [16:0] Updated based on bits [16:0]
FLT	1	1	1	Fault Status - Depending on Fault Status, the DATA bits are defined differently Cleared when all of the following bits are '0': STG, STB, CURRENT_HI, OPENDET, RSTEMP, NODATA Set when any of the following bits are '1': STG, STB, CURRENT_HI, OPENDET, RSTEMP, NODATA 0 No fault 1 Fault
On/Off	0	0	0	Channel On/Off Status Cleared by SSM_RESET or when channel is commanded OFF via SPI RSCTRL or when the STG bit is set or the RSTEMP bit is set Set when channel is commanded ON by SPI RSCTRL 0 Off 1 On
LCID[0:3]	0000	0000	0000	Logical Channel ID

Updated based on SPI read request

0000 RSU0

0100 RSU1

DATA[9:0] $000 $000 $000 10-bit data from Manchester decoder

Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL

updated when a valid PSI5 frame is received

Bit 15 = 1 FAULTED condition

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	CRC			X	FLT=1	On/Off	LCID [3:0]				STG	STB	CURRENT_HI	OPENDET	RSTEMP	INVALID	NODATA	0	X	X

Address: 50 (RSDR0)
51 (RSDR1)

Type: R

Buffer: $5000 (RSDR0)
$5100 (RSDR1)

Reset: -

	POR	WSM	SSM	
CRC[2:0]	000	000	000	CRC based on bits [16:0] Updated based on bits [16:0]
FLT	1	1	1	Fault Status - Depending on Fault Status, the DATA bits are defined differently Cleared when all of the following bits are '0': STG, STB, CURRENT_HI, OPENDET, RSTEMP, NODATA Set when any of the following bits are '1': STG, STB, CURRENT_HI, OPENDET, RSTEMP, NODATA 0 No fault 1 Fault
On/Off	0	0	0	Channel On/Off Status Cleared by SSM_RESET or when channel is commanded OFF via SPI RSCTRL or when the STG bit is set or the RSTEMP bit is set Set when channel is commanded ON by SPI RSCTRL 0 Off

				1 On
LCID[0:3]	0000	0000	0000	Logical Channel ID Updated based on SPI read request 0000 RSU0 0100 RSU1
STG	0	0	0	Short to Ground (in current limit condition) Cleared by SSM_RESET or when channel is commanded OFF via SPI RSCTRL 0 No fault 1 Fault
STB	0	0	0	Short to Battery Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL - not cleared by channel OFF caused by STG or RSTEMP Set when channel voltage exceeds VSUP for a time greater than TSTBTH 0 No fault 1 Fault
CURRENT_HI	0	0	0	Current High Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL Set when channel current exceeds ILKGG for a time determined by an up/down counter 0 No fault 1 Fault
OPENDET	0	0	0	Open Sensor Detected Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL Set when channel current exceeds ILKGB for a time determined by an up/down counter 0 No fault 1 Fault
RSTEMP	0	0	0	Over temperature detected Cleared by SSM_RESET or when channel is commanded OFF via SPI RSCTRL Set when over-temp condition is detected 0 No fault 1 Fault

INVALID 0 0 0 Invalid Data

Cleared by SSM_RESET or SPI read or when channel is commanded OFF via SPI RSCTRL or if one of the following is set: STG, STB, CURRENT_HI, OPEN_DET, RSTEMP

Set when two valid start bits are received and a Manchester error (# of bits, bit timing) or parity error is detected

0 No fault

1 Fault

NODATA 1 1 1 No Data in buffer

Cleared when a valid PSI frame is received or if one of the following is set: STG, STB, CURRENT_HI, OPEN_DET, RSTEMP

Set upon SPI read of RSDRx if FIFO empty and none of the following bits are set: STG, STB, CURRENT_HI, OPEN_DET, RSTEMP

0 No fault

1 Fault

5.1.35 Safing algorithm configuration register (SAF_ALGO_CONF)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				NO_DATA	X	ARMN_TH				ARMP_TH				SUB_VAL			ADD_VAL		
MISO	0	0	0	0	NO_DATA	0	ARMN_TH				ARMP_TH				SUB_VAL			ADD_VAL		

Address: 66

Type: R/W

Buffer: $6600

Reset: $00CC

	POR	WSM	SSM	
NO_DATA	0	0	0	Event counter no data select Updated by SSM_RESET or SPI write while in DIAG state 0 Event counter reset to 0 if CC=0 when SPI read of SAF_CC bit is performed (end of sample cycle) 1 Event counter decremented by SUB_VAL if CC=0 when SPI read of SAF_CC bit is performed (end of sample cycle)
ARMN_TH	0011	0011	0011	Negative event counter threshold to assert arming Updated by SSM_RESET or SPI write while in DIAG state 0000 Negative event counter disabled
ARMP_TH	0011	0011	0011	Positive event counter threshold to assert arming Updated by SSM_RESET or SPI write while in DIAG state 0000 Positive event counter disabled
SUB_VAL	011	011	011	Decremental step size of the event counter Updated by SSM_RESET or SPI write while in DIAG state
ADD_VAL	001	001	001	Incremental step size of the event counter Updated by SSM_RESET or SPI write while in DIAG state

5.1.36 Arming signals register (ARM_STATE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	0	0	0	ACL_PIN_STATE	ACL_VALID	0	0	ARMINT_2	ARMINT_1	FENL	FENH

Address: 6A

Type: R

Buffer: $6A00

Reset: -

	POR	WSM	SSM	
ACL_VALID	0	0	0	Valid ACL detection 0 Cleared when ACL_BAD=2 1 Set when ACL_GOOD=3
ACL_PIN_STATE	-	-	-	Echo of ACL pin
ARMINT_x	0	0	0	State of armint signals Updated per Safing Engine output logic diagram
FENH/FENL	-	-	-	State of external arming control signals Updated based on pin state

5.1.37 ARMx assignment registers (LOOP_MATRIX_ARMx)

Assignment of ARM1 to specific loops (LOOP_MATRIX_ARM1)

Assignment of ARM2 to specific loops (LOOP_MATRIX_ARM2)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	ARMx_L3	ARMx_L2	ARMx_L1	ARMx_L0
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ARMx_L3	ARMx_L2	ARMx_L1	ARMx_L0

Address: 6E (LOOP_MATRIX_ARM1)
6F (LOOP_MATRIX_ARM2)

Type: RW

Buffer: $6E00 (LOOP_MATRIX_ARM1)
$6F00 (LOOP_MATRIX_ARM2)

Reset: $00DC (LOOP_MATRIX_ARM1)
$00DE (LOOP_MATRIX_ARM2)

	POR	WSM	SSM	
ARMx_Ly	0	0	0	Configures ARMx for Loop_y Updated by SSM_RESET or SPI write while in DIAG state 0 ARMx signal is not associated with Loopy 1 ARMx signal is associated with Loopy

5.1.38 ARMx pulse stretch registers (AEPSTS_ARMx)

ARM1 enable pulse stretch timer status (AEPSTS_ARM1)

ARM2 enable pulse stretch timer status (AEPSTS_ARM2)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	0	Timer Count[9:0]									

Address: 73 (AEPSTS_ARM1)
74 (AEPSTS_ARM2)

Type: RW

Buffer: $7300 (AEPSTS_ARM1)
$7400 (AEPSTS_ARM2)

Reset: - (AEPSTS_ARM1)
- (AEPSTS_ARM2)

	POR	WSM	SSM	
Timer Count	0000	0000	0000	10-bit ARMing Enable Pulse Stretcher timer value Cleared by SSM_RESET Loaded with initial value based on ARMx bit and DWELL[1:0] of SAF_CONTROL_y while safing is met for record y provided current value is < DWELL[1:0] value Decremented every 2ms while > 0 Contains remaining pulse stretcher timer value

5.1.39 Safing records enable register (SAF_ENABLE)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	EN_SAF4	EN_SAF3	EN_SAF2	EN_SAF1
MISO	0	0	0	0	0	0	0	0	0	0	0	0					EN_SAF4	EN_SAF3	EN_SAF2	EN_SAF1

Address: 7F

Type: RW

Buffer: $7F00

Reset: $00FE

	POR	WSM	SSM	
EN_SAFx	0	0	0	Safing Record enable Updated by SSM_RESET or SPI write 0 Disable 1 Enable

5.1.40 Safing records request mask registers (SAF_REQ_MASK_x)

Safing record request mask for record 1 (SAF_REQ_MASK_1)

Safing record request mask for record 2 (SAF_REQ_MASK_2)

Safing record request mask for record 3 (SAF_REQ_MASK_3)

Safing record request mask for record 4 (SAF_REQ_MASK_4)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				SAF_REQ_MASKx[15:0]															
MISO	0	0	0	0	SAF_REQ_MASKx[15:0]															

Address: 80 (SAF_REQ_MASK_1)
81 (SAF_REQ_MASK_2)
82 (SAF_REQ_MASK_3)
83 (SAF_REQ_MASK_4)

Type: RW

Buffer: $8000 (SAF_REQ_MASK_1)
$8100 (SAF_REQ_MASK_2)
$8200 (SAF_REQ_MASK_3)
$8300 (SAF_REQ_MASK_4)

Reset: $8000 (SAF_REQ_MASK_1)
$8002 (SAF_REQ_MASK_2)
$8004 (SAF_REQ_MASK_3)
$8006 (SAF_REQ_MASK_4)

	POR	WSM	SSM	
SAF_REQ_MASKx [15:0]	0000	0000	0000	Safing Request Mask for safing record x - 16-bit request mask that is bit-wise ANDed with MOSI data from SPI monitor Updated by SSM_RESET or SPI write while in DIAG state

5.1.41 Safing records request target registers (SAF_REQ_TARGET_x)

Safing record request mask for record 1 (SAF_REQ_TARGET_1)

Safing record request mask for record 2 (SAF_REQ_TARGET_2)

Safing record request mask for record 3 (SAF_REQ_TARGET_3)

Safing record request mask for record 4 (SAF_REQ_TARGET_4)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				SAF_REQ_TARGETx[15:0]															
MISO	0	0	0	0	SAF_REQ_TARGETx[15:0]															

Address: 93 (SAF_REQ_TARGET_1)
94 (SAF_REQ_TARGET_2)
95 (SAF_REQ_TARGET_3)
96 (SAF_REQ_TARGET_4)

Type: RW

Buffer: $9300 (SAF_REQ_TARGET_1)
$9400 (SAF_REQ_TARGET_2)
$9500 (SAF_REQ_TARGET_3)
$9600(SAF_REQ_TARGET_4)

Reset: $8026 (SAF_REQ_TARGET_1)
$8028 (SAF_REQ_TARGET_2)
$802A (SAF_REQ_TARGET_3)
$802C (SAF_REQ_TARGET_4)

	POR	WSM	SSM	
SAF_REQ_TARGETx [15:0]	0000	0000	0000	Safing Request target for safing record x - 16-bit request target that is compared to the bit-wise AND result of the SAF_REQ_MASKx and MOSI data from SPI monitor Updated by SSM_RESET or SPI write while in DIAG state

5.1.42 Safing records response mask registers (SAF_RESP_MASK_x)

Safing record response mask for record 1 (SAF_RESP_MASK_1)

Safing record response mask for record 2 (SAF_RESP_MASK_2)

Safing record response mask for record 3 (SAF_RESP_MASK_3)

Safing record response mask for record 4 (SAF_RESP_MASK_4)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				SAF_RESP_MASKx[15:0]															
MISO	0	0	0	0	SAF_RESP_MASKx[15:0]															

Address: A6 (SAF_RESP_MASK_1)
A7 (SAF_RESP_MASK_2)
A8 (SAF_RESP_MASK_3)
A9 (SAF_RESP_MASK_4)

Type: RW

Buffer: $A600 (SAF_RESP_MASK_1)
$A700 (SAF_RESP_MASK_2)
$A800 (SAF_RESP_MASK_3)
$A900 (SAF_RESP_MASK_4)

Reset: $804C (SAF_RESP_MASK_1)
$804E (SAF_RESP_MASK_2)
$8050 (SAF_RESP_MASK_3)
$8052 (SAF_RESP_MASK_4)

	POR	WSM	SSM	
SAF_RESP_MASKx [15:0]	0000	0000	0000	Safing Response Mask for safing record x - 16-bit response mask that is bit-wise ANDed with MISO data from SPI monitor Updated by SSM_RESET or SPI write while in DIAG state

5.1.43 Safing records response target registers (SAF_RESP_TARGET_x)

Safing record response target for record 1 (SAF_RESP_TARGET_1)

Safing record response mask for record 2 (SAF_RESP_TARGET_2)

Safing record response mask for record 3 (SAF_RESP_TARGET_3)

Safing record response mask for record 4 (SAF_RESP_TARGET_4)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				SAF_RESP_TARGETx[15:0]															
MISO	0	0	0	0	SAF_RESP_TARGETx[15:0]															

Address: B9 (SAF_RESP_TARGET_1)
BA (SAF_RESP_TARGET_2)
BB (SAF_RESP_TARGET_3)
BC (SAF_RESP_TARGET_4)

Type: RW

Buffer: $B900 (SAF_RESP_TARGET_1)
$BA00 (SAF_RESP_TARGET_2)
$BB00 (SAF_RESP_TARGET_3)
$BC00 (SAF_RESP_TARGET_4)

Reset: $8072 (SAF_RESP_TARGET_1)
$8074 (SAF_RESP_TARGET_2)
$8076 (SAF_RESP_TARGET_3)
$8078 (SAF_RESP_TARGET_4)

	POR	WSM	SSM	
SAF_RESP_TARGETx [15:0]	0000	0000	0000	Safing Response target for safing record x - 16-bit response target that is compared to the bit-wise AND result of the SAF_RESP_MASKx and MISO data from SPI monitor Updated by SSM_RESET or SPI write while in DIAG state

5.1.44 Safing records data mask registers (SAF_DATA_MASK_x)

Safing record data mask for record 1 (SAF_DATA_MASK_1)

Safing record data mask for record 2 (SAF_DATA_MASK_2)

Safing record data mask for record 3 (SAF_DATA_MASK_3)

Safing record data mask for record 4 (SAF_DATA_MASK_4)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				SAF_DATA_MASKx[15:0]															
MISO	0	0	0	0	SAF_DATA_MASKx[15:0]															

Address: CC (SAF_DATA_MASK_1)
CD (SAF_DATA_MASK_2)
CE (SAF_DATA_MASK_3)
CF (SAF_DATA_MASK_4)

Type: RW

Buffer: $CC00 (SAF_DATA_MASK_1)
$CD00 (SAF_DATA_MASK_2)
$CE00 (SAF_DATA_MASK_3)
$CF00 (SAF_DATA_MASK_4)

Reset: $8098 (SAF_DATA_MASK_1)
$809A (SAF_DATA_MASK_2)
$809C (SAF_DATA_MASK_3)
$809E (SAF_DATA_MASK_4)

	POR	WSM	SSM	
SAF_DATA_MASKx[15:0]	0000 0000	0000		Safing Data Mask for safing record x - 16-bit data mask that is bit-wise ANDed with MISO data from SPI monitor Updated by SSM_RESET or SPI write while in DIAG state

5.1.45 Safing records threshold registers (SAF_THRESHOLD_x)

Safing record threshold for record 1 (SAF_THRESHOLD_1)

Safing record threshold for record 2 (SAF_THRESHOLD_2)

Safing record threshold for record 3 (SAF_THRESHOLD_3)

Safing record threshold for record 4 (SAF_THRESHOLD_4)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				SAF_THRESHOLDx[15:0]															
MISO	0	0	0	0	SAF_THRESHOLDx[15:0]															

Address: DF (SAF_THRESHOLD_1)
E0 (SAF_THRESHOLD_2)
E1 (SAF_THRESHOLD_3)
E2 (SAF_THRESHOLD_4)

Type: RW

Buffer: $DF00 (SAF_THRESHOLD_1)
$E000 (SAF_THRESHOLD_2)
$E100 (SAF_THRESHOLD_3)
$E200 (SAF_THRESHOLD_4)

Reset: $80BE (SAF_THRESHOLD_1)
$80C0 (SAF_THRESHOLD_2)
$80C2 (SAF_THRESHOLD_3)
$80C4 (SAF_THRESHOLD_4)

	POR	WSM	SSM	
SAF_THRESHOLDx [15:0]	$FFFF	$FFFF	$FFFF	Safing threshold for safing record x - 16-bit threshold used for safing data comparison Updated by SSM_RESET or SPI write while in DIAG state

5.1.46 Safing control registers (SAF_CONTROL_x)

Safing control register for record 1 (SAF_CONTROL_1)

Safing control register for record 2 (SAF_CONTROL_2)

Safing control register for record 3 (SAF_CONTROL_3)

Safing control register for record 4 (SAF_CONTROL_4)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				ARMSELx		SPIFLDSELx	LIM SELx	LIM Enx	COMBx	DWELLx[1:0]		X	X	ARM2x	ARM1x	CSx[2:0]			IFx
MISO	0	0	0	0	ARMSELx		SPIFLDSELx	LIM SELx	LIM Enx	COMBx	DWELLx[1:0]		0	0	ARM2x	ARM1x	CSx[2:0]			IFx

Address: $EF (SAF_CONTROL_1)
$F0 (SAF_CONTROL_2)
$F1 (SAF_CONTROL_3)
$F2 (SAF_CONTROL_4)

Type: RW

Buffer: $EF00 (SAF_CONTROL_1)
$F000 (SAF_CONTROL_2)
$F100 (SAF_CONTROL_3)
$F200 (SAF_CONTROL_4)

Reset: $80DE (SAF_CONTROL_1)
$80E0 (SAF_CONTROL_2)
$80E2 (SAF_CONTROL_3)
$80E4 (SAF_CONTROL_4)

	POR	WSM	SSM	
ARMSELx	00	00	00	ARMINT select for safing record x - correlates ARMINT 1 and ARMINT2 (as determined by ARM1x and ARM2x bits) to ARMP and ARMN Updated by SSM_RESET or SPI write while in DIAG state 00 ARMP OR ARMN 01 ARMP 10 ARMN 11 ARMP OR ARMN
SPIFLDSELx	0	0	0	SPI field select for safing record x - determines which 16-bit field in long SPI messages (>31 bit) to use for response on MISO of SPI monitor. In case of messages less than 32 bits this bit is don't care.

				Updated by SSM_RESET or SPI write while in DIAG state 0 First 16 bits of SPI MISO frame used for Response Mask and Data Mask bit-wise AND 1 Last 16 bits of SPI MISO frame used for Response Mask and Data Mask bit-wise AND
LIM SELx	0	0	0	Data range limit select for safing record x - When enabled, determines the range limit used for incoming sensor data Updated by SSM_RESET or SPI write while in DIAG state 0 8-bit data range limit - incoming |data| >120d is not recognized as valid data 1 10-bit data range limit - incoming |data| > 480d is not recognized as valid data
LIM Enx	0	0	0	Data range limit enable for safing record x Updated by SSM_RESET or SPI write while in DIAG state 0 Data range limit disabled 1 Data range limit enabled
COMBx	0	0	0	Combine function enable for safing record x Updated by SSM_RESET or SPI write while in DIAG state 0 Combine function disabled 1 Combine function enabled For record pairs = x,x+1, the comparison for record x uses |data(x) + data(x+1)| and the comparison for record x+1 uses |data(x) - data(x+1)| Record pairs are 1,2 and 6,7
DWELLx[1:0]	00	00	00	Safing dwell extension time select for safing record x Updated by SSM_RESET or SPI write while in DIAG state 00 2048 ms 01 256 ms 10 32 ms 11 0 ms
ARM2x	0	0	0	ARM2INT select for safing record x - correlates safing result to ARM2INT Updated by SSM_RESET or SPI write while in DIAG state 0 Safing record x not assigned to ARM2INT 1 Safing record x assigned to ARM2INT
ARM1x	0	0	0	ARM1INT select for safing record x - correlates safing result to ARM1INT Updated by SSM_RESET or SPI write while in DIAG state

0 Safing record x not assigned to ARM1INT

1 Safing record x assigned to ARM1INT

CSx[2:0]	000	000	000	SPI Monitor CS select for safing record x Updated by SSM_RESET or SPI write while in DIAG state 000 None selected for record x 001 SAF_CS0 selected for record x 010 SAF_CS1 selected for record x 011 None selected for record x 100 None selected for record x 101 SPI_CS selected for record x 110 None selected for record x 111 None selected for record x
IFx	0	0	0	SPI format select for safing record x - selects response protocol for SPI monitor Updated by SSM_RESET or SPI write while in DIAG state 0 Out of frame response for record x 1 In Frame response for record x

5.1.47 Safing record compare complete register (SAF_CC)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI	-				X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
MISO	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CC_4	CC_3	CC_2	CC_1

Address: FF

Type: R

Buffer: $FF00

Reset: -

	POR	WSM	SSM	
CC_xx	0	0	0	Indicates compare complete status of each of the 4 safing records, and defines the end of the sample cycle for safing Cleared by SSM_RESET or SPI read, set by safing engine when request, response mask and target registers match the incoming SPI frame 0 Compare not completed for record x 1 Compare completed for record x

6 Deployment drivers

The squib deployment block consists of 4 independent high side drivers and 4 independent low side drivers. Squib deployment logic requires a deploy command received through SPI communications and either an arming condition processed by safing logic or a proper FENH and FENL input pin assessment, depending on whether the internal safing engine is used or not. FENH signal is used to enable high side squib drivers and is active high, while FENL enables low side drivers and is active low. Both conditions must exist in order for the deployment to occur. Once a deployment is initiated, it can only be terminated by a RESET event.

L9678 allows all 4 squib loops to be deployed at the very same time or in other possible timing sequence. Deployment drivers are capable of granting a successful deployment also in case of short to ground on low-side circuit (SRx pins). Firing voltage capability across high side circuit is maximum 25 V. High side and low side drivers account for a maximum series total resistance of 2 Ω. Each loop is granted for a minimum number of deployments of 50, under all normal operating conditions and with a deployment repetition time higher than 10s.

6.1 Control logic

A block diagram representing the deployment driver logic is shown below. Deployment driver logic features include:

- Deploy command logic
- Deployment current selection
- Deployment current monitoring and deploy success feedback
- Diagnostic control and feedback

Figure 20. Deployment driver control blocks

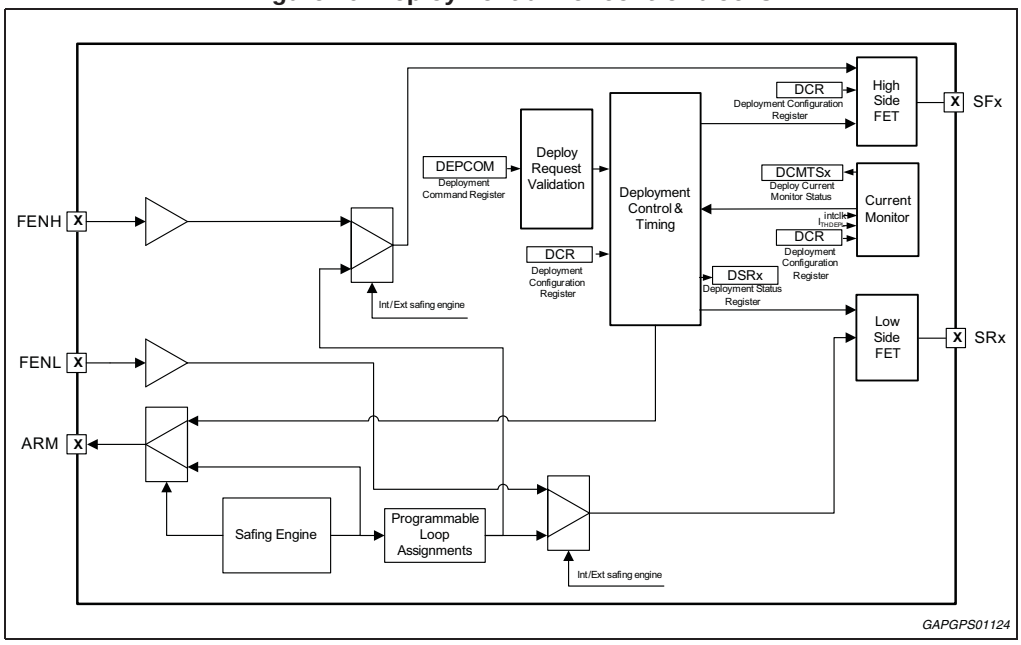


Figure 21. Deployment driver control logic - Enable signal

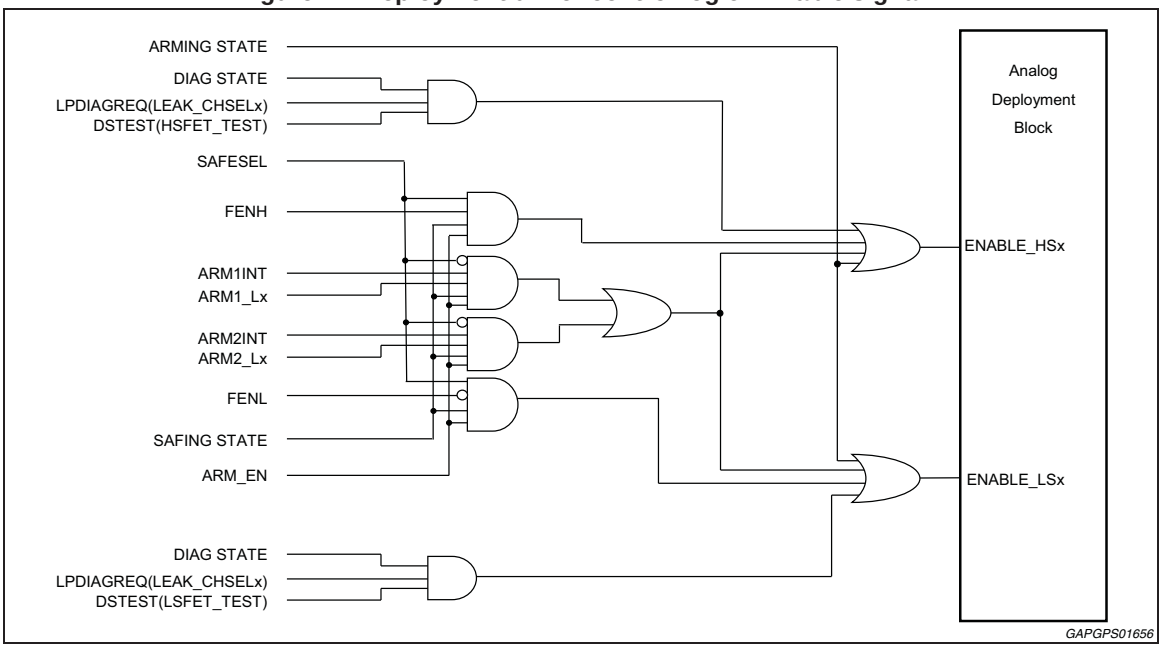
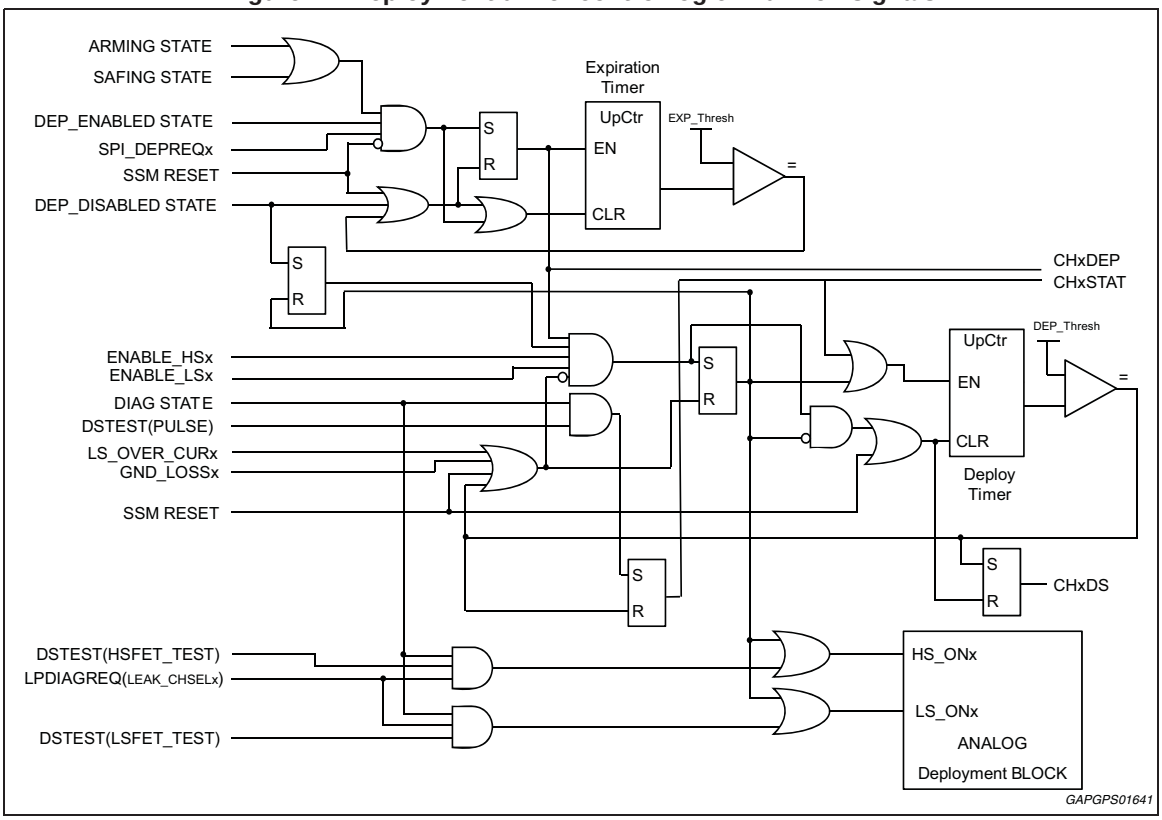
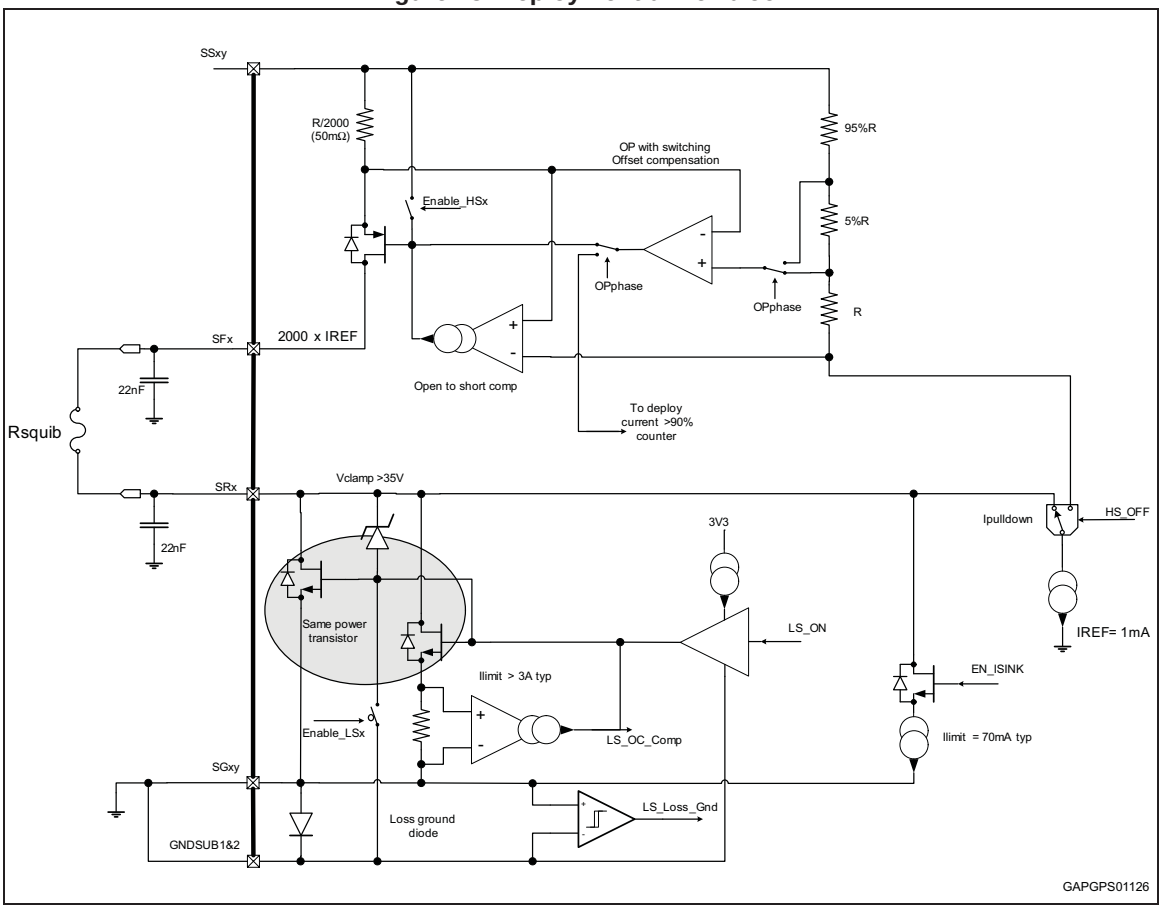


Figure 22. Deployment driver control logic - Turn-on signals



The high level block diagram for the deployment drivers is shown below:

Figure 23. Deployment driver block



6.1.1 Deployment current selection

Deployment current is programmed for all channels using the Deploy Configuration Register (DCRx) shown in “Deployment Configuration register (DCRx).

If 1.75 A deployment current is selected, the 2 ms deployment time cannot be chosen. If a SPI command with 2 ms and 1.75 A selection is received, L9678 will discard it and switch to a 500 µs and 1.2 A selection instead. This misuse is flagged with the CHxDD bit in the Deploy Status Register (DSR).

6.1.2 Deploy command expiration timer

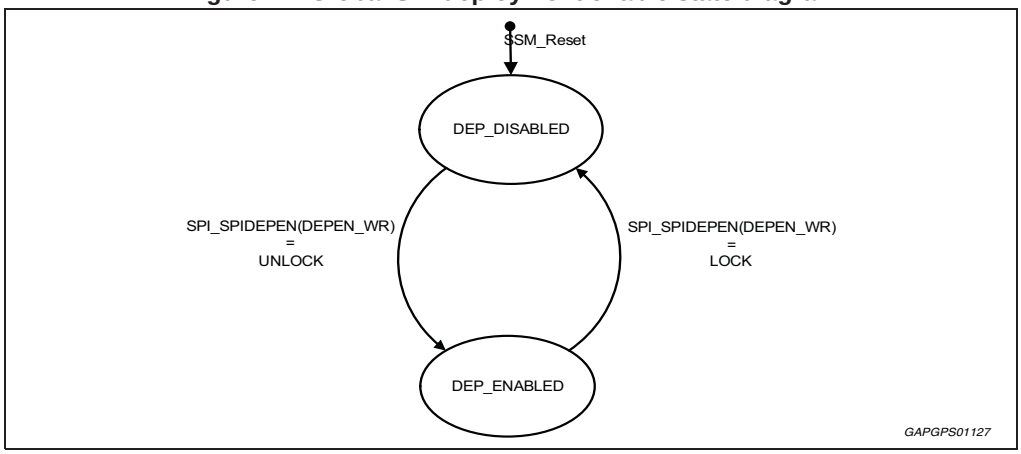
Deploy commands are received for all channels using SPI communications. Once a deploy command is received, it will remain valid for a specified time period selected in the Deploy Configuration Register (DCRx). The deploy status and deploy expiration timer can be read through the Deploy Status Register (DSRx). The deploy expiration timer is 6 bits and the maximum time is 500 ms nominal.

6.1.3 Deployment control flow

Deployment control logic requires the following conditions to be true to successfully operate a deployment:

- POR = 1
- SSM to be either in Safing State or Arming State
- a valid arming condition processed by safing logic or FENH and FENL signals to be set (depending on selection of internal or external safing engine)
- "channel-specific deploy command request bits to be set via SPI in the Deploy command Register (DEPCOM)
- a global deployment state has to be active, as described in the following figure.

Figure 24. Global SPI deployment enable state diagram



In case a multiple deployment request would be needed, i.e. deploying the same channel in sequence, a toggle on DEP_DISABLED has to be performed and a new DEPCOM command on the same channel has to be sent.

The SPI DEPCOM command is ignored if the device is in the DEP_DISABLED state and the deploy command is not set. While in DEP_ENABLED state, the following functionalities that could be active are forced to their reset state:

- All squib and DC sensor diagnostic current or voltage sources
- All squib, DC sensor and ADC diagnostic mux settings, state machine, etc.

The SPI_LOCK and SPI_UNLOCK signals are available in the SPIDEPEN command:

High-side and Low-side enablers by internal/external safing are global and apply to all channels. The Deploy commands in the Deploy Command Register (DEPCOM) are channel specific.

Deployment requires a valid arming command from safing logic or the FENH and FENL signals to be set any time before, during or after the specific sequence of deploy commands is received. It is feasible for a deploy command to be received without a valid arming command from safing logic or the FENH and FENL being set. In this case, the deploy command will be terminated according to the Deploy Command Expiration Timer described in *Section 6.1.2*. Likewise, a valid arming command or the FENH and FENL signals can be set without receiving a Deploy Command. In this case, the enabling signals will remain active according to the Arming Enable Pulse Stretch Timer or the FENx enabling state. The Arming Enable Pulse Stretch Timers is available in the AEPSTS register.

6.1.4 Deployment success

Deploy success flag is set when the deploy timer elapses. This bit (CHxDS) is contained in the Deploy Status Register. Within the Global Status Word register (GSW), a single bit (DEPOK) is also set once any of the four deployment channels sets a deploy success flag.

6.2 Energy reserve - deployment voltage

One deployment voltage source pin is used for channels 0 and 1 (SS01) and one for channels 2 and 3 (SS23). These pins are directly connected to the high side drivers for each channel.

6.3 Deployment ground return

There are dedicated power ground connections for deployment current, SGx pins. One ground connection is sufficient for two deployments occurring simultaneously.

6.4 Deployment driver protections

6.4.1 Delayed low-side deactivation

To control voltage spikes at the squib pins during drivers deactivation at the end of a deployment, the low side driver is switched off after $t_{DEL\_SD\_LS}$ delay time with respect to the high side deactivation.

6.4.2 Low-side voltage clamp

The low side driver is protected against overvoltage at the SRx pins by means of a clamping structure as shown in *Figure 23*. When the Low side driver is turned off, voltage transients at the SRx pin may be caused by squib inductance. In this case a low side FET drain to gate clamp will reactivate the low side FET allowing for residual inductance current recirculation, thus preventing potential low side FET damage by overvoltage.

6.4.3 Short to battery

The low side driver is equipped with current limitation and overcurrent protection circuitry. In case of short to battery at the squib pins, the short circuit current is limited by the Low side driver to I_{LIM_SR}. If this condition lasts for longer than $T_{FLT\_ILIM\_LS}$ deglitch filter time then the low and high-side drivers will be switched off and latched in this state until a new deployment is commanded after SPI_DEPEN is re triggered.

6.4.4 Short to ground

The squib driver is designed to stand a short to ground at the squib pins during deployment. In particular, the current flowing through the short circuit is limited by the high side driver (deployment current) and the high-side FET is sized to handle the related energy.

In case the short to ground during deployment occurs after an open circuit, a protection against damage is also available. The high side current regulator would have normally reacted to the open circuit by increasing the Vgs of the high side FET. Thanks to a dedicated

fast comparator detecting the open condition, the driver is able to discharge the FET gate quickly in order to reduce current overshoot and prevent potential driver damage when the short to ground occurs.

6.4.5 Intermittent open squib

A dedicated protection is also available in case of intermittent open load during deployment. In this case, if load is restored after an open circuit, due to slow reaction of the high-side current regulation loop, the current through the squib is limited only to I_{LIMSRx} by the low side driver. If this condition lasts for longer than t_{LIMOS} then the high side is turned off for $t_{HSOFFOS}$ and then reactivated. By this feature, intermittent open squib and short to battery faults may be distinguished and handled properly by the drivers.

6.5 Diagnostics

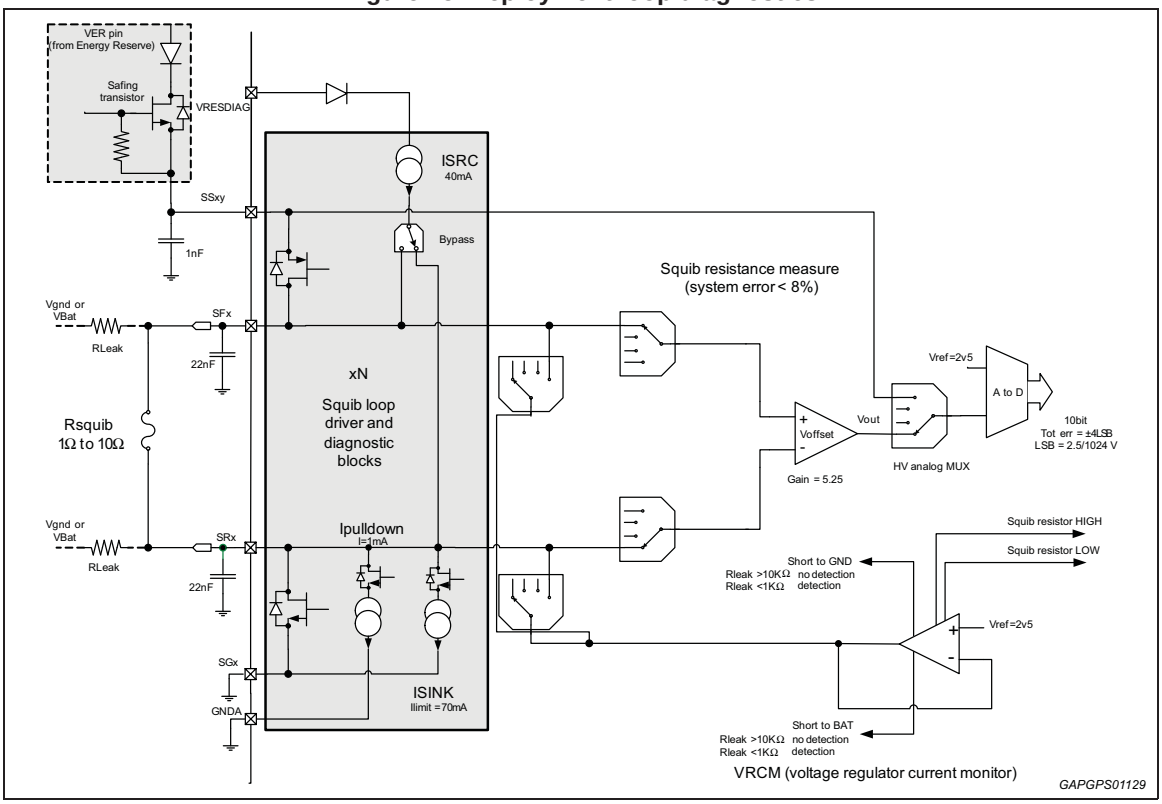
The L9678 provides the following diagnostic feedback for all deployment channels:

- High voltage leakage test for oxide isolation check on SFx and SRx
- Leakage to battery and ground on both SFx and SRx pins with or without a squib
- Loop to loop short diagnostics
- Squib resistance measurement with leakage cancellation
- High squib resistance with range from 500 Ω to 2000 Ω
- SSxy, SFx and VER voltage status
- High and low side FET diagnostics
- High side driver diagnostics
- Loss of ground return diagnostics
- High side safing FET diagnostics
- Deployment Timer diagnostic

The above diagnostic results are processed through a 10 bit Analog to digital algorithmic converter. These tests can be addressed in two different ways, with a high level approach or a low-level one. The main difference between the two approaches is that with the low level approach the user is allowed to precisely control the diagnostic circuitry, also deciding the proper timings involved in the different tests. On the other hand, the high level approach is an automatic way of getting diagnostic results for which an internal state machine is taking care of instructions and timings.

The following is the block diagram of the squib diagnostics.

Figure 25. Deployment loop diagnostics



The leakage diagnostic includes short to battery, short to ground and shorts between loops. The test is applied to each SFx and SRx pin so shorts can be detected regardless of the resistance between the squib pins.

6.5.1 Low level diagnostic approach

In this approach, each of the test steps described in the sections below requires user intervention by issuing the proper SPI command.

High voltage leakage test for oxide isolation check

This test is mandatory to address possible leakages that could not be experienced at low voltages on SFx or SRx pins. The I_{source} current generator (ISRC) is enabled on the chosen SFx pin. To confirm that the SFx pin has then reached a suitable voltage level, a dedicated ADC measurement on the SFx pin can be requested. Once this test is performed, a leakage test on SFx and SRx pins can be issued to double check possible leakages.

Leakage to battery/ground diagnostics

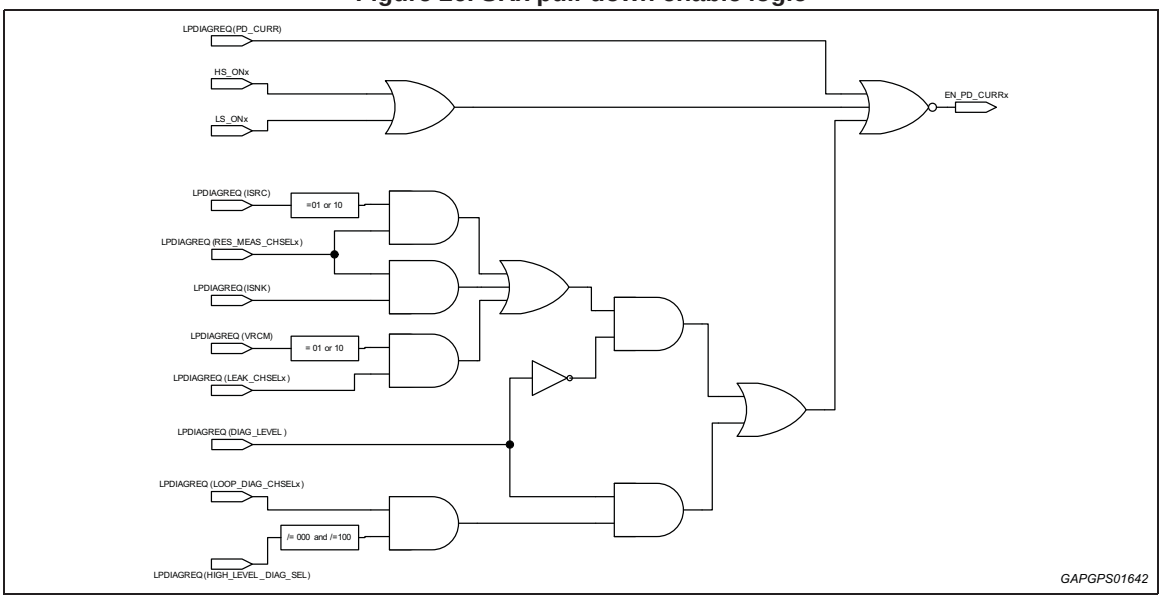
Prior to the real test, the Voltage Regulator Current Monitor block (VRCM) has to be tested and validated. The validation of VRCM goes into verifying both the short to battery and short to ground flags.

The I_{source} current generator (ISRC) is first connected to SFx pin to raise its voltage to VRESDIAG. Then, the Voltage Regulator Current Monitor block (VRCM) is enabled and connected to the selected SFx pin. The I_{sink} current limited switch (ISNK) is turned off, as

well as the pull-down current generator. If the VRCM block works properly, the short to battery flag would be asserted.

Then, the I_{sink} current limited switch (ISNK) is connected to SRx pin, the Voltage Regulator Current Monitor block (VRCM) is enabled and connected to the selected SRx pin. The I_{source} current generator (ISRC) is turned off, as well as the pull-down current generator. If the VRCM block works properly, the short to ground flag would be asserted.

Figure 26. SRx pull-down enable logic



Once the VRCM block is validated, the real leakage tests can be performed. ISRC and ISNK currents have to be kept switched off. The VRCM shall be connected to the desired pin (either SFx or SRx pins); by doing this, also the pull-down current on the selected SRx pin is automatically deactivated). During the test, if no leakage is present the voltage on the selected SFx or SRx pin will be forced by the VRCM to the VREF level and no current is detected or sourced by the VRCM. If there is leakage to ground or battery, the VRCM will sink or source current trying to maintain VREF. Two current comparators, ISTB and ISTG, will detect the abnormal current flow and the relative flags will be given in the LPDIAGSTAT (these flags are not latched and report the real time status of the relevant comparators in case of low-level leakage diagnostic test). In LPDIAGSTAT register are also reported the channel and the pin (SFx or SRx) under test, respectively with LEAK_CHSEL and SQP bit fields.

The pull-down currents on the other SRx pins are still active. Therefore, the leakage test that would show a leakage to ground may be depending on a real leakage on the pin under test or on a short between loops.

Short between loops diagnostics

In case the previous test has reported a leakage to ground fault, the short between loops diagnostics shall be run. The same procedure is followed as described for normal leakage tests except the fact that in this case all the pull-down current generators have to be deactivated (not only the one for the pin under test), by means of the PD_CURR bit in the Diagnostic Request Register (LPDIAGREQ). If a leakage or ground fault is not present, then the channel under test has a short to another squib loop.

Table 8. Short between loops diagnostics decoding

Fault condition on squib channel	Channel leakage diagnostics with PD_CURR on (for other channels than the one under test	Channel leakage diagnostics with PD_CURR off (for all channels)
No shorts	No fault	No fault
Short to battery	STB fault	STB fault
Short to ground	STG fault	STG fault
Short between loops	STG fault	No fault

The condition of two open channels, i.e. without squib resistance connecting SFx to SRx, that have a short between loops on SFx cannot be detected. If only one of the two shorted SFx pins is open, the fault is indicated on the open channel.

Squib resistance measurement

During a resistance measurement, a two-step process is performed. At the first step, both ISRC current generator and ISNK current limited switch are enabled and connected to the selected SFx and SRx channel, through ISRC, ISNK and RES_MEAS_CHSEL bit fields in the Loop Diagnostic Request Register (LPDIAGREQ). A differential voltage is created between the SFx and SRx pin based in the ISRC current and squib resistance between the pins. The SPI interface will provide the first resistance measurement voltage (Vout1) based on the amplifying factor of the differential amplifier and a 10 bit internal ADC conversion. The second measurement step (bypass measurement) is performed redirecting ISRC to the selected SRx pin, while keeping ISNK on; this way, the differential amplifier and following ADC will output the offset measurement through SPI (Vout2). Microcontroller is then allowed to calculate the mathematical difference between first and second measurements to obtain the real squib resistance value. The current sources ISRC and ISNK used for Squib Resistance measurements are completely controlled by the user via SPI. Optionally, an automatic control by the IC for current sources switch-off after ADC reading can be activated by enabling the EN_AUTO_SWITCH_OFF bit in the SYS_CFG register.

$$V_{out1} = G \times \left[I_{source} \times \left(\frac{R_{leak} \times R_{sq}}{R_{leak} + R_{sq}} \right) + \frac{R_{sq}}{R_{leak} + R_{sq}} (V_{gnd} - V_{refSQL}) \right] + G \times V_{offset}$$

$$V_{out2} = \frac{G \times R_{sq}}{R_{leak} + R_{sq}} \times (V_{gnd} - V_{refSQL}) + G \times V_{offset}$$

$$R_{sq} = \frac{\Delta V_{out}}{G \times I_{src}} \text{ (assuming } R_{leak} >> R_{sq})$$

where:

G = differential amplifier gain.

The simplification in the calculation method reported above can result in some amount of error that is already incorporated in the overall tolerance of the squib resistance measurement reported in the electrical parameters table.

Values of each measurement step can be required addressing the proper ADCREQx code in the Diagnostic Control command (DIAGCTRL) on *Table 11: Diagnostics control register (DIAGCTRLx) on page 159*.

This calculation is tolerant to leakages and, thanks to a dedicated EMI low-pass filter, also to high frequency noises on squib lines. Moreover, L9678 features a slew rate control on the ISRC current generator to mitigate emissions.

High squib resistance diagnostics

With this test, the device is able to understand if the squib resistance value is below 200 Ω, between 500 Ω and 2000 Ω or beyond 5000 Ω. During a high squib resistance diagnostics, VRCM and ISNK are enabled and connected respectively to SFx and SRx on the selected channel. VREF voltage level outputs on SFx. Current flowing on SFx is measured and compared to I_{SRlow} and I_{SRhigh} thresholds to identify if the resistance is above or below R_{SRlow} or R_{SRhigh} levels. The results are reported in the LPDIAGSTAT register. The relative flags (HSR_HI and HSR_LO) are not latched and reflect the current status of the comparators.

High and low side FET diagnostics

This couple of tests can only be run during the diagnostic mode of the power-up sequence (*Figure 9*). Tests are performed individually for HS driver or LS driver, with two dedicated commands. Prior to either the HS or LS FET diagnostics being run, the VRCM has to be first enabled. Within the command to enable the VRCM, also the channel onto which the FET test will be run has to be selected with the LEAK_CHSEL bit field. Running the leakage diagnostics with the appropriate delay time prior to either the HS or LS FET diagnostics will precondition the squib pin to the appropriate voltage level. When the FET diagnostic command is issued with the Diagnostic Register SPI command (SYSDIAGREQ), the VRCM flags will be cleared.

The device monitors the current through the VRCM. If the FET is working properly, this current will exceed I_{STB} (HS test) or I_{STG} (LS test) and the driver under test is turned off immediately. If the current does not exceed I_{STB} or I_{STG} then the test will be terminated and the output is anyway turned off within $T_{FETTIMEOUT}$. During $T_{FETTIMEOUT}$ period, the bit stating that the FET is enabled will be set (FETON=1) and will be cleared as soon as the FET is switched back off.

For all conditions the current on SFx/SRx will not exceed $I_{LIM\_VRCM\_X}$, the VRCM block current limitation value. There may be higher currents on the squib lines due to the presence of filter capacitors. During these FET tests, energy available to the squib is limited to less than $E_{FETtest}$.

For high side FET diagnostics, if no faults were indicated in the preceding leakage diagnostics then a normal result would be [STB=1, STG=0]. If the returned result for the high side FET test is not as the previous then either the FET is not functional, a short to ground occurred during the test, or there is a missing SSxy connection for that channel.

For low side FET diagnostics if no faults were indicated in the preceding leakage diagnostics then a normal result would be [STB=0, STG=1]. If the returned result for the low side FET test is not as the previous one then either the FET is not functional or a short to battery occurred during the test. In case of SGx loss the low-side FET diagnostic would not indicate a FETfault.

The VRCM flags will be given in the LPDIAGSTAT register. The status of the VRCM flags after FET test is latched and can be cleared upon either LPDIAGREQ or SYSDIAGREQ SPI commands.

Loss of ground return diagnostics

This diagnostics is available during a squib measurement or a high side driver diagnostics. This test is based on the voltage drop across the ground return, if the voltage drop exceeds V_{SGopen}, ground connection is considered as lost. Should the ground connection on the squib driver circuit be missing, the bit related to the channel under test by the two above diagnostics will be activated in the LP_GNDLOSS register. The flag is latched after a proper filter time t_{SGopen} and cleared upon read.

High side safing FET diagnostics

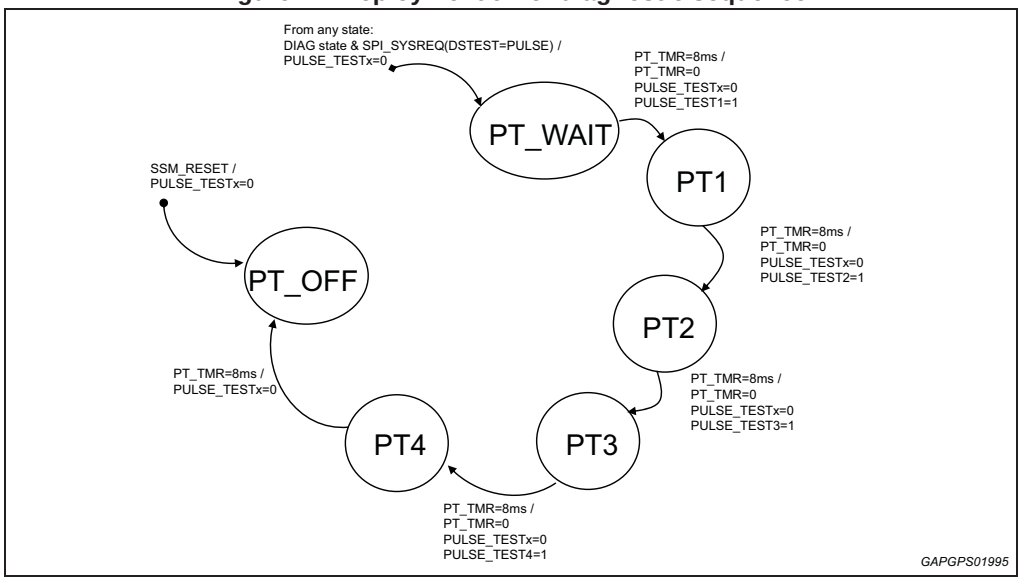
This test has to be issued during the Diag state of the power-up sequence (*Figure 9*). Safing FET has to be switched on with the proper code in DSTEST bit field of the SYSDIAGREQ. Therefore, when the command is received, the device activates VSF regulator to supply the external safing FET controller. The user can measure the voltage levels of both the VSF regulator and the SSxy nodes. If the safing FET is properly switched on, the voltage on SSxy is regulated.

The measurement request is done via Diagnostic Control command (DIAGCTRLx), while results are reported through ADCRESx bit fields, as shown in *Table 11*.

Deployment timer diagnostic

This test allows verifying the correct functionality and duration of the timers used to control the deployment times. This test can be executed only when the IC is in the Diag state by setting the appropriate code in the DSTEST field of the SYSDIAGREQ register. When the test is launched, the IC sequentially triggers the activation of the deployment timers of the various channels (each of them separated by 8ms idle time) and outputs the relevant waveform to the ARM output discrete pin. See the sequence detail in *Figure 27*. The MCU can therefore test the deployment times by measuring the duration of the high pulses sent by the IC on the ARM pin. The deployment time configuration used during this test is the latest one programmed in the DCRx registers. In case the test is run on a channel with no DCRx deployment time previously configured, a default 8us high pulse is output on ARM for the relevant channel.

Figure 27. Deployment timer diagnostic sequence



Loop diagnostics control and results registers

Diagnostic tests and channels for each test are controlled through the Loop Diagnostic Request Register (LPDIAGREQ), diagnostic results are stored in the Loop Diagnostic Status Register (LPDIAGSTAT).

6.5.2 High level diagnostic approach

In this approach, the test steps described in the sections below are coded into a dedicated state machine that helps reducing the user intervention to a minimum.

The high-level diagnostic commands are contained in the LPDIAGREQ, LOOP_DIAG_SEL, and LOOP_DIAG_CHSEL registers. These settings are described in the SPI Table for these commands in *Read/write register*.

The high-level diagnostic response is available in the LPDIAGSTAT register. These are described in the SPI Table for this command in *Read/write register*.

The concept is depicted in the following figures.

Figure 28. High level loop diagnostic flow1

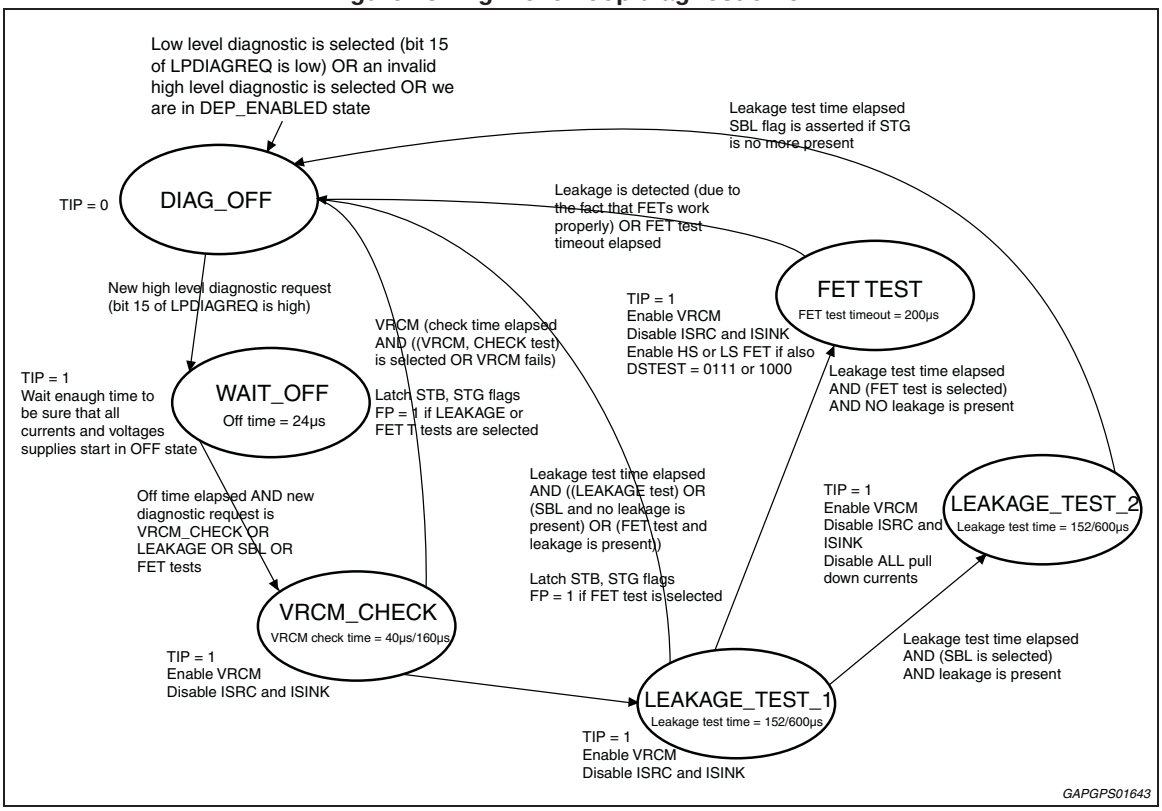
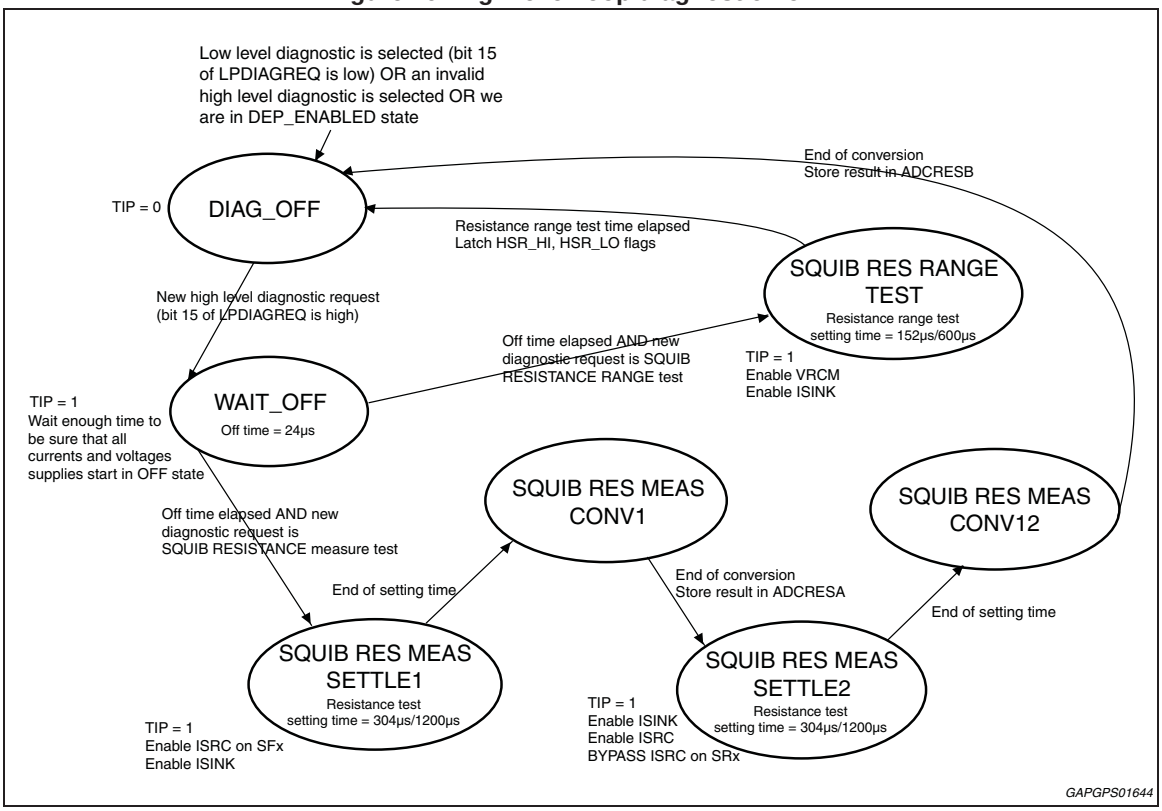


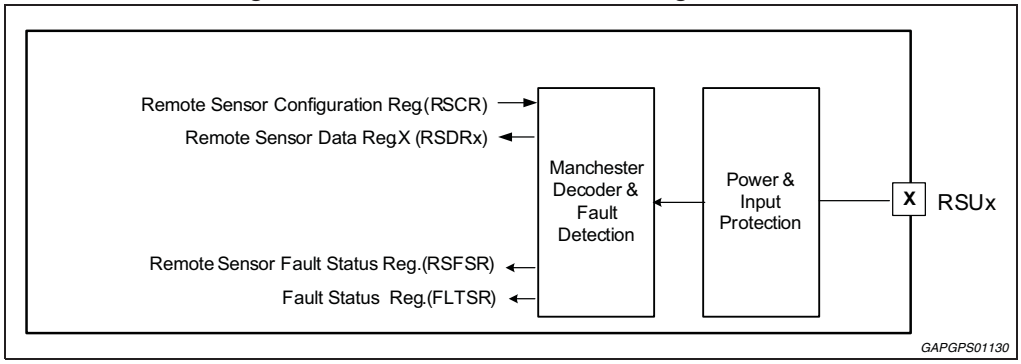
Figure 29. High level loop diagnostic flow2



7 Remote sensor interface

The L9678-S contains 2 remote sensor interfaces, capable of supporting PSI-5 protocol (standard voltage range). A block diagram of the interface is shown below. The circuitry consists of a power interface that demodulates current flowing in the external sensor and transmits these current states to the decoder, which produces a digital value for each satellite channel. Data are then output through the Remote Sensor Data Registers (RSDRx). The power interface also contains error detection circuitry. When a fault is detected, the error code is stored in a global SPI data buffer in the Remote Sensor Data Registers (RSDRx).

Figure 30. Remote sensor interface logic blocks



The Remote Sensor Configuration Registers (RSCRx) allow for configuration of the particular PSI5 protocol adopted by the sensor and the transceiver current limit blanking time.

The Remote Sensor Control Register (RSCTRL) allow for interface channels to be switched on and off via SPI.

RSU interface has 2 registers per channel, which can report either data or fault information, that can be readout by sending 2 consecutive Read commands of the Remote Sensor Data Register (RSDRx). It is a FIFO, so the first SPI reading contains the oldest received data and the next SPI reading contains the most recent one. SPI accesses both from the same address, i.e. the MCU should do 2 reads of the same RID to get both data samples. The couple of registers will retain only the last two received messages, regardless they have been qualified as valid or invalid data. In case of driver fault (Short to Ground, Short to Battery, Over-current, Open detection, Over-temperature) any message is lost. To re-start a correct reception of messages, it is needed to have no more fault present and fault flag read by MCU.

If the device detects an error on the sensor interface, the fault bit in RSDRx (FLTBIT) will be set to '1' and the following bits will be used to report the detected errors. Otherwise, the register will contain only data information. Detailed information on data and fault reporting are explained in the following sections.

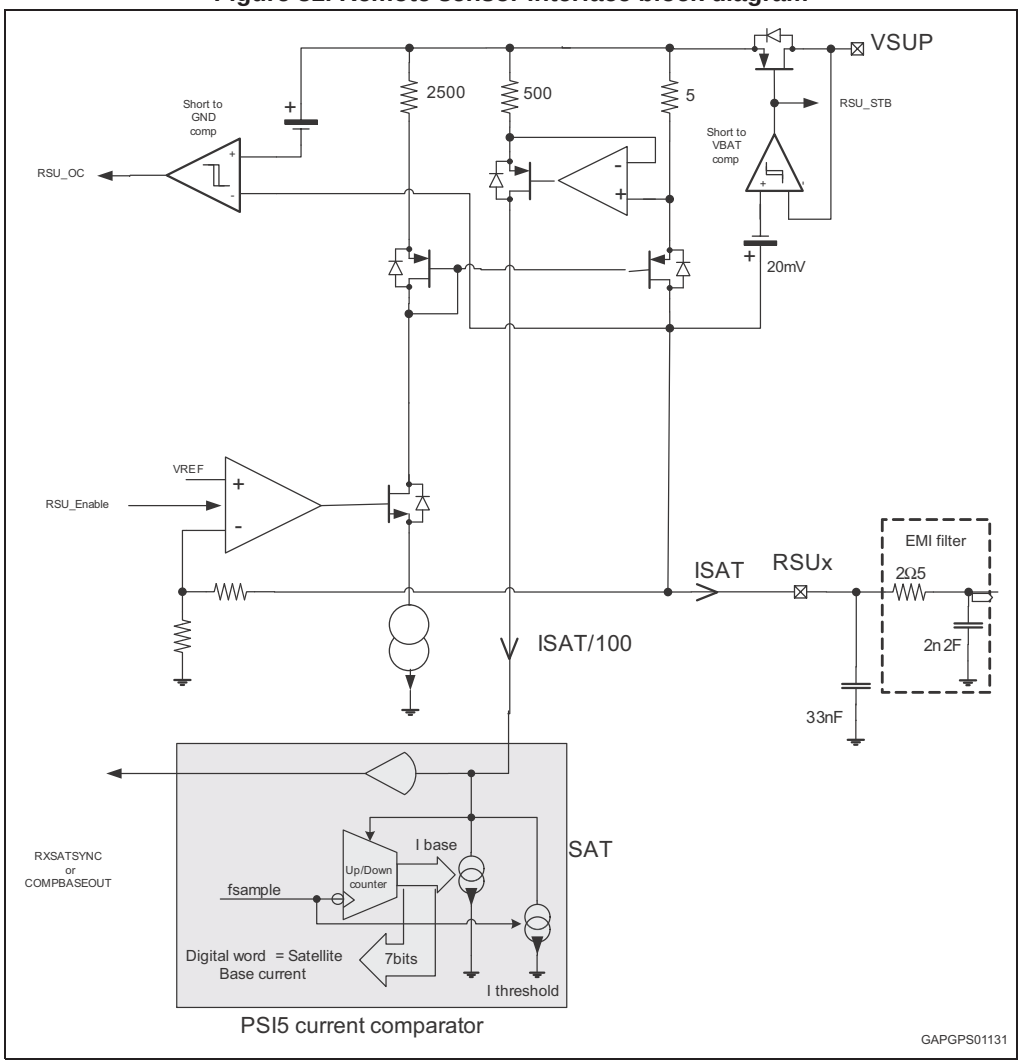
When a fault condition is detected, the RSFLT bit of the global status word (GSW) is set to 1, except in the case the register is empty for which NODATA fault bit will be set instead.

Data are cleared upon reading the RSDRx register.

RSU interface is supplied by VSUP regulator as showed in *Figure 31*. To avoid a too low RSU output voltage in case of battery loss, the upper VINGOOD and VBATMOND

thresholds must be selected. In this way the device will detect the battery loss condition in time to guarantee the minimum RSU output voltage required.

Figure 31. Remote sensor interface block diagram



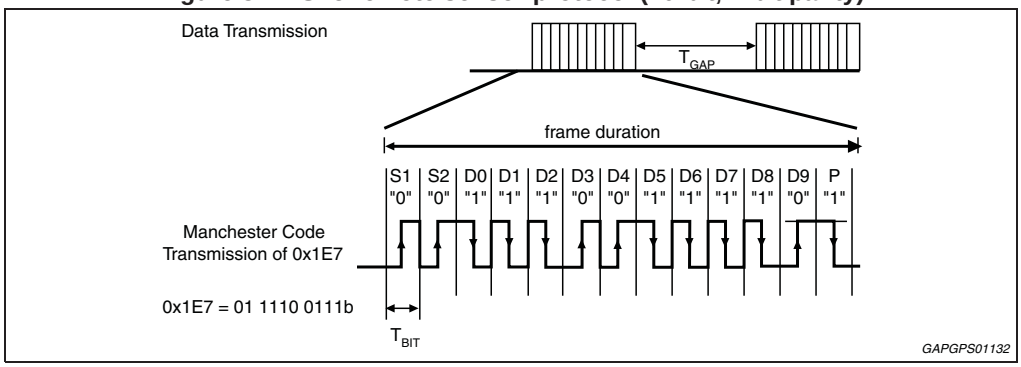
7.1 PSI-5 protocol

All channels are compliant to the PSI-5 v1.3 specification as described below:

- Two-wire current interface
- Manchester coded digital data transmission
- High data transmission speeds of 125 kbps and 189 kbps
- Variable data word length (8 & 10 bit only)
- 1-bit parity
- Asynchronous operation mode

An example of the data format for one possible PSI-5 protocol configuration is shown below. Data size may vary, but the presence of 2 sync start bits (referenced below as sync bits) and T_{Gap} time is consistent regardless.

Figure 32. PSI-5 remote sensor protocol (10-bit, 1-bit parity)



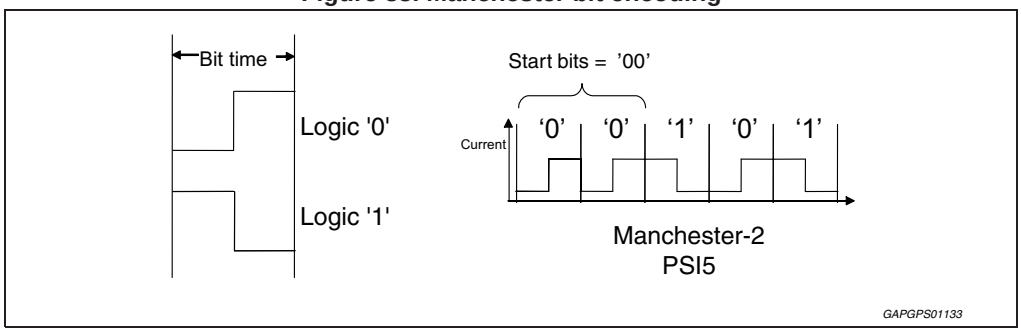
7.1.1 Functional description - remote sensor modes

The Remote sensor Interface block provides a hardware connection between the microcontroller and up to two remote sensors. Each channel is independent of the other, and is not influenced by fault conditions, such as short circuits to ground or vehicle battery, on the other channel. Each channel supplies an independently current limited DC voltage to its remote sensor derived from VSUP, and monitors the current draw to extract encoded data. The remote sensors modulate the current draw to transmit Manchester-encoded data back to the receiver. The current level detection threshold for all channels is automatically set by the integrated current adjust feature in order to adapt to the quiescent current draw of the sensors.

All channels can be enabled or disabled independently via SPI commands. The operational status of all channels can also be read via SPI command.

The message bits are encoded using a Manchester format, in which logic values are determined by a current transition in the middle of the bit time. The interface supports Manchester 2 encoding as shown in *Figure 33*.

Figure 33. Manchester bit encoding



The received message data are stored in input data registers that are read out by the microcontroller via the SPI interface. All bits of these registers are simultaneously updated upon reception of the remote sensor message to prevent partial frame data from being sampled via the SPI interface. After the data for a given channel is read via the SPI

interface, subsequent requests for data from this channel will result in an error response (NODATA fault).

The remote sensor interface is also able to detect faults occurring on the sensor interface. The Remote Sensor Data Register (RSDRx) will report multiple fault flags.

When the number of bits decoded is incorrect (either too many or too few), a bit error is indicated. When any bit error is detected (bit time, too many bits or too few bits), the message is discarded.

Error bit INVALID is an OR-ed combination of the following errors:

- Data length error or stop bit error
- Parity Error of received Remote sensor Message
- Bit time error (a data bit edge is not received inside the expected time window)

Should one or more of the channel faults (STG, STB, CURRENT_HI, OPENDET and RSTEMP) be set, the INVALID and NODATA bits are cleared.

7.1.2 RSU data fields and CRC

The remote sensor interface reports both data information and fault information in the Remote Sensor Data Register (RSDRx). Independent data registers are defined for each remote sensor interface and the data contained therein is formatted differently based on whether a fault is detected. See SPI command in *Remote sensor data/fault registers w/o fault (RSDRx) on page 91*.

The data available in the RSDRx register is separated into several bit fields. The Logical Channel ID is a 4-bit field to identify the satellite sensor. The DATA bits are appended to the LCID at the output of the Manchester decoder. The 3-bit CRC bit field is computed on the entire data packet of fields, bits[16:0], which also includes the CHxON and FLTBIT. To satisfy safety requirements, the LCID, DATA and CRC bit fields propagate through the same data path as a single item to the SPI output.

The polynomial calculation implemented for PSI5 data is described as in PSI5 specification g(x)=1+x+x^3 with the initialization value equal to "111".

Below are the equations to calculate the CRC in combinatorial way:

CRC[2] = CRCext[0]+D[0]+D[1]+D[3]+D[6]+D[7]+D[8]+D[10]+D[13]+D[14]+D[15]

CRC[1] = CRCext[2]+D[0]+D[1]+D[2]+D[4]+D[7]+D[8]+D[9]+D[11]+D[14]+D[15]+D[16]

CRC[0] = CRCext[1]+CRCext[0]+D[0]+D[2]+D[5]+D[6]+D[7]+D[9]+D[12]+D[13]+D[14]+D[16]

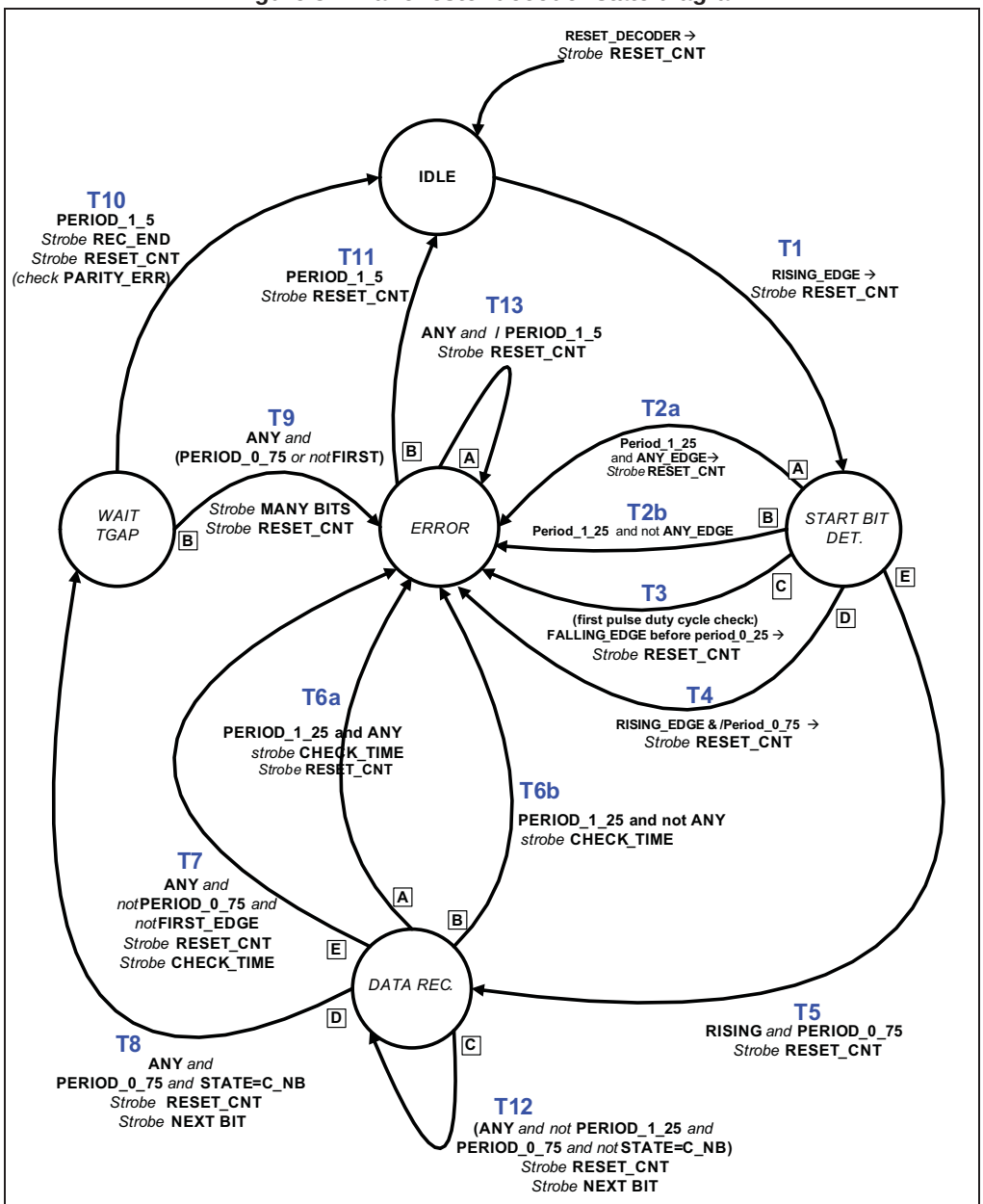
where D[16:0]= RSDR[16:0] and CRCext[n] are the starting seed values (all '1').

7.1.3 Detailed description

Manchester decoding

The Manchester decoder will support remote sensor communication as per PSI specification rev 1.3 for the modes configurable via the STS bits in the RSCRx registers.. The Manchester Decoder checks the duty-cycle and period of the start bits to determine their validity, depending on the configuration of the PERIOD_MEAS_DISABLE bit in the RSCRx registers. The expected time windows for the mid bit transitions of each subsequent bit within the received frame is determined by means of the internal oscillator time base. Glitches shorter than 25% of the minimum bit time duration are rejected.

Figure 34. Manchester decoder state diagram



DataFilt	:= Filtered Raw Data (RXSAT) from Current Demodulator (after deglitcher)
RISING_EDGE	:= DataFilt(n+1, n) == "01"
FALLING_EDGE	:= DataFilt(n+1, n) == "10"
ANY	:= RISING_EDGE or FALLING_EDGE
C_NB	:= 8bit frame configurated ? 10 : 12
STATE	:= {0@IDLE, 1@STATBITDET, 2@T5, STATE++@T12, 0xE@WAIT, 0xF@ERROR}
BitCounter	:= RESET_CNT ? 0 : BitCounter++
Period_1_50	:= BitCounter >= BitPeriod*1.5
Period_1_25	:= BitCounter >= BitPeriod*1.25
Period_0_75	:= BitCounter >= BitPeriod*0.75
FIRST_EDGE	:= Period_0_75? 1 : ANY? 0 : FIRST_EDGE after a delay of Tck (Remark: not a combinatorial signal)

End of message definition for use in timeslot control: EOM = T10+T9+T7+T6a+T6b

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A Manchester Decoder Error occurs if one or more of the following conditions are true:

- Two valid start bits are detected, and at least one of the expected 13 mid-bit transitions are not detected
- Two valid start bits are detected, and more than 13 mid-bit transitions are detected
- When the number of bits decoded is incorrect (either too many or too few), a bit error is indicated. When any bit error is detected (bit time, too many bits, too few bits), the decoder will revert to the minimum bit time of the selected range and the message is discarded.

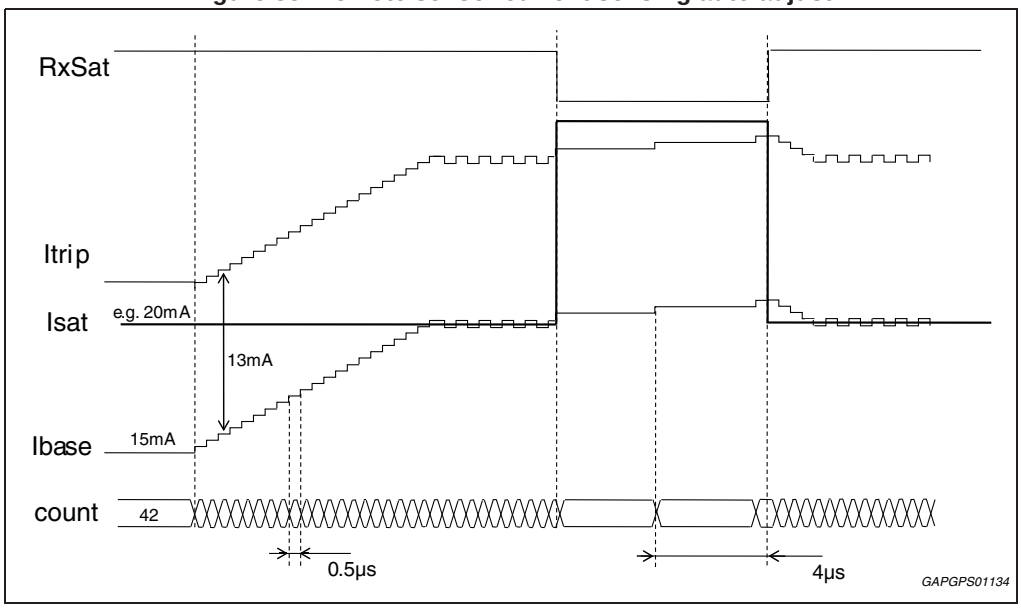
All errors are readable through the Sensor Fault Status Register and the RSFLT bit in the Global Status Word Register.

When a valid message is correctly decoded, the 10/8 data bits are stored into the appropriate RSDRx register together with the related LCID. The RSDRx register contains the 10/8 bits data as they are received from the sensor (no data range check/mask is done at this stage). The 8-bit data word is right-justified inside the 10-bit data field in the RSDRx registers.

Current sensor with auto-adjust trip current

The current sensor is responsible for translating the current drawn by the sensor into a digital state (refer to *Figure 35*). Each satellite channel has a dedicated current sensor with hysteresis.

Figure 35. Remote sensor current sensing auto adjust



The auto adjust feature uses a 7 bit D/A to converter to step up and down the threshold level for detecting the base current through the remote sensor before start bits are transmitted. Once start bits are received, the counter stops and the D/A value remains fixed until the remote sensor message is received. This procedure is repeated for each cycle of the remote sensor. The auto adjust circuit uses the following equation:

$I_{base} = I_{offset} + (D/A\ counts) * 300\ \mu A$ where I_{offset} is fixed to 2.5 mA

The converter default count value is 42, therefore,

I_{base} = 2.5 mA + 42 * 300 µA

I_{base} = 15 mA

I_{trip} = I_{base} + threshold where threshold is a fixed at 12 mA

Thanks to this implementation, I_{base} can span from 2.5 mA up to 41 mA covering PSI-5 specification range. As an example, for a remote sensor that operates at 10 mA base current, I_{trip} = 23 mA.

7.2 Remote sensor interface fault protection

7.2.1 Short to ground, current limit

Each output is short circuit protected by an independent current limit circuit. Should the output current level reach or exceed the ILIMTH for a time period greater than TILIMTH the output stage is disabled and an internal up-down counter will count in 25 µs increment up to TILIMTH. The filter time is chosen in order to avoid false current limit detection for in-rush current that may happen at interface switch-on. When the output is turned off due to current limit, the appropriate fault code STG is set in the Remote Sensor Data Register (RSDR). The fault timer latch is cleared when the sensor channel is first disabled and then re-enabled through the Remote Sensor Configuration Register (RSCR). This fault condition does not interfere with the normal operation of the IC, nor with the operation of the other channels. When a sensor fault is detected, the RSFLT bit of the GSW is set indicating a fault occurred and can be decoded by addressing the RSFSR register.

In order to fulfil the blanking time requirement at channel activation as per PSI-5 specification, a dedicated masking time is applied to the current limitation fault detection each time a channel is activated.

7.2.2 Short to battery

All outputs are independently protected against a short to battery condition. Short to battery protection disconnects the channel from its supply rail to guarantee that no adverse condition occurs within the IC. The short-to-battery detection circuit has input offset voltage (10 mV, minimum) to prevent disconnecting of the output under an open circuit condition. A short to battery is detected when the output RSUx pin voltage increases above VSUP supply pin voltage for a T_{STBTH} time. An internal up-counter will count in 1.5 µs increment up to T_{STBTH}. The counter will be cleared if the short condition is not present for at least 1.5 µs. Short to battery protection blocks the battery condition to guarantee that no adverse condition occurs within the IC. The channel in short to battery is not shut down by this condition. Other channels are not affected in case of short of one output pin. As in the case previously described, the STB fault code can be read from RSDR bits and any fault will set the RSFLT bit of the global status word register (GSW). The STB bit is cleared upon read.

7.2.3 Cross link

The device provides also the capability of a cross link check between outputs, in order to reveal conditions where two output channels are in short. This functionality is allowed by enabling one output channel, while asking for voltage measurement on any of the other ones.

7.2.4 Leakage to battery, open condition

The remote sensor interface offers detection of an open sensor condition. The auto-adjusting counter for remote sensor current sensing will drop to 0 in case the current flowing through RSUx pin is lower than 3 mA. The OPENDET fault flag is asserted when the fault condition lasts for longer than T_{RSUOP_FILT} deglitch filter time. This fault flag can be read from RSDR bits and any fault will set the RSFLT bit of the global status word register (GSW). The channel in this condition is not shutdown.

7.2.5 Leakage to ground

The sensor interface offers as well the detection of a leakage to ground condition, that will possibly raise the sensor current higher than 36 mA. The CURRENT_HI fault flag is asserted when the fault condition lasts for longer than T_{RSUCH_FILT} deglitch filter time. This fault flag can be read from RSDR bits and any fault will set the RSFLT bit of the global status word register (GSW). The channel in this condition is not shutdown.

7.2.6 Thermal shutdown

Each output is protected by an independent over-temperature detection circuit Should the remote sensor interface thermal protection be triggered the output stage is disabled and a corresponding thermal fault is latched and reported through the RSTEMP flag in the Remote Sensor Data Register (RSDRx). The thermal fault flag is cleared when the sensor channel is first disabled and then re-enabled through the Remote Sensor Configuration Register (RSCRx).

8 Watchdog timer

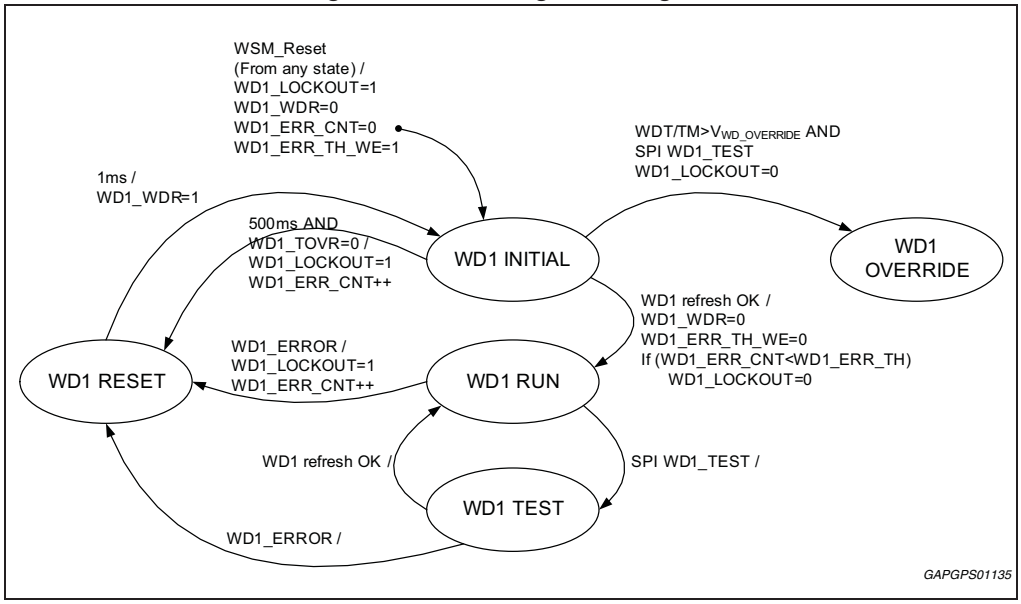
This device offers a watchdog implementation by means of a temporal WD. Window times are SPI programmable and a couple of specific codes has to be written within this window in order to serve the WD control.

8.1 Temporal watchdog

The temporal watchdog ensures the system software is operating correctly by requiring periodic service from the microcontroller at a programmable rate. This service (watchdog refresh) must occur within a time window, and if serviced too early or too late will enter an error state (WD1_ERROR) reported via the WD1_WDR bit of the FLTSR register.

The overall WD1 functionality is described in the state diagram reported in *Figure 36*.

Figure 36. Watchdog state diagram



Following the description of the above states:

Table 9. Watchdog timer status description

State/Signal	Description
WD1 INITIAL	Default state entered from startup. While in this state, no watchdog service is required, and the IC may stay in this state indefinitely. For system safety, all arming signals are disabled during this state to prevent deployment.
WD1 RUN	Normal run-time state where WD1 service is required.
WD1 TEST	A special state used to test the watchdog function. Normally, this state will only be checked once per power cycle by the software, but there is no inherent restriction in the watchdog logic preventing periodic testing. This state allows testing of the watchdog refresh function without setting WD1_LOCKOUT=1, which can only be cleared via WSM reset. Deployment is inhibited when the WD state machine is in this state.
WD1 RESET	State entered when a WD1_ERROR occurs. This is a timed-duration state that is automatically exited after 1ms.
WD1 OVERRIDE	A special state used to disable watchdog functionality for development purposes. Other logic within the IC can use this state to emulate the WD1 RUN state without the need to service WD1.
WSM_RESET	Signal used to reset the WD1 state machine to the WD1 INITIAL state and all signals to their inactive values
WD1_refresh OK	Signal that is asserted only if the watchdog is refreshed ('A' - 'B' or 'B' - 'A' seq.) within the WD1 time window
WD1_ERROR	Signal that is asserted if the watchdog refresh fails to occur during the WD1 time window.
WD1_WDR	Watchdog Reset – latched signal that is activated whenever a watchdog error is qualified. For WD1, this occurs when WD1 service is required, but not received. This signal is SPI-readable.
WD1_TM	Test Mode – a signal that indicates that WD1 is being tested. This signal is SPI-readable.
WD1_LOCKOUT	A latched signal activated if an unexpected WD1 error occurs. This signal is permanently latched when set (until WSM_RESET). When set, all arming signals are disabled, preventing deployment. This signal is SPI-readable.
SPI_WD1_TEST	SPI command used to enter WD1 TEST state from WD1 RUN state, or to enter WD1 OVERRIDE state from INITIAL state if WDT/TM pin voltage is greater than the threshold. This command has no effect in other states.
WD1_ERR_CNT	Retry counter to let the microcontroller fails multiple times before set LOCKOUT and prevent deployment.
WD1_ERR_TH	SPI configurable threshold for the retry counter.
WD1_ERR_TH_WE	Signal to lock the writing of WD1_ERR_TH when watchdog entered RUN state.

A single SPI command (WD_TEST) is used to activate test states for the watchdog circuitry.

8.1.1 Watchdog timer configuration

The watchdog timer can be configured on two different frequency modes:

- Fast watchdog with maximum range of 2 ms and a resolution of 8 µs;
- Slow watchdog with maximum range of 16.3 ms and a resolution of 64 µs.

The watchdog window times are SPI programmable. The configuration of watchdog timer frequency and window times can be done by setting the Watchdog Timer Configuration Register (WDTCR) with the appropriate values. However, this configuration is accepted only when the device is in the Init operating state, as shown in *Figure 9*. As soon as the Diag state is entered, the watchdog control is enabled and the watchdog configuration is fixed and cannot be changed anymore.

8.1.2 Watchdog timer operation

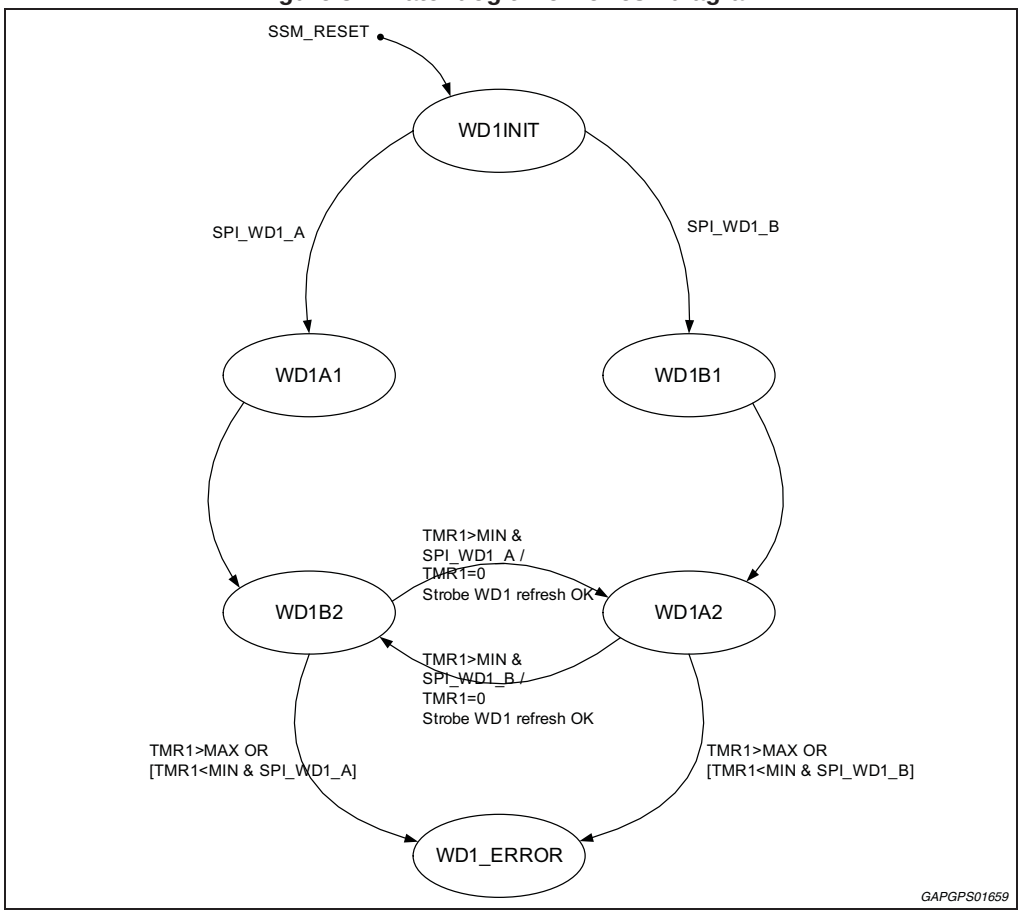
While in the WD1_INITIAL state, watchdog service must begin or a SPI command with WD1_TOVR=1 must be received within the first 500 ms. If the WD1 timer override bit is set, the device can stay in the WD1_INITIAL state indefinitely without watchdog service.

To refresh WD1, the logic must receive a Watchdog Timer Register (WD1T) SPI command containing the expected key value within the WD1 time window (WDTMIN+WDTDELTA). If it is received too early or too late the WD1_ERROR signal will be asserted. The WD1_ERROR will not be asserted in case a SPI command containing the Watchdog Timer Register (WD1T) with an incorrect key value is received at any time relative to the window (WDTMIN+WDTDELTA). This allows the system software to repeatedly transmit the key value until it needs to change to the correct key value.

Upon reception of the correct key value within the window, the logic will reset the watchdog timer to create a new window.

The timer is cleared upon writing code 'A' and code 'B' (either in 'A' - 'B' or 'B' - 'A' sequences) to the WD1CTL[1:0] bits, in the WD1T register. The watchdog timer value can be read via the WD1T register.

Figure 37. Watchdog timer refresh diagram



8.2 Watchdog reset assertion timer

Upon a watchdog reset, the watchdog logic will momentarily assert the RESET pin for time duration t_{wdrst}. When the RESET pin has been asserted through the watchdog reset assertion timer, stored faults are maintained and can be read by the microcontroller via SPI following the RESET period.

8.3 Watchdog timer disable input (WDT/TM)

This input pin has a passive pull-down and is used to disable the watchdog timer. The state of this pin can be read by SPI through the WDTDIS_S bit in the GSW register. When WDT/TM pin is asserted, the watchdog timer is disabled, the timer is reset to its starting value and no faults are generated.

9 DC sensor interface

L9678 implements a circuitry able to interface with a variety of positioning sensors. The sensors that can be connected to the device are Hall-effect, resistive or simple switches.

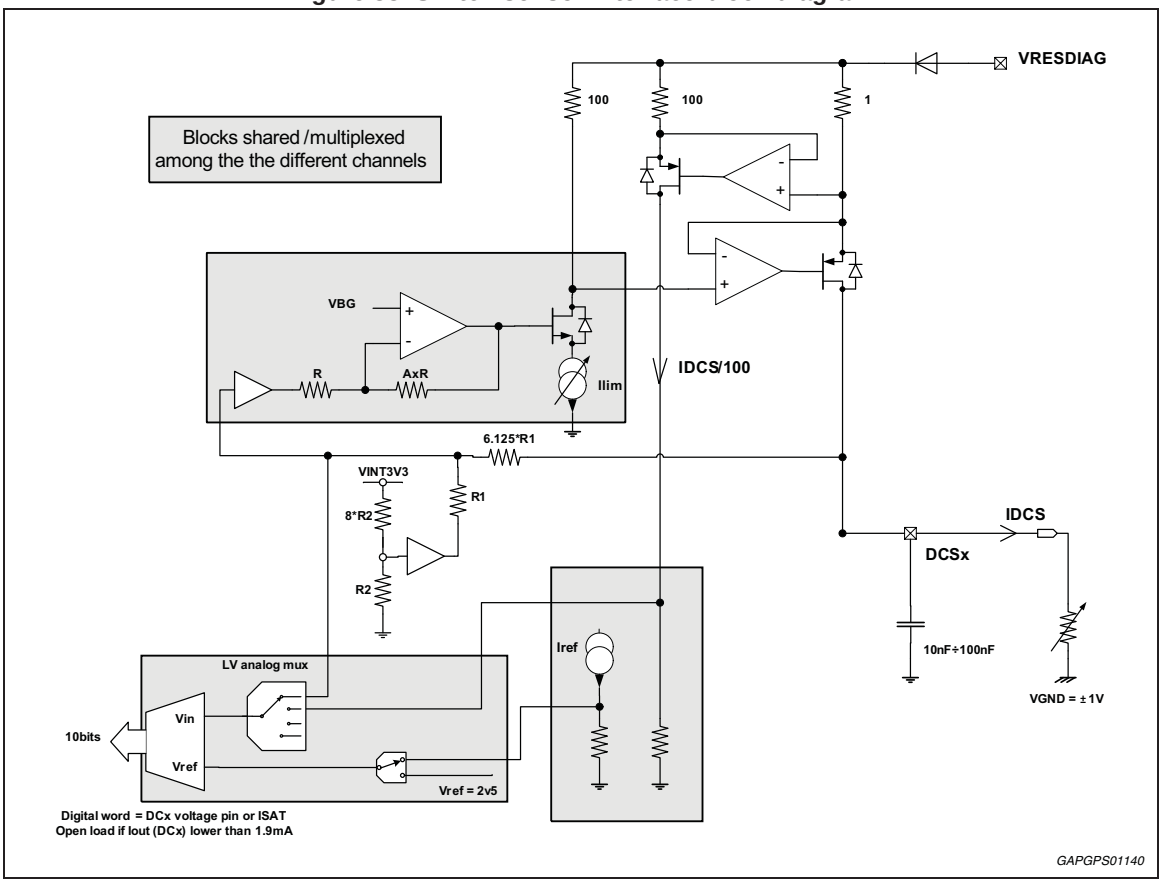
Range of measurements is:

- Resistive sensor: 65 Ω to 3 kΩ
- Hall-effect sensor: 2 mA to 20 mA.

Within the above ranges, accuracy of ±15% is granted. A reduced accuracy is given in the range 1 mA to 2 mA.

Hall sensor and switch interface block diagram is shown below.

Figure 38. Switch sensor interface block diagram



The global SPI contains several bits to control and configure the interface. The SWOEN bit is used to enable the output voltage on DCSx pins. The channel to be activated can be chosen by accordingly setting CHID bits. The interface activation is completely controlled by user SPI command. The interface could be optionally configured for "automatic switch-off" immediately after the current or resistance measurement completion by setting the EN_AUTO_SWITCH_OFF bit in the SYS_CFG register.

The voltage and current for the selected channel are made available to the main ADC by selecting the proper channel and enabling the measurement process by dedicated DIAGCTRLx commands.

The device offers the capability to actively keep all the DCSx lines discharged by means of a weak pull down. The pull down is active by default on all channels and it comes to be deactivated in either of the following cases:

1. when the voltage source is active on the relevant channel
2. when a voltage measurement is requested on the relevant channel
3. if SPI bit SWCTRL(DCS_PD_CURR) is set (global pull-down disable for all channels)

In case of Hall-effect sensors, a single current measurement is processed. The current load needed for regulating the pin is internally reflected to a reference resistance, whose voltage drop is then measured through the internal ADC converter.

When resistive or switch sensors are used, a more complex measurement is performed. In a first step the current information as above described is provided. Then, also the information on the voltage level achieved on the output pin is provided via ADC. By processing these two values, the micro-controller can understand the resistive value. The DCSx voltage is internally rescaled by a voltage divider into the ADC converter voltage range as shown in *Figure 38*. Additionally a positive voltage offset is internally applied to the scaled voltage in order to allow voltage measurement capability for DCSx down to -1V.

In order to have accurate resistive information even in case of an external ground voltage shift on the sensor of up to ±1V, the voltage measurement step actually needs two DCSx voltage measurements. A first voltage measurement has to be done with selection of 6.25 V on the output channel and a second one with the regulator switched off. The difference between the two measurements will cancel out the offsets (both external ground shift and internal offset).

The DCSx current and voltage can be retrieved from ADC readings according to the following formulas and related parameters specified in *Section 15.19: DC sensor interface* and *Section 15.23: Voltage diagnostics (analog Mux)*:

$$I_{DCSx} = \frac{1}{R_{REF1\_IDCSx}} \cdot \frac{ADC_{REF\_hi}}{2^{ADC_{RES}}} \cdot DIAGCTRLn(ADCRESn)$$

@DIAGCTRL(ADCREQn = $04

$$V_{DCSx} = RATIO_{VDCSx} \cdot \left(\frac{ADC_{REF\_hi}}{2^{ADC_{RES}}} \cdot DIAGCTRLn(ADCRESn) - V_{OFF\_DCSx} \right)$$

@DIAGCTRL(ADCREQn = $03

The DCSx sensor resistance can be calculated according to the following formula:

$$R_{sensor_x} = \frac{\Delta V_{DCSx}}{I_{DCSx}} = \frac{V_{DCSx}@(SWCTRL(SWOEN)=1 - V_{DCSx}@(SWCTRL(SWOEN)=0}{I_{DCSx}}$$

@SWCTRL(CHID) = x

The device provides also the capability of a cross link check between outputs, in order to reveal conditions where two output channels are in short. This functionality is allowed by enabling one output channel, while asking for voltage measurement on any of the other ones.

All parametric requirements for this block can be found in specification tables.

Each output is protected against

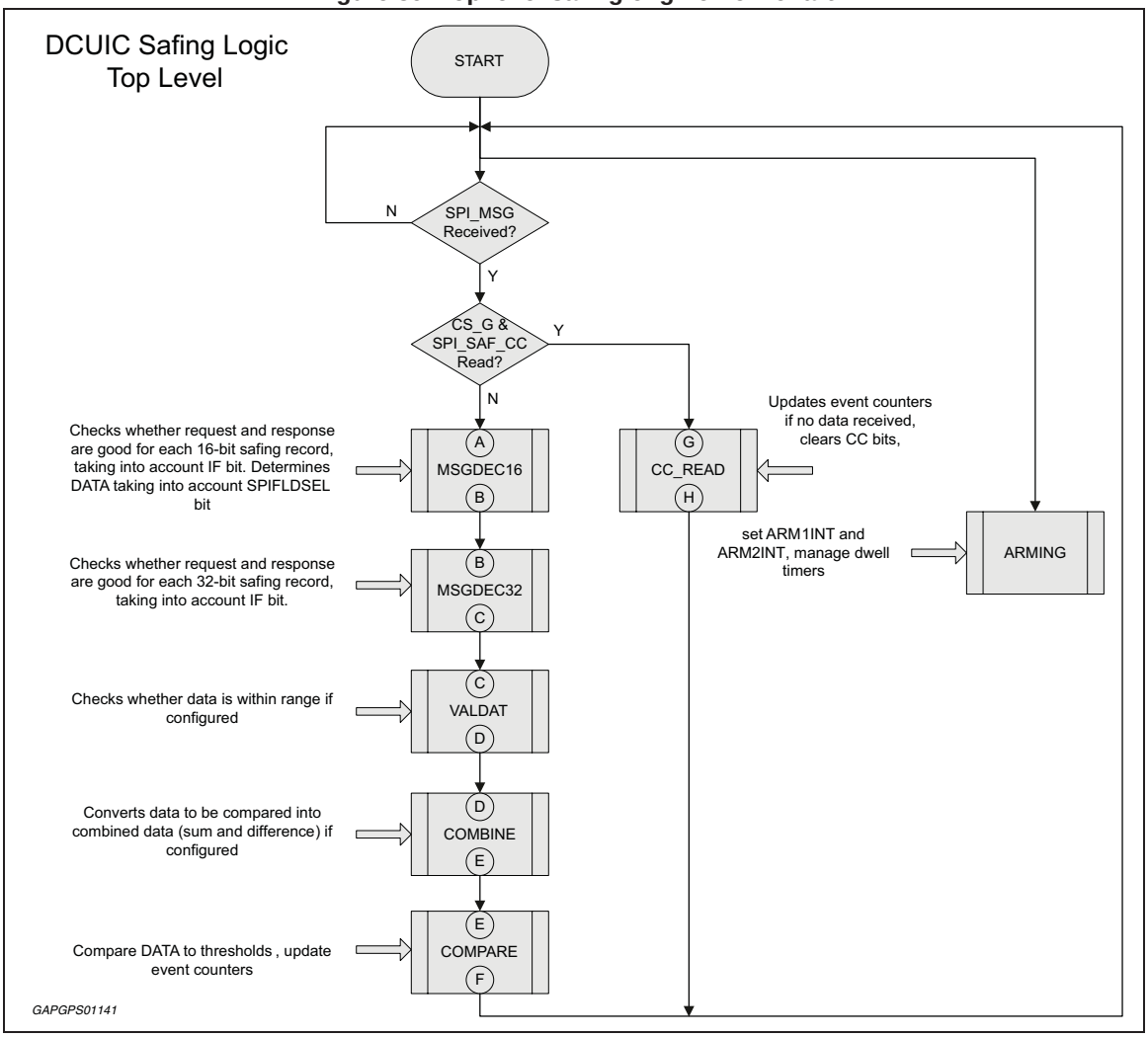
- Overload conditions by current limit
- Ground offset between the ECU and the loads of up to ±1 V.
- Loss of ECU battery
- Loss of ground
- Shorts to ground

10 Safing logic

10.1 Safing logic overview

The integrated safing logic uses data from on-board and remote locations by decoding the various SPI communications between the interfaces and the main microcontroller. The safing logic has several programmable features enabling its ability to decode SPI transmissions and can process data from up to 4 sensors. The operating mode involves simple symmetrical data threshold comparisons, with the use of symmetrical or asymmetrical counters. A high level diagram is shown in the figure below. Please note that this top-level diagram is simplified, and references to more detailed flowcharts to show a) message decoding, b) valid data limits, c) effects of the 'combine' function, d) comparison to thresholds and arming, and e) the setting of the 'compare complete bit. Two independent arming outputs, ARM1INT and ARM2INT, are also mapped internally to any of the integrated squib drivers.

Figure 39. Top level safing engine flow chart



10.2 SPI sensor data decoding

Sensor data is regularly communicated with the main microcontroller through multiple SPI messages. Since not all communications between sensors and the microcontroller contain data, it is important for the decoder to properly sort the communications and extract only the targeted data. The solution involves defining specific masking functions, contained within independent safing records, programmed by the user. The following figures detail the SPI message decoding methodology and the ensuing comparisons of valid sensor data to the programmed thresholds.

Figure 40. Safing engine - 16-bit message decoding flow chart

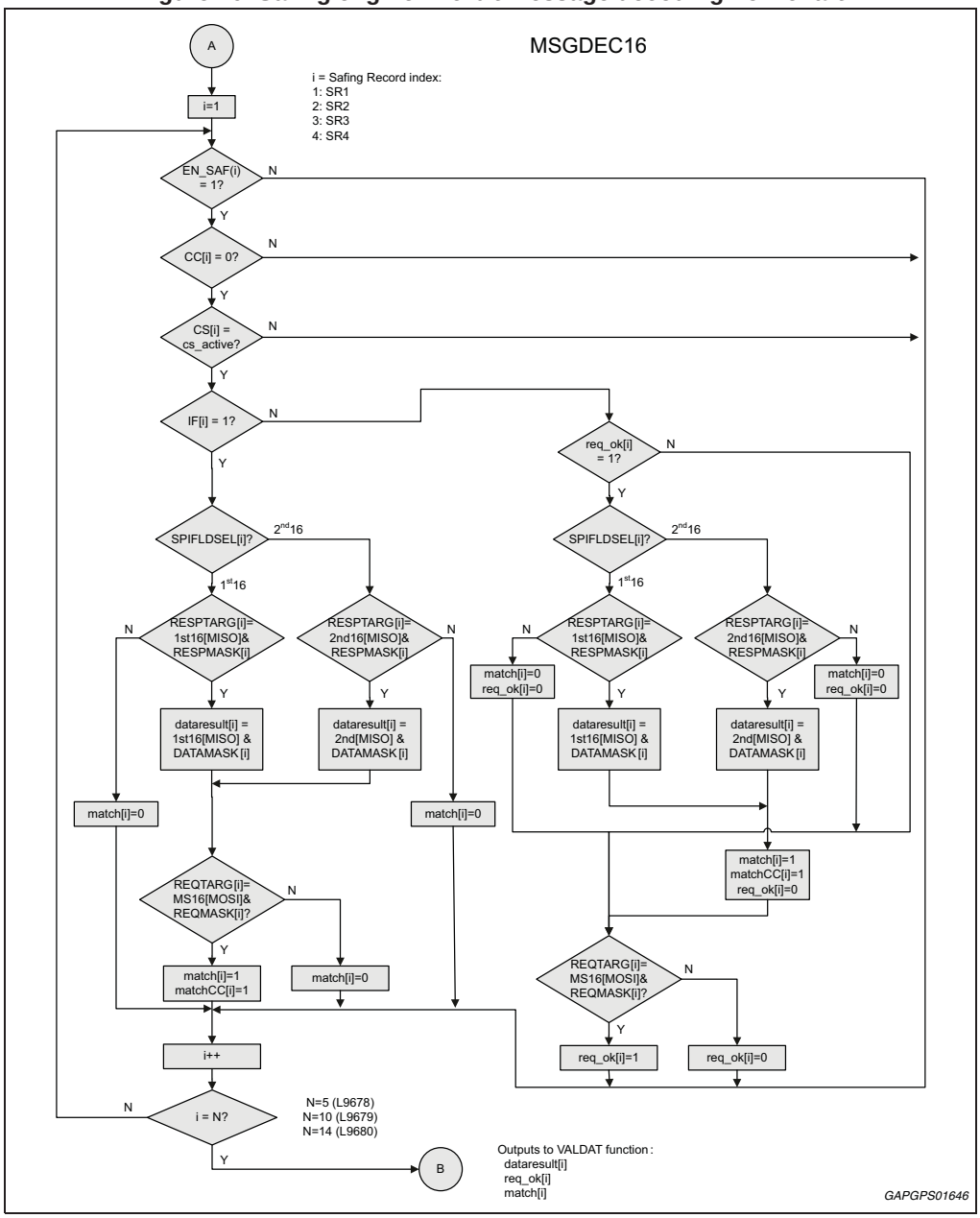


Figure 41. Safing engine - 32-bit message decoding flow chart

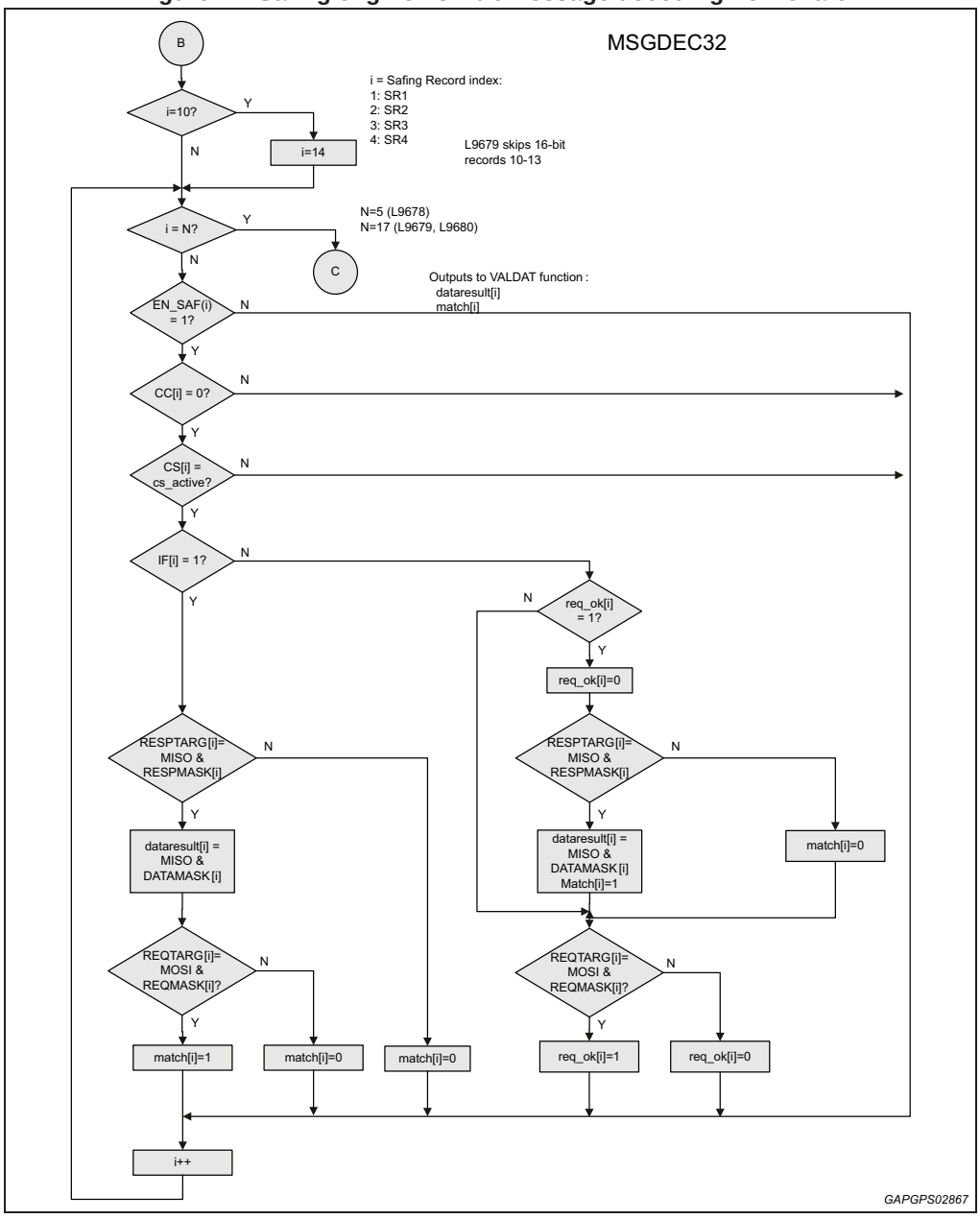


Figure 42. Safing engine - validate data flow chart

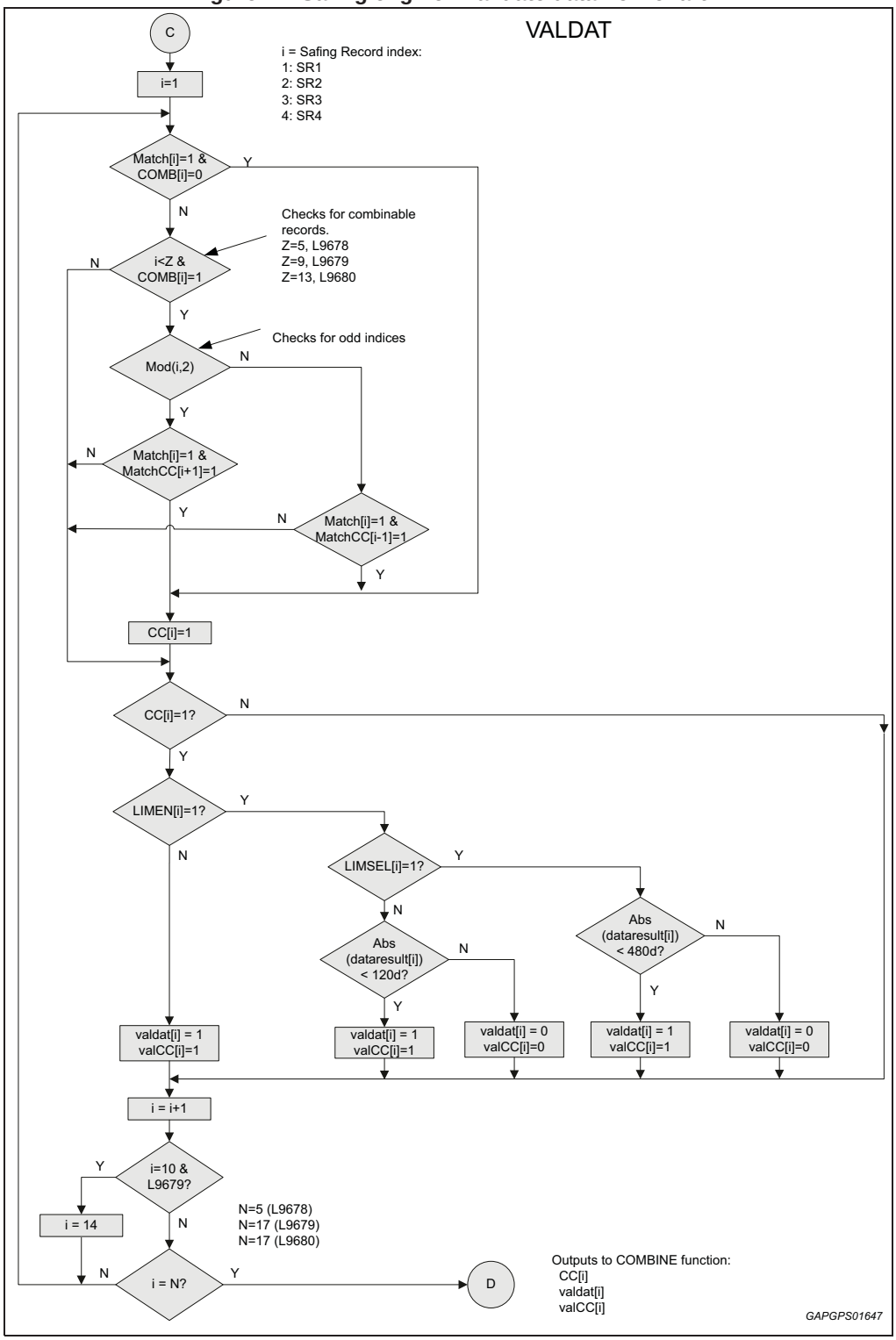


Figure 43. Safing engine - combine function flow chart

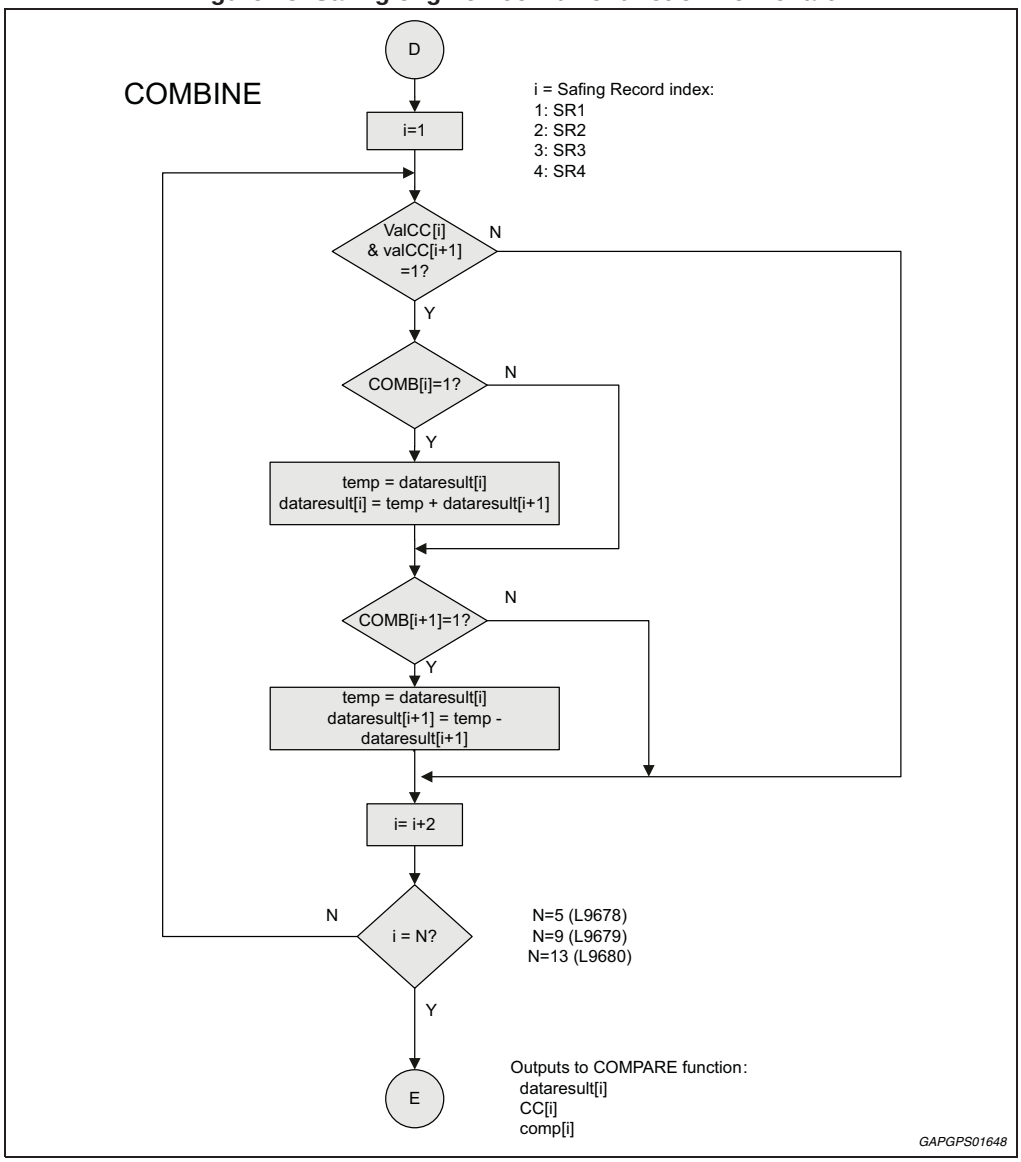


Figure 44. Safing engine threshold comparison

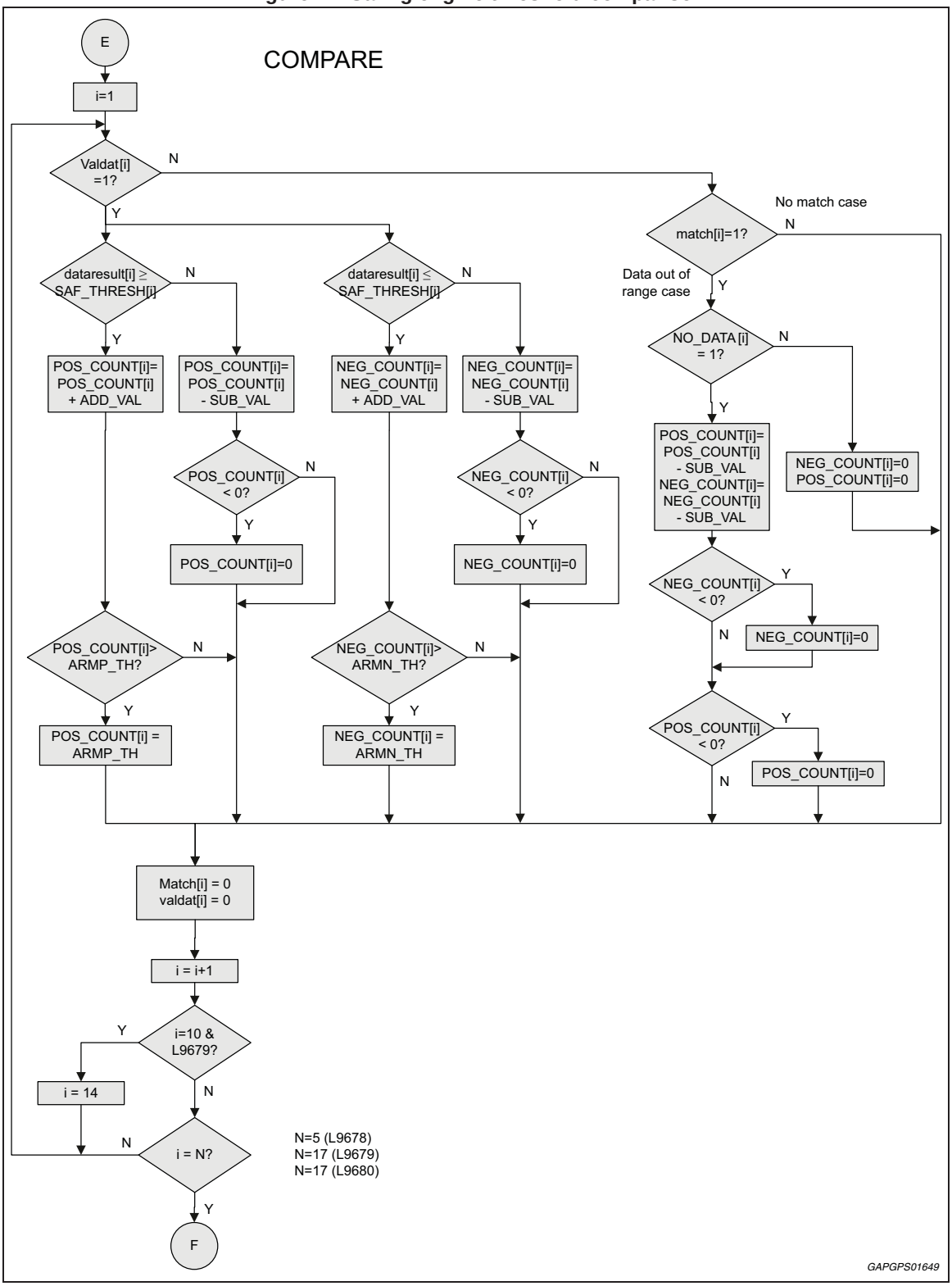
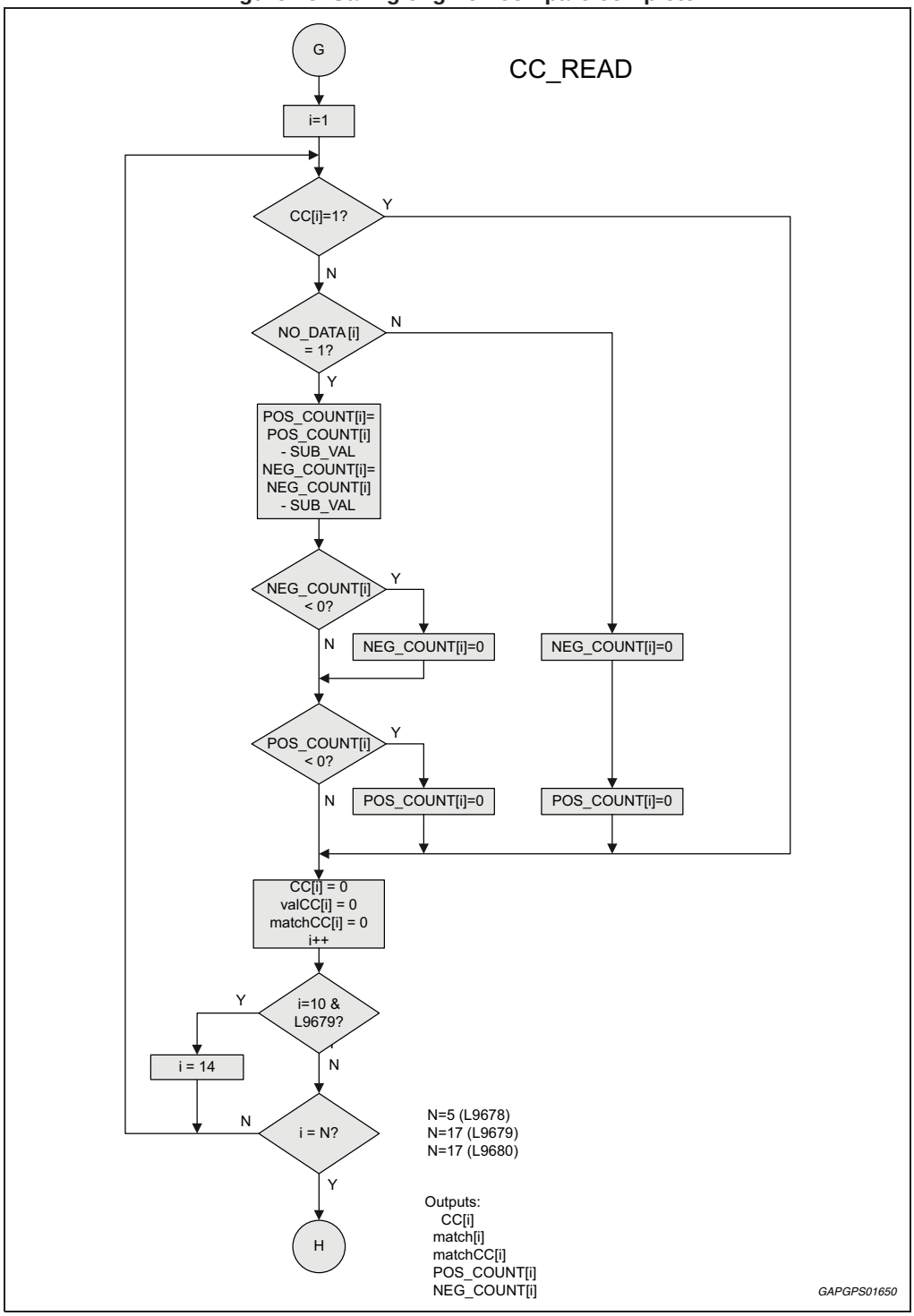


Figure 45. Safing engine - compare complete



Each safing record has SPI accessible registers defined in the SPI command tables and summarized below:

- Request Mask and Request Target - to understand what sensor the microcontroller is addressing
- Response Mask and Response Target - to identify the sensor response
  - Data Mask - to extract relevant sensor data from the response. Sensor data is extracted as a bit-wise AND result of the SAF_DATA_MASKx and monitored SPI_MISO data
  - The extracted data is then right-justified into a 16-bit register for 16-bit safing records, respectively, prior to further processing steps which assume data is signed - two-s complement represented
- Safing Threshold - specific value that sets the comparator limit for successful arming
- Control:
  - IF, In Frame - to indicate serial data response is "in frame". There are two types of potential serial data responses, "in-frame" and "out of frame"
  - CS - to align safing record with a specific SPI CS. The device contains 2 SPI CS inputs for the safing function (SAF_CS0 and SAF_CS1)
  - ARM - there are two internal arming signals, each active record is assigned or mapped to any arming signal. Several safing records can be mapped to a single arming output
  - Dwell - Once an arming condition is detected, the safing record remains armed for the specified dwell time
  - Comb (Combined Data) - specific solution for dual axis high-g sensors specifically oriented off-axis
  - Lim En (Limit Enable) - to enable PSI5 out-of-range control
  - Lim Sel (Limit Select) - to select PSI5 out-of-range thresholds between 8-bit and 10-bit protocol
  - SPIFLDSEL (Spi Field Select) â€“ to determine which 16-bit field in long SPI messages (>31 bit) to use for response on MISO of SPI monitor. If the SPIFLDSEL bit is set to 0 the message bits from 0 (first bit received) to 15 are processed, while if set to 1 the message bits from 16 to 31 are processed. SPIFLDSEL bit will not help L9678 device to work with sensor that places data across this boundary or has response and data in separate 'fields'.
    In case of message less than 32-bit, always the first 16bits received will be processed regardless of the SPIFLDSEL value.

If input packet matches multiple safing records, the safing engine should process all of them and treat them independently.

Safing record can only be evaluated on the first matching input packet. Any further data packet matches are ignored (i.e. once CC is set, record can't be processed until is cleared).

The En (Record Enable) bit for any record is programmable as on or off at any time and will enable/disable the record itself upon the following sensor sampling period.

All CC bits are available in one register (SAF_CC) for access in one single SPI read.

Safing Engine must not process sensor data in any state but Safing state (refer to *Figure 9*).

All safing records are cleared on SSM RESET.

Comb (Combined Data) bit allows combining X and Y for off-axis oriented sensors. In this case, it is typical for such orientations to add or subtract the sensor response to translate the sensor signal to an on-axis response. Only couples of 16-bit long records have this feature (i.e. 1&2, 3&4).

Records are added and subtracted and results compare against two thresholds. Safing engine will process data as follows:

- Use record (n) and record (n+1), where n = 1, 3.
- The matching inputs used for math combinations are processed only after both are captured.
- The sum of the two matching inputs will be compared to the threshold of record (n).
- The difference of the two records will be compared to the threshold of record (n+1).
- If the Comb feature was enabled on only one of the two records in a couple, math would be performed only on it as shown in *Figure 43*.

Example:

Table 10. Records results compare against two threshold

	Combine Bit	Data	Resulting Value	Record Threshold (assume ARMP)	ARMing Result
Record 1	0	12	12	48	0
Record 2	0	50	50	48	1
Record 3	0	12	12	48	0
Record 4	1	50	50 – 12 = 38	48	0
Record 1	1	12	12 + 50 = 62	48	1
Record 2	0	50	50	48	1
Record 3	1	12	12 + 50 = 62	48	1
Record 4	1	50	50 – 12 = 38	48	0

In this example the ARM and dwell assignments for record1 only would be asserted.

All items in the safing records, except En(Record Enable) bit, can be configured only in Diag state (refer to *Figure 9*). Additionally, the global bit to select internal or external safing engine is set in Diag state.

10.3 In-frame and out-of-frame responses

Some sensors will communicate data within the current communication frame while others will send data on the next communication frame. Sometimes this is sensor specific and sometimes this is due to the amount of data to be transmitted. A simplified diagram shows the basic communication differences of in and out of frame responses.

Figure 46. In-frame example

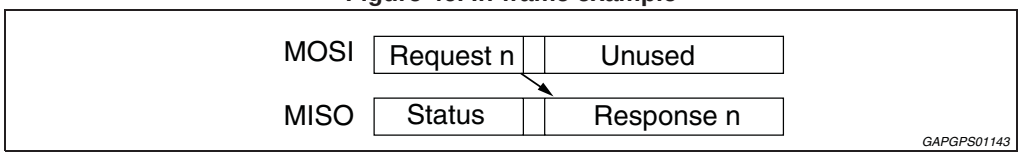
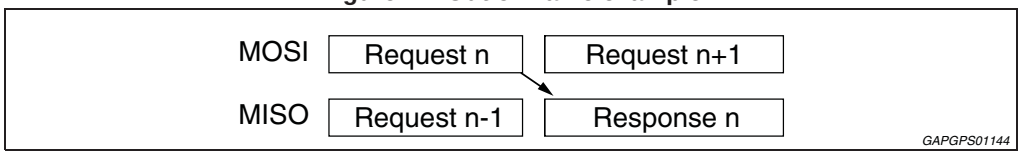


Figure 47. Out of frame example



Synchronization between clock domains relies upon inter-frame gap.

10.4 Safing state machine operation

State machine operation is disabled when the safing state machine reset signal is active as described in the power supply diagnostics and controls section of this document. The outputs of the state machine are ARM1INT and ARM2INT. As previously stated, there is a maximum of 4 safing records available to the state machine. Inputs to the safety state machine are programmed safing records and sensor data. The configuration of the state machine is common to all sensors.

10.4.1 Simple threshold comparison operation

In this mode, sensor data received through the sensor SPI interface and validated by the safing record is passed to the safing algorithm. The simple threshold comparison algorithm compares the received data to two thresholds, SAF_TH (positive threshold) and (-SAF_TH) (negative threshold). If the sensor data is greater than SAF_TH or is less than (-SAF_TH) then and event is flagged and the event counter is incremented based on the programmed value of ADD_VAL. If sensor data does not trigger the SAF_TH comparators, the counter is decremented by SUB_VAL. SUB_VAL is programmed by the user and can be same or different than ADD_VAL. This feature allows for an asymmetrical counter function making the system either more or less sensitive to sensor data. Since sensor data can indicate a positive or negative event, the algorithm maintains separate event counters, POS_COUNT and NEG_COUNT. The ADD_VAL and SUB_VAL programmed values are the same for all safing sources.

On each sensor sample, the event counters, both POS_COUNT and NEG_COUNT, are updated. Each event counter is then compared with a corresponding arming threshold. In this case, POS_COUNT value is compared to ARMP_TH and NEG_COUNT to ARMN_TH. ARMP_TH and ARMN_TH are programmable thresholds set by the user. The compared result will set ARMP and ARMN to either "1" or "0" depending on the comparison status. If

ARMP_TH or ARMN_TH are set to 0, the arming will be activated immediately entering in safing state.

POS_COUNT and NEG_COUNT are not updated if microcontroller stops reading SAF_CC bits (this must be avoided otherwise ARMING set and reset will not be possible).

By way of the assignment of the ADD_VAL, SUB_VAL, ARMP_TH and ARMN_TH settings, the safing engine can be configured to assert arming for either a simple accumulation of COUNTs in a non-consecutive manner, or it could be set to require some number of consecutive samples.

10.5 Safing engine output logic (ARMxINT)

SPI messages are monitored and mapped to specific safing records. Each safing record is configured with its own threshold, dwell time and the appropriate ARMxINT internal signal to activate if safing criteria are met.

Any enabled safing record can be programmed to an arming signal. All safing records arming status is logically "OR'd" to its programmed arming signal. For example, if safing records 1, 2, 4 are programmed to ARMINT1 and the records are enabled, any of the records can set the ARMINT1 signal. Configuration of safing record mapping to ARMxINT signals is specified in the SAF_CONTROL_x register (refer to *Safing control registers (SAF_CONTROL_x) on page 106*).

While in Diag state, L9678 allows diagnostics of the squib driver HS and LS FETs, ARM pin, VSF output and firing timers. The ARM and VSF output tests are mutually exclusive.

For safety purposes, the safing logic circuitry is physically separated from the circuitry that contains the deployment logic.

Figure 48. Safing Engine Arming flow diagram

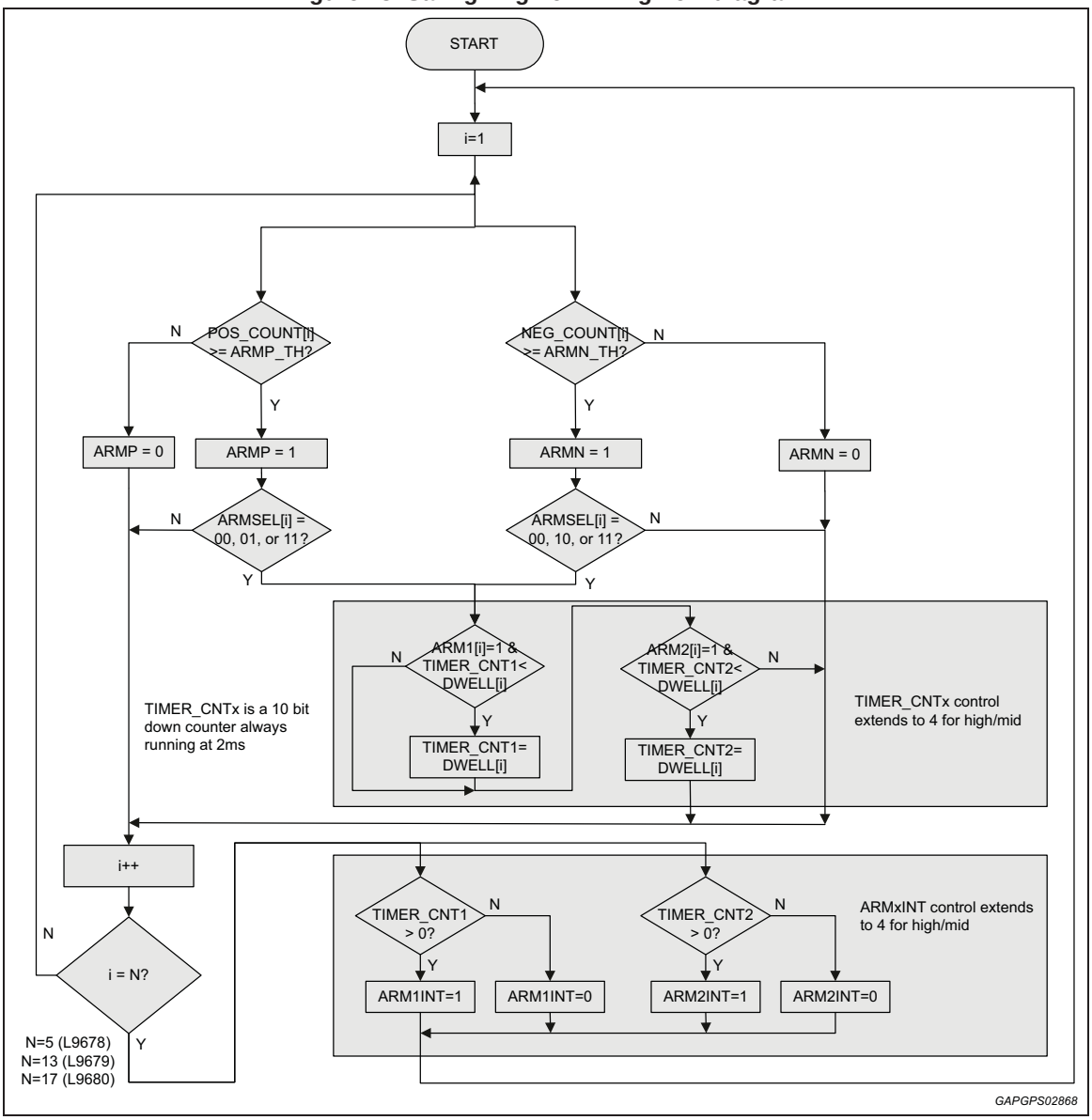
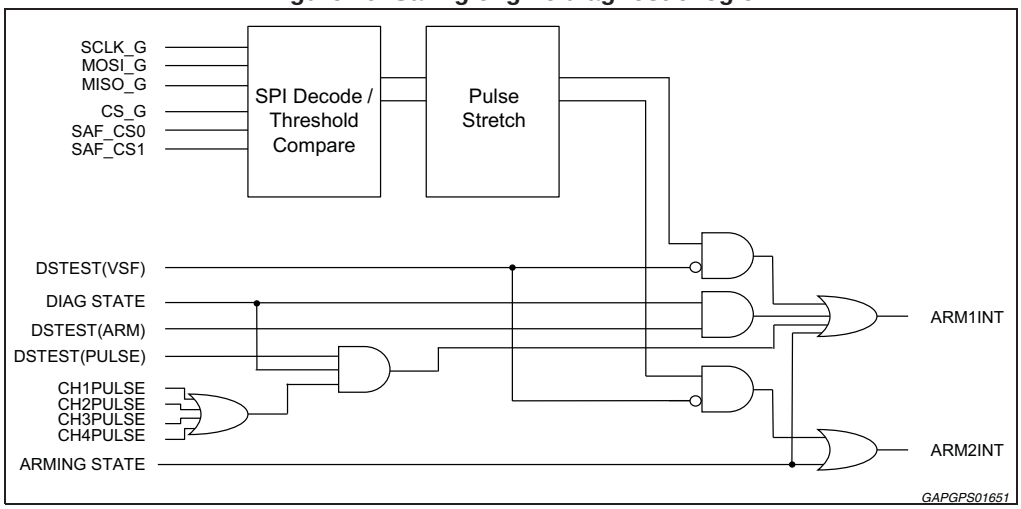


Figure 49. Safing engine diagnostic logic

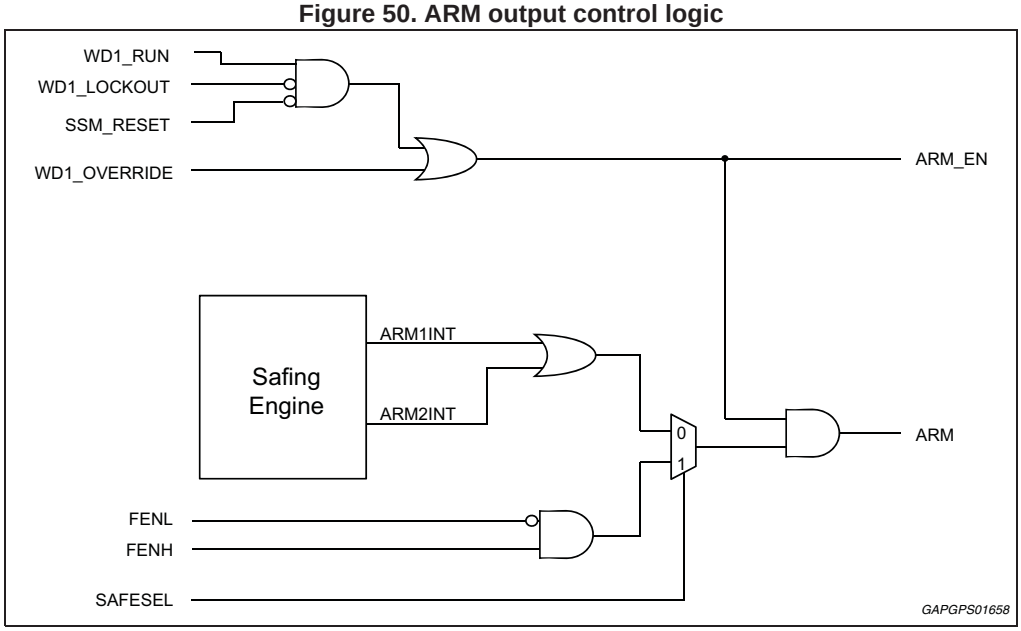


A configurable mask for each internal ARMxINT signal is available for all of the integrated deployment loops (refer to *ARMx assignment registers (LOOP_MATRIX_ARMx) on page 97*). The un-masked ARMxINT signal for each loop will enable the respective loop drivers (refer to *Figure 21*).

Activation of VSF (regulation rail for High Side Safing FET) occurs upon ARMxINT or FENH/FENL, depending on SPI configuration (refer to *Figure 17*). Actual High Side Safing FET activation still requires microcontroller signal.

L9678 is able to provide arming signals to external deployment loops by means of the discrete output ARM pin. The ARM pin can either output an arming signal generated by the integrated safing engine or an arming signal made by the combination of FENH and FENL input signals, coming from external safing logic.

Figure 50. ARM output control logic



10.6 Arming pulse stretch

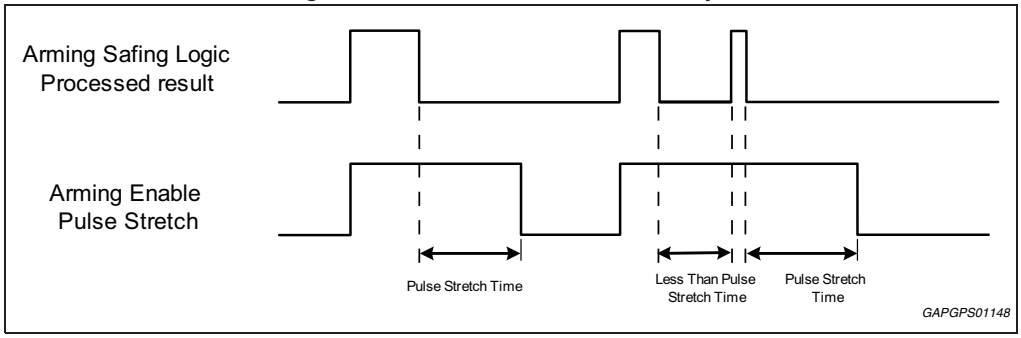
Upon a valid command processed by the safing logic, the Dwell bits to stretch the arming time assertion (dwell time) apply to each safing record and is used to help safe the deployment sequence to avoid undesired behaviour.

Once dwell time has started, it will continue, regardless of the En (Record Enable) bit. Dwell will be truncated in case of SSM reset. Dwell values in the safing records are transferred to the ARM signal. A dedicated counter is designed for ARM output pin. If different dwell values are assigned to ARM, the longer value is used. Dwell times can only be extended, not reduced. If the remaining dwell time is less than the new dwell extension setting, the new setting will be loaded into the dwell counter.

Dwell times are user programmable.

The behavior of the pulse stretch timer is shown in *Figure 51*.

Figure 51. Pulse stretch timer example



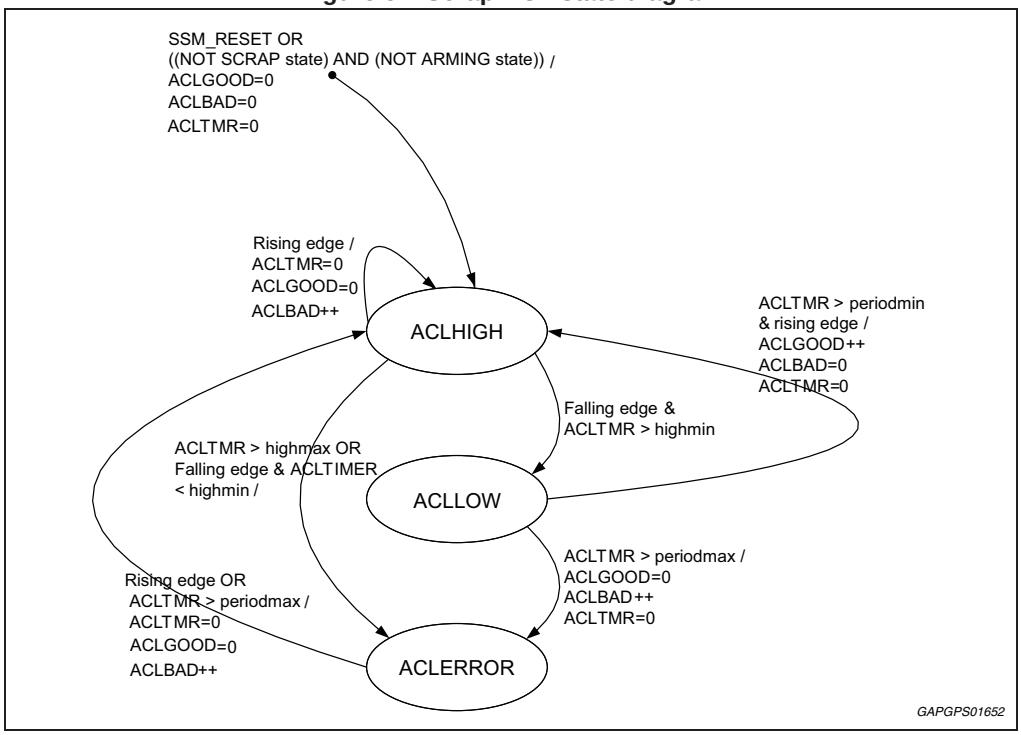
10.7 Additional communication line

The ACL pin is the Additional Communication Line input that provides a means of safely activating the arming outputs (ARM and VSF) for disposal of restraints devices at the end of vehicle life.

A valid ACL detection (as described below) allows L9678 to transition from Scrap state to Arming state. To remain in Arming state L9678 must receive the correct ACL signal; this must occur before the scrap time-out timer expires (T_{disEOL}).

While the System Operating State Machine is in Arming state, the arming outputs are asserted (ARM=1, VSF on). If the ACL is not correctly received before the time-out expires, the System Operating State Machine reverts back to the Scrap state, and the arming outputs are deactivated.

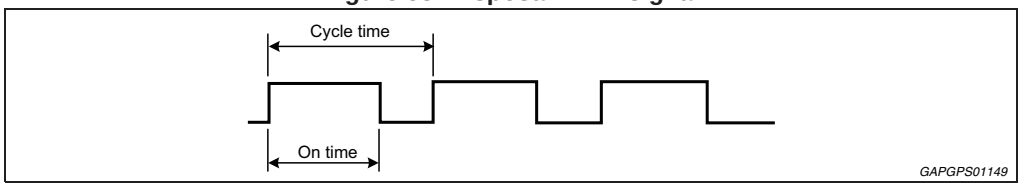
Figure 52. Scrap ACL state diagram



A specific waveform needs to be present on this input in order to instruct L9678 to arm all deployment loops. L9678 is designed to support the Additional Communication Line (ACL) aspect of the ISO-26021 standard, which requires an independent hardwired signal (ACL) to implement the scrapping feature. The disposal signal may come from either the vehicle's service connector, or the systems main microcontroller, depending on the end customer's requirements.

The arming function monitors the disposal PWM input (ACL pin) for a command to arm all loops for vehicle end-of-life airbag disposal. The disposal signal characteristic is shown in *Figure 53*. To remain in Arming state, at least three cycles of the ACL signal must be qualified. For the device to qualify the periodic ACL signal, the period and duty cycle are checked. Two consecutive cycles of invalid disposal signal are to be received to disqualify the ACL signal.

Figure 53. Disposal PWM signal



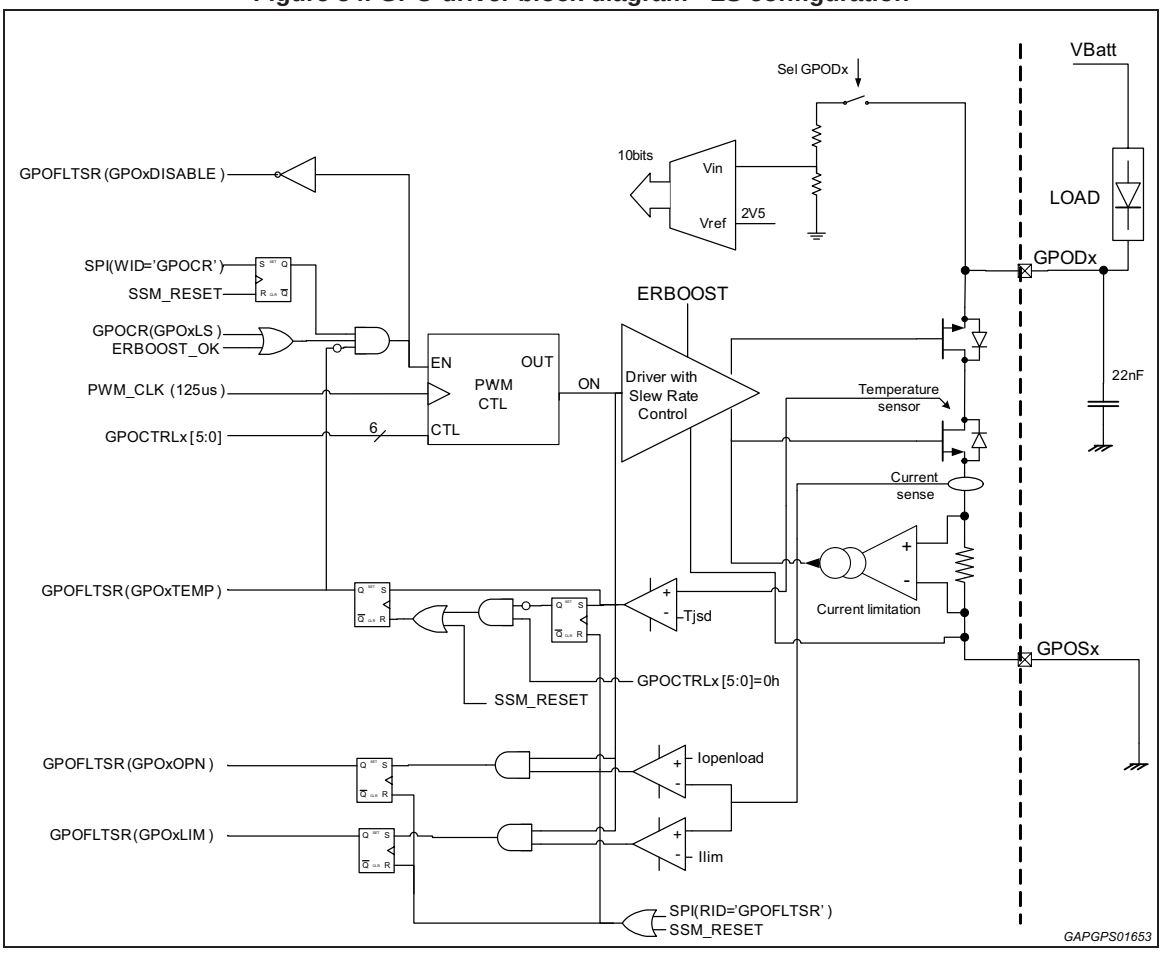
The disposal PWM signal cycle time and on time parameters can be found in the electrical parameters tables.

11 General purpose output (GPO) drivers

The L9678 contains two GPO drivers configurable either as high-side or low-side modes, controlled in ON-OFF mode or in PWM mode setting the desired duty cycle value through the GPO Control Register (GPOCTRLx).

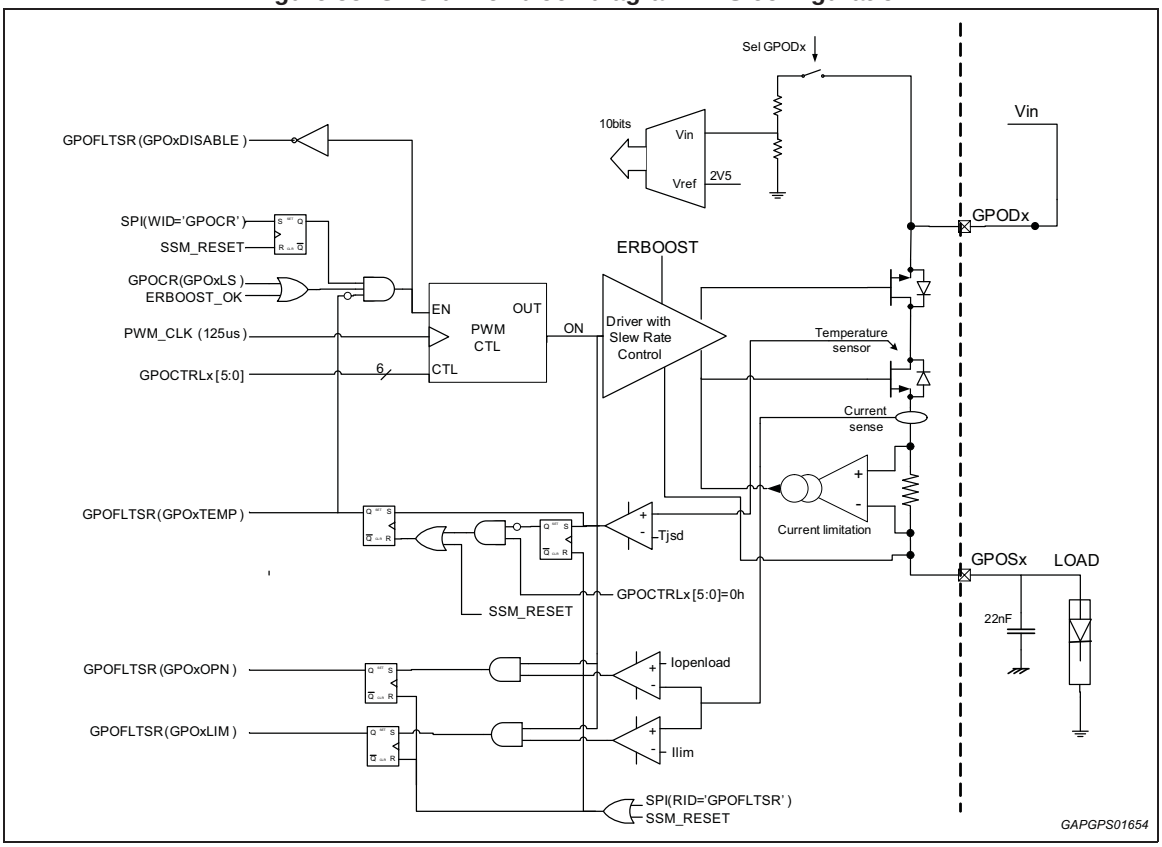
For low side driver configuration, the GPODx pin is the equivalent drain connection of the internal MOSFET and it is the current sink for the output driver. The GPOSx pin is the source connection of the GPO driver and is externally connected to ground.

Figure 54. GPO driver block diagram - LS configuration



For high side driver configuration, the GPODx pin will be connected to battery and GPOSx pin will be connected to the load high side.

Figure 55. GPO driver block diagram - HS configuration



The drivers have to be configured in one of the two modes through the GPO Configuration Register (GPOCR) register before being activated. This hardware configuration is only allowed during the Init and Diag states.

When configured as high-side, the drivers need ER Boost voltage to be above the VERBST_OK threshold to be enabled.

The default state of both drivers is off. The drivers can be independently activated via SPI control bits on GPO Control Register (GPOCTRLx). In addition, a set point on the GPOCTRLx will control the output drivers in PWM with a 125Hz frequency. If PWM control is desired, user should set the needed set point in the GPOxPWM bits of the GPOCTRLx while activating the interface. When all bits are set to '0', the GPOx output will be disabled.

PWM control is based on a 125 Hz frequency. 6 bits of GPOCTRLx are reserved to this mode, in order to control the drivers with 64 total levels from a 0% to a full 100% duty cycle. When both GPO channels are used in PWM Mode at the same frequency they are synchronized to provide parallel configuration capability.

PWM control is implemented through a careful slew rate control to mitigate EMC emissions while operating the interface. The driver output structure is designed to stand -1V on its terminals and a +1V reverse voltage across source and drain.

The GPO driver is protected against short circuits and thermal overload conditions. The output driver contains diagnostics available in the GPO Fault Status Register (GPOFLTSR). All faults except for thermal overload will be latched until the GPOFLTSR register is read.

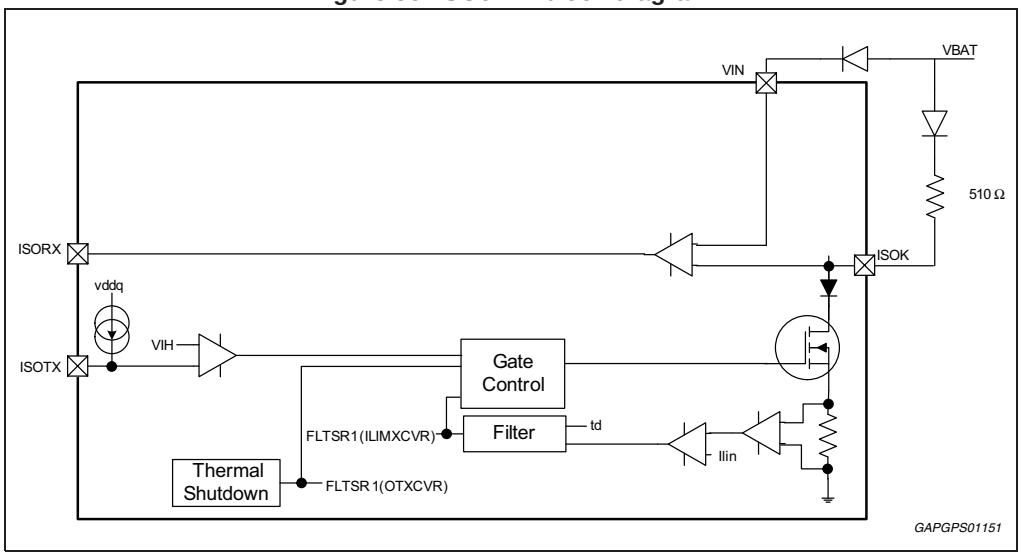
Thermal overload faults will remain active after reading the GPOFLTSR register should the temperature remain above the thermal fault condition. For current limit faults, the output driver will operate in a linear mode (ILIM) until a thermal fault condition is detected.

The device offers also an open load diagnostics while in ON state. The diagnostics is run comparing the current through the output stage with a reference threshold $I_{OpenLoad}$: should the output current be lower than the threshold, the open detection flag is asserted.

12 ISO9141 transceiver

A block diagram of the function is shown below. Data transmitted by the main microcontroller is sent via the ISOTX pin and data is received via the ISORX pin. The bus output is ISOK.

Figure 56. ISO9141 block diagram



When the ISOTX pin is asserted, logic high, the ISOK output will be disabled (pulled high by an external resistor). When the ISOTX pin is deasserted, logic low, the ISOK output will be enabled (pulled low by the internal driver). This input pin contains an internal pull-up to command the output to the disabled state in the event of an open circuit condition.

The ISORX pin has a push-pull output stage referenced to VDDQ voltage. This output is asserted high when the voltage on the ISOK pin is above the ISOK input receiver threshold, VBATMON, as defined in the electrical tables. This output is deasserted low when the voltage on the ISOK pin is below the ISOK input receiver threshold with hysteresis.

ISOK output is a low side driver compatible with ISO9141 physical layer.

The output stage is protected against short circuits and diagnostics provide feedback for current limit and thermal shutdown. While in current limit, the output stage will continue to function until thermal limit is reached. Should thermal limit occur, the output stage will shut down until the temperature decreases below the limit threshold with hysteresis. The fault status is reported in the ISO9141 Fault Status Register (ISOFLTSR).

13 System voltage diagnostics

L9678 has an integrated dedicated circuitry to provide diagnostic feedback and processing of several inputs. These inputs are addressed with an internal analog multiplexer and made available through the SPI digital interface with the Diagnostic Data commands. In order to avoid saturation of high voltage internal signals, an internal voltage divider is used. The diagnostics circuitry is activated by four SPI Diagnostics Control commands (DIAGCTRLx); each of them can address all the available nodes to be monitored, except for what mentioned in *Table 11: Diagnostics control register (DIAGCTRLx) on page 159*.

DIAGCTRLx SPI command bit fields are structured in the following way:

DIAGCTRL_A (ADDRESS HEX 3A)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					x	x	x	x	x	x	x	x	x	ADCREQ_A[6:0]						
MISO	NEWDATA_A	0	0	ADCREQ_A[6:0]							ADCRES_A[9:0]									

DIAGCTRL_B (ADDRESS HEX 3B)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					x	x	x	x	x	x	x	x	x	ADCREQ_B [6:0]						
MISO	NEWDATA_B	0	0	ADCREQ_B [6:0]							ADCRES_B [9:0]									

DIAGCTRL_C (ADDRESS HEX 3C)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					x	x	x	x	x	x	x	x	x	ADCREQ_C [6:0]						
MISO	NEWDATA_C	0	0	ADCREQ_C [6:0]							ADCRES_C [9:0]									

DIAGCTRL_D (ADDRESS HEX 3D)

	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MOSI					x	x	x	x	x	x	x	x	x	ADCREQ_D [6:0]						
MISO	NEWDATA_D	0	0	ADCREQ_D [6:0]							ADCRES_D [9:0]									

ADCREQ[A-D] bit fields, used to address the different measurements offered, are listed in *Table 11: Diagnostics control register (DIAGCTRLx) on page 159* for reference.

L9678 diagnostics are structured to take four automatic conversions at a time. In order to get four measurements, four different SPI commands have to be sent (DIAGCTRL_A, DIAGCTRL_B, DIAGCTRL_C and DIAGCTRL_D), in no particular order.

In case the voltage to be measured is not immediately available, the desired inputs for conversion have to be programmed by SPI in advance, to allow them to attain a stable voltage value. This case applies to the squib resistance measurement and diagnostics (refer to *Loop diagnostics control and results registers*) and to the switch sensor measurement (refer to *Section 9: DC sensor interface*).

CONVRDY_0 bit in GSW is equal to (NEWDATA_A or NEWDATA_B), while CONVRDY_1 bit in GSW corresponds to (NEWDATA_C or NEWDATA_D).

Each NEWDATAx flag is asserted when conversion is finished and cleared when result is read out. However result is cleared only when new result for that register is available.

When a new request is received it is queued if other conversions are ongoing. The conversions are executed in the same order as their request arrived. The queue is 4 measures long so it's possible to send all 4 requests at the same time and then wait for the results. If a DIAGCTLRx command is received twice, the second conversion request will overwrite the previous one.

Requests are sent to the L9678 IC via the ADC measurement Registers (ADCREQx) as shown in *Table 11: Diagnostics control register (DIAGCTRLx) on page 159*. All diagnostics results are available on the ADCRESx registers, when addressed by the related ADCREQx register (e.g. data requested by ADCREQA would be written to ADCRESA).

Table 11. Diagnostics control register (DIAGCTRLx)

ADC Request (ADCREQx)									Voltage measurement selection	ADC Results (ADCRESx)
Bit [6:0]								Hex		Bit [9:0]
0	0	0	0	0	0	0	0	$00	Unused	
0	0	0	0	0	0	1	1	$01	ADC Test Pattern 1	Ground reference
0	0	0	0	0	1	0	2	$02	ADC Test Pattern 2	Full scale reference
0	0	0	0	0	1	1	3	$03	DC Sensor ch. selected, Voltage	DCSV_selected
0	0	0	0	1	0	0	4	$04	DC Sensor ch. selected, Current	DCSI_selected
0	0	0	0	1	0	1	5	$05	DC Sensor ch. selected, Resistance(1)	DCSV and DCSI selected
0	0	0	0	1	1	0	6	$06	Squib measurement loop selected	Voutx
0	0	0	0	1	1	1	7	$07	Bandgap reference Voltage	VBGR
0	0	0	1	0	0	0	8	$08	Bandgap reference monitor Voltage	VBGM
0	0	0	1	0	0	1	9	$09	Unused	
0	0	0	1	0	1	0	10	$0A	Temperature Measurement	TEMP
0	0	0	1	0	1	1	11	$0B	DC Sensor ch 0, Voltage	DCSV_0
0	0	0	1	1	0	0	12	$0C	DC Sensor ch 1, Voltage	DCSV_1
0	0	0	1	1	0	1	13	$0D	DC Sensor ch 2, Voltage	DCSV_2
0	0	0	1	1	1	0	14	$0E	DC Sensor ch 3, Voltage	DCSV_3
0	0	0	1	1	1	1	15	$0F	Unused	
0	0	1	0	0	0	0	16	$10	Unused	
0	0	1	0	0	0	1	17	$11	Unused	
0	0	1	0	0	1	0	18	$12	Unused	

Table 11. Diagnostics control register (DIAGCTRLx) (continued)

ADC Request (ADCREQx)									Voltage measurement selection	ADC Results (ADCRESx)
Bit [6:0]								Hex		Bit [9:0]
0	0	1	0	0	1	1	19	$13	Unused	
0	0	1	0	1	0	0	20	$14	Unused	
0	0	1	0	1	0	1	21	$15	Unused	
0	0	1	0	1	1	0	22	$16	Unused	
0	0	1	0	1	1	1	23	$17	Unused	
0	0	1	1	0	0	0	24	$18	Unused	
0	0	1	1	0	0	1	25	$19	Unused	
0	0	1	1	0	1	0	26	$1A	Unused	
0	0	1	1	0	1	1	27	$1B	Unused	
0	0	1	1	1	0	0	28	$1C	Unused	
0	0	1	1	1	0	1	29	$1D	Unused	
0	0	1	1	1	1	0	30	$1E	Unused	
0	0	1	1	1	1	1	31	$1F	Unused	
0	1	0	0	0	0	0	32	$20	Battery monitor Voltage	VBATMON
0	1	0	0	0	0	1	33	$21	Device battery Voltage	VIN
0	1	0	0	0	1	0	34	$22	Analog internal supply Voltage	VINT3V3
0	1	0	0	0	1	1	35	$23	Digital internal supply Voltage	CVDD
0	1	0	0	1	0	0	36	$24	ERBOOST voltage	ERBOOST
0	1	0	0	1	0	1	37	$25	Unused	
0	1	0	0	1	1	0	38	$26	VER Voltage	VER
0	1	0	0	1	1	1	39	$27	VSUP Voltage	VSUP
0	1	0	1	0	0	0	40	$28	VDDQ Voltage	VDDQ
0	1	0	1	0	0	1	41	$29	WAKEUP Voltage	WAKEUP
0	1	0	1	0	1	0	42	$2A	VSF Regulator Voltage	VSF
0	1	0	1	0	1	1	43	$2B	WDT/TM Voltage	WDTDIS
0	1	0	1	1	0	0	44	$2C	GPO Driver 0 drain Voltage	GPOD0
0	1	0	1	1	0	1	45	$2D	GPO Driver 0 source Voltage	GPOS0
0	1	0	1	1	1	0	46	$2E	GPO Driver 1 drain Voltage	GPOD1
0	1	0	1	1	1	1	47	$2F	GPO Driver 1 source Voltage	GPOS1
0	1	1	0	0	0	0	48	$30	Unused	
0	1	1	0	0	0	1	49	$31	Unused	
0	1	1	0	0	1	0	50	$32	Remote sensor Interface Voltages ch. 0	RSU0
0	1	1	0	0	1	1	51	$33	Remote sensor Interface Voltages ch. 1	RSU1

Table 11. Diagnostics control register (DIAGCTRLx) (continued)

ADC Request (ADCREQx) Bit [6:0]								Hex	Voltage measurement selection	ADC Results (ADCRESx) Bit [9:0]
0	1	1	0	1	0	0	52	$34	Unused	
0	1	1	0	1	0	1	53	$35	Unused	
0	1	1	0	1	1	0	54	$36	SSxy Voltage ch. 0	SS01
0	1	1	0	1	1	1	55	$37	SSxy Voltage ch. 1	SS01
0	1	1	1	0	0	0	56	$38	SSxy Voltage ch. 2	SS23
0	1	1	1	0	0	1	57	$39	SSxy Voltage ch. 3	SS23
0	1	1	1	0	1	0	58	$3A	Unused	
0	1	1	1	0	1	1	59	$3B	Unused	
0	1	1	1	1	0	0	60	$3C	Unused	
0	1	1	1	1	0	1	61	$3D	Unused	
0	1	1	1	1	1	0	61	$3E	Unused	
0	1	1	1	1	1	1	63	$3F	Unused	
1	0	0	0	0	0	0	64	$40	Unused	
1	0	0	0	0	0	1	65	$41	Unused	
1	0	0	0	0	1	0	66	$42	VRESDIAG	VRESDIAG
1	0	0	0	0	1	1	67	$43	VDD5	VDD5
1	0	0	0	1	0	0	68	$44	VDD3V3	VDD3V3
1	0	0	0	1	0	1	69	$45	ISOK output voltage	ISOK
1	0	0	0	1	1	0	70	$46	SF0 voltage	SF0
1	0	0	0	1	1	1	71	$47	SF1 voltage	SF1
1	0	0	1	0	0	0	72	$48	SF2 voltage	SF2
1	0	0	1	0	0	1	73	$49	SF3 voltage	SF3

1. The DC sensor resistance measurement can only be addressed through DIAGCRTL_A command. Results are available through DIAGCTRL_A and DIAGCTRL_B, where ADCRES_A will contain DCSI and ADCRES_B will contain DCSV.

Proper scaling is necessary for various voltage measurements. The divider ratios vary by measurement and are summarized by function in the table below.

Table 12. Diagnostics divider ratios

Measurements	Divider Ratio					
	15:1	10:1	7.125:1	7:1	4:1	1:1
VER	X					
ERBOOST	X					
VSF	X					
SSxy	X					

Table 12. Diagnostics divider ratios (continued)

Measurements	Divider Ratio					
	15:1	10:1	7.125:1	7:1	4:1	1:1
SFx	X					
VRESDIAG	X					
GPODx		X				
GPOSx		X				
VIN		X				
VBATMON		X				
WAKEUP		X				
ISOK				X		
VSUP				X		
WDTDIS				X		
RSUx					X	
DCSx			X			
VDDQ					X	
VDD5					X	
VDD3V3					X	
VINT3V3					X	
Bandgap (BGR/BGM)						X
TEMP						X

For measurements other than voltage (current, resistance, temperature etc.) the ranges are specified in the electrical parameters section of the relevant block.

13.1 Analog to digital algorithmic converter

The device hosts an integrated 10 bit Analog to Digital converter, running at a clock frequency of 16MHz. The ADC output is processed by a D to D converter with the following functions:

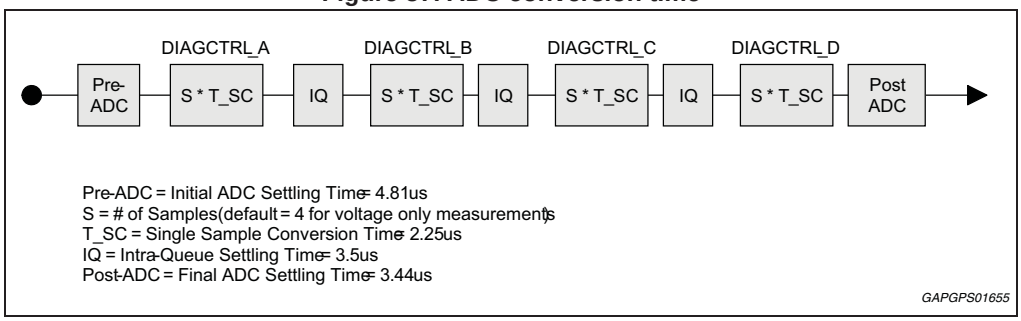
- Use of trimming bits to recover ADC offset and gain errors;
- Digital low-pass filtering;
- Conversion from 12 to 10 bits.

10 bits data are filtered inside the digital section. The number of samples that are filtered vary depending on the chosen conversion. As per *Section 5.1.2: System configuration register (SYS_CFG)*, the number of used samples in converting DC sensor, squib or temperature measurements defaults to 8. The number of samples for all other measurements defaults to 4. The sample number can be configured by accessing the SYS_CFG register. After low pass filter, the residual total error is ±4 LSB. This error figure

applies to the case of a precise reference voltage: the spread of reference voltage causes a proportional error in the conversion output. The reference voltage of the ADC is set to 2.5 V.

The conversion time is comprised of several factors: the number of measurements loaded into the queue, the number of samples taken for any measurement, and the various settling times. An example of conversion time calculation for a full ADC request queue is reported in *Figure 57*. The timings reported in *Figure 57* are nominal ones, min/max values can be obtained by considering the internal oscillator frequency variation reported in the DC characteristics section.

Figure 57. ADC conversion time



14 Temperature sensor

The L9678 provides an internal analog temperature sensor. The sensor is aimed to have a reference for the average junction temperature on silicon surface. The sensor is placed far away from power dissipating stages and squib deployment drivers. The output of the temperature sensor is available via SPI through ADC conversion, as shown in *Table 11*. The formula to calculate temperature from ADC reading is the following one:

$$T(°C) = 180 - \left\{\left(\frac{220}{1.652}\right) \cdot \left[\left(\frac{ADC_{REF\_hi}}{2^{ADC_{RES}}} \cdot DIAGCTRLn(ADCRESn)\right) - 0.739\right]\right\}$$

@ DIAGCTRLn(ADCREQn) = $0A_{hex}$

All parametric requirements for this block can be found in specification tables.

15 Electrical characteristics

Every parameter in this chapter is fulfilled down to $VIN_{GOOD(max)}$.

No device damage is granted to occur down to VIN_{BAD}(min).

GNDA pin is used as ground reference for the voltage measurements performed within the device, unless otherwise stated.

All table or parameter declared "Design Info" are not tested during production testing

15.1 Configuration and control

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD}(max) ≤ VIN ≤ 35 V.

Table 13. Configuration and control DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	V_{NOV}	Normal operating voltage	Design Info Depending on power supply configuration	6	13	18	V
2	V_{JSV}	Jump start voltage	Design Info -40 °C ≤ Ta ≤ 50 °C	18.00	-	26.50	V
3	V_{LDV}	Load dump voltage	Transient Design Info	26.50	-	40	V
4	WU_mon	WAKEUP monitor threshold	-	-	-	1.5	V
5	WU_off	WAKEUP Off threshold	-	2	2.5	3	V
6	WU_on	WAKEUP On threshold	-	4	4.5	5	V
7	WU_{RPD}	WAKEUP pull-down resistor	-	120	300	480	kΩ
8	VB_{GOOD1}	VBATMON input voltage thresholds	SYS_CTL(VBATMON_TH_SEL)=00	5.5	-	6	V
9	VB_{BAD1}		SYS_CTL(VBATMON_TH_SEL)=00	5	-	5.5	V
10	VB_{GOOD2}		SYS_CTL(VBATMON_TH_SEL)=01	6.3	-	6.8	V
11	VB_{BAD2}		SYS_CTL(VBATMON_TH_SEL)=01	5.8	-	6.3	V
12	VB_{GOOD3}		SYS_CTL(VBATMON_TH_SEL)=10	7.5	-	8	V
13	VB_{BAD3}		SYS_CTL(VBATMON_TH_SEL)=10	7	-	7.5	V
14	VB_{GOOD4}		SYS_CTL(VBATMON_TH_SEL)=11	8.3	-	8.8	V
15	VB_{BAD4}		SYS_CTL(VBATMON_TH_SEL)=11	7.8	-	8.3	V

Table 13. Configuration and control DC specifications (continued)

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
16	$I_{LKG\_VBATMON\_OFF}$	VBATMON input leakage	Device OFF	-5		5	µA
17	$I_{LKG\_VBATMON\_ON}$		Device ON Design Info	20	24	30	µA
18	$R_{PD\_VBATMON}$	VBATMON pull-down resistance	Device ON VBATMON < 10V Design Info	125	250	375	kΩ
19	$I_{LKG\_VBATMON\_TOT}$	VBATMON total input leakage	$I_{LKG\_VBATMON\_ON}$ + R_{PD_VBATMO} VBATMON = 18V	35	70	105	µA
20	VIN_{GOOD1}	VIN input voltage thresholds	SYS_CTL(VIN_TH_SEL)=0	5	-	5.5	V
21	VIN_{BAD1}		SYS_CTL(VIN_TH_SEL)=0	4.5	-	5	V
22	VIN_{GOOD2}		SYS_CTL(VIN_TH_SEL)=1	7	-	7.5	V
23	VIN_{BAD2}		SYS_CTL(VIN_TH_SEL)=1	6.5	-	7	V
24	$VIN_{FASTSLOPE\_H}$	VIN Thresholds used to change boost regulator transition time	-	9.3	9.8	10.3	V
25	$VIN_{FASTSLOPE\_L}$		-	9	9.5	10	V
26	$VIN_{FASTSLOPE\_HYS}$		-	0.2	0.3	0.4	V
27	$I_{LKG\_VIN\_OFF}$	VIN input leakage	Device OFF, VIN = 40V	-10	-	10	µA
28	$I_{LKG\_VIN\_ON}$		Device ON, VIN = 12V	-	-	30	mA
29	C_{VIN}	External VIN capacitor	-	1	-	-	-
30	$I_{LKG\_VER\_OFF}$	VER input leakage	Device OFF, VER = 40 V	-5	-	5	µA
31	$I_{LKG\_VER\_ON\_L}$		Device ON ERBOOST > VER	-5	-	5	µA
32	$I_{LKG\_VER\_ON\_H}$		Device ON ERBOOST < VER	-	-	200	µA
33	$V_{WD\_OVERRIDE\_th}$	WDT/TM threshold	-	10	12	14	V
34	V_{WDTDIS_HYST}	WDT/TM hysteresis	-	0.2	0.4	0.5	V
35	I_{PD_WDTDIS}	WDT/TM pull-down Current	V_{WDTDIS} ≤ 5 V	20	45	70	µA
36	I_{LKG_BAT}	Battery line Input Leakage	Total leakage at RT from VIN, VBATMON, ERBSTSW, ERBOOST, BVDD5, VDD5, VDDQ, BVSUP, VSUP VBAT = 12 V Guaranteed by design	-	-	100	µA
37	T_j	Junction temperature	Design Info	-	-	150	°C

Table 14. Configuration and control AC specifications

No	Symbol	Parameter	Condition	Min	Typ	Max	Units
1	$T_{FLT\_VBATMONTH}$	VBATMON thresholds deglitch filter time	-	26	30	34	µs
2	T_{FLT_VINTH}	VIN thresholds deglitch filter time	-	3	3.5	4	µs
3	T_{FLT_WAKEUP}	Wakeup deglitch filter time	-	0.95	1.05	1.15	ms
4	T_{LATCH_WAKEUP}	Wakeup latch time	-	9.7	10.8	11.9	ms
5	t_{don}	Power-up delay time – Wake-up to RESET released	-	-	-	10	ms

Table 15. Open ground detection DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$GNDA_{OPEN}$	GNDA threshold	GNDSUBx=0	100	200	300	mV
2	$GNDD_{OPEN}$	GNDD threshold	GNDSUBx=0	100	200	300	mV
3	$BSTGND_{OPEN}$	BSTGND threshold	GNDSUBx=0	100	200	300	mV
4	I_{PU_BSTGND}	BSTGND pull-up current	-	80	120	160	µA

Table 16. Open ground detection AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$T_{FLT\_GNDREFOPEN}$	GNDA and GNDD Open Deglitch Filter Time	-	7	11	16	µs
2	$T_{FLT\_BSTGNDOPEN}$	BSTGND Latch Filter Time	-	1.9	2.3	2.7	µs

15.2 Internal analog reference

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35 V.

Table 17. Internal analog reference

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	V_{BG1}	Bandgap reference	-	-1%	1.2	+1%	V
2	V_{BG2}	Bandgap monitor	-	-1%	1.2	+1%	V
3	V_{ADC_GROUND}	ADC Ground reference	-	-3%	103	+3%	mV
4	$V_{ADC\_FULLSCALE}$	ADC Full scale reference	-	-1.5%	2.5	+1.5%	V

15.3 Internal regulators

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35 V.

Table 18. Internal regulators DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$V_{OUT\_VINT3V3}$	VINT3V3 output voltage	-	3.14	3.3	3.46	V
2	$V_{OV\_VINT3V3}$	VINT3V3 over voltage	-	3.47	-	3.7	V
3	$V_{UV\_VINT3V3}$	VINT3V3 under voltage	-	2.97	-	3.13	V
4	V_{OUT_VDD}	VDD output voltage	-	3.14	3.3	3.46	V
5	I_{OUT_VDD}	VDD current capability	External Load is not allowed	-	-	50	mA
6	I_{LIM_VDD}	VDD current limit	-	80	-	-	mA
7	V_{OV_VDD}	VDD over voltage	-	3.47	-	3.7	V
8	V_{UV_VDD}	VDD under voltage	-	2.7	-	2.9	V
9	C_{VDD}	VDD output capacitance	Design Info	60	100	140	nF

Table 19. Internal regulators AC specifications

N°	Symbol	Parameter	Condition	Min	Typ.	Max	Unit
1	$T_{FLT\_VINT\_VDD\_OV}$	Internal regulator OV Deglitch filter time	-	7	11	16	µs
2	$T_{FLT\_VINT\_VDD\_UV}$	Internal regulator UV Deglitch filter time	-	7	11	16	V

15.4 Oscillators

All electrical characteristics are valid for the following conditions unless otherwise noted.
-40 °C ≤ Ta ≤ +95 °C, 3.14 ≤ CVDD ≤ 3.46.

Table 20. Oscillators AC specifications

No	Symbol	Parameter	Conditions / Comments	Min	Typ	Max	Unit
1	f_{OSC}	Main oscillator average frequency	-	15.2	16	16.8	MHz
2	f_{MOD_OSC}	Main oscillator modulation frequency	SPI_CLK_CNF(MAIN_SS_DIS=0) Design Info	-	$\frac{f_{OSC}}{128}$	-	MHz
3	I_{MOD_OSC}	Main oscillator modulation index	SPI_CLK_CNF(MAIN_SS_DIS=0)	3	4	5	%
4	f_{AUX}	Aux oscillator average frequency	-	7.125	7.5	7.875	MHz
5	f_{MOD_AUX}	Aux oscillator modulation frequency	SPI_CLK_CNF(AUX_SS_DIS=0) Design Info	-	$\frac{f_{OSC\_AUX}}{128}$	-	MHz

Table 20. Oscillators AC specifications (continued)

No	Symbol	Parameter	Conditions / Comments	Min	Typ	Max	Unit
6	I_{MOD_AUX}	Aux oscillator modulation index	SPI_CLK_CNF(AUX_SS_DIS=0)	3	4	5	%
7	$f_{OSC\_LOW\_TH}$	Main oscillator Low Frequency Detection Threshold	-	-	$\frac{128}{174} \cdot f_{AUX}$	-	MHz

15.5 Watchdog

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ Ta ≤ +95 °C,VIN_{GOOD1}(max) ≤ VIN ≤ 35 V

Table 21. Temporal watchdog timer AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$T_{WDT1\_TIMEOUT}$	Temporal watchdog timeout	-	-	-	2.00	ms
				-	-	16.3	ms
2	T_{WDT1_RST}	Temporal Watchdog Reset Time	-	0.9	-	1.1	ms

15.6 Reset

All electrical characteristics are valid for the following conditions unless otherwise noted:
-40 °C ≤ Ta ≤ +95 °C; VIN_{GOOD1}(max) ≤ VIN ≤ 35 V, VDDx(min) ≤ VDDx ≤ VDDx(max), VDDQ = VDD5 or VDD3V3

Table 22. Reset DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	V_{OH_RESET}	RESET output voltage	I_{LOAD} = -0.5 mA	VDDQ -0.6	-	VDDQ	V
2	V_{OL_RESET}		I_{LOAD} = 2.0 mA	0	-	0.4	V
3	R_{PD_RESET}	RESET pull down resistance	RESET=VDDQ, Device OFF	65	100	135	kΩ

Table 23. Reset AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	T_{RISE_RESET}	Rise Time	80pF load, 20%-80%	-	-	1.00	µs
2	T_{FALL_RESET}	Fall Time	80pF load, 20%-80%	-	-	1.00	µs
3	T_{HOLD_RESET}	Reset Hold Time	-	0.45	0.5	0.55	ms

15.7 SPI interface

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35 V, VDDx(min) ≤ VDDx ≤ VDDx(max)
VDDQ = VDD5 or VDD3V3.

Table 24. SPI DC specifications

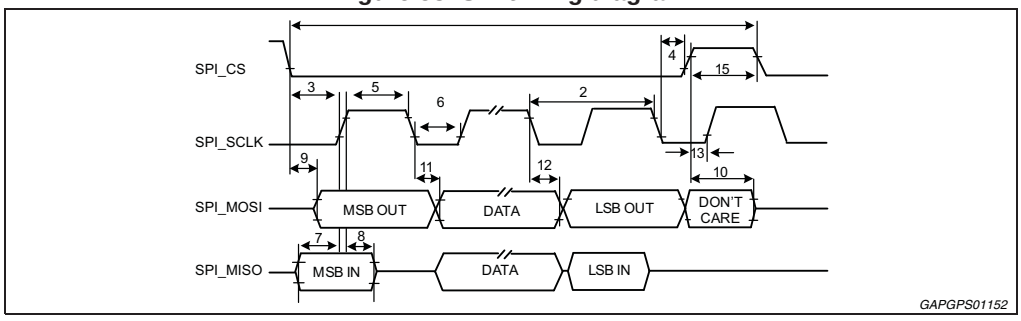
N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	V_{IH_CS}	SPI_CS high level input voltage	-	2	-	-	V
2	V_{IL_CS}	SPI_CS low level input voltage	-	-	-	0.8	V
3	I_{PU_CS}	SPI_CS pull up current	SPI_CS = 0V	-70	-45	-20	µA
4	V_{IH_MOSI}	MOSI high level input voltage	-	2	-	-	V
5	V_{IL_MOSI}	MOSI low level input voltage	-	-	-	0.8	V
6	I_{PD_MOSI}	SPI_MOSI pull down current	SPI_MOSI = VDDQ	20	45	70	µA
7	V_{IH_SCK}	SCK high level input voltage	-	2	-	-	V
8	V_{IL_SCK}	SCK low level input voltage	-	-	-	0.8	V
9	I_{PD_SCK}	SPI_SCK pull down current	SPI_SCK = VDDQ	20	45	70	µA
10	V_{OH_MISO}	SPI_MISO high level output voltage	I_{LOAD} = -800µA	VDDQ -0.5	-	VDDQ	V
11	V_{OL_MISO}	SPI_MISO low level output voltage	I_{LOAD} = 2.0mA	-	-	0.4	V
12	V_{IH_MISO}	SPI_MISO high level input voltage	-	2	-	-	V
13	V_{IL_MISO}	SPI_MISO low level input voltage	-	-	-	0.8	V
14	I_{LKG_MISO}	SPI_MISO tri-state leakage	SPI_MISO= VDDQ or 0V	-10	-	10	µA

Table 25. SPI AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	F_{SCLK}	SPI Transfer frequency	-	-	8	8.08	MHz
2	T_{SCLK}	SPI_SCK period	-	123.8	-	-	ns
3	T_{LEAD}	Enable lead time	-	250	-	-	ns
4	T_{LAG}	Enable lag time	-	50	-	-	ns
5	T_{HIGH_SCLK}	SPI_SCK high time	-	50	-	-	ns
6	T_{LOW_SCLK}	SPI_SCK low time	-	50	-	-	ns
7	T_{SETUP_MOSI}	SPI_MOSI input setup time	-	20	-	-	ns
8	T_{HOLD_MOSI}	SPI_MOSI input hold time	-	20	-	-	ns
9	T_{ACC_MISO}	SPI_MISO access time	80pF load	-	-	60	ns
10	T_{DIS_MISO}	SPI_MISO disable time	80pF load	-	-	100	ns
11	$T_{VALID\_MISO\_OUT}$	SPI_MISO output valid time	80pF load	-	-	30	ns
12	$T_{HOLD\_MISO\_OUT}$	SPI_MISO output hold time	80pF load	0	-	-	ns
13	$T_{SETUP\_MISO\_IN}$	SPI_MISO Input Setup Time		20			ns
14	$T_{HOLD\_MISO\_IN}$	SPI_MISO Input Hold Time		20			ns
15	T_{HOLD_SCLK}	SPI_SCK hold time	-	20	-	-	ns
16	T_{FLT_CS}	SPI_CS noise glitch rejection time	-	50	-	300	ns
17	T_{NODATA}	SPI interframe time	-	400	-	-	ns

Note: All timing is shown with respect to 10% and 90% of the actual delivered VDDQ voltage.

Figure 58. SPI timing diagram



15.8 ER boost

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 18 V.

Table 26. ER Boost converter DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	V_{O_ERBST}	Boost output voltage	Across all line and I_{O_BST} load (steady state) ERBST33V=0 Test conditions: I_{O_BST} = 0.1 & 40mA	22.4	23.8	25	V
2			Across all line and I_{O_BST} load (steady state) ERBST33V=1 Test conditions: I_{O_BST} = 0.1 & 20mA	31.4	33	35	V
3	I_{O_ERBST}	Boost output current	BST33V = 0	0.1	-	60	mA
4			BST33V = 1	0.1	-	40	mA
5	dV_{SR_ac}	Line transient response	All line, load; dt=100us; BST33V = 0/1 Design Info	-8%	-	8%	%
6	dV_{LR_ac}	Load transient response	All line, load; dt=100us; BST33V = 0/1 Design Info	-8%	-	8%	%
7	R_{DSON_ERBST}	Power switch resistance	-	-	-	1	Ω
8	I_{OC_ERBST}	Over current detection	-	550	-	800	mA
9	I_{LKG_ERBST}	ERBOOST leakage current	ERBOOST=40V Device off	-	-	5	µA
10	V_{ERBST_OK}	ERBOOST voltage threshold	BST33V = 0	18	20	22	V
11			BST33V = 1	26	28	30	V
12	V_{ERBST_OV}	ERBOOST Over Voltage threshold	BST33V = 0	22.6		25	V
13			BST33V = 1	31.65		35	V
14	$V_{ERBST\_DIS\_TH}$	Voltage difference between VIN and ERBOOST to deactivate the ER Boost regulator	VIN – ERBOOST	1.6	2.2	2.5	V
15	$V_{CLAMP\_EN\_TH}$	Voltage difference between ERBSTSW and ERBOOST to activate the ER Boost CLAMP	ERBSTSW – ERBOOST	1.6	2.2	2.5	V
16	T_{JSD_ERBST}	Thermal shutdown	-	150	175	190	°C
17	$T_{HYS\_TSDERBST}$		-	5	10	15	°C

Table 27. ER boost converter AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	F_{SW_ERBST}	ERBOOST switching frequency	-	1.8	1.882	2.0	MHz
2	$T_{RISE\_ERBSTSW\_SLOW}$ $T_{FALL\_ERBSTSW\_SLOW}$	ERBSTSW transition time	10% to 90% voltage on ERBSTSW VIN ≥ $VIN_{FASTSLOPE\_L}$ = 10.3 V Iload = 60mA ERboost settings 23 V Guaranteed by design	10 15	-	25 35	ns
3	$T_{RISE\_ERBSTSW\_FAST}$ $T_{FALL\_ERBSTSW\_FAST}$		10% to 90% voltage on ERBSTSW VIN ≤ $VIN_{FASTSLOPE\_H}$= 9 V Iload=60mA ERboost settings 23 V Guaranteed by design	10	-	25	ns
4	T_{ON_ERBST}	ERBOOST charge-up time	$C_{ERBOOST}$ = 2.2µF, Vin =12V, I_{O_ERBST}= 5mA BST33V = 1 Measured from CS edge to V_{O_ERBST}(min)	-	-	5	ms
5	$T_{FLT\_TSD\_ERBST}$	Thermal shutdown filter time	-		-	10	µs

Table 28. ER boost converter external components (Design Info)

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	L_{ERBST}	Inductance	-	8	10	-	µH
2	ESL_{ERBST}	Inductance resistance	-	-	-	0.1	Ω
3	C_{BLK_ERBST}	Output bulk capacitance to ensure regulator stability	Min capacitance value including derating factors	1	2.2		µF
4	ESR_{CBLK_ERBST}	Bulk capacitor ESR	-	-	-	0.1	Ω
5	V_{FSTR_ERBST}	Steering diode forward voltage	I_F=100 mA	-	-	0.85	V
6	I_{LKGSTR_ERBST}	Steering diode reverse leakage	Ta = 95 °C	-	-	100	µA

15.9 ER charge

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35 V, 8 V ≤ ERBOOST.

Table 29. ER current generator DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	I_{ER_CHARGE}	ER charge current	ERBOOST – VER ≥ 3 V	-33	-30	-27	mA
2	$R_{DSON\_ERCHARGE}$	ER charge power resistance	($V_{ERBOOST}$ - V_{VER}) / I_{VER} I_{VER} = 10mA	-	-	22	Ω

Table 30. ER current generator AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	T_{ON_ERCAP}	Energy reserve capacitor charge-up time	C_{VER} ≤ 4.7mF nominal, BST33V = 0; Design Info	-	-	6	s

15.10 ER switch

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35 V.

Table 31. ER switch DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$R_{DSON\ ERSW}$	Power switch resistance	$I_{LIM,ERSW}$(min)	0.5	-	3	Ω
2	$I_{LIM,ERSW}$	ER switch current limit	-	400	-	600	mA
3	T_{JSD_ERSW}	Thermal shutdown	-	150	175	190	°C
4	$T_{HYS\_TSDERSW}$		-	5	10	15	°C

Table 32. ER switch AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	T_{ON_ERSW}	ER turn-on time (time to reach either R_{DSON_ERSW} or I_{LIM_ERSW})	C_{VIN} = 10µF	-	-	5	µs
2	$T_{FLT\_TSD\_ERSW}$	Thermal shutdown filter time	-	-	-	10	µs
3	T_{BLK_ERSW}	ER switch activation blanking time after thermal shutdown	-	-	1	-	ms

15.11 COVRACT

All electrical characteristics are valid for the following conditions unless otherwise noted: -40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35 V, VDDx(min) ≤ VDDx ≤ VDDx(max), VDDQ = VDD5 or VDD3V3

Table 33. COVRACT DC Specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$V_{OH\_COVRACT}$	COVRACT output voltage	I_{LOAD} = -0.5 mA	VDDQ -0.6	-	VDDQ	V
2	$V_{OL\_COVRACT}$		I_{LOAD} = 2.0 mA	0	-	0.4	V

Table 34. COVRACT AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$T_{RISE\_COVRACT}$	Rise time	80pF load, 20%-80%	-	-	0.5	µs
2	$T_{FALL\_COVRACT}$	Fall time	80pF load, 20%-80%	-	-	0.5	µs

15.12 VDD5 regulator

All electrical characteristics are valid for the following conditions unless otherwise noted. -40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35 V.

Table 35. VDD5 regulator DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	V_{O_VDD5}	Output voltage	Across all line and load, steady state	4.85	5	5.15	V
2	I_{O_BVDD5}	Base driver current limit	VDD5 > $VDD5_{UVL}$	4	7	10	mA
3	$I_{O\_BVDD5\_LOW}$	Base driver current limit Low level	VDD5 < $VDD5_{UVL}$	2	-	5	mA
4	I_{O_VDD5}	Output load current	-	0.5	-	200	mA
5	dV_{SR_ac}	Line transient response	All load I_{O_VDD5}; VIN=6V to 18V @ dt = 1 µs; Design Info	4.5	-	5.5	V
6	dV_{LR_ac}	Load transient response	All line; I_{O_VDD5}= 1mA to 100mA @dt = 1 µs; Design Info	4.5	-	5.5	V
7	I_{OF_VDD5}	Open feedback current on VDD5	Active only during VDD5_rampup state	55	80	105	µA
8	$VDD5_{OV}$	Over voltage detection	-	5.2	-	5.50	V

Table 35. VDD5 regulator DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
9	$VDD5_{UV}$	Under voltage detection	-	4.5	-	4.8	V
10	$VDD5_{UVL}$	Under voltage detection low level	-	1.8	2	2.2	V

Table 36. VDD5 regulator AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	T_{SOFTST_VDD5}	Soft start time	From 10% to 90%	1	2	3	ms
2	T_{FLT_VDD5OV}	Over voltage detection deglitch filter time	-	27	30	33	µs
3	T_{FLT_VDD5UV}	Under voltage detection deglitch filter time	-	27	30	33	µs
4	$T_{FLT\_VDD5UVL}$	Under voltage low detection deglitch filter time	-	1.5	2	2.5	µs

Table 37. VDD5 regulator external components (Design Info)

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	h_{FE_PNP}	Output transistor gain	-	50	250	500	A/A
2	F_{t_PNP}	Output transistor transit frequency	-	30	-	-	MHz
3	R_{VDD5BE}	Output transistor base-emitter Pull-up resistance	-	-	3	-	kΩ
4	C_{BLK_VDD5}	Output bulk capacitance	Min 4.7µF nominal	3	-	30	µF
5	ESR_{CBLK_VDD5}	Bulk capacitor ESR	-	-	-	50	mΩ

15.13 VDD3V3 regulator

All electrical characteristics are valid for the following conditions unless otherwise noted.
-40 °C ≤ Ta ≤ +95 °C, VDD5(min) ≤ VDD5.

Table 38. VDD3V3 regulator DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	V_{O_VDD3V3}	Output voltage	Across all line and load, steady state	3.2	3.3	3.4	V
2	I_{O_VDD3V3}	Output load current capability	-	0.5	-	125	mA
3	$I_{O\_LIM\_VDD3V3}$	Output load current limit	-	150	-	-	mA
6	dV_{SR_ac}	Line transient response	All load IO_VDD3V3; VIN = 6 V to 18 V @ dt = 1 µs; Guaranteed by design	3	-	3.6	V
7	dV_{LR_ac}	Load transient response	All line; I_{O_VDD3V3}= 1mA to 100mA @dt = 1 µs; Guaranteed by design	3	-	3.6	V
4	$VDD3V3_{OV}$	Over-voltage threshold	-	3.43	-	3.6	V
5	$VDD3V3_{UV}$	Under voltage reset threshold	-	3	-	3.17	V

Table 39. VDD3V3 regulator AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	T_{SOFTST_VDD3}	Soft start time	From 10% to 90%	1	2	3	ms
2	T_{FLT_VDD3OV}	Over voltage detection deglitch filter time	-	27	30	33	µs
3	T_{FLT_VDD3UV}	Under voltage detection deglitch filter time	-	27	30	33	µs

Table 40. VDD3V3 regulator external components (design info)

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	C_{BLK_VDD3}	Output bulk capacitance	Min 4.7µF nominal	3	-	30	µF
2	ESR_{CBLK_VDD3}	Bulk capacitor ESR	-	-	-	50	mΩ

15.14 VSUP regulator

All electrical characteristics are valid for the following conditions unless otherwise noted.
-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD2}(max) ≤ VIN ≤ 35 V.

Table 41. VSUP regulator DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	V_{O_VSUP}	Output voltage	Across all line and load, steady state	6.5	6.8	7.1	V
2	I_{O_BVSUP}	Base driver current limit	-	4	7	10	mA
3	I_{O_VSUP}	Output load current	-	0.5		200	mA
4	dV_{SR_ac}	Line transient response	All load I_{O_VDD5}; VIN = 6 V to 18 V @ dt = 1 µs; Design Info	6.2		7.4	V
5	dV_{LR_ac}	Load transient response	All line; I_{O_VDD5}= 1mA to 100mA @dt = 1µs; Design Info	6.2		7.4	V
6	$VSUP_{OV}$	Over voltage detection	-	7.6		8	V
7	$VSUP_{UV}$	Under voltage detection	-	1.8	2	2.2	V

Table 42. VSUP AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	T_{SOFTST_VSUP}	Soft start time	From 10% to 90%	1	2	3	ms
2	T_{FLT_VSUPOV}	Over voltage deglitch filter time	-	27	30	33	µs
3	T_{FLT_VSUPUV}	Under voltage deglitch filter time	-	27	30	33	µs

Table 43. VSUP regulator external components (Design Info)

N°	Symbol	Component	Conditions	Min	Typ	Max	Unit
1	h_{FE_PNP}	Output transistor gain	-	50	250	500	A/A
2	F_{t_PNP}	Output transistor transit frequency	-	30	-	-	MHz
3	R_{VSUPBE}	Output transistor Base-Emitter Pull-up Resistance	-	-	3	-	kΩ
4	C_{BLK_VSUP}	Output Bulk Capacitance	Min 4.7µF nominal	3	-	30	µF
5	ESR_{CBLK_VSUP}	Bulk Capacitor ESR	-	-	-	50	mΩ

15.15 VSF regulator

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35 V, VSF + 2V ≤ ERBOOST

Table 44. VSF regulator DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	VSF	Output voltage	All line, load, I_{O_VSF} up to 6 mA SYS_CFG(VSF_V)= 0	18	20	22	V
2			All line, load, I_{O_VSF} up to 6 mA BST33V = 1, SYS_CFG(VSF_V)= 1	23	25	27	V
3	I_{LIM_VSF}	Output load current limit	Test conditions: VSF = 0	7	10	13	mA
4	V_{DO_VSF}	Drop-out voltage	V(ERBOOST-VSF)	-	-	2	V
5	C_{VSF}	Output capacitance	Design Info.	2.9	-	14	nF
6	$I_{LKG\_VSF\_OFF}$	VSF input leakage	Device OFF	-5		5	µA
7	R_{PD_VSF}	VSF pull-down resistance	Device ON VSF regulator OFF or ON 1.5V<VSF<25V Test condition: VSF = 25V	60	125	188	kΩ
8	I_{PD_VSF}	VSF pull-down current	Device ON VSF regulator ON Design Info	34	40	46	µA
9	$I_{PD\_VSF\_TOT}$	VSF total pull-down current	IPD_VSF_TOT = IPD_VSF + RPD_VSF Device ON VSF regulator ON Test conditions: – VSF = 25V – SYS_CGF(VSF_V)= 0	166	230	462	µA

Table 45. VSF regulator AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$T_{ON,VSF}$	VSF turn on time	CVSF = 14 nF and IO_VSF=0 Measured from VSF_EN = 1 to VSF inside regulation limits	-	-	100	µs

15.16 Deployment drivers

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35 V, 6 V ≤ SSxy ≤ 35 V, SSxy - SFx ≤ 25 V.

Table 46. Deployment drivers - DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	I_{DEPL_LO}	Deployment current	R = 2 ohms Considering 9mA as not detected leakage with a 1kOhm equivalent resistance from SFx to GND	1.33	1.4	1.55	A
2	I_{DEPL_HI}		R = 2 ohms, 9 V ≤ SSxy Considering 13.5 mA as not detected leakage with a 1 kΩ equivalent resistance from SFx to GND, Not available with t_{depl} = 2 ms selection	1.94	1.99	2.2	A
3	I_{OC_SR}	Low side over current detection	-	2.2	3.1	4	A
4	I_{LIM_SR}	Low side current limitation	-	2.2	3.1	4	A
5	$\Delta I_{LIM\_OC\_SR}$	Difference between current limitation and OC threshold	I_{LIM_SR} - I_{OC_SR}	0.1	-	-	A
6	R_{DSONT}	Total high and low side MOS on resistance	Ta = 95 °C	-	-	2	Ω
7	I_{RV_SF}	Reverse current on SFx	Without device malfunction (1) Not to be tested in series production	-	-	-100	mA
8	$I_{LKG\_SS\_OFF}$	SSxy leakage current	Device OFF SSxy ≤ 35V SFx = SFy = 0	-10	-	10	µA
9	$I_{LKG\_SS\_ON}$		Device ON SSxy ≤ 35V SFx = 0	46	66	86	µA
10	$I_{LKG\_SS\_CH\_ARMED}$		Device ON One channel armed SSxy ≤ 35V SFx = 0	410	490	570	µA

Table 46. Deployment drivers - DC specifications (continued)

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
11	$I_{LKG\_SF\_ON}$	SF leakage current	Device ON, VRESDIAG = VSSxy = 35 V, SFx = 0V-35 V	-50	-	50	µA
12	$I_{LKG\_SF\_OFF}$		Device OFF, VRESDIAG = open, VSSxy = open but all SSxy pins connected, SEx = 0 V - 35 V	-50	-	50	µA
13	$I_{LKG\_SR\_ON}$	SR leakage current	Device ON, VRESDIAG = VSSxy = 35 V, SFx = 0V-35 V	-	-	50	µA
14	$I_{LKG\_SR\_OFF}$		Device OFF, VRESDIAG = open, VSSxy = open but all SSxy pins connected, SEx = 0 V - 35 V	-	-	50	µA
15	L_{DEPL}	Load Inductance	Maximum load inductance Design Information(2)	0	-	60	µH
16	C_{SFx}	Load capacitance	Maximum capacitance to GND	13	-	455	nF
17	C_{SRx}		Design Information	13	-	455	nF
18	C_{SSxy}	SSxy capacitance	Maximum capacitance to GND connected directly to SSxy pin Design Information	-	-	10	nF
19	R_{SFLx}	Load Impedance	Design Information	-	-	6.5	Ω
20	-	Wire Length	Squib Loops containing a clockspring shall be limited to a maximum length of 3m	1	-	10	m
21	R_{Wirex}	Wire resistance	Design information	16.8	-	63.4	mΩ/m
22	L_{Wirex}	Wire Inductance	Design Information	0.6	-	1.8	µH/m
23	R_{CSx}	Clock spring resistance	Maximum number of clock springs is 3 for any IC Design Information	0	-	0.7	Ω
24	L_{CSx}	Clock spring inductance	Design Information	0	-	42.9	µH
25	$k_{L\_CS1 - L\_CS2}$	Clocks pring coupling	Design Information	0.739	-	0.903	-
26	L_{EMI}	Squib EMI protection	Design Information	0	-	7.7	µH

1. In case of an unsupplied device and shorted deployment pins (e.g. to battery voltage), the dynamic reverse current through the high side power stage depends on CSSxy.
2. LDEPL could be calculated in the following way:
   - Non-ClockSpring Loops
     $L_{DEPL(max)}$ = LWire(10m*2) + L_{EMI} = (3.6 µH/m * 10m) + 7.7 µH = 43.7 µH
   - ClockSpring Loops
     $L_{DEPL(max)} = L_{Wire}$(3m*2) + L_{CSx} + L_{EMI} = (3.6µH/m * 3m) + [42.9 µH * (1 - 0.739)] + 7.7 µH = 29.7 µH
   - ClockSpring Loops with short to ground
     $L_{DEPL(max)} = L_{Wire}$(3m) + L_{CSx} + L_{EMI} = (1.8µH/m * 3m) + 42.9µH + 7.7µH = 56 µH.

Figure 59. Deployment drivers diagram

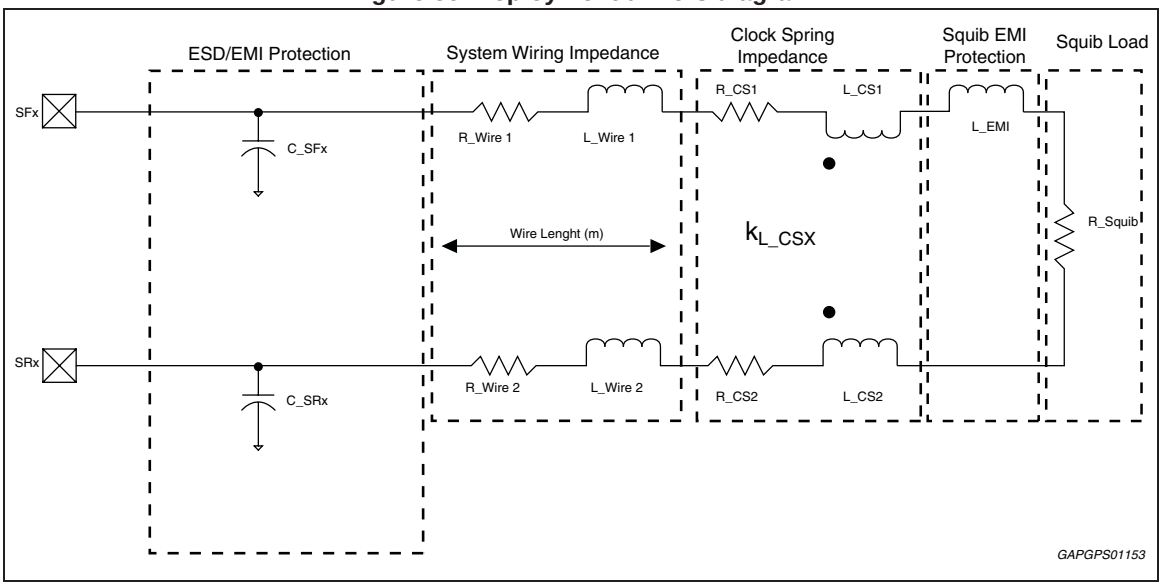


Table 47. Deployment drivers - AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	T_{DEPL_LO}	Deployment time	1.209 A rising to 1.209 A falling	2	-	2.268	ms
2	T_{DEPL_HI}		1.764 A rising to 1.764 A falling	0.7	-	0.832	ms
3				0.5	-	0.613	ms
4	T_{DEP_RES}	Deployment current counter resolution	-	0	-	16	µs
5	T_{RISE_IDEPL}	Rise time 10% - 90% of I_{DEPL}	SSxy = 25 V; R_{SQ} = 2.2 Ω, C = 22 nF, L = 44 µH	-	-	32	µs
6	T_{DEL_IDEP}	Delay time SPI_CS to 90% I_{DEPL}		-	-	65	µs
7	T_{FALL_IDEPL}	Fall time 90% - 10% I_{DEPL}		-	-	32	µs
8	T_{DEL_SD-LS}	Low-side shutdown delay time (with respect to high-side deactivation)	-	50	-	-	µs
9	$T_{FLT\_LIM\_LS}$	Low-side overcurrent to low-side deactivation deglitch time in short to battery condition	-	80	100	120	µs
10	$T_{OFF\_OS\_HS}$	Low-side overcurrent to high-side deactivation deglitch time in case of intermittent open squib condition	-	-	-	20	µs
11	$T_{OFF\_OS\_HS}$	High-side off time in case of intermittent open squib condition	-	4	-	12	µs

15.17 Squib diagnostic

15.17.1 Squib resistance measurement

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35 V, 6 V ≤ SSxy ≤ 35 V; 7V ≤ VRESDIAG ≤ 35V.

Table 48. Deployment drivers diagnostics (Squib resistance)

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$R_{SQ\_RANGE\_1}$	Squib Resistance Range 1	LPDIAGREQ(ISRC_CURR_SEL)= 0	0	-	10	Ω
2	$R_{SQ\_RANGE\_2}$	Squib Resistance Range 2	LPDIAGREQ(ISRC_CURR_SEL)= 1	0	-	50	Ω
3	G_{RSQ}	Squib resistance measurement differential amplifier gain	-	-2%	5.2	+2%	V/V
4	V_{OFF_RSQ}	Squib Resistance Measurement Differential Amplifier Output Offset	$V_{OUT\_RSQ} = G_{RSQ} \times (V_{SF} - V_{SR}) + V_{off\_RSQ}$	200	-	400	mV
5	$I_{SRC\_HI\_SF}$ $I_{SRC\_HI\_SR}$	Squib resistance measurement high current source	R_{SQ_RANGE} = 1 Ω to 10 Ω LPDIAGREQ(ISRC_CURR_SEL) = 0 LPDIAGREQ(ISRC) = "01" or "10"	-5%	40	+5%	mA
6	$I_{SRC\_LO\_SF}$ $I_{SRC\_LO\_SR}$	Squib resistance measurement low current source	R_{SQ_RANGE} = 1 Ω to 50 Ω LPDIAGREQ(ISRC_CURR_SEL) = 1 LPDIAGREQ(ISRC) = "01" or "10"	-10%	8	+10%	mA
7	I_{SRC_DELTA}	Squib Resistance Measurement Delta Current Source	-	-5%	32	+5%	mA
8	SR_{ISRC}	Squib resistance measurement current source slew-rate	-	4	7.5	11	mA/µs
9	V_{SRx_RM}	SRx voltage during Resistance Measurement	LPDIAGREQ(ISRC) = ”01” or “10” LPDIAGREQ(ISINK) = 1	0.5	0.7	1	V
10	$I_{SINK\_HI\_SR}$	SRx current sink limit high level	LPDIAGREQ(ISRC_CURR_SEL) = 0 LPDIAGREQ(ISINK) = 1	50	70	90	mA
11	$I_{SINK\_LO\_SR}$	SRx current sink limit low level	LPDIAGREQ(ISRC_CURR_SEL) = 1 LPDIAGREQ(ISINK) = 1	10	17.5	25	mA
12	I_{PD_SR}	SRx current pull down	-	0.7	1	1.3	mA
13	R_{LKG_SF}	Leakage resistance on SFx	Leakage to GND ±1 V or to Battery from 6 V to 18 V. Design info	1	-	-	kΩ

Table 48. Deployment drivers diagnostics (Squib resistance) (continued)

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
14	R_{SQ_ACC}	Accuracy of digital resistance measurement	After software calculation All errors included RSQ between 1.0 Ω and 10.0 Ω With High Current Source (40mA)	-8	-	+8	%
15	-	EMI Input Low-pass filter	Design Info	50	-	100	kHz

15.17.2 Squib leakage test (VRCM)

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35 V,
VDD3V3(min) ≤ VDD3V3 ≤ VDD3V3(max).

Table 49. Squib leakage test (VRCM)

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	V_{OUT_VRCM}	Output Voltage on SF or SR pins during Leakage test	I_{OUT} = 0 mA	-10%	2.5	+10%	V
2			I_{OUT} = 6.6 mA	-8.7%	2.3	+8.7%	V
3	$R_{LKG\_GSQ\_TH}$	Detection threshold, leakage to GND	Leakage detected if R_{LKG_GSQ} ≤ 1 kΩ and not detected if R_{LKG_GSQ} ≥ 10 kΩ Design Info	1	-	10	kΩ
4	$I_{LKG\_GSQ\_TH}$		Equivalent to resistance range	-15%	450	+15%	µA
5	$R_{LKG\_BSQ\_TH}$	Detection threshold, leakage to BATTERY	Leakage detected if $_{LKG\_BSQ}$ ≤ 1 kΩ and not detected if R_{LKG_BSQ} ≥ 10 kΩ Design Info	1	-	10	kΩ
6	$I_{LKG\_BSQ\_TH}$		Equivalent to resistance range	-15%	1.8	+15%	mA
7	$I_{LIM\_VRCM\_SRC}$	VRCM current limitation	-	-20	-	-10	mA
8	$I_{LIM\_VRCM\_SINK}$		-	10	-	20	mA
9	V_{SHIFT}	External ground or battery shift	Design Info	-1	-	1	V
10	$R_{SQ\_LOW\_TH}$	Detection Threshold for “resistance too low”	Design Info	200	-	500	Ω
11	$I_{RSQ\_LOW\_TH}$		Equivalent to resistance range	-12%	6	+12%	mA
12	$R_{SQ\_HIGH\_TH}$	Detection threshold for “resistance too high”	Design Info	2	-	5	kΩ
13	$I_{RSQ\_HIGH\_TH}$		Equivalent to resistance range	-15%	700	+15%	µA
14	T_{FLT_LKG}	Leakage test deglitch filter time	-		8		µs

15.17.3 High/low side FET test

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35 V, 6 V ≤ SSxy ≤ 35 V, 7V ≤ VRESDIAG ≤ 35V.

Table 50. High/low side FET test

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$I_{HS\_FET\_TH}$	Detection threshold (HS FET test)	-	-10%	1.8	+10%	mA
2	$I_{LS\_FET\_TH}$	Detection threshold low side FET test	-	-10%	450	+10%	µA
3	E_{FET_TESt}	Energy transferred to squib during HS/LS FET tests	Design Info	-	-	170	µJ
4	$T_{FLT\_HS\_FET\_TH}$ $T_{FLT\_LS\_FET\_TH}$	FET Test deglitch filter time	-	1.3	1.5	1.7	µs
5	$T_{FETTIMEOUT}$	HS/LS FET test time-out	-	190	200	210	µs
6	$SGxy_{\_OPEN}$	Squib open ground detection	GNDSUBx as ground reference	300	450	600	mV
7	T_{FLT_SGOPEN}	Squib open ground detection filter time	-	46	50	54	µs

15.17.4 Deployment timer test

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35 V

Table 51. Deployment timer test

No	Symbol	Parameter	Comments / Conditions	Min	Typ	Max	Unit
1	t_{PULSE_IDLE}	Deployment timer pulse Test Idle Time	SYSDIAGREQ(DSTEST)=PULSE	7	8	9	ms
2	$I_{PULSE\_HIGH\_00}$	Deployment timer pulse Test High Time	SYSDIAGREQ(DSTEST)=PULSE DCR_x(Deploy_Time) = 00	-5%	8	+5%	µs
3	$I_{PULSE\_HIGH\_01}$		SYSDIAGREQ(DSTEST)=PULSE DCR_x(Deploy_Time) = 01	-5%	584	+5%	µs
4	$I_{PULSE\_HIGH\_10}$		SYSDIAGREQ(DSTEST)=PULSE DCR_x(Deploy_Time) = 10	-5%	792	+5%	µs
5	$I_{PULSE\_HIGH\_11}$		SYSDIAGREQ(DSTEST)=PULSE DCR_x(Deploy_Time) = 11	-5%	2160	+5%	µs

15.18 Remote sensor interface

All electrical characteristics are valid for the following conditions unless otherwise noted.
-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD2}(max) ≤ VIN ≤ 35V, VSUP(min) ≤ VSUP ≤ VSUP(max).

Table 52. Remote sensor I/F DC parameters

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	I_{S_LOW}	Interface quiescent current (low signal current level)	*According to PSI-5 v1.3, section 5.1.2 - parameter #4* Design info	-19	-	-4	mA
2	ΔIs	Delta signal current	I_{S_HIGH} - I_{S_LOW} *According to PSI-5 v1.3, section 5.4 - parameter #6* Design Info	22	-	30	mA
3	V_{LIM_RSU}	Output voltage limitation	VSUP = VIN *According to PSI-5 v1.3, section 5.1.1 - parameter #1*	-	-	11	V
4	R_{DSON_RSU}	RSU power switch resistance	(V_{VSUP} – V_{RSU}) / I_{RSU} I_{RSUx} = 4-50 mA *According to PSI-5 v1.3, section 6.2 - parameter #3*	-	-	12.5	Ω
5	V_{STB_RSU}	Output short to battery threshold	-	10	50	100	mV
6	I_{STB_RSU}	Static reverse current into RSU pin	V_{RSU} > V_{VSUP} + V_{STB_RSU}	-	-	5	mA
7	I_{OC_RSU}	Over current detection threshold	Interface disabled after $T_{FLT\_STD\_RSU}$ *According to PSI-5 v1.3, section 5.1.2 - parameter #8-9*	-105	-	-50	mA
8	I_{LIM_RSU}	Current limitation	RSU = 0 According to PSI-5 v1.3, section 5.1.2, parameter #8-9	-105	-	-65	mA
9	$\Delta I_{LIM\_OC\_RSU}$	Difference between current limitation and OC threshold	I_{LIM_RSU} - I_{OC_RSU}	0.1	-	-	mA
10	I_{B0_RSU}	Internal base current starting value	Default value of internal 7 bit counter	-18	-15	-13	mA
11	$I_{S\_TH\_RSU}$	Trigger point for signal current threshold	I_{RSU} = I_{LOW_RSU} = -19mA to -4mA	I_{B_RSU} + (12-11%)	I_{B_RSU} + 12	I_{B_RSU} + (12+11%)	mA
12	I_{LKGG_RSU}	Trigger point for fault current detection	Leakage to GND; detected by I_B	-48	-	-36	mA
13	I_{LKGB_RSU}		Leakage to BATTERY; detected by I_B	-3.5	-	-1.5	mA
14	I_{OL_RSU}	Output open load detection threshold	RSU open	$I_{LKGB(min)}$	-	$I_{LKGB(max)}$	-

Table 52. Remote sensor I/F DC parameters (continued)

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
15	DAC_{RES}	DAC resolution	Design info	-	7	-	Bit
16	I_{LSB}	LSB current	-	270	-	330	µA
17	C_{RSU}	EMC capacitor	22nF nominal Design Info	13	-	-	nF
18	T_{JSD_ERBST}	Thermal shutdown	-	150	175	190	°C
19	$T_{HYS\_TSDERBST}$		-	5	10	15	°C

Table 53. PSI-5 remote sensor transceiver - AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$T_{FLT\_STD\_RSU}$	Over Current Shutdown Filter Time	Normal operation	500	-	600	µs
2	$T_{BLK\_OC\_RSU}$	Over current shutdown filter time	At interface power on (BLKTxSEL = 0) *According to PSI-5 v1.3, section 5.2 - parameter #1*	4.6	-	5.4	ms
3			At interface power on (BLKTxSEL = 1) *According to PSI-5 v1.3, section 5.2 - parameter #2*	9.4	-	10.8	ms
4	T_{STB_RSU}	Short to battery comparator response time	Guaranteed by design	-	-	200	ns
5	$T_{STB\_REC\_RSU}$	Short to battery recovery time	-	12	-	16	µs
6	$T_{FLT\_TSD\_RSU}$	Thermal shutdown filter time	-		-	10	µs
7	$T_{FLT\_OPEN\_RSU}$	Open detection deglitch filter time	-	10	-	15	µs
8	$T_{FLT\_LKG\_RSU}$	Leakage deglitch filter time	-	10	-	15	µs

15.19 DC sensor interface

All electrical characteristics are valid for the following conditions unless otherwise noted.
-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD2}(max) ≤ VIN ≤ 35V, 8.5 V ≤ VRESDIAG ≤ 35 V.

Table 54. DC sensor interface specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	V_{OUT_DCSREG}	Output voltage regulation mode	DCS Regulator enabled	-10%	6.25	+10%	V
2	I_{LIM_DCSREG}	Current limitation regulation mode	DCS Regulator enabled DCS = 0	24	27	30	mA
3	V_{DCS_RANGE1}	Voltage measurement range1	First voltage measurement (V_{DCS_MEAS1}) to compensate external ground shift and internal offset	-1	-	1.4	V
4	V_{DCS_ACC1}	Voltage measurement accuracy 1	V_{DCS} = V_{DCS_RANGE1} Included ADC error	-15	-	15	%
5	V_{DCS_RANGE2}	Voltage measurement range 2	-	1.5	-	10	V
6	V_{DCS_ACC2}	Voltage measurement accuracy 2	V_{DCS} = V_{DCS_RANGE2} Included ADC error	-8	-	+8	%
7	I_{DCS_RANGE1}	Current measurement range 1	-	1	-	2	mA
8	I_{DCS_ACC1}	Current measurement accuracy 1	I_{DCS} = I_{DCS_RANGE1} Included ADC error	-30	-	+30	%
9	I_{DCS_RANGE2}	Current measurement range 2	-	2	-	22	mA
10	I_{DCS_ACC2}	Current measurement accuracy 2	I_{DCS} = I_{DCS_RANGE2} Included ADC error	-12	-	+12	%
11	I_{DCS_RANGE3}	Current measurement range 3	Regulator in current limitation	-	I_{LIM_DCSREG}	-	mA
12	I_{DCS_ACC3}	Current measurement Accuracy 3	DCS = 0 Included ADC error	-12	-	+12	%
13	R_{DCS_RANGE}	Resistance Measurement Range	Design info	65	-	3000	Ω
14	R_{DCS_ACC}	Accuracy of digital resistance measurement	Performing both voltage measurements 1 and 2 After Software calculation All errors included	-15		15	%

Table 54. DC sensor interface specifications (continued)

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
15	I_{PD_DCS}	Pull down current	V_{DCS} = 1.5V	70	100	130	µA
16	R_{PD_DCS}	Pull down resistance	Device ON, DCS Pull Down Current disabled	90	150	210	kΩ
17	$I_{TOT\_PD\_DCS}$	Total pull down current	$I_{TOT\_PD\_DCS} = I_{PD\_DCS} + R_{PD\_DCS}$ V_{DCS} = 6.5V	100	140	200	µA
18	C_{DCS}	Output capacitance	Design Info	10		-	nF
19	I_{REF_IDCS}	Internal current reference for DCS current measurement	-	-5%	300	+5%	µA
20	Ratio_VDCS	Divider ratio for DCS voltage measurement	-	-3%	7.125	+3%	V/V
21	V_{OFF_DCS}	Internal offset during voltage measurement	-	-4%	0.375	+4%	V

15.20 Safing engine

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35V, VDDx(min) ≤ VDDx ≤ VDDx(max), VDDQ = VDD5 or VDD3V3.

Table 55. Arming interface - DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	$V_{TH\_H\_ACL}$	ACL input voltage thresholds	-	2.33	-	2.42	V
2	$V_{TH\_L\_ACL}$		-	1.58	-	1.67	V
3	V_{HYS_ACL}	ACL hysteresis	-	0.6	0.75	0.9	V
4	R_{PD_ACL}	ACL pull down resistance	V_{ACL} = 3.3V	120	200	280	kΩ
5	V_{OH_ARM}	ARM output high voltage	I_{LOAD} = -0.5 mA Internal safing selected	VDDQ -0.60	-	VDDQ	V
6	V_{OL_ARM}	ARM output low voltage	I_{LOAD} = 2.0 mA Internal safing selected	0	-	0.4	V
7	R_{PD_ARM}	ARM pull down resistance	-	65	100	135	kΩ
14	V_{IH_FENH}	FENH high level input voltage	-	2	-	-	V
15	V_{IL_FENH}	FENH low level input voltage	-	-	-	0.8	-
16	I_{PU_FENH}	FENH pull down current	FENH = VDDQ	20	45	70	µA
14	V_{IH_FENL}	FENL high level input voltage	-	2	-	-	V

Table 55. Arming interface - DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
15	V_{IL_FENL}	FENL low level input voltage	-	-	-	0.8	
16	I_{PU_FENL}	FENL pull up current	FENL = 0	-70	-45	-20	µA
14	$V_{IH\_SAF\_CSx}$	SAF_CSx high level input voltage	-	2	-	-	V
15	$V_{IL\_SAF\_CSx}$	SAF_CSx low level input voltage	-	-	-	0.8	-
16	$I_{PU\_SAF\_CSx}$	SAF_CSx pull up current	SAF_CSx = 0V	-70	-45	-20	µA

Table 56. Arming interface - AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	T_{ARM}	Sensor sampling period	-	475	500	525	µs
2	T_{ACL_HI}	ACL period	-	213	-	237	ms
3	T_{ACL_LO}		-	168	-	187	ms
4	$T_{ON\_ACL\_HI}$	ACL on-time	-	154	-	171	ms
5	$T_{ON\_ACL\_LO}$		-	114	-	126	ms
6	T_{VALID_EOL}	Scrap validation T_{ACL} and T_{ON_ACL} valid	-	3	-	-	cycles
7	T_{DIS_EOL}	Scrap timeout	-	2 * T_{ACL}		ms	
8	T_{PULSE_STRECH}	Arming enable pulse stretch time	-	-	-	0	ms
9			-	30	32	34	ms
10			-	242		270	ms
11			-	1934		2162	ms
12	T_{RISE_ARM}	ARM rise time	80pF load, 20% to 80% Internal Safing Selected	-	-	1.00	µs
13	T_{FALL_ARM}	ARM fall time	80pF load, 20% to 80% Internal Safing Selected	-	-	1.00	µs

15.21 General purpose output drivers

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD1}(max) ≤ VIN ≤ 35V; GPODx + 5V ≤ ERBOOST.

Table 57. GPO interface DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	V_{SAT_GPO}	Output saturation voltage	$V_{GPOD} – V_{GPOS}$ I_{LOAD} = 70 mA	-	-	0.5	V
2	I_{LIM_GPO}	Current limitation	$V_{GPOD} – V_{GPOS}$ = 1.5 V	73	110	155	mA
3	I_{OC_GPO}	Over current detection threshold	-	73	110	155	mA
4	$\Delta I_{LIM\_OC\_GPO}$	Difference between current limitation and OC threshold	I_{LIM_GPO} - I_{OC_GPO}	0.1	-	-	mA
5	I_{OL_GPO}	Open load current threshold	GPO ON condition; LS and HS configuration	0.1	1	3	mA
6	I_{DIAG_GPO}	Diagnostic current on load	Voltage measurement in progress through Analog MUX Increased leakage for a short specified time (32 µs)	-	-	130	µA
7	$I_{LKG\_GPOD\_OFF}$	GPOD output leakage current	V_{GPOD} = 18V V_{GPOS} = 0V Power-off or sleep mode	-5	-	5	µA
8	$I_{LKG\_GPOD\_ON}$		V_{GPOD} = 18V V_{GPOS} = 0V Active or passive mode Driver off	-	-	100	µA
9	$I_{LKG\_GPOS\_OFF}$	GPOS output leakage current	V_{GPOD} = 18V V_{GPOS} = 0V Power-Off or Sleep Mode or ERBOOST = ERBOOST_OK Driver OFF	-5	-	5	µA
10	$I_{LKG\_GPOS\_ON}$		V_{GPOD} = 18V V_{GPOS} = 0V (Active or Passive Mode) and ERBOOST = ERBOOST_OK Driver OFF	-	-	100	µA
11	I_{REV_GPO}	Reverse current	$V_{GPOS} = V_{GPOD}$ + 1V Driver OFF	-		1	mA
12	T_{JSD_GPO}	Thermal Shutdown	-	150	175	190	°C
13	$T_{HYS\_TSD\_GPO}$		-	5	10	15	°C
14	C_{GPO}	Load capacitor	Min 10nF nominal Design Info	6	-	-	nF

Table 58. GPO Driver Interface - AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	SR_{GPO}	Output voltage slew rate	30% - 70%; R_{LOAD} = 273Ω, C_{LOAD} = 100nF	0.1	0.25	0.4	V/µs
2	$T_{FLT\_OC\_GPO}$	Over current detection filter time	-	10	12	14	µs
3	$T_{FLT\_OL\_GPO}$	Open load detection filter time	-	8	10	12	µs
4	$T_{MASK\_ON\_GPO}$	Diagnostic mask delay after switch ON	C_{GPO} = 100nF typ	40	50	60	µs
5	T_{FLT_TSD}	Thermal shutdown filter time	-	-	-	10	µs
6	F_{PWM_GPO}	PWM frequency	-	-	125	-	Hz
7	DC_{PWM_GPO}	PWM duty cycle	Increment Step = 1.6%	0	-	100	%

15.22 ISO9141 interface (K-LINE)

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD}(max) ≤ VIN ≤ 35V.

Table 59. ISO9141 interface DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	V_{IH_ISOTX}	ISOTX high level input voltage	-	2	-	-	V
2	V_{IL_ISOTX}	ISOTX low level input voltage	-	-	-	0.8	V
3	V_{HYS_ISOTX}	ISOTX hysteresis input voltage	-	150	-	500	mV
4	I_{PU_ISOTX}	ISOTX pull up current	ISOTX = 0	-70	-45	-20	µA
5	C_{IN_ISOTX}	ISOTX input capacitance	Design Info	-	-	5	pF
6	$V_{TH\_DOM\_ISOK}$	ISOK input receiver threshold	ISOTX = 0V	VIN * 0.4	VIN * 0.45	VIN * 0.5	V
7	$V_{TH\_REC\_ISOK}$		ISOTX = VDDQ	VIN * 0.5	VIN * 0.55	VIN * 0.6	V
8	V_{HYS_ISOK}		-	VIN * 0.07	VIN * 0.1	VIN * 0.13	V
9	$V_{O\_DOM\_ISOK}$	ISOK output voltage	ISOTX = 0V, I_{ISOK} = 40mA	-	-	1.2	V
10	I_{OC_ISOK}	ISOK over current detection	-	50	-	100	mA
11	I_{LIM_ISOK}	ISOK current limitation	-	50	-	100	mA
12	$\Delta I_{LIM\_OC\_ISOK}$	Difference between current limitation and OC threshold	I_{LIM_ISOK} - I_{OC_ISOK}	0.1	-	-	mA
13	I_{SINK_ISOK}	ISOK sink current capability	Design Info	40	-	-	mA
14	I_{LKG_ISOK}	ISOK input leakage current	VIN < 18V, Driver Off (device is supplied)	-10	-	10	µA
15	V_{OH_ISORX}	ISORX output high voltage	I_{LOAD} = -0.5 mA	VDDQ -0.60	-	VDDQ	V
16	V_{OL_ISORX}	ISORX output low voltage	I_{LOAD} = 2 mA	0	-	0.4	V
17	C_{IN}	ISOK Input Capacitance	Design info	-	-	10	pF
18	T_{JSD_ISOK}	Thermal shutdown	-	150	175	190	°C
19	$T_{HYS\_TSD\_ISOK}$		-	5	10	15	°C

Table 60. ISO9141 interface transceiver AC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	T_{FLT_TSD}	Thermal shutdown filter time	-	-	-	10	µs
2	T_{BLK_ISOK}	Current limit fault blanking time	-	8	-	12	µs
3	T_{RISE_ISORX}	ISORX rise time	80pF load, 20%-80%	-	-	0.5	µs
4	T_{FALL_ISORX}	ISORX fall time	80pF load, 20%-80%	-	-	0.5	µs
5	-	Baud rate	Design Info	-	62.5	-	kBd
6	T_{PD_ILTX}	Propagation delay transmitter	ISOTX High to Low to ISOK = 70% * $V_{O\_REC\_ISOK}$ R_{ISOK}=510Ω, C_{ISOK}=470pF	-	-	1	µs
7	T_{PD_IHTX}		ISOTX Low to High to ISOK = 30% * $V_{O\_DOM\_ISOK}$ R_{ISOK}=510Ω, C_{ISOK}=470pF	-	-	1.5	µs
8	T_{PD_ILRX}	Propagation delay receiver	ISOK = $V_{TH\_DOM\_ISOK}$ to ISORX High to Low R_{ISOK}=510Ω, C_{ISOK}=470pF	-	-	1.5	µs
9	T_{PD_IHRX}		ISOK = $V_{TH\_REC\_ISOK}$ to ISORX Low to High R_{ISOK}=510Ω, C_{ISOK}=470pF	-	-	1.5	µs
10	T_{RISE_ISOK}	ISOK rise time	30% to 70% RISOK=510Ω, CISOK=470pF	-	-	1.5	µs
11	T_{FALL_ISOK}	ISOK fall time	70% to 30% RISOK=510Ω, CISOK=470pF	-	-	1.5	µs
12	T_{PDW_RX}	Receiver pulse width symmetry	T_{PD_ILRX} - T_{PD_IHRX}	-	-	1	µs
13	T_{PDW_TX}	Transmitter pulse width symmetry	$(T_{PD\_ILTX} + T_{FALL\_ISOK}) - (T_{PD\_IHTX} + T_{RISE\_ISOK})$	-	-	1	µs

15.22.1 Analog to digital converter

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD}(max) ≤ VIN ≤ 35V.

Table 61. Analog to digital converter

N°	Symbol	Parameter	Condition	Min	Typ	Max	Unit
1	V_{ADC_RANGE}	ADC input voltage range	-	0.1	-	2.5	V
2	V_{ADC_REF}	ADC reference voltage	-	-1.5%	2.5	+1.5%	V
3	ADC_RES	ADC resolution(1)	Design Info	-	10	-	bit
4	DNL	Differential non linearity error (DNL)	Separation between adjacent levels, measured bit to bit of actual and an ideal output step. No missing codes	-1	-	+1	LSB
5	INL	Integral non linearity error (INL)	Maximum difference between the actual analog value at the transition between 2 adjacent steps and its ideal value	-3	-	+3	LSB
6	E_{QUANT}	Quantization Error	Design Info	-0.5	-	0.5	LSB
7	TotErr	Total error	Includes INL, DNL, ADC Reference voltage tolerance and quantization error	-15	-	+15	LSB
8	TotErr_0v1	ADC total error for 0.1V input voltage	-	-5	-	+5	LSB
9	TotErr_2v4	ADC total error for 2.4V input voltage	-	-15	-	+15	LSB
10	-	Pre-ADC settling time	-	-	4.81	-	µs
11	-	Single conversion time	-	-	2.25	-	µs
12	-	Intra-queue settling time	-	-	3.5	-	µs
13	-	Post- ADC settling time	-	-	3.44	-	µs
14	-	ADC conversion time - voltage	4x sampling for each of the 4 conversions in the queue Design Info	-	54.75	-	µs
15	-	ADC conversion time – current and voltage	8x sampling for DCS, temperature and squib loop resistance measurements + 4x sampling for remaining 2 conversions in the queue Design Info	-	51.25	-	µs

1. LSB = (2.5 V / 1024) = 2.44 mV

15.23 Voltage diagnostics (analog Mux)

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD}(max) ≤ VIN ≤ 35V.

Table 62. Voltage diagnostics (Analog MUX) DC specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Units
1	Ratio_1	Divider ratios	V_{IN_RANGE1} = 0.1V … 2.5V	-	1	-	V/V
2	Ratio_4		V_{INPUT_RANGE2} = 1V … 10V (where applicable)	-3%	4	+3%	V/V
3	Ratio_7		$V_{INPUT\_RANGE\_3}$ = 1.5V … 17.5V (where applicable)	-3%	7	+3%	V/V
4	Ratio_10		$V_{INPUT\_RANGE\_4}$ = 2V … 25V (where applicable)	-3%	10	+3%	V/V
5	Ratio_15		$V_{INPUT\_RANGE\_5}$ = 3V … 35V (where applicable)	-3%	15	+3%	V/V
6	$V_{OFFSET\_RATIO\_X}$	Divider offset	High impedance	-10	-	10	mV
7	R_{RATIO_4}	Multiplexer input resistance	Multiplexer input to GNDA	80	-	-	kΩ
8	R_{RATIO_7}		Multiplexer input to GNDA	120	-	-	kΩ
9	R_{RATIO_10}		Multiplexer input to GNDA	160	-	-	kΩ
10	R_{RATIO_15}		Multiplexer input to GNDA	200	-	-	kΩ
11	$I_{LEAK\_RATIO\_X}$	Additional multiplexer on-state input leakage current	For All Divider Ratio expect Ratio_1	-	-	60	µA
12	V_{MEAS_ACC}	Voltage measurement accuracy	All range All errors included	-12	-	+12	%

15.24 Temperature sensor

All electrical characteristics are valid for the following conditions unless otherwise noted.

-40 °C ≤ Ta ≤ +95 °C, VIN_{GOOD}(max) ≤ VIN ≤ 35V.

Table 63. Temperature sensor specifications

N°	Symbol	Parameter	Condition	Min	Typ	Max	Units
1	T_{MON_RANGE}	Monitoring temperature range	-	-40	-	150	°C
2	T_{MON_ACC}	Monitoring temperature accuracy	-	-15	-	15	°C

16 Quality information

16.1 OTP trim bits

The device has 43 fuse programmable bits which are used to tune and refine performance characteristics of the device and also provide detailed identification of each component. These bits are only available during production testing and require activation of a special test mode. These bit values are confirmed every transition from POR, and reported in *Section 5.1.1: Fault status register (FLTSR)* if an error is found.

The OTP CRC is implemented using the polynomial calculation (g(x)=1+x+x^3 with initialization value equal to "111").

Equivalent equations are:

CRC[2] =

C0in + C1in + C2in + d1 + d11 + d12 + d13 + d15 + d18 + d19 + d20 + d22 + d25 + d26 + d27 + d29 + d32 + d33 + d34 + d36 + d39 + d4 + d40 + d41 + d5 + d6 + d8

CRC[1] =

C0in + C1in + d0 + d12 + d13 + d14 + d16 + d19 + d2 + d20 + d21 + d23 + d26 + d27 + d28 + d30 + d33 + d34 + d35 + d37 + d40 + d41 + d42 + d5 + d6 + d7 + d9

CRC[0] =

C1in + C2in + d0 + d10 + d11 + d12 + d14 + d17 + d18 + d19 + d21 + d24 + d25 + d26 + d28 + d3 + d31 + d32 + d33 + d35 + d38 + d39 + d4 + d40 + d42 + d5 + d7

where d[42:0] are the 43 OTP bits and Cxin are the starting seed values (all '1').

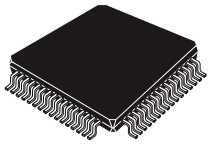
17 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

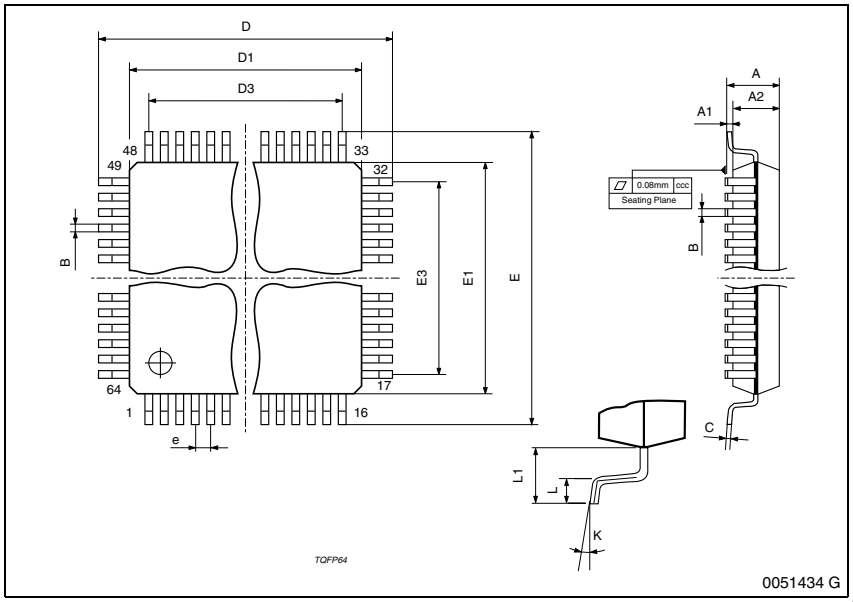
Figure 60. LQFP64 (10 x 10) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.17	0.22	0.27	0.0066	0.0086	0.0106
C	0.09		0.20	0.0035		0.0079
D	11.80	12.00	12.20	0.464	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.401
D3		7.50			0.295	
e		0.50			0.0197	
E	11.80	12.00	12.20	0.464	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.401
E3		7.50			0.295	
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0393	
K	0° (min.), 3.5° (min.), 7°(max.)					
ccc			0.080			0.0031

OUTLINE AND MECHANICAL DATA



LQFP64 (10 x 10 x 1.4mm)



18 Revision history

Table 64. Document revision history

Date	Revision	Changes
10-Feb-2014	1	Initial release.
19-Feb-2014	2	Updated *Features* and *Table 1: Device summary on page 1*.
22-May-2014	3	Updated: *Figure 25: Deployment loop diagnostics on page 116* and *Section 15.17.1: Squib resistance measurement on page 183* (conditions).

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