

KSZ9031RNX Evaluation-Socket Board Revision 1.1

REVISION HISTORY

DATE	DESCRIPTION	REVISION
6/15/12	Initial Release	1.0
8/16/12	Added note to change FB2 from ferrite bead to 0 Ohm when PMOS (Q2) is populated. Added LDO_O output drive range for PMOS gate input. Added note to place copper ground PCB heat sink for PMOS (Q2).	1.1
9/28/12	Changed U1 (KSZ9031RNX) pin 13 from VSS_PS to NC and pin 47 from AVDDH to NC.	1.2

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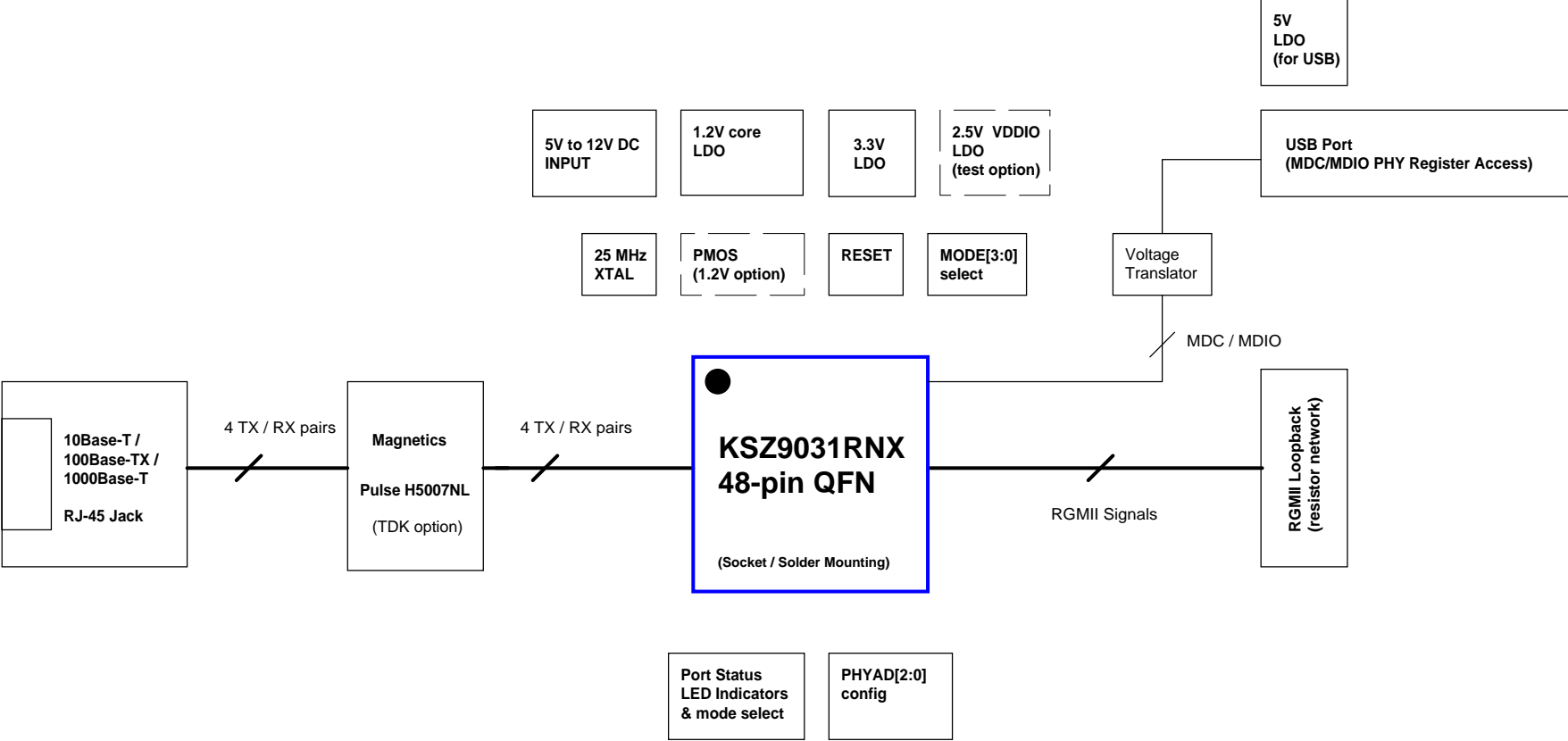
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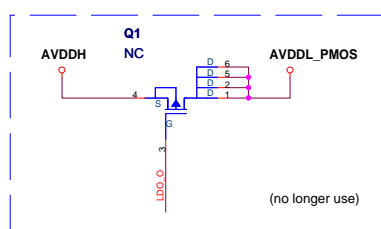
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KSZ9031RNX EVALUATION-SOCKET BOARD - BLOCK DIAGRAM

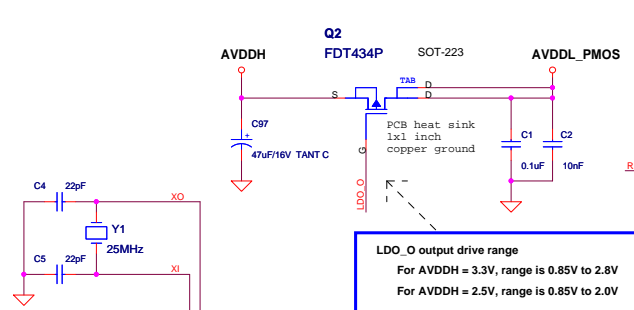


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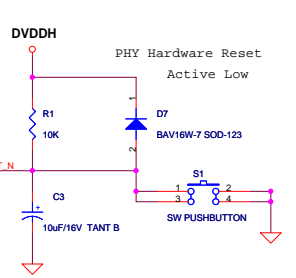
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For KSZ9021RN footprint compatibility, KSZ9031RNX
 * Pin 13 (not bonded out) can be tied to PCB signal ground.
 * Pin 47 (not bonded out) can be tied to AVDDH power.



LDO_O output drive range
 For AVDDH = 3.3V, range is 0.85V to 2.8V
 For AVDDH = 2.5V, range is 0.85V to 2.0V



Strapping Pins

MODE3

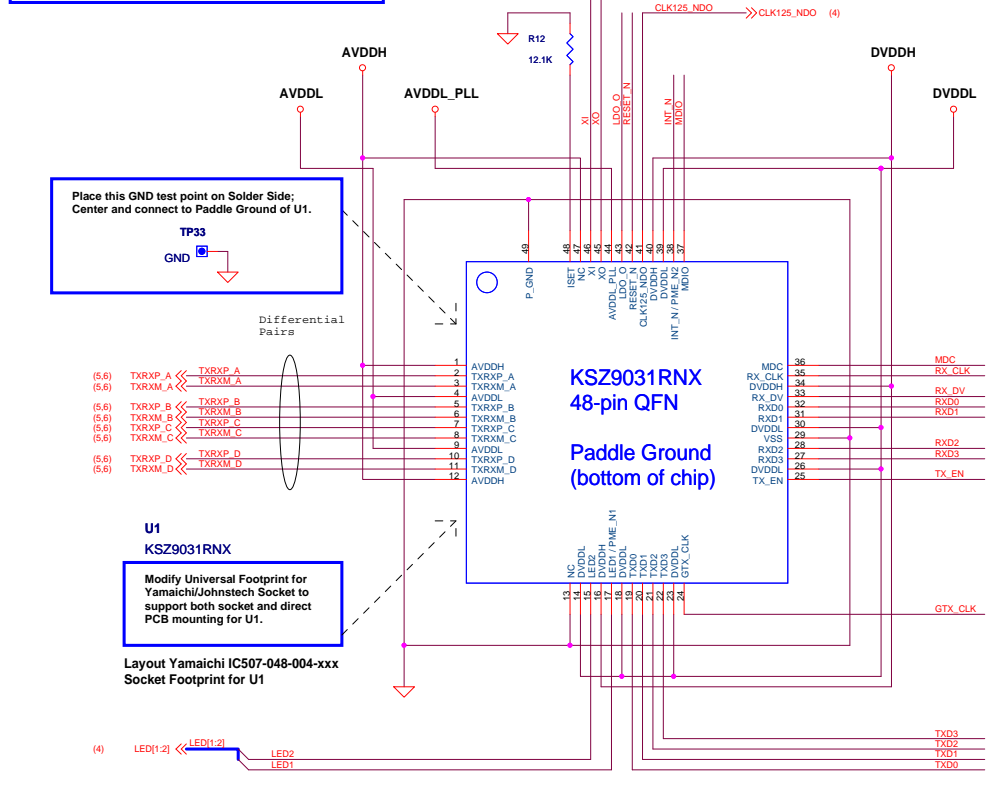
MODE2

MODE1

MODE0

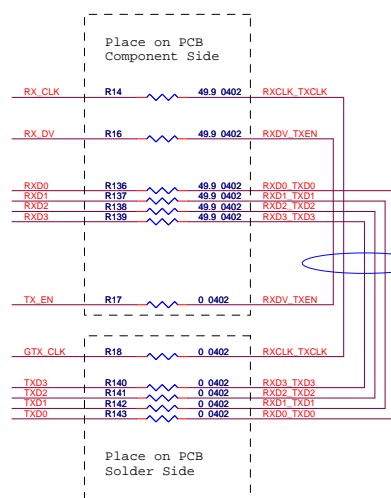
MODE[3:0]	Description
0000	reserved
0001	reserved
0010	reserved
0011	reserved
0100	NAND Tree mode
0101	reserved
0110	reserved
0111	Chip Power Down

MODE[3:0]	Description
1000	reserved
1001	reserved
1010	reserved
1011	reserved
1100	Advertise 1000BT full-duplex only (RGMII)
1101	Advertise 1000BT full- and half-duplex only (RGMII)
1110	Advertise all capabilities, except 1000BT half-duplex (RGMII)
1111	Advertise all capabilities (RGMII)



RGMII Loopback

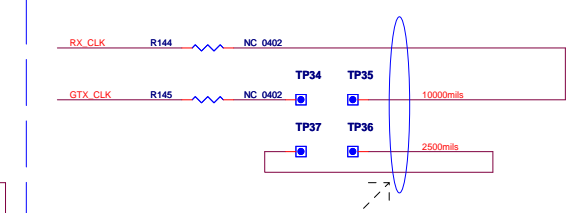
(Default: select KSZ9031RNX on-chip data-to-clock skew and no PCB skew)



RGMII Clock Delay (test option)

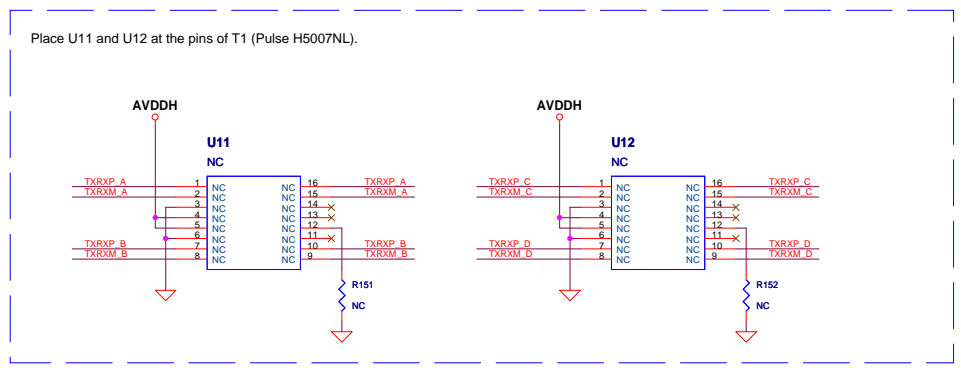
(Select PCB data-to-clock skew and program KSZ9031RNX for no on-chip skew)

Trace Delay is 180ps/1000mil for stripline layer (inside PCB layer) for FR-4 PCB.
 Place R144 on PCB Component Side next to R14.
 Place R145 on PCB Solder Side next to R18.

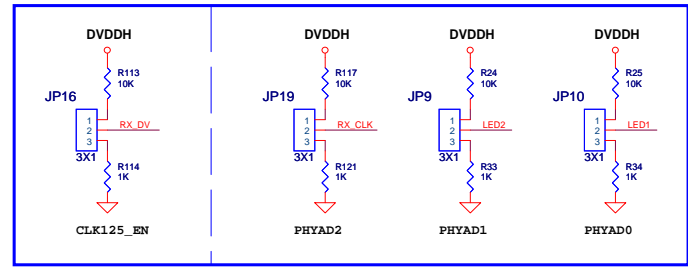


Route these RGMII nets on layer 3.

Test options (no longer use)



Strapping Pins

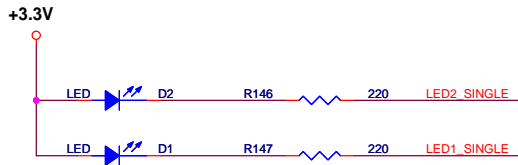


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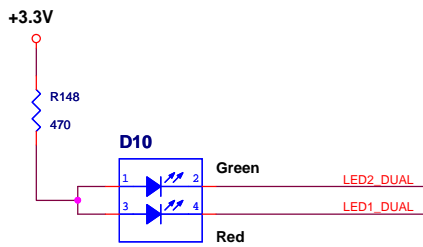
Single LED Mode

Pin	Description
LED2	1 : Link off 0 : Link on (any speed), solid color
LED1	Blinking : Activity (RX, TX)



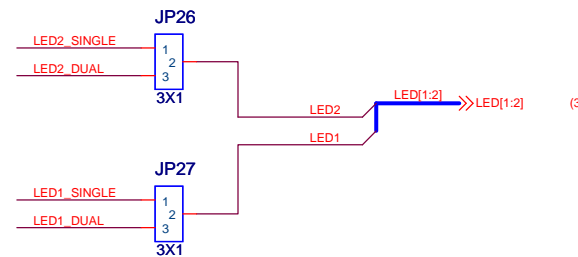
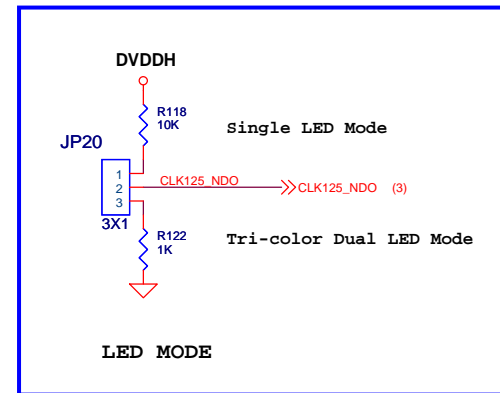
Tri-color Dual LED Mode

Pins [LED2, LED1]	Description	
[0, 1] [togglng, 1]	Solid Color : 1G Link Blinking : Activity (RX, TX)	Green
[1, 0] [1, togglng]	Solid Color : 100M Link Blinking : Activity (RX, TX)	Red
[0, 0] [togglng, togglng]	Solid Color : 10M Link Blinking : Activity (RX, TX)	Orange
[1, 1]	Link off	



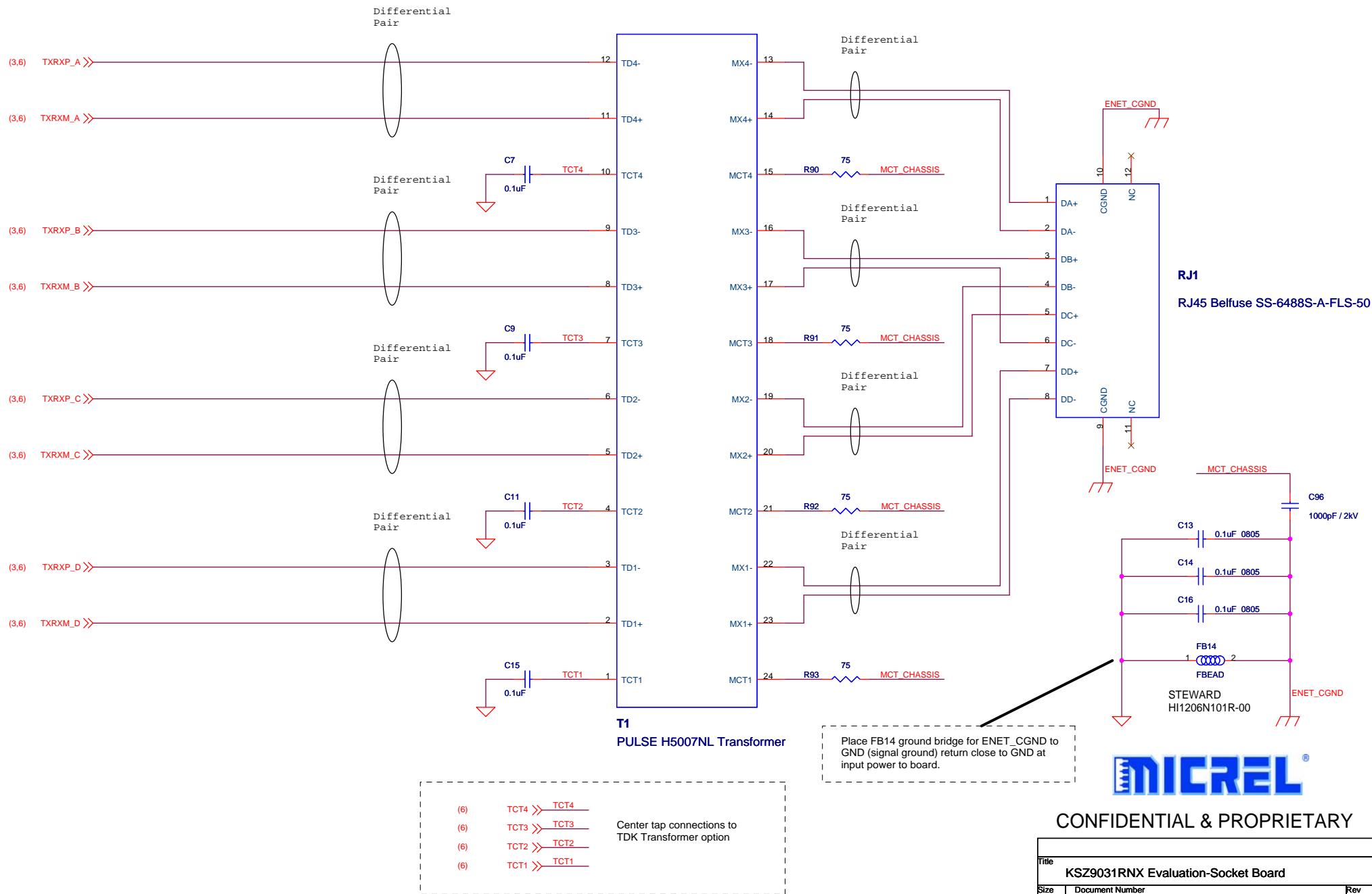
Dialight 598-8610-207F / 1210 SMD

Strapping Pin



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KSZ9031RXN Evaluation-Socket Board		
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	RJ-45 Connector / Pulse H5007NL Transformer	1.2
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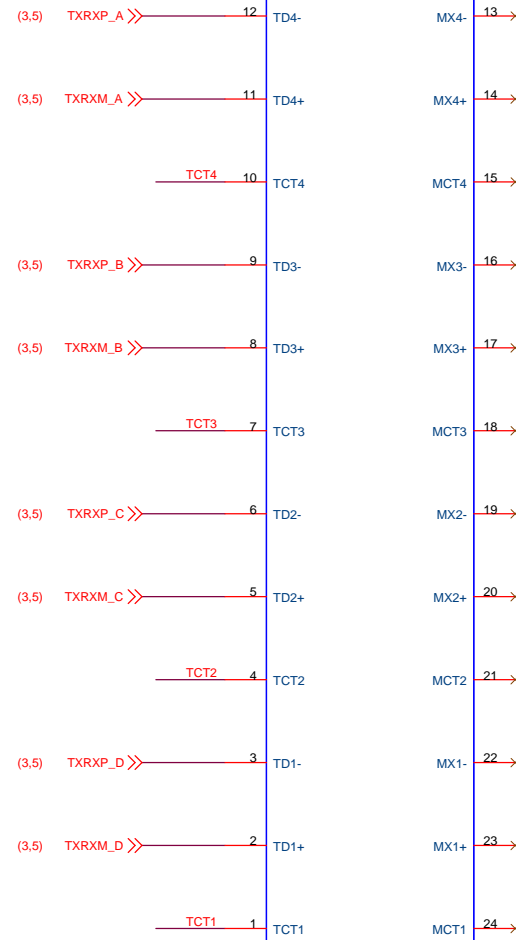
TDK TLA-7T101LF Transformer Option

TDK Transformer has the same pinouts as the Pulse H5007NL (T1), but is narrower.

Layout TDK Transformer as detailed on this page.

When populating TDK Transformer, add rework wires to connect the corresponding pads between TDK Transformer and Pulse Transformer on the RJ-45 Jack side.

KSZ9031RNX PHY Side
Overlay these pins with those
of Pulse H5007NL Transformer (T1)



T2
TDK TLA-7T101LF Transformer

RJ-45 Jack Side
Place PCB pads only for these pins

(5) TCT4 >> TCT4
(5) TCT3 >> TCT3
(5) TCT2 >> TCT2
(5) TCT1 >> TCT1

Center tap connections to
Pulse H5007NL Transformer

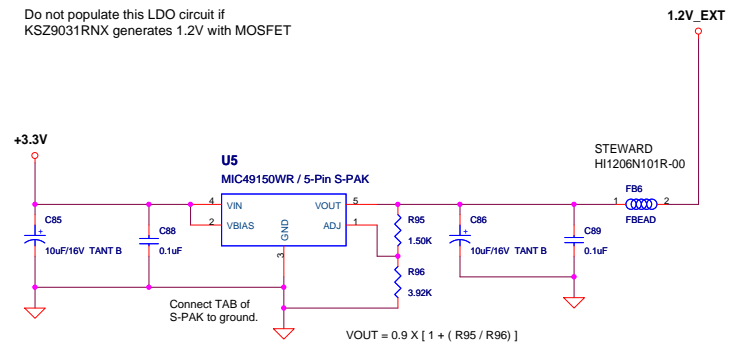


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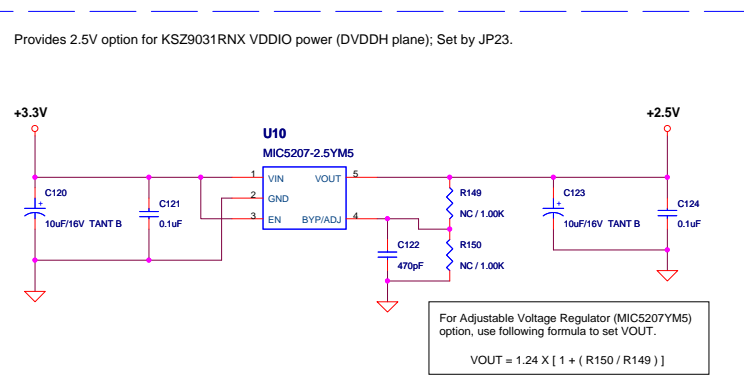
1.2V Power option

Do not populate this LDO circuit if KSZ9031RNX generates 1.2V with MOSFET

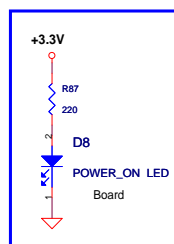
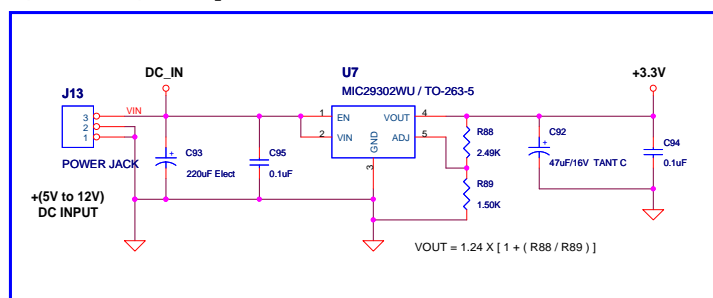


2.5V Power (test option)

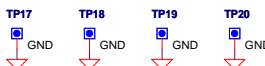
Provides 2.5V option for KSZ9031RNX VDDIO power (DVDDH plane); Set by JP23.



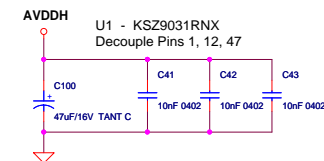
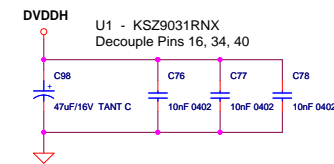
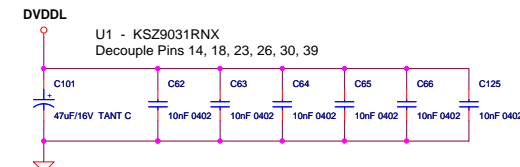
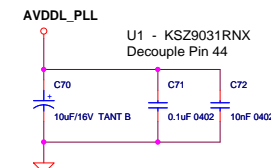
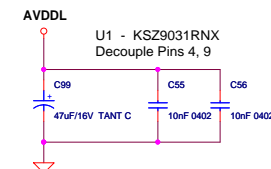
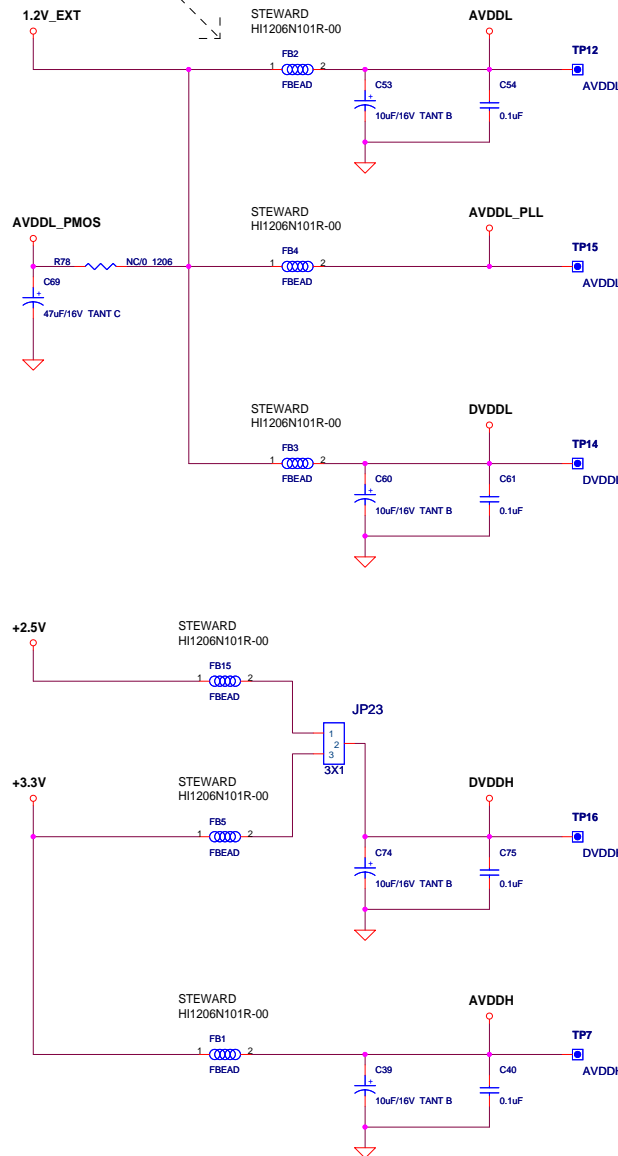
+(5V to 12V) DC Input



Place GND test points evenly across PCB.



AVDDL is the feedback for the KSZ9031RNX on-chip LDO controller. Change FB2 from ferrite bead to 0 Ohm when PMOS (Q2) is populated.



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