Power, Connect and Protect

Introduction

This application note provides recommended guidelines in designing a product that complies with both EMI and ESD standards using Micrel's 10/100 family of Ethernet switches and PHYs.

The printed circuit board (PCB) is the single most important factor that effects EMI, ESD and overall Ethernet cable performance. Meeting these requirements depends on good PCB design practices. The goal is to minimize digital and common mode noise, and to provide shielding between the PCB's internal circuitry and its external environment. These PCB design practices can also be applied to the entire PCB design, not just the Micrel Ethernet device's layout.

General Rules

- Position components so as to avoid long loop traces.
- Choose a metal box/case to shield the circuit board if possible.
- Use a ferrite core on the DC power cord to reduce EMI.
- Follow layout guidelines for differential pairs, ground plane, and high-speed signals.
- Provide termination on clock lines and high-speed digital signals.
- Provide impedance matching on high-speed signal traces to prevent reflections.
- Keep power and ground noise under 50mV peak-to-peak.
- Ensure power supply is rated for the application.
- Ensure switching DC-DC converters are filtered and shielded properly since these power components can produce a lot of EMI noise.

Power and Ground Planes

- Do not split the ground plane into separate planes for analog, digital and power pins. A single ground plane is recommended for Micrel's 10/100 Ethernet products.
- Route high-speed signals above a continuous unbroken ground plane.
- Fill copper in the unused area of signal planes, and connect these copper fills to the ground plane with vias.
- Stagger the placement of vias to avoid creating long gaps in the planes due to via voids.

Analog VCC Planes

Place and route the analog components within the Analog VCC plane.

Digital VCC planes

Place and route the digital components within the Digital VCC plane.

Signal Ground

The signal ground region should be one continuous, unbroken plane. GNDD, GNDA, and GNDS should be connected directly to the signal ground plane for Micrel's 10/100 Ethernet products.
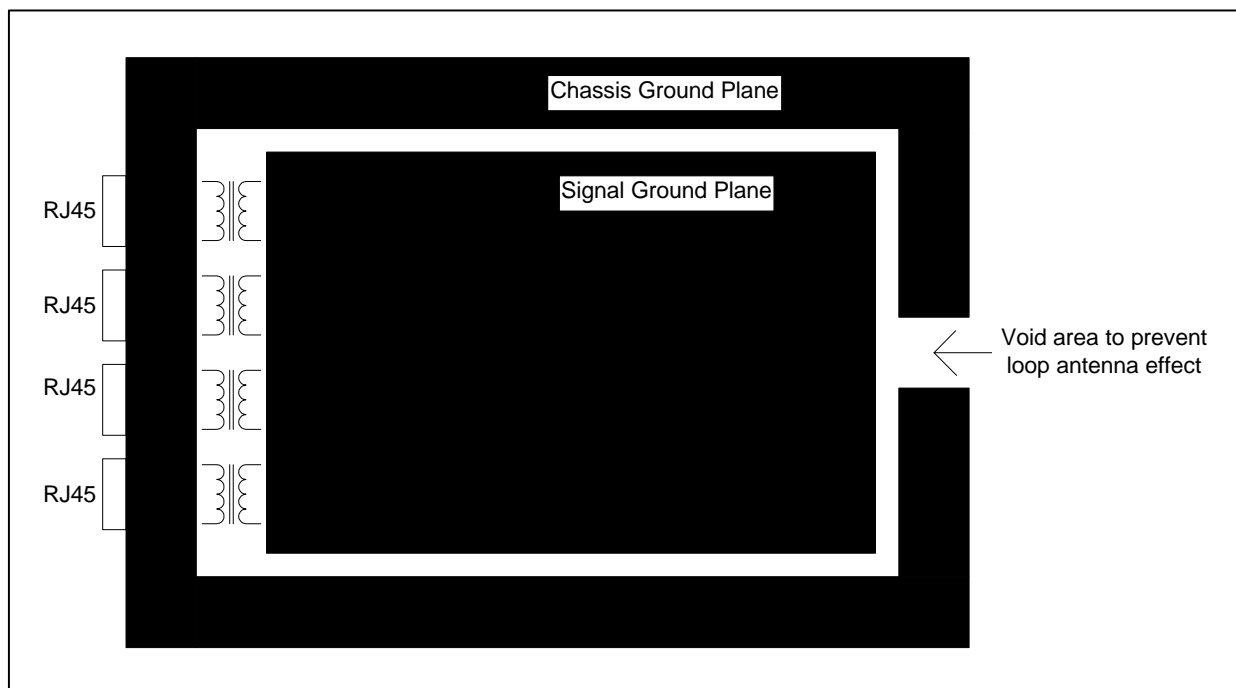
Chassis Ground

The chassis ground and magnetics serve two purposes. They help to reduce EMI noise emissions from the signal ground plane to the PCB's external environment, and also act as an shield to protect the PCB components from ESD.

The chassis ground should be placed on all PCB layers, except the power plane layer(s). Super vias are used to join the chassis ground on the different PCB layers.

The chassis ground plane should be multi-point connected to the external chassis and/or metal frame.

A trench is used to isolate the chassis ground plane from the signal ground plane.

The chassis ground region extends from the front edge of the PCB (RJ45 connectors) to the magnetics and around the edge of the board. See Figure 1.

Figure 1: Ground Planes

Magnetic Noise Zone

- Void power and ground planes on all PCB layers directly under the magnetics.
- Chassis ground should extend from the magnetics to the RJ45 connectors.
- Do not route any digital signals between the PHY and RJ45 connectors.

Differential Signal Layout

- Route differential signal pairs close together and away from all other signals.
- Route each differential pair on the same PCB layer.
- Keep both traces of each differential pair as identical to each other as possible.
- Keep transmit and receive differential pairs at least 3X spacing away from each other.
- Route transmit and receive differential pairs using 5 mil trace width and 5 mil spacing. See Figure 2.
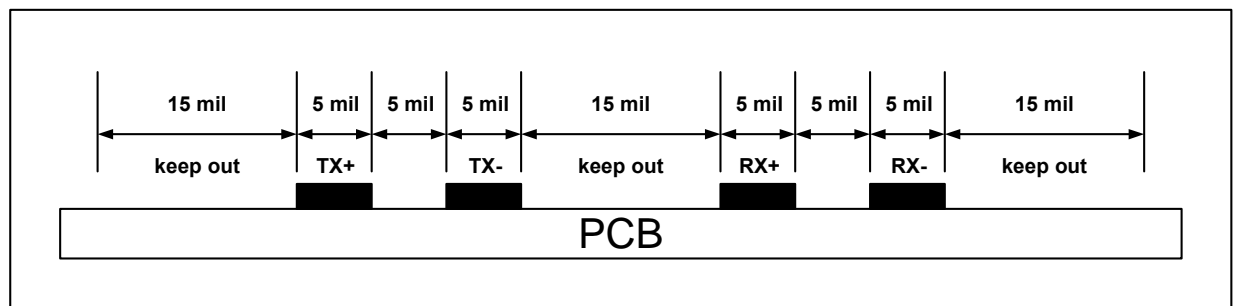

Figure 2: Transmit/Receive Differential Pair

PCB Layer Stacking

6-layer example:

_____ layer 1 component side (short traces), 1 oz copper
_____ layer 2 ground plane, 1 oz copper
_____ layer 3 signal, 1 oz copper
_____ layer 4 signal, 1 oz copper
_____ layer 5 power plane, 1 oz copper
_____ layer 6 signal, 1 oz copper

Keep layers 3 and 4 as far apart as possible.

4-layer example:

_____ layer 1 component side, 1 oz copper
_____ layer 2 ground plane, 1 oz copper
_____ layer 3 power plane, 1 oz copper
_____ layer 4 signal, 1 oz copper

Clock Layout Guidelines

- Clock traces should be as short as possible.
- All clock traces should have an unbroken reference ground plane.
- Use a clock driver when driving multiple loads from a single oscillator.
- All clock signals should be terminated with a 33-50 Ohm series resistor placed close to the clock source.

ESD Protection

- Place TVS transient suppression devices (optional) on the transmit and receive differential pair I/Os to further increase ESD protection. These devices are connected in parallel with the I/O lines to be protected.
- ESD protection devices are available from numerous suppliers. Two notable vendors are Protek Devices (http://www.protekdevices.com/) and Semtech (http://www.semtech.com/TVSnet/T).
- Various ESD protection methods can be used. The level of ESD protection provided by each method will vary and depend on the type of protection device used. The manufacturer's datasheet should be consulted for the level of ESD protection and proper connection. Figures 3 and 4 show two ESD protection methods using the Protek Devices SR2.8.
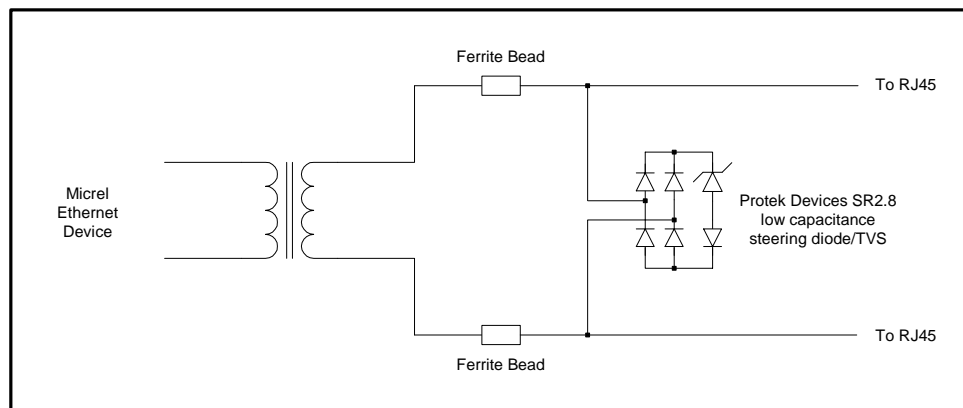
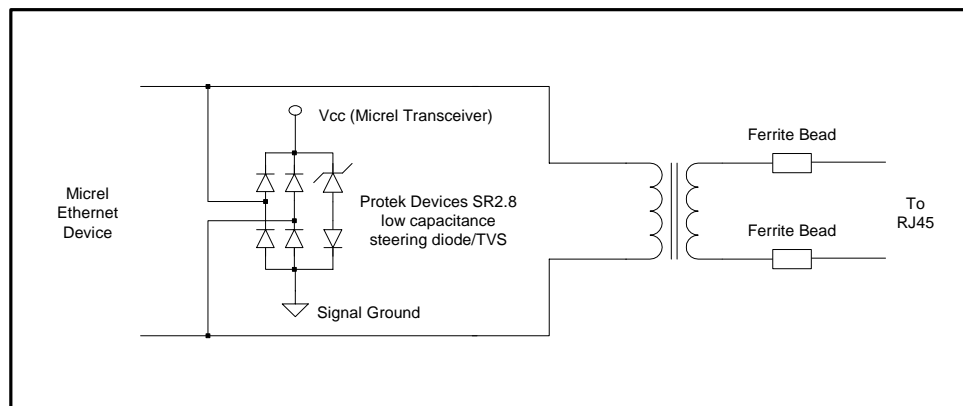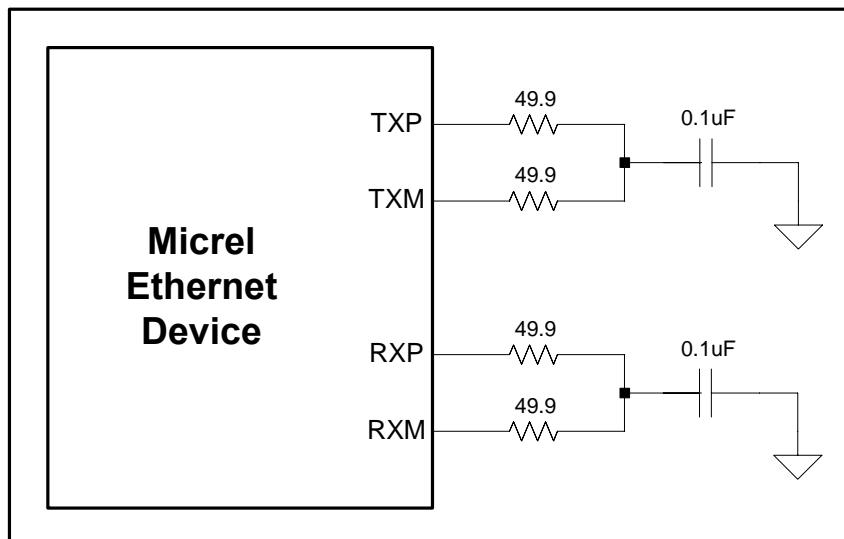**Figure 3: ESD Protection on RJ45 side**

Figure 4: ESD Protection on Micrel Ethernet Device side

- All unused inputs are connected to either ground with a 1K resistor or power with a 10K resistor, depending on the desired strap in setting of the chip.
- Place the termination resistors for the transmit and receive differential pairs close to the Micrel chip. See Figure 5.

Figure 5: Termination of transmit and receive differential pairs

- During FCC and ESD testing, remove all unused headers pins, jumpers, test point pins, etc. These parts will act as antennas and degrade the test results.