



# **KS8999 Demo Board User Guide**

## **KS8999 Integrated 9-port 10/100 Ethernet Switch with PHY and frame buffer**

Rev 1.1 June, 2002

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## Table of contents

1.0 Introduction.....	3
2.0 Features .....	3
3.0 Kit contents .....	3
4.0 Reference Documents .....	3
5.0 Hardware Description .....	4
5.1 Power-up .....	4
5.2 LED indicators .....	4
5.3 9-port 10/100 Ethernet Switch Set-up.....	4
5.4 Force mode configuration .....	6
5.5 MII and 7-wire Interface Setup.....	6
5.6 Power Requirement.....	8
6.0 Software Description.....	8
7.0 Bill of Material.....	8
8.0 ESD/PCB Reference Guideline .....	11
9.0 Appendix for block diagram and schematics.....	13

## List of Tables

Table 1 LED1, 2, 3, 4, 5, 6, 7, 8, and LED9 Indicators .....	4
Table 2 Feature setting jumpers.....	5
Table 3 MII and 7-wire mode jumper selection.....	7
Table 4 10/100BT and Full/Half duplex Jumper Selection .....	7
Table 5 PINOUT for the 40-Pin MII Interface .....	7

## Revision History

Revision	Date	Change
1.0	03/26/02	Preliminary release
1.1	06/07/02	Editorial changes; JP33 change to port 3, JP28 changes to duplex mode, table1 change to LED mode 0.

## 1.0 Introduction

The KS8999 demo board is designed to evaluate the performance of Micrel/Kendin 9-port integration switch with PHY and frame buffer. KS8999 is configured as standalone switch with 8 ports operating in 10Mbit/s or 100Mbit/s. All of the 8 ports are set up as auto negotiation as default.

The KS8999 demo board provides an industry standard MII (media independent Interface) to interface to external Processors for router and gateway applications.

For Advanced set up such as QoS and VLAN, please refer to the KS8999 datasheet.

This board is not intended for reference design or manufacturing. Please contact Micrel/Kendin FAE for consultation of layout and other advanced setup.

## 2.0 Features

- ✂✂ Micrel/ Kendin KS8999 integrated 9-port Ethernet 10/100 switch
- ✂✂ 8 RJ45 jacks for Ethernet LAN port
- ✂✂ 1 MII (media independent Interface) connector for router and gateway applications
- ✂✂ Micrel MIC29302BT Regulator to step down to 3.3v or 2.5v
- ✂✂ Three LED's per port to indicate the status and activities
- ✂✂ 5VDC, 2.5A Universal wall power supply
- ✂✂ All 8 ports support auto-MDI/MDIX cross over
- ✂✂ All ports support the 100FX fiber mode

## 3.0 Kit contents

The KS8999 Evaluation kit includes the following:

- ✂✂ KS8999 evaluation board
- ✂✂ +5V VDC Wall Power supply

## 4.0 Reference Documents

KS8999 Data Sheet (contact Micrel/Kendin for latest datasheet)

KS8999 schematics in OrCAD format

KS8999 Gerber file

KS8999 EEPROM Configuration software

MIC29302BT Datasheet (get the latest datasheet from [www.micrel.com](http://www.micrel.com))

## 5.0 Hardware Description

### 5.1 Power-up

Upon power up, the KS8999 will go through a series of LED -testing. LED will flash a few seconds.

### 5.2 LED indicators

There are three columns of LED indicators for port1, port2, port3, port4, port5, port6, port7, port8, and port9. Each row of LED is used to indicate the speed, duplex and traffic activities.

- D1 = LED1, indicates the activities on Port 1
- D2 = LED2, indicates the activities on Port 2
- D3 = LED3, indicates the activities on Port 3
- D4 = LED4, indicates the activities on Port 4
- D5 = LED5, indicates the activities on Port 5
- D6 = LED6, indicates the activities on Port 6
- D7 = LED7, indicates the activities on Port 7
- D8 = LED8, indicates the activities on Port 8
- D9 = LED9, indicates the activities on Port 9
- D10 = indicates 2.0V Power on and off
- D11 = indicates 3.3V Power on and off

The Demo board LED default setup is **MODE 0**:

**Table 1 LED1, 2, 3, 4, 5, 6, 7, 8, and LED9 Indicators**

<b>LED1, LED2, LED3, &amp; LED4</b>	<b>ON</b>	<b>OFF</b>	<b>Toggling</b>
Top Row	100 Base-T	10 Base-T	N/A
2 <sup>nd</sup> Middle Row	Full Duplex	Half Duplex	N/A
3 <sup>rd</sup> Middle Row	Collision	No Collision	N/A
Bottom Row	Link	No Link	Data receiving and transmitting

### 5.3 8-port 10/100 Ethernet Switch Set-up

## KS8999 Demo Board User Guide

9-port SOHO switch is set up as default and port 9 is set to 100BT & Full duplex as default. The data traffic can be connected through eight RJ45 connectors. Any of all 9 ports can be used as up link or down link. The 9<sup>th</sup> port will be required external PHY for using as 9-port SOHO switch. In the case of Up-link port, there is no need of using a cross-over cable since the KS8999 has auto MDI/MDIX cross-over feature.

**Table 2 Feature setting jumpers**

Jumper	Description	Open	Closed
JP1	N/A	Connect to 3.3V for VDD IO or 2.0V	
JP2	EN1P	Enable 802.1p selected by EEPROM	Enable 802.1p field for all port
JP3	PRSV	No priority reserve	Enable 6KB priority buffer reserved
JP4	CFGMODE	Enable EEPROM interface	Enable processor interface
JP5	CLKMODE	Reserved, factory test pin	
JP6	BIST	Reserved, factory test pin	
JP7	SWM	Reserved, factory test pin	
JP8, 9	MODESEL[0:1]	LED mode selection MODESEL[0:1] = 00 for LED mode 0 MODESEL[0:1] = 01 for LED mode 1 MODESEL[0:1] = 10 for LED mode 2 MODESEL[0:1] = 11 for LED mode 3	
JP10, 11	MIIS[0:1]	MII mode selections MIIS[0:1] = 00 for disable MII interface MIIS[0:1] = 01 for enable forward MII interface MIIS[0:1] = 10 for enable reverse MII interface MIIS[0:1] = 11 for enable SNI mode (7 wire interface)	
JP12	LED[1][0]	Enable auto negotiation port 4	Disable auto negotiation port 4
JP13	LED[2][0]	Enable auto negotiation port 8	Disable auto negotiation port 8
JP14	LED[3][0]	Force to 100BT on port 4	Force to 10BT on port 4
JP15	LED[4][0]	Force to 100BT on port 8	Force to 10BT on port 8
JP16	LED[1][1]	Enable auto negotiation port 3	Disable auto negotiation port 3
JP17	LED[2][1]	Enable auto negotiation port 7	Disable auto negotiation port 7
JP18	LED[3][1]	Force to 100BT on port 3	Force to 10BT on port 3
JP19	LED[4][1]	Force to 100BT on port 7	Force to 10BT on port 7
JP20	LED[1][2]	Enable auto negotiation port 2	Disable auto negotiation port 2
JP21	LED[2][2]	Enable auto negotiation port 6	Disable auto negotiation port 6
JP22	LED[3][2]	Force to 100BT on port 2	Force to 10BT on port 2
JP23	LED[4][2]	Force to 100BT on port 6	Force to 10BT on port 6
JP24	LED[1][3]	Enable auto negotiation port 1	Disable auto negotiation port 1
JP25	LED[2][3]	Enable auto negotiation port 5	Disable auto negotiation port 5
JP26	LED[3][3]	Force to 100BT on port 1	Force to 10BT on port 1
JP27	LED[4][3]	Force to 100BT on port 5	Force to 10BT on port 5
JP28	LED[5][0]	Force to half duplex on port 4	Force to full duplex on port 4
JP29	LED[6][0]	Reserved, factory test pin	
JP30	LED[7][0]	Reserved, factory test pin	
JP31	LED[8][0]	Enable half duplex back pressure	Disable half duplex back pressure
JP32	LED[9][0]	Force to half duplex on port 8	Force to full duplex on port 8
JP33	LED[5][1]	Force to half duplex on port 3	Force to full duplex on port 3
JP34	LED[6][1]	Reserved, factory test pin	
JP35	LED[7][1]	Share buffers up to 512 buffers on a	Enable equal amount of buffers per

		single port	port (113 buffers)
JP36	LED[8][1]	Reserved, factory test pin	
JP37	LED[9][1]	Force to half duplex on port 7	Force to full duplex on port 7
JP38	LED[5][2]	Force to half duplex on port 2	Force to full duplex on port 2
JP39	LED[6][2]	Continue sending frame regardless of number of collisions	Enable to drop frame after 16 collisions
JP40	LED[7][2]	Unlimited broadcast frames	Enable 5% broadcast frame allowed
JP41	LED[8][2]	Max length is 1536 byte	Enable enforce the max frame length for VLAN is 1522
JP42	LED[9][2]	Force to half duplex on port 6	Force to full duplex on port 6
JP43	LED[5][3]	Force to half duplex on port 1	Force to full duplex on port 1
JP44	LED[6][3]	Enable more aggressive back-off	Enable less aggressive back-off
JP45	LED[7][3]	Enable flow control	Disable flow control
JP46	LED[8][3]	Enable 5 minute aging	Disable aging
JP47	LED[9][3]	Force to half duplex on port 5	Force to full duplex on port 5
JP48	MRXD[0]	Reserved, factory test pin	
JP49	MRXD[1]	Disable flow control on port 9	Enable flow control on port 9
JP50	MRXD[2]	Force to half duplex on port 9	Force to half duplex on port 9
JP51	MRXD[3]	Force to 100BT on port 9	Force to 10BT on port 9
J6	N/A	Jumper on 2.0V	
J7	N/A	Jumper on 3.3V	
J8	N/A	connect to 3.3V for 1&2 and 2.5V for 2&3	

## 5.4 Force mode configuration

Port 1 through Port 8 are set up as auto-negotiation with Full Duplex mode. In this demo board, all ports can be configured as forced 10BT full/half or 100BT full/half duplex by the above jumpers. The below example is to show how to set the jumper to configured as forced 10BT full/half or 100BT full/half duplex.

Example) Port 1 configuration;

Disable auto negotiation = short JP24.

Forced 100BT/full duplex = NC JP26 and short JP43

Forced 100BT/half duplex = NC JP26 and JP43

Forced 10BT/full duplex = short JP26 and JP43

Forced 10BT/half duplex = short JP26 and NC JP43

## 5.5 MII and 7-wire Interface Setup

Micrel-Kendin 9 ports 10/100 integrated switch with 8 physical layer transceiver board you received is a multi functional board that can be configured for different interfaces. Port 9 can be configured as **Forward MII**, **Reverse MII** or **7-wire (SNI)** interface. The default of this board is configured as 8 ports switch. All ports have been set up for auto-negotiation enabled mode. Note that the port 9 has only the MAC interface and there is no PHY. Since MII/SNI interfaces do not support auto-negotiation, the user needs to set up the Full/Half duplex and 10/100speed using the following jumpers.

**Table 3 MII and 7-wire mode jumper selection**

Mode	JP10 jumper	JP11 jumper
Disable MII	Open	Open
Reverse MII	Short	Open
Forward MII	Open	Short
7-wire (SNI)	Short	Short

**Table 4 10/100BT and Full/Half duplex Jumper Selection**

Mode	JP50 jumper	JP51 jumper
100BT/Full duplex	Open	Open
100BT/Half duplex	Short	Open
10BT/Full duplex	Open	Short
10BT/Half duplex	Short	Short

(Note: SNI can only operate in 10BT mode).

1. Reverse MII mode (9<sup>th</sup> MAC act as a PHY), shown as a male MII connector (J4) on the demo board.
  - ✍✍ Enable Reverse MII mode by shorting JP10 jumper
  - ✍✍ Select 10/100BT or Full/Half duplex in table 3.
1. Forward MII mode (9<sup>th</sup> MAC acts as a MAC). The female MII connector (J5) is not installed on the demo board. It can be available upon request.
  - ✍✍ Enable forward MII mode by shorting JP11 jumper
  - ✍✍ Select 10/100BT or Full/Half duplex in table 3.
2. 7-wire (SNI) mode, shown as test point (TP1 – TP7) on the demo board
  - ✍✍ Enable 7-wire mode by shorting both JP10 and JP11 jumpers.
  - ✍✍ Select Full or Half duplex in table 3
  - ✍✍ Select 10BaseT mode only (note: 7-wire can only operate in 10BaseT mode) in table 3

The power supply for MII Interface I/O should be selected as 3.3V by short on JP1 (default). The pin1&19 VCC on the connector is the voltage supply from link partner, so the pin1 VCC can be 5V or 3.3V depends on link partner.

**Table 5 PINOUT for the 40-Pin MII Interface**

Pin	Signal	Pin	Signal
1	+5V	21	+5V
2	MDIO	22	Common
3	MDC	23	Common
4	RxD<3>	24	Common
5	RxD<2>	25	Common
6	RxD<1>	26	Common

7	RxD<0>	27	Common
8	Rx_DV	28	Common
9	Rx_CLK	29	Common
10	Rx_Er	30	Common
11	TX_Er	31	Common
12	Tx_CLK	32	Common
13	Tx_EN	33	Common
14	TxD<0>	34	Common
15	TxD<1>	35	Common
16	TxD<2>	36	Common
17	TxD<3>	37	Common
18	Col	38	Common
19	CRS	39	Common
20	+5V	40	+5V

## 5.6 Power Requirement

5V DC 2Amp at J3

## 6.0 Software Description

KS8999 is designed for unmanaged standalone operation via I/O strapping at system reset and there is no needed for any software driver or utility for basic operation.

However, we provide the sample DOS program software for EEPROM and CPU programming. Please contact Micrel FAE for support on software programs.

## 7.0 Bill of Material

KS8999 9-port Ethernet Switch Demo Board PCB Revised: 07/2001  
Revision: 3.1

Item	Quantity	Reference	Part
1	18	V2,QL2,QH2,DOUT2,BTOUT2, AOUT2,QL3,QH3,QL4,QH4, QL5,QH5,EN1P1,V2_0A,DOUT, DGND,AOUT,AGND	TP
2	21	TP1,TEST1,T1,RLPBK1,MUX1, TP2,TEST2,T2,MUX2,CTOUT2, TP3,TEST3,T3,TP4,T4,TP5, T5,TP6,TP7,CTOUT,BTOUT	TestPoint



## KS8999 Demo Board User Guide

3	54	C1,C2,C3,C6,C7,C8,C9,C10, 0.1UF C11,C13,C14,C15,C17,C18, C19,C20,C21,C22,C23,C24, C25,C26,C31,C32,C33,C34, C36,C37,C38,C39,C52,C55, C57,C58,C62,C63,C64,C65, C66,C67,C68,C69,C70,C72, C73,C74,C75,C76,C77,C78, C79,C82,C84,C85	
4	6	C4,C5,C16,C30,C35,C86	10uf
5	2	C41,C40	22PF
6	9	C42,C43,C44,C45,C46,C47, C48,C49,C59	1000PF/2KV
7	3	C50,C60,C80	22UF/16V
8	2	C51,C61	10NF
9	4	C53,C71,C81,C83	47UF/16V
10	8	C87,C88,C89,C90,C91,C92, C93,C94	1000pf
11	9	D1,D2,D3,D4,D5,D6,D7,D8, LEDx4 D9	
12	2	D10,D11	LED
13	1	D12	1N4148
14	1	D14	1N4004
15	5	FB1,FB4,FB6,FB7,FB8	FBEAD
16	1	JP1	HEADER 3
17	50	JP2,JP3,JP4,JP5,JP6,JP7, JP8,JP9,JP10,JP11,JP12, JP13,JP14,JP15,JP16,JP17, JP18,JP19,JP20,JP21,JP22, JP23,JP24,JP25,JP26,JP27, JP28,JP29,JP30,JP31,JP32, JP33,JP34,JP35,JP36,JP37, JP38,JP39,JP40,JP41,JP42, JP43,JP44,JP45,JP46,JP47, JP48,JP49,JP50,JP51	JUMPER
18	2	J2,J1	RJ45x4
19	1	J3	HEADER 3x1
20	1	J4	Male MII connector
21	1	J5	Female MII connector
22	3	5V,J6,J7	HEADER 2
23	1	J8	CON3
24	1	OSC1	66M Hz
25	1	P1	CONNECTOR DB25
26	9	RN1,RN2,RN3,RN4,RN5,RN6, RN7,RN8,RN9	330
27	42	R1,R4,R5,R6,R7,R8,R9,R12,	1K

## KS8999 Demo Board User Guide

		R13,R15,R51,R52,R53,R54, R55,R56,R57,R58,R59,R61, R62,R63,R65,R95,R96,R97, R98,R100,R101,R102,R103, R106,R107,R110,R111,R112, R113,R133,R174,R175,R176, R177	
28	2	R3,R2 47K	
29	16	R10,R11,R14,R16,R18,R19, 10K R20,R151,R153,R154,R197, R199,R202,R203,R204,R205	
30	1	R17 3K	
31	1	R21 500K	
32	8	R22,R29,R36,R43,R66,R73, 75 R80,R87	
33	48	R23,R24,R25,R26,R27,R28, 51 R30,R31,R32,R33,R34,R35, R37,R38,R39,R40,R41,R42, R44,R45,R46,R47,R48,R49, R67,R68,R69,R70,R71,R72, R74,R75,R76,R77,R78,R79, R81,R82,R83,R84,R85,R86, R88,R89,R90,R91,R92,R93	
34	9	R50,R60,R64,R94,R99,R104, R105,R108,R109	1K
35	2	R114,R116 49.9 1%	
36	30	R115,R117,R118,R119,R120, R121,R122,R123,R124,R125, R126,R127,R128,R129,R130, R131,R134,R135,R136,R137, R139,R140,R141,R142,R143, R144,R145,R146,R147,R148	49.9 1%
37	1	R132 220	
38	1	R138 1.8K	
39	1	R149 2.4K	
40	1	R150 R	
41	2	R201,R152 1.5K	
42	19	R155,R156,R157,R158,R159, R160,R161,R162,R163,R164, R165,R166,R167,R168,R169, R170,R171,R172,R173	49.9
43	1	R178 10	
44	2	R200,R198 1K(NC)	
45	1	S1 SW PUSHBUTTON	
46	2	T7,T6 H1164	
47	1	U1 74F125	

48	1	U2	AT24C02
49	1	U3	KS8999_208
50	2	U4,U5	MIC29302BT
51	1	Y1	25 Mhz

## 8.0 ESD/PCB Reference Guideline

ESD and EMI (FCC) are basically the same problem for the system design. ESD is absorbing energy and EMI is emitting energy. If your PC board is good in EMI, it is also has good ESD proof.

All high speed signal must has a unbroken reference ground plane.

Minimum 6 layer PCB is recommended, the layer stacking could be as following:

_____	layer 1 component side (short traces)	1 oz copper
_____	layer 2 power plane	2 oz copper
_____	layer 3 GND plane	2 oz copper
_____	layer 4 signal	5 mil trace /10 mil spacing 1 oz copper
_____	layer 5 signal	5 mil trace /10 mil spacing 1 oz copper
_____	layer 6 GND	signal 1 oz copper

Differential pair is 5mil trace/5mil spacing.

So very few signal traces are exposed to outside, except the short traces from device pins to internal layers. It will improve ESD, EMI and signal integrity.

4 layer PCB is not recommended but if that is the only option, use the following layer stacking:

_____	layer 1 component side	1 oz copper
_____5mil_____	layer 2 GND plane	1 oz copper
_____	layer 3 power plane	1 oz copper
_____5mil_____	layer 4 signal	oz copper

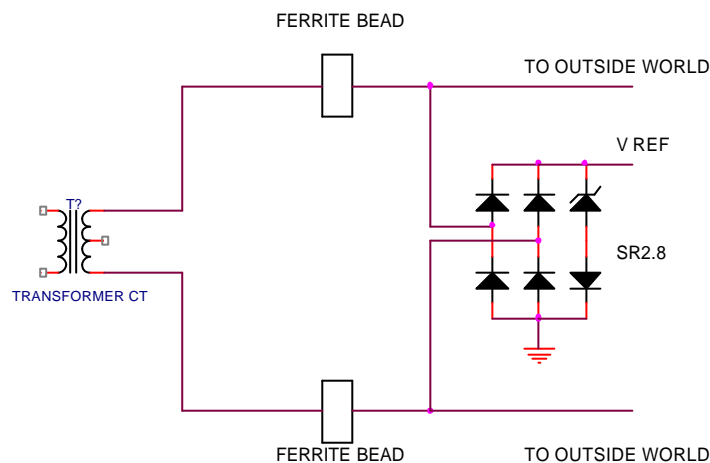
The thickness between layer 1 and 2 is 5mil, the thickness between layer 3 and 4 is 5 mil.

The following are the PCB layout guideline:

1. Keep Transmit differential pair on component side and Receive pairs on other layer, and route the differential pairs close together 5mil/5mil space (parallel) and minimum 20 mil away from other signals.
2. Route Clock traces directly above unbroken Ground plane and keep 2X trace width away from other signal traces. Add damping resistor (33 to 50 OHM) at Clock output.
3. Keep all signal traces inside the unbroken ground plane (in different layer).
4. The ground nets are all common.
5. Void power and ground planes directly under the magnetic.

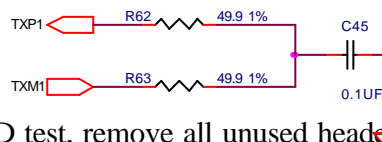
## KS8999 Demo Board User Guide

6. Use bulk capacitors 47uf to 100uf between power and ground plane on each corner of MICREL/KENDIN chip.
7. Each power pin should have a 0.1uf de-coupling cap close to the power pin, and drop via near the cap side.
8. Broke the ground loop in certain location to avoid loop antenna effect.
9. Poorly regulated or over-burdened power supply will generate digital switching noise. Increase power traces width (60mil min.) or use copper pour whenever possible. A minimum 220uF (470uF is recommended) capacitor should be used in the main DC outputs (3.3V, 2.5V 2.0V etc).
10. Add damping resistors at all high speed digital signals and clock traces. The resistor should be located near the source side.
11. Metal case should be connected to chassis ground and at least 50 mil away from any signal traces. The chassis ground should be isolated from the rest of the circuitry.
12. Fill up the unused area on top and bottom side of the PCB with GND plane.
13. Add TVS transient suppression device at the I/O. The device is placed in parallel with the line to be protected.



Protek Devices SR2.8 low capacitance TVS  
[www.protek.tvs.com](http://www.protek.tvs.com)

14. All unused inputs are connected to ground or power with a 1K resistor or 1K to VDD and 1K to ground for floating inputs.
15. Place the RX and TX terminators (50 or 100 ohm resistors) close to the Micrel/Kendin Chip.

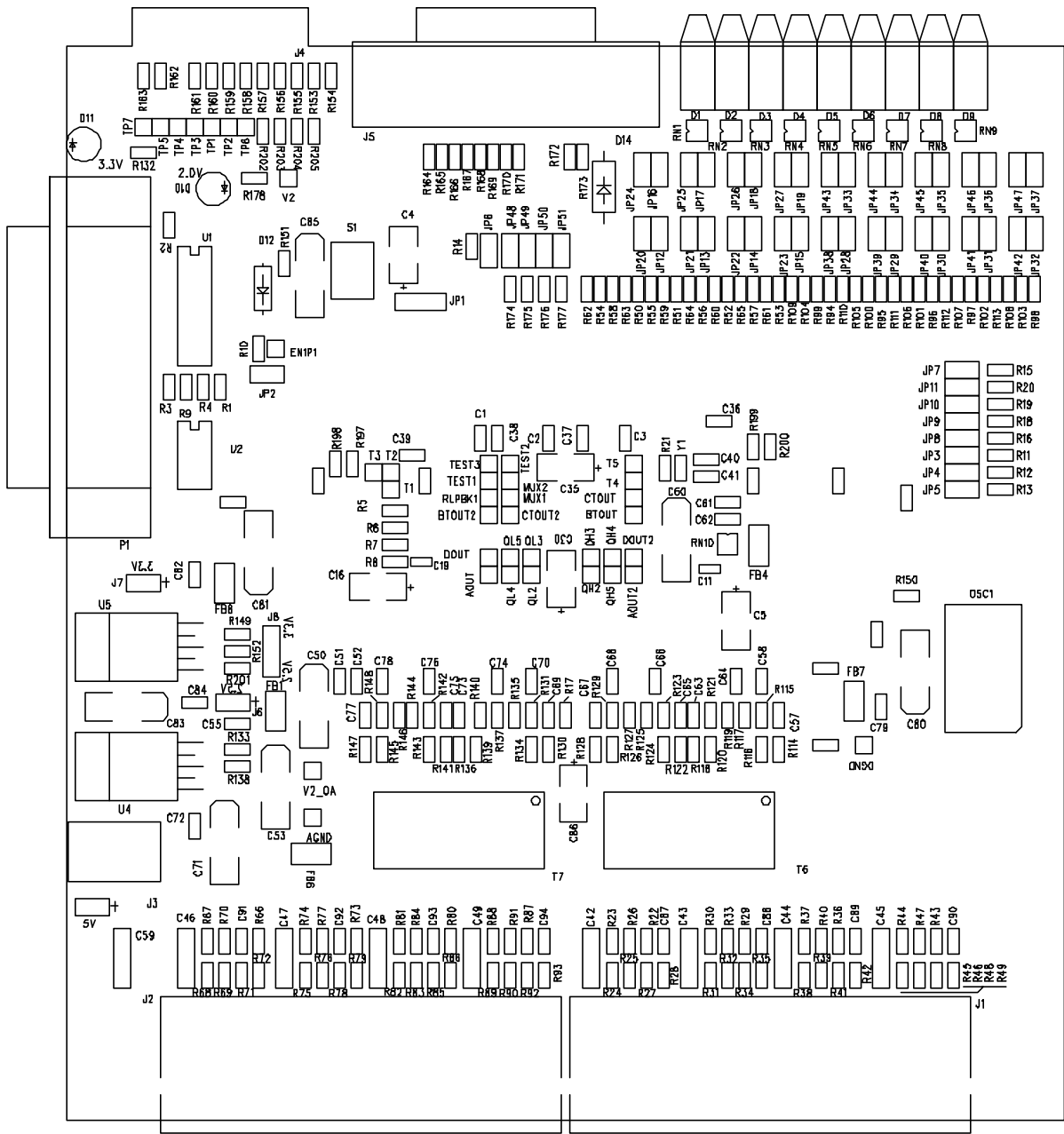


16. During FCC or ESD test, remove all unused headers pins, jumpers, test point pins etc. These parts will act as antenna.

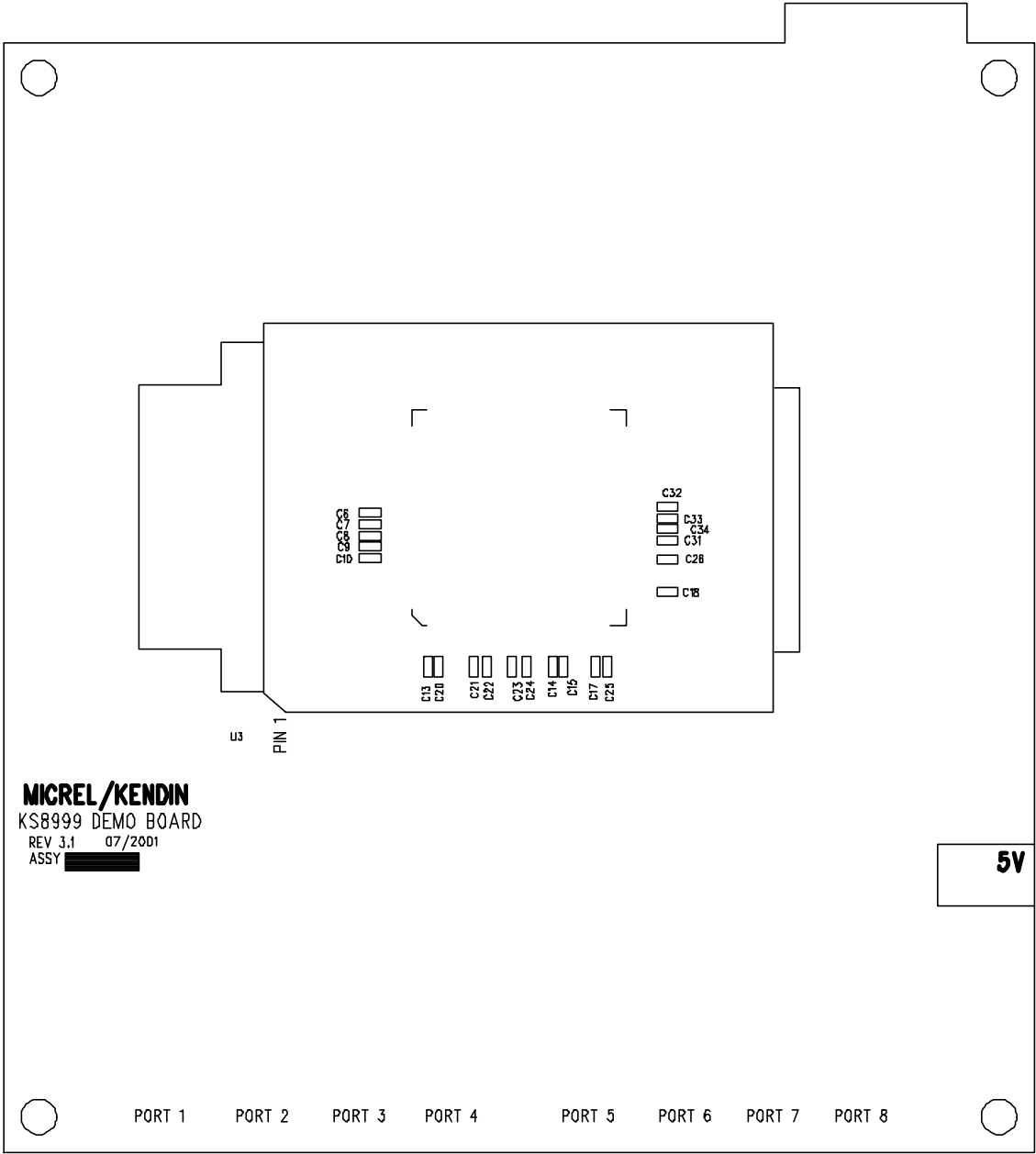
## 9.0 Appendix for block diagram and schematics

See the following pages for the below documents:

1. KS8999 Demo Board Block Diagram
2. Board Schematics Rev 3.3
3. PQFP208 package outline drawing



2IKSCREEN BOTTOM  
K28000 DEMO BOARD REV 3.1



KS8999 DEMO BOARD REV 3.1

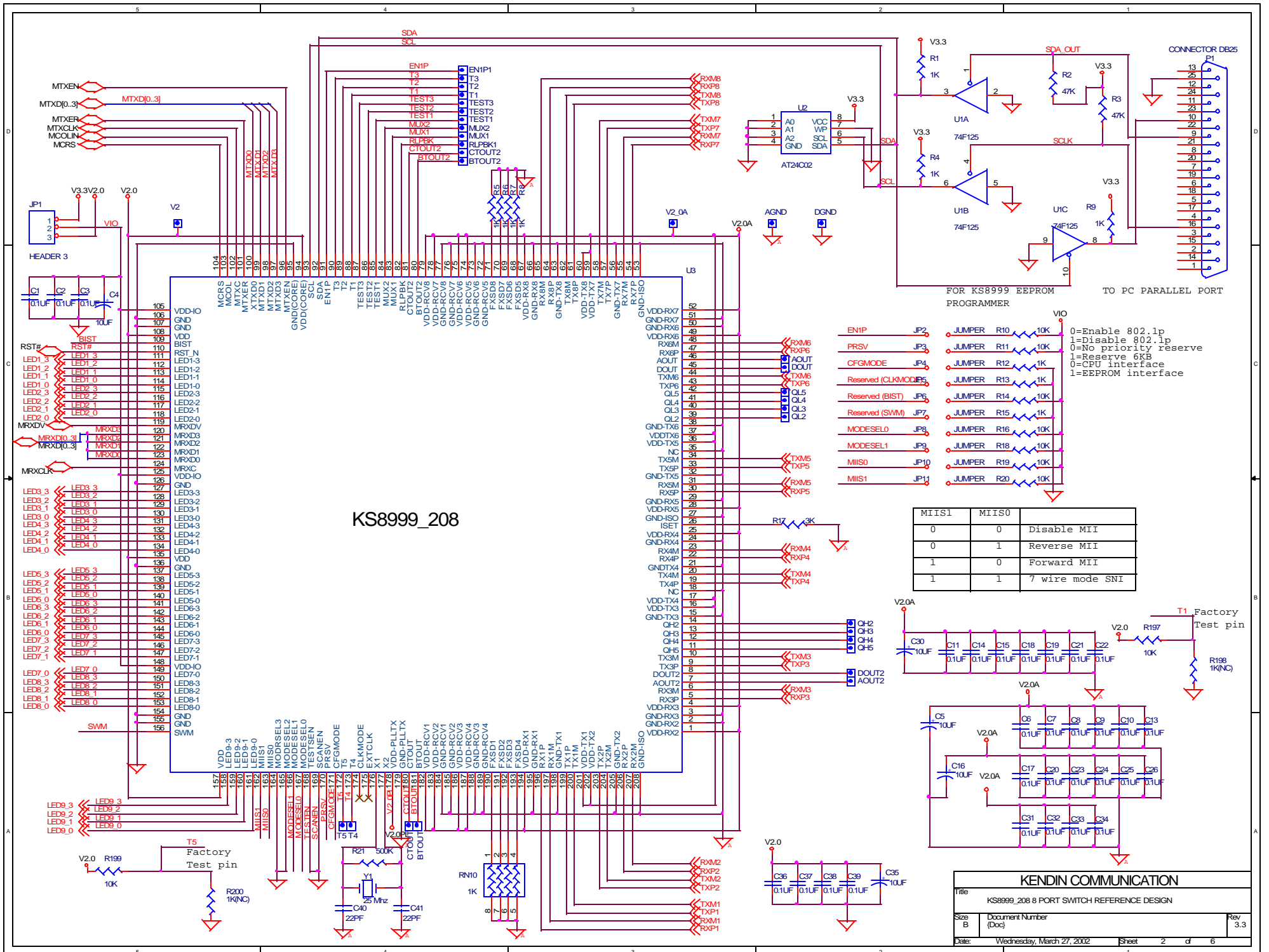
SILKSCREEN TOP

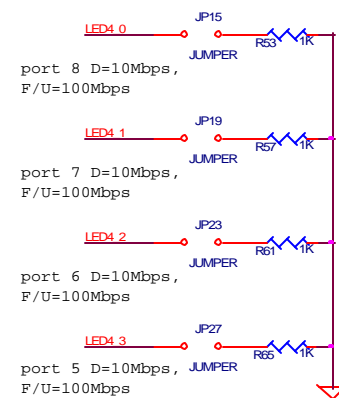
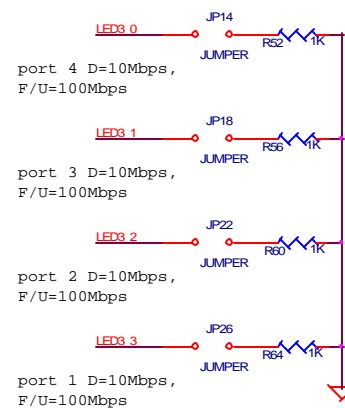
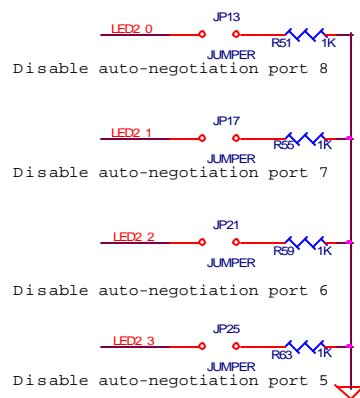
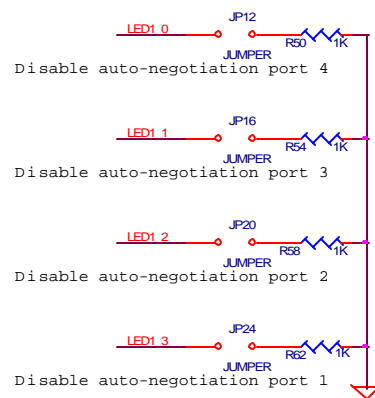
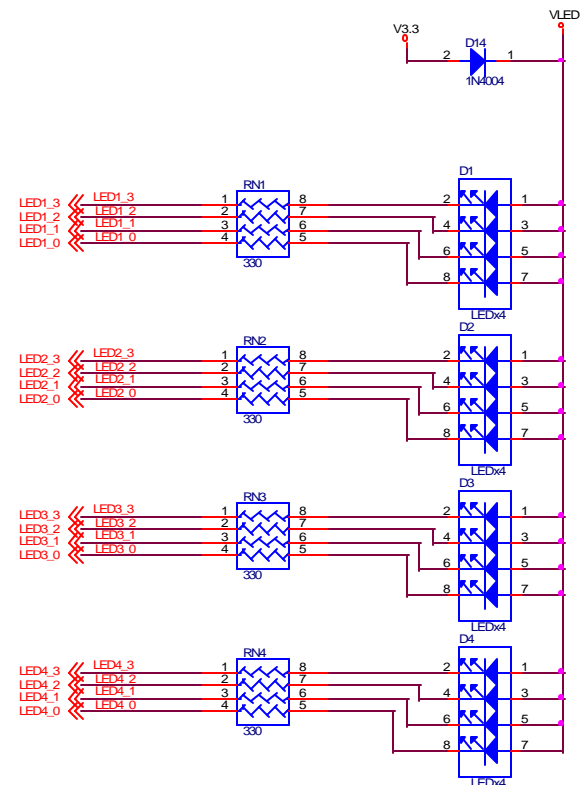
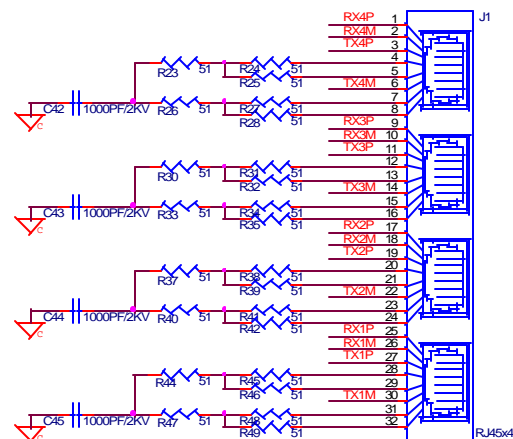
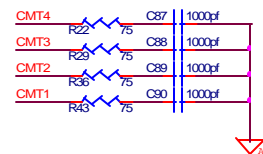
REVISION HISTORY

DATE:	DESCRIPTION	REVISION
3/15/01	ADD D13,D14,R179,C86	2.0
6/18/01	DELETE D13,R179,R180-187,R188-195 RENAME V1.8A TO V2.0A RENAME VDDTX TO V2.0A RENAME V1.8 TO V2.0 CONNECT T6,T7 ALL CT TO V2.0A ADD 3.3V AND 2.5V OPTION FOR VIO	3.0
6/25/01	REPLACE U4,5 WITH MIC29302BT ADD 3.3/2.5V OPTIONS FOR VIO ADD MRXD0-3 10K PULL UP R202-205 ADD KS8999 T1, T5 PULL UP OPTION	3.1
7/25/01	JOIN MCOL AND MCOLIN (P.6)	3.2
3/26/02	REMOVE PORT TRUNKING TABLE REMOVE OSC1 TO 66MHz ADD NO CONNECTION ON PIN 174 & 175 RENAME LED8_1 TO RESERVED	3.3

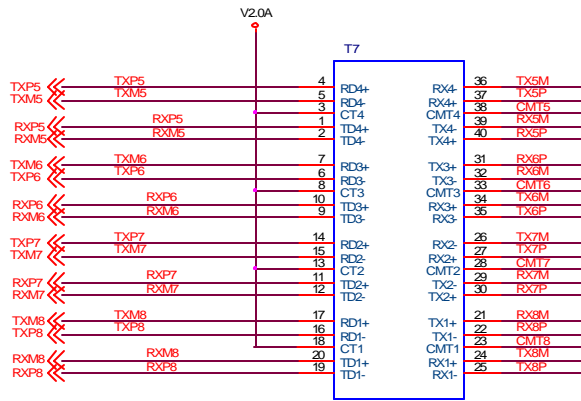


# KS8999\_208

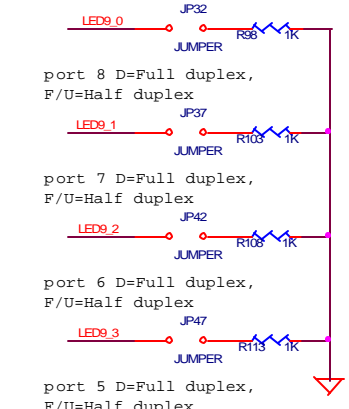
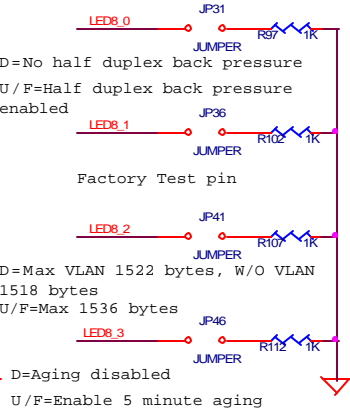
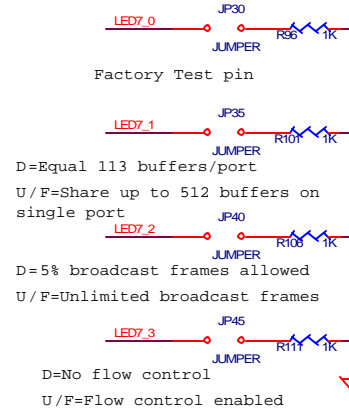
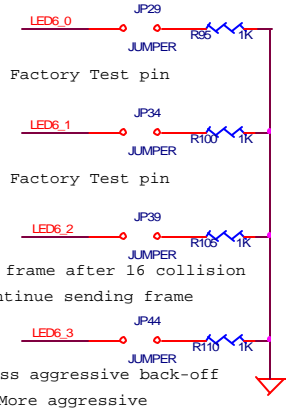
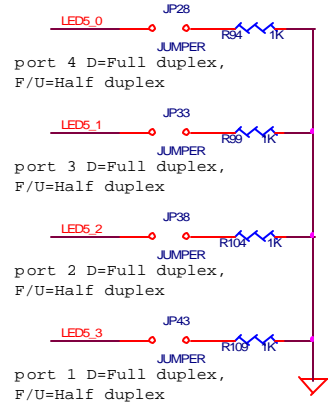
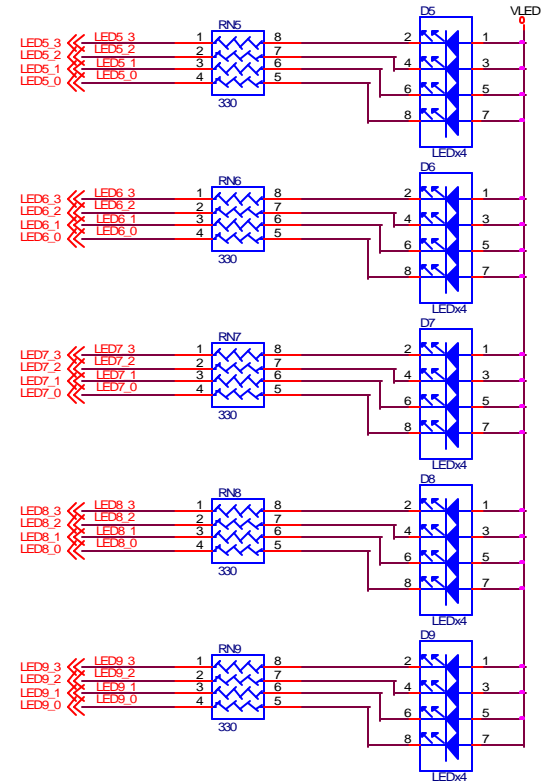
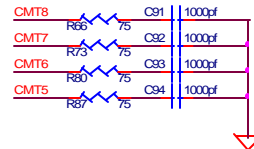
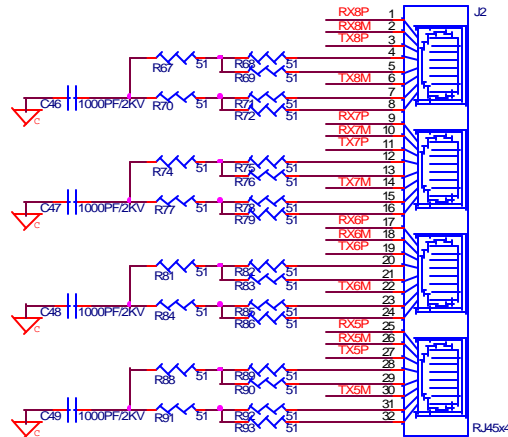




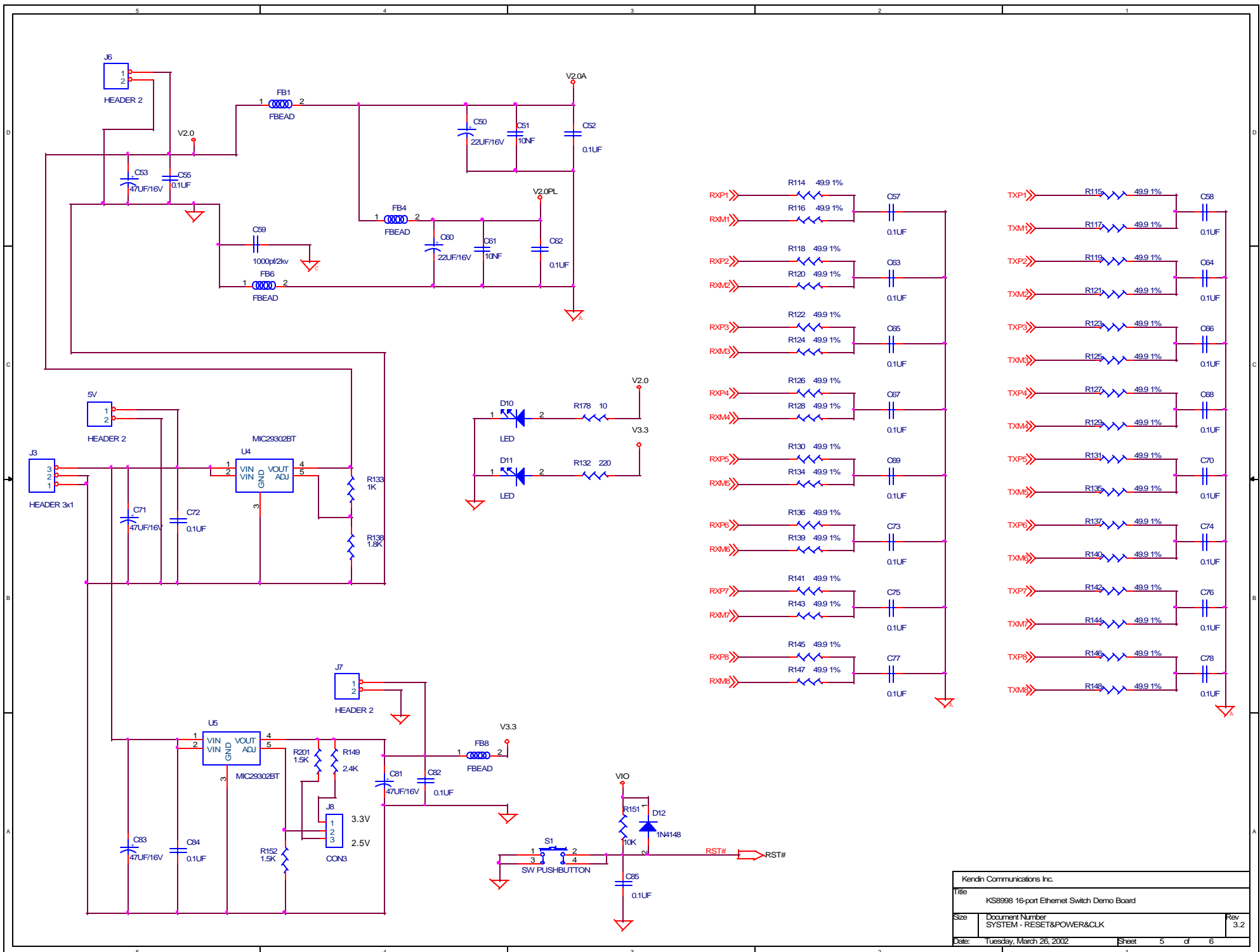
Kindin Communications Inc.			
Title KS8999 8-port Ethernet Switch Demo Board			
Size	Document Number SWTCH_1 - PHY_TRANSCEIVER_TRANSFORMER1	Rev 3.2	
Date:	Wednesday, March 27, 2002	Sheet	3 of 6

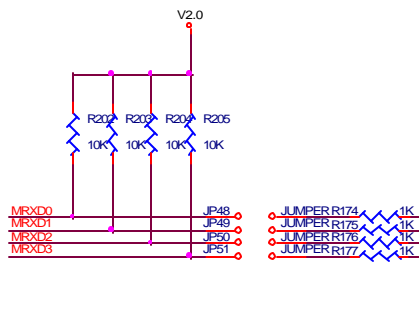
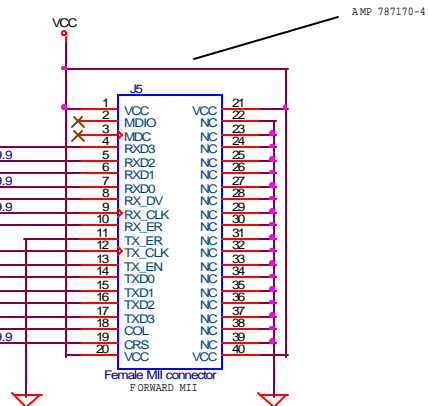
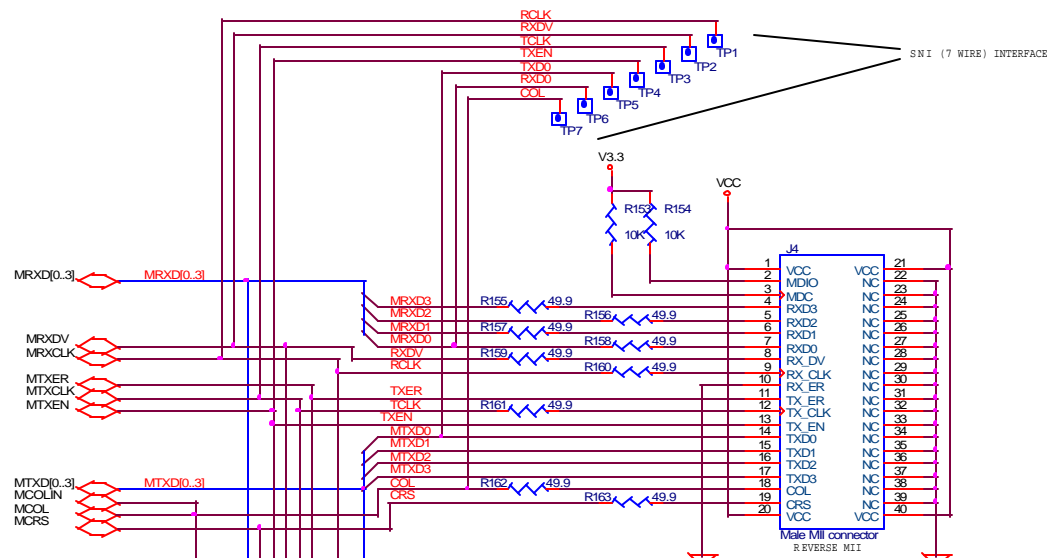


Pulse H1164  
 Bel Fuse 558-5999-Q9  
 YCL PH406466  
 Transpower HB826-2  
 DELTA LF8731

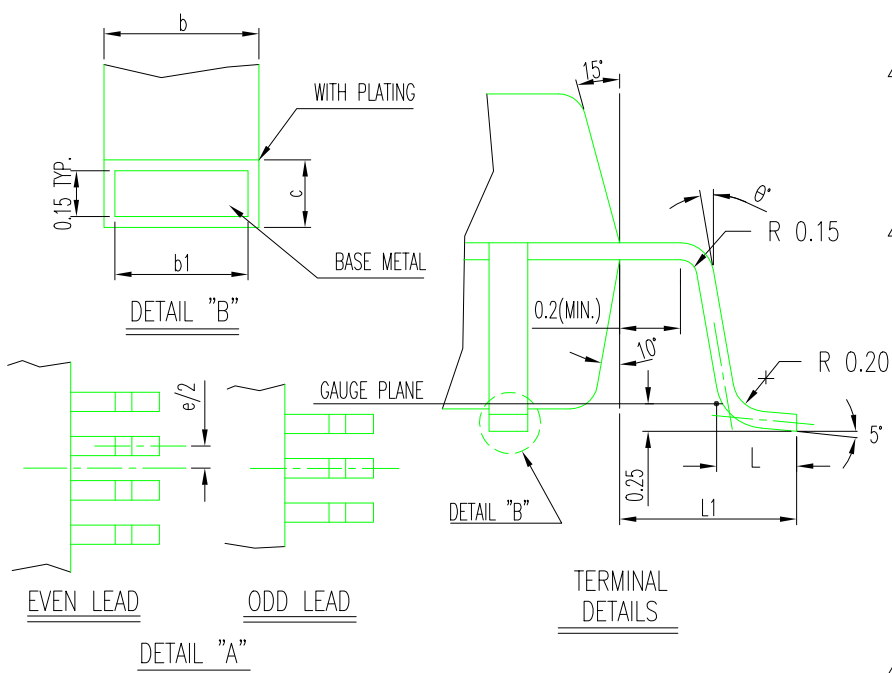
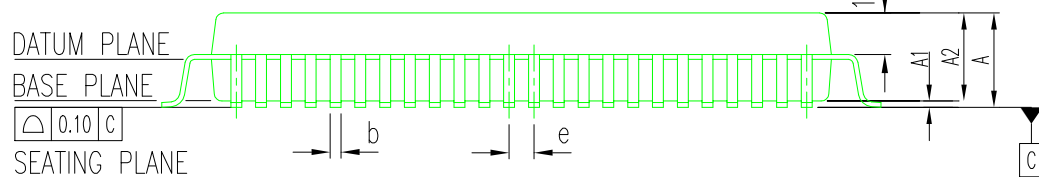
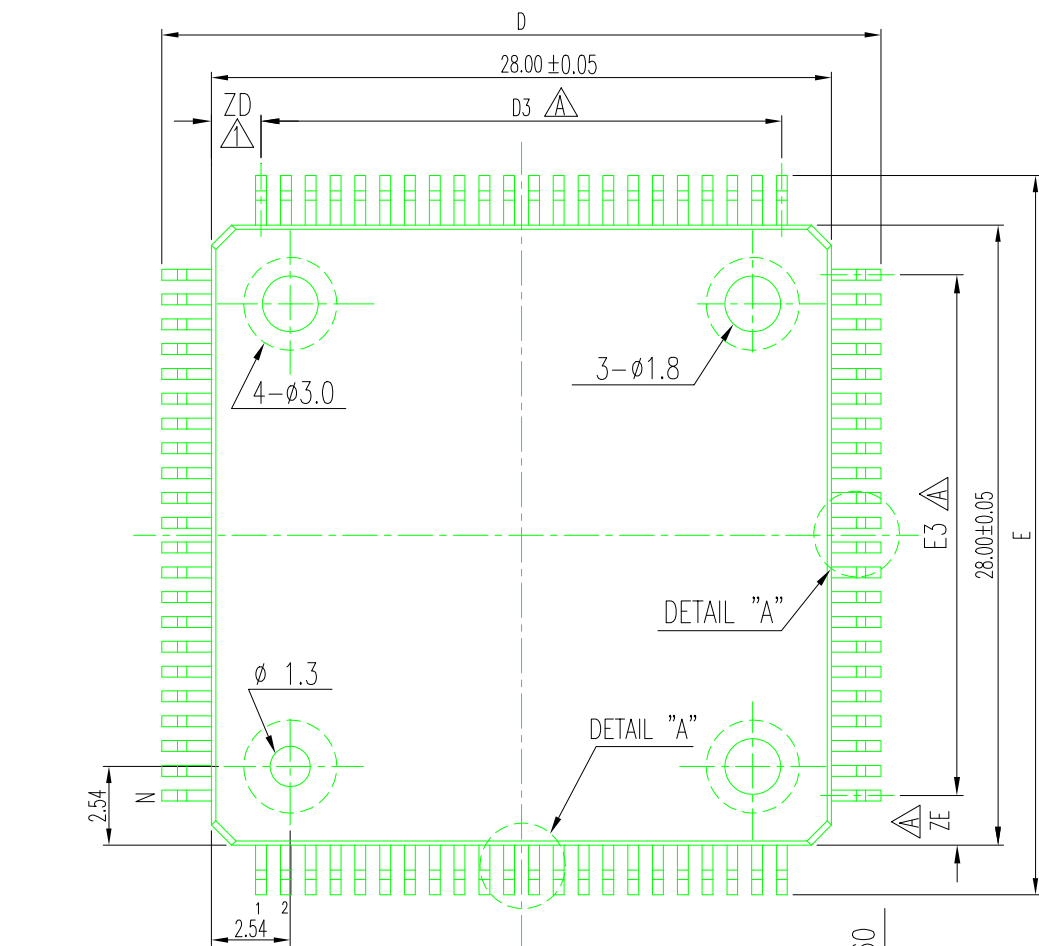


\* U/F=default







MRXD1	Port 9 D=Flow control Port 9 U=No flow control
MRXD2	Port 9 D=Half duplex Port 9 U=Full duplex
MRXD3	Port 9 D=10Mbps Port 9 U=100Mbps



	△	△		
DETAIL "A"	EVEN	EVEN	EVEN	EVEN
b ±0.05	0.32	0.22	0.18	0.18
c ±0.10	0.20	0.20	0.20	0.20
b1 ±0.03	0.30	0.20	0.16	0.16
e ±0.05	0.65	0.50	0.40	0.40
L1 ±0.10	1.60	1.30	1.30	1.30
L ±0.10	0.87	0.58	0.58	0.58
ZE (REF.)	1.33	1.25	1.40	2.20
E3 (REF.)	25.35	25.50	25.20	23.60
E ±0.2	31.2	30.6	30.6	30.6
ZD (REF.)	1.33	1.25	1.40	2.20
D3 (REF.)	25.35	25.50	25.20	23.60
D ±0.2	31.2	30.6	30.6	30.6
A2 ±0.05	3.35	3.35	3.35	3.35
A1 ±0.10	0.35	0.35	0.35	0.35
A (MAX.)	3.80	3.80	3.80	3.80
N	160L	208L	256L	240L
JEDEC		MQ-029AMS-029A FA-1	FB-1	—

UNLESS OTHERWISE SPECIFIED	DECIMAL .X ± .XX ±.10 .XXX ±.05	ANGULAR ±3°	THIRD ANGLE PROJECTION : 		 華泰電子股份有限公司 ORIENT SEMICONDUCTOR ELECTRONICS <i>A partner you can count on</i>				
DRAWN	Clare Chou 2000.10.16		UNIT: mm	SCALE: 4:1	TITLE:  Package outline dimension drawing for QFP(QUAD FLAT PACK)28X28mm family				
CHECKED			JEDEC NO.: MS-029A						
APPROVED			PACKAGE CODE : P4BB						
APPROVED			DWG NO. : PD-P4BB	REV.: B	DOC NO.: PD-P405	REV.: B	SHEET :	1	A3