IS32LT3147

SIX-CHANNEL LINEAR LED DRIVER WITH THERMAL SHUNT AND INDIVIDUAL PWM DIMMING

March 2022

GENERAL DESCRIPTION

The IS32LT3147 is a six-channel linear LED driver supporting a thermal shunt resistor for power dissipation to minimize the device thermal stress. Each channel has its own individual PWM control input. For added system reliability, the IS32LT3147 integrates fault detection circuitry for LED open/short circuit, single LED short circuit, thermal roll-off and thermal shutdown conditions. The FAULTB is a bi-directional open drain pin for reporting fault conditions and receiving system fault signal inputs. The FMODE pin configures the type of response to a fault signal, either “One Fail Other On” or “One Fail All Fail”.

The IS32LT3147 device is available in an eTSSOP-20 package with exposed pad for enhanced thermal dissipation.

APPLICATIONS

- Sequential turn light
- Welcome light
- Rear light
- Stop or taillight
- Interior lighting

FEATURES

- Wide input voltage range: 5V~40V
- Thermal shunt resistor to optimize the device thermal stress
- 6-CH current source driver
- Parallel outputs for higher current using multiple channels of a single IC or multiple ICs
- Individual PWM dimming to each channel
- Adjustable constant output current set by reference resistor
  - Max. current: 75mA per channel
  - Max. current: 450mA in Parallel Operation
- Low headroom voltage
  - Max. headroom: 500mV at 25mA per channel
  - Max. headroom: 900mV at 75mA per channel
- Robust fault protection with reporting:
  - Fault modes selectable: “one fails all fail” or “one fails other on”
  - Single LED short - single resistor to set the detection threshold
  - LED string open/short
  - Current setting pin (ISET) open/short
  - Thermal shutdown
  - External UVLO setting for single LED short and LED string open detection
  - FAULTB pin for failure reporting, allowing parallel bus connection
- Current slew rate control to optimize EMI performance
- Thermal roll-off – over junction temperature current derating
- Operating junction temperature range -40°C to 150°C
- AEC-Q100 Qualified

TYPICAL APPLICATION CIRCUIT

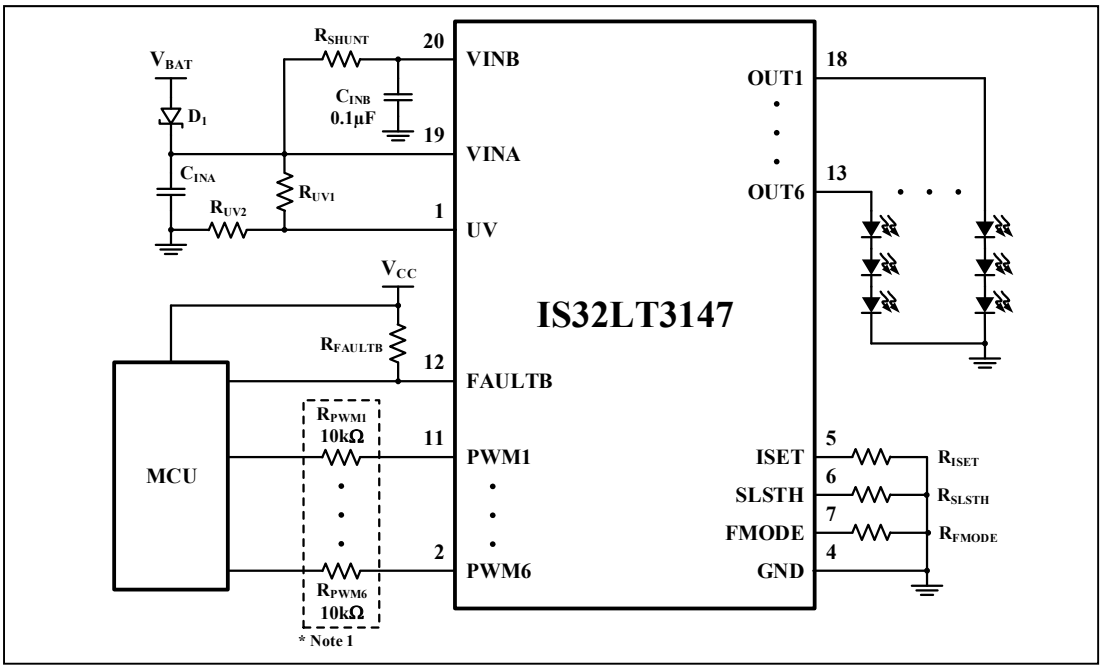
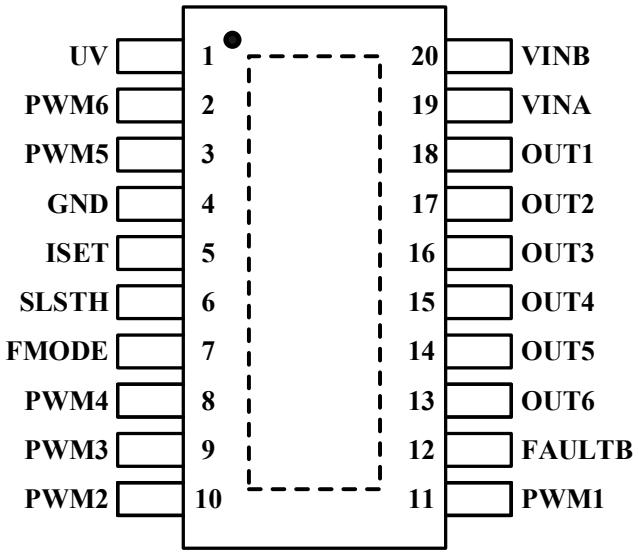


Figure 1 Typical Application Circuit

Note 1: The R_{PWM1}~R_{PWM6} resistors must always be installed to prevent the current flowing into the PWMx pins. Recommended value is 10kΩ.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-20	

PIN DESCRIPTION

No.	Pin	Description
1	UV	With an external resistor divider, it can set external UVLO for LED string open and single LED short fault detection.
2, 3	PWM6, PWM5	PWM dimming pin to OUT6 and OUT5. Pulling all PWM1~PWM6 pins low for >t_{SD} will force the device into shutdown mode.
4	GND	Ground pin.
5	ISET	Resistor on this pin to GND sets the maximum output current for channel OUT1~OUT6.
6	SLSTH	Single LED short detection voltage setting pin. Connect a resistor to ground to set.
7	FMODE	Fault action modes select pin. Connect a proper value resistor to ground to select.
8~11	PMW4~ PWM1	PWM dimming pin to OUT4~OUT1. Pulling all PWM1~PWM6 pins low for >t_{SD} will force the device into shutdown mode.
12	FAULTB	Open drain I/O diagnostic pin. Active low output driven by the device when it detects a fault condition. As an input (R_{FMODE}=0Ω or 27kΩ), this pin will accept an externally generated FAULTB signal to disable the device output to satisfy the “One-Fail-All-Fail” function. Note this pin requires an external pull up resistor (R_{FAULTB}).
13~18	OUT6~ OUT1	Current output pin. Connect the anode of the LED string to this pin and cathode to GND.
19	VINA	Power supply pin.
20	VINB	Thermal shunt pin. Connect a power resistor from VINA to this pin to shunt the power dissipation on the device.
	Thermal Pad	Must be connected to GND with sufficient copper for heat sink.

ORDERING INFORMATION
Automotive Range: -40°C to +125°C

Order Part No.	Package	QTY/Reel
IS32LT3147-ZLA3-TR	eTSSOP-20, Lead-free	2500

ABSOLUTE MAXIMUM RATINGS (NOTE 2)

Voltage at VINA and VINB pins	-0.3V ~ +45V
Voltage at UV, PWM1~PWM6, FAULTB and OUT1~OUT6 pins	-0.3V ~ V_{INA}+0.3V
Voltage at ISET, SLSTH and FMODE pins	-0.3V ~ +7V
Operating temperature, T_A=T_J	-40°C ~ +150°C
Storage temperature, T_{STG}	-65°C ~ +150°C
Junction temperature, T_{JMAX}	+150°C
Package thermal resistance, junction to ambient (4-layer standard test PCB based on JESD 51-2A), θ_{JA}	31.8°C/W
Package thermal resistance, junction to thermal PAD (4-layer standard test PCB based on JESD 51-8), θ_{JP}	14.46°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 2: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

Valid at V_{INA}= 12V, unless noted otherwise. Refer to each condition description.
"●" symbol indicates specifications across the full operating temperature range with T_A= T_J= -40°C to +150°C, other specifications are at T_A= T_J= 25°C; unless noted otherwise. (Note 4)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
Input Supply							
V_{INA}	Operating input voltage range		●	5.0		40	V
V_{INA_UV}	V_{INA} undervoltage release	Voltage rising	●		4.7	4.9	V
V_{INA_UVHY}	V_{INA} undervoltage-lockout hysteresis	IC disabled			280		mV
I_{IN}	Quiescent current (I_{VINA}+I_{VINB})	PWMx=High, R_{ISET}=6.2kΩ, FAULTB=High	●	5	7	9	mA
I_{SD}	Shutdown current (I_{VINA}+I_{VINB})	PWMx=Low longer than t_{SD}	●	50	85	120	μA
I_{FAULT}	Shutdown current in fault mode (I_{VINA}+I_{VINB})	R_{FMODE}=0Ω, one fail all fail mode, FAULTB=Low	●	1.4	2.2	3	mA
t_{ON}	Startup time from VIN rising edge to current rising edge after first power-up	All PWM pins tied to VINA			110	200	μs
Current Regulation							
I_{OUT_R}	Output current range per channel			-75		-10	mA
V_{ISET}	ISET pin reference voltage				1.15		V
I_{OUT}	Output current per channel	R_{ISET}=6.2kΩ, VINA=VINB, (V_{INA}-V_{OUT})=1.5V	●	-81	-75	-69	mA
		R_{ISET}=18.6kΩ, VINA=VINB, (V_{INA}-V_{OUT})=1.5V	●	-28	-25	-22	
E_{OUT_M}	OUT1~OUT6 current matching in one device	R_{ISET}=6.2kΩ	●	-6		6	%
		R_{ISET}=18.6kΩ	●	-12		12	
I_{OUT_L}	Output current limit	ISET shorted to GND	●	-150	-112	-85	mA
V_{HR_MIN}	Minimum headroom voltage from VINA to OUTx (VINB pin tied to VINA pin)	Measured at (V_{INA}-V_{OUTx}), R_{ISET}=6.2kΩ	●			900	mV
		Measured at (V_{INA}-V_{OUTx}), R_{ISET}=18.6kΩ	●			500	

ELECTRICAL CHARACTERISTICS (CONTINUE)

Valid at V_{INA}= 12V, unless noted otherwise. Refer to each condition description.

"●" symbol indicates specifications across the full operating temperature range with T_A= T_J= -40°C to +150°C, other specifications are at T_A= T_J= 25°C; unless noted otherwise. (Note 4)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
t_{SL}	Current rising/falling slew time (rising from 10% to 90% levels and falling from 90% to 10% levels)	R_{ISET}=6.2kΩ	●	6	16	38	μs
		R_{ISET}=18.6kΩ	●	3	13	23	
V_{ABTR}	The voltage threshold of current full transition from VINA to VINB	R_{ISET}=6.2kΩ, measured at (V_{INB}-V_{OUT_MAX})			1.1		V
t_{ABTR}	The period time of 85% current full transition from VINA to VINB	R_{ISET}=6.2kΩ			600		μs
Input and Output							
V_{IL}	PWMx and FAULTB pins input low voltage	Below V_{IL} level, input voltage considered as logic LOW	●			0.7	V
V_{IH}	PWMx and FAULTB pins input high voltage	Above V_{IH} level, input voltage considered as logic HIGH	●	2.3			V
I_{PD}	PWMx pins internal pull-down current	Pin connected to 12V	●	4	7	15	μA
f_{PWM}	Recommended PWM frequency at PWM pin	(Note 3)				1	kHz
t_{PWM_RD}	Delay time of PWM rising edge to 10% output current	R_{ISET}=6.2kΩ	●	10	20	30	μs
t_{PWM_FD}	Delay time of PWM falling edge to 90% output current	R_{ISET}=6.2kΩ	●	15	25	35	μs
t_{SD}	Duration time all PWM pins kept low to shutdown device		●	55	68	80	ms
V_{OL_FLTB}	FAULTB pin output voltage	I_{SINK}=1mA	●		0.1	0.4	V
V_{UVTH}	UV pin threshold voltage	Voltage rising	●	1.13	1.24	1.35	V
V_{UVTH_HY}	UV pin threshold voltage hysteresis		●		30		mV
Protection							
I_{FMODE}	FMODE pin output current		●		30		μA
R_{FMODE1}	FMODE pin resistance range for fault action mode 1		●		0	100	Ω
R_{FMODE2}	FMODE pin resistance range for fault action mode 2		●	24	27	30	kΩ
R_{FMODE3}	FMODE pin resistance range for fault action mode 3		●	58	62	66	kΩ
R_{FMODE4}	FMODE pin resistance range for fault action mode 4		●	140	150	160	kΩ

ELECTRICAL CHARACTERISTICS (CONTINUE)

Valid at V_{INA}= 12V, unless noted otherwise. Refer to each condition description.

"●" symbol indicates specifications across the full operating temperature range with T_A= T_J= -40°C to +150°C, other specifications are at T_A= T_J= 25°C; unless noted otherwise. (Note 4)

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
R_{ISET_OC}	Maximum R_{ISET} of ISET pin open circuit detection	Monitor FAULTB pin low	●	300			kΩ
R_{ISET_SC}	Minimum R_{ISET} of ISET pin short circuit detection	Monitor FAULTB pin low	●			1	kΩ
t_{FBDT}	ISET pin open/short detection deglitch time		●		40		μs
V_{SCV}	LED string short detection voltage	Voltage falling, measured at OUTx to GND	●	0.8	1	1.2	V
V_{SCV_HY}	LED string short detection voltage hysteresis	Measured at OUTx to GND	●		210		mV
I_{RTR}	Fault retry current		●		4		mA
V_{OCV}	LED string open fault detection voltage	V_{UV}>V_{UVTH}, measured at (V_{INB}-V_{OUTx}), voltage falling	●	29	40	49	mV
V_{OCV_HY}	LED string open fault detection voltage hysteresis	V_{UV}>V_{UVTH}, measured at (V_{INB}-V_{OUTx}), voltage rising	●		20		mV
I_{SLSTH}	SLSTH pin output current		●	30	32	34	μA
V_{SLSTH_RG}	Maximum voltage threshold of single LED short detection	(Note 3)				8.5	V
V_{SLSTH}	Single LED short detection voltage	Voltage falling, R_{SLSTH}=30kΩ	●	2.64	2.88	3.09	V
		Voltage falling, R_{SLSTH}=51kΩ	●	4.546	4.896	5.2	
V_{SLSTH_HY}	Single LED short detection voltage hysteresis		●		100		mV
t_{FBDEL}	LED string open/short and single LED short fault reporting delay time	No PWM dimming	●		2.8		ms
		PWM dimming	●		8		PWM cycles
T_{RO}	Thermal roll-off activation temperature	(Note 3)			150		°C
T_{SD}	Over temperature shutdown	Temperature increasing (Note 3)			175		°C
T_{SDHY}	Over temperature hysteresis	Recovery= T_{SD} -T_{SDHY} (Note 3)			20		°C

Note 3: Guaranteed by design.

Note 4: Limits are 100% production tested at -40ºC, 25ºC and 125ºC. Limits over the full operating temperature range verified through either bench and/or tester testing and correlation using Statistical methods.

TYPICAL PERFORMANCE CHARACTERISTICS

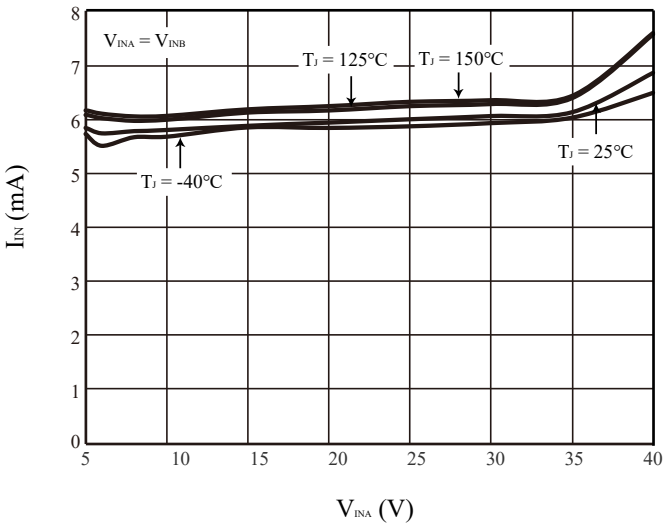


Figure 2 I_{IN} vs. V_{INA}

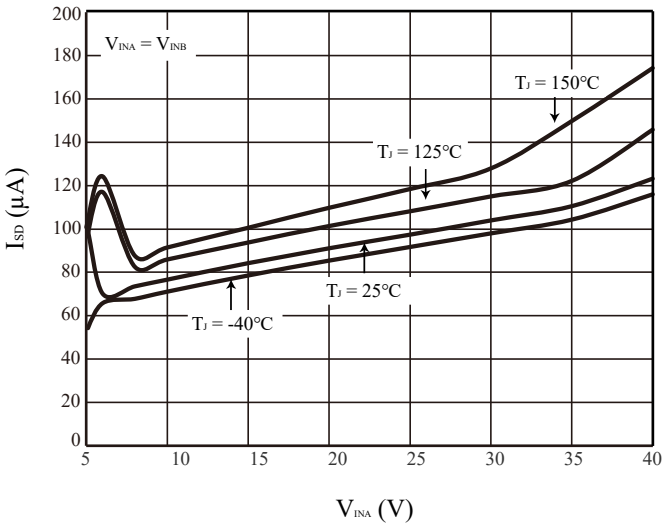


Figure 3 I_{SD} vs. V_{INA}

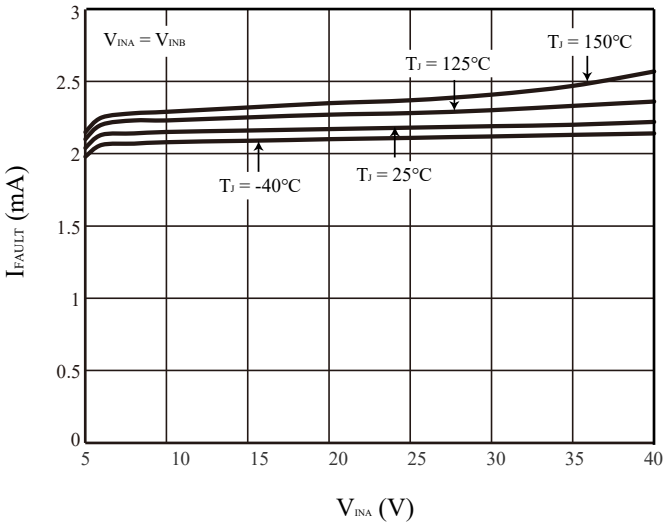


Figure 4 I_{FAULT} vs. V_{INA}

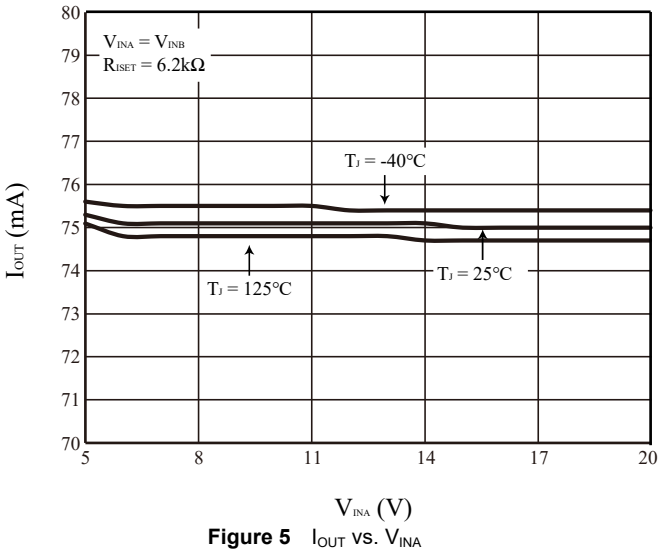


Figure 5 I_{OUT} vs. V_{INA}

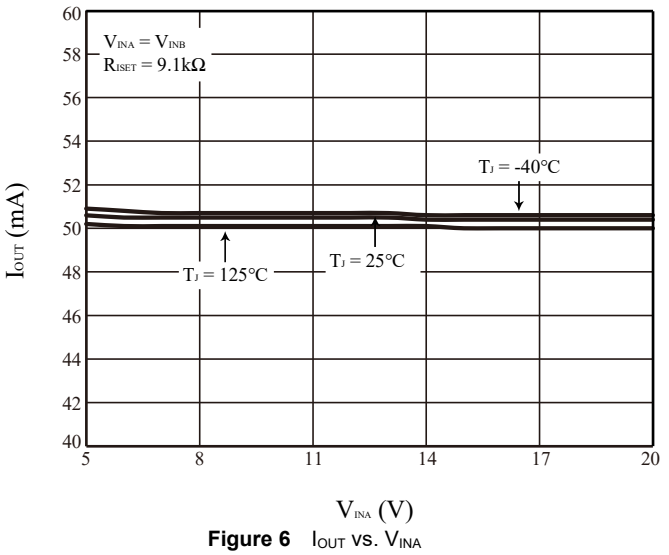


Figure 6 I_{OUT} vs. V_{INA}

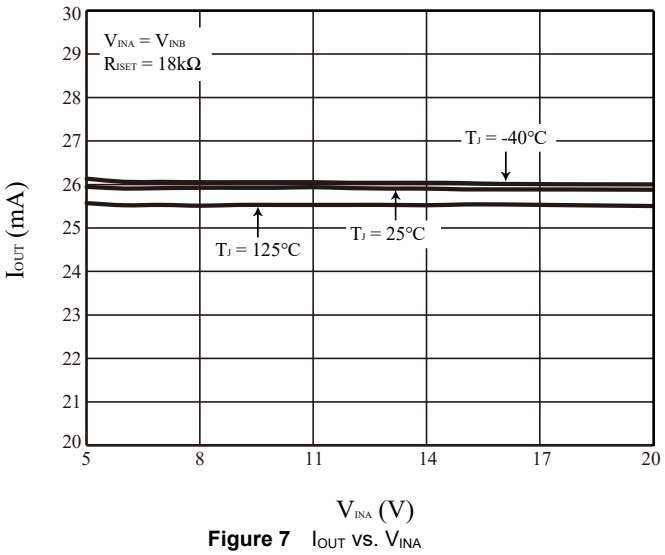


Figure 7 I_{OUT} vs. V_{INA}

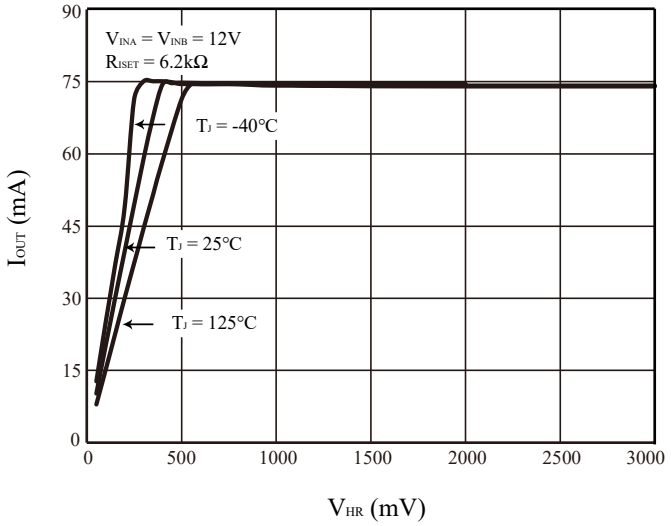


Figure 8 I_{OUT} vs. V_{HR}

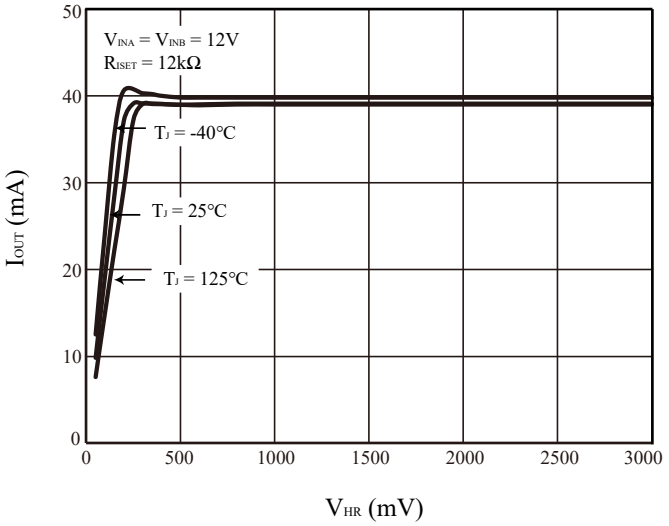


Figure 9 I_{OUT} vs. V_{HR}

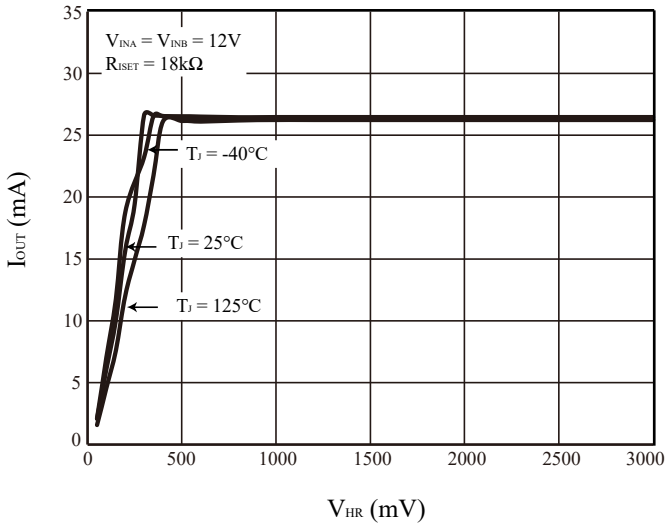


Figure 10 I_{OUT} vs. V_{HR}

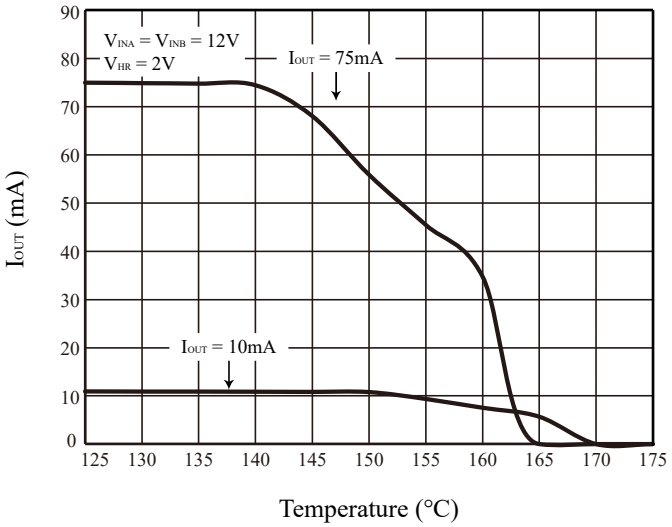


Figure 11 I_{OUT} vs. Temperature (Thermal Roll-Off)

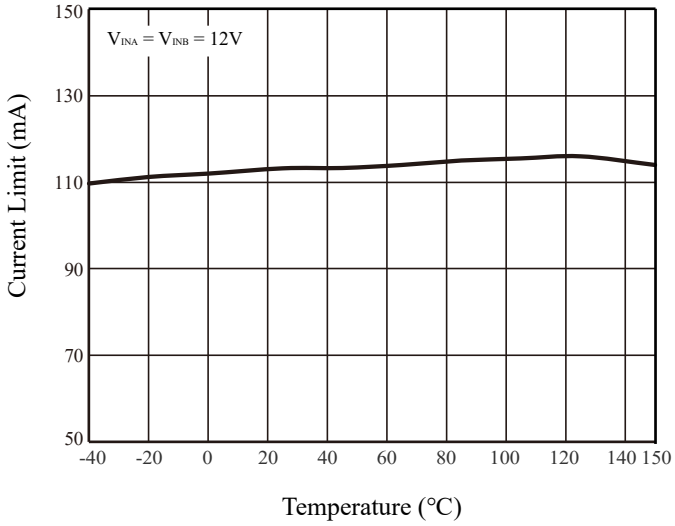


Figure 12 I_{OUT_L} vs. Temperature

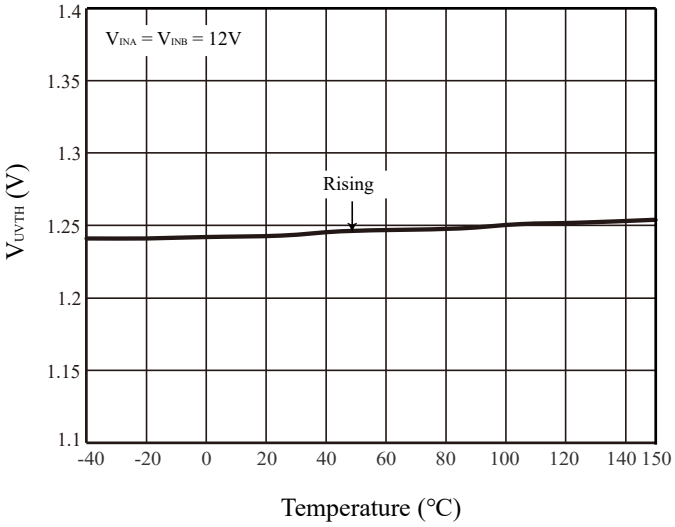


Figure 13 V_{UVTH} vs. Temperature

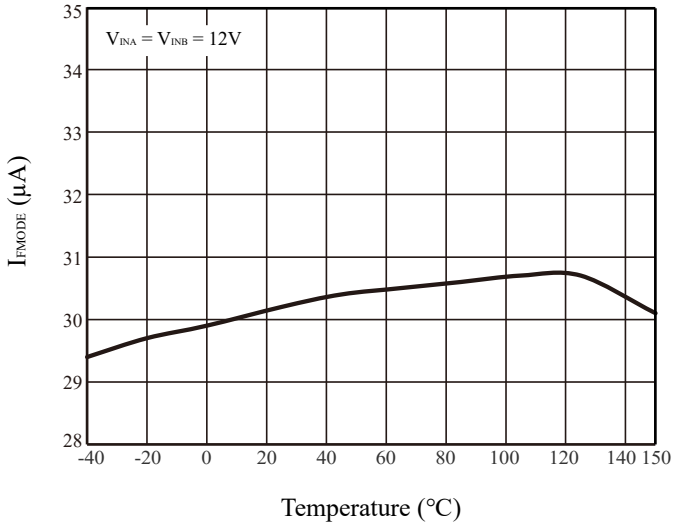


Figure 14 I_{FMODE} vs. Temperature

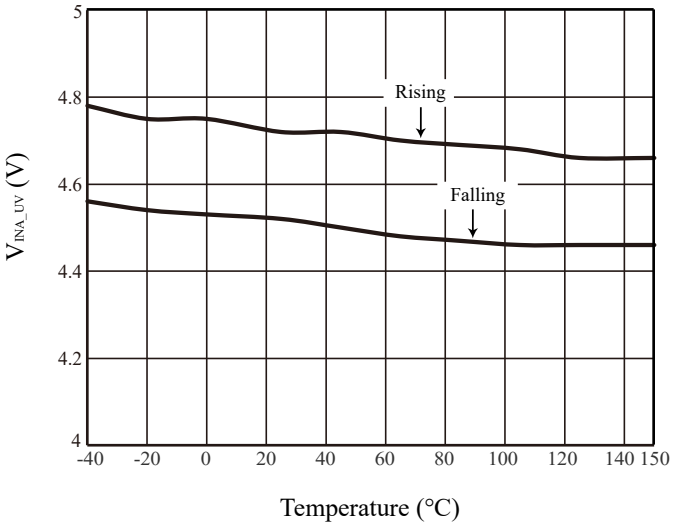


Figure 15 V_{INA_UV} vs. Temperature

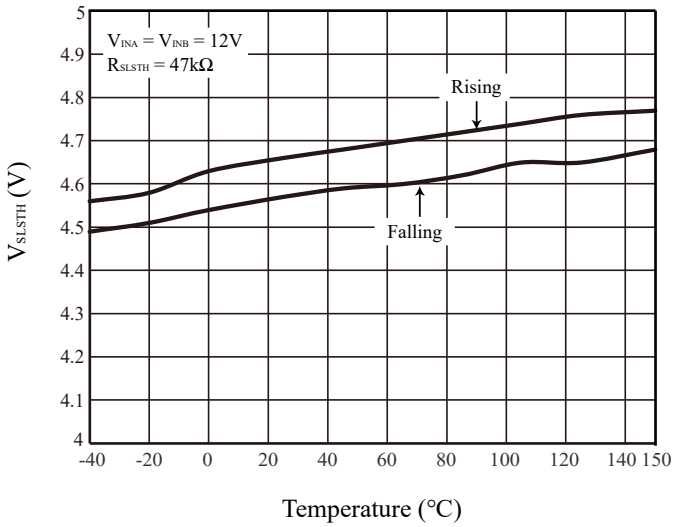


Figure 16 V_{SLSTH} vs. Temperature

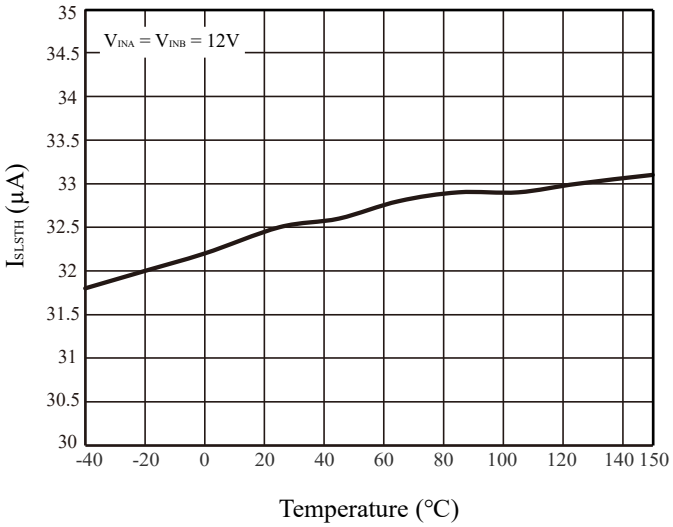


Figure 17 I_{SLSTH} vs. Temperature

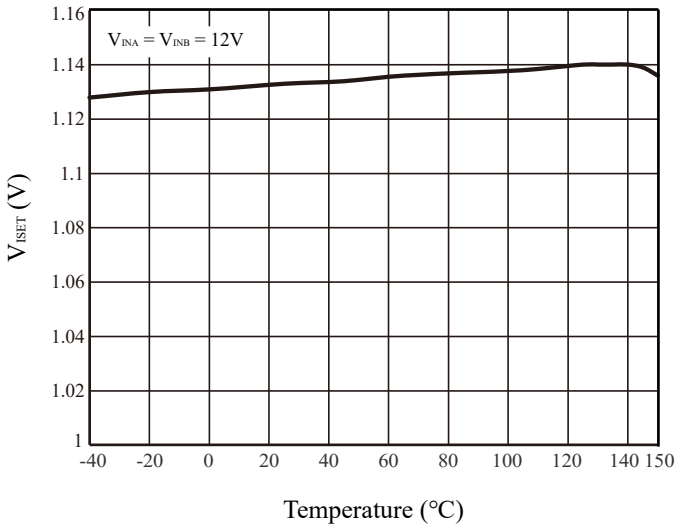


Figure 18 V_{ISET} vs. Temperature

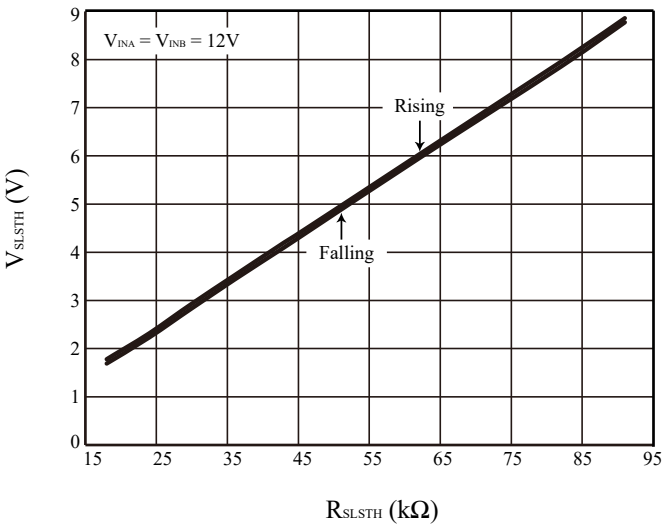


Figure 19 V_{SLSTH} vs. R_{SLSTH}

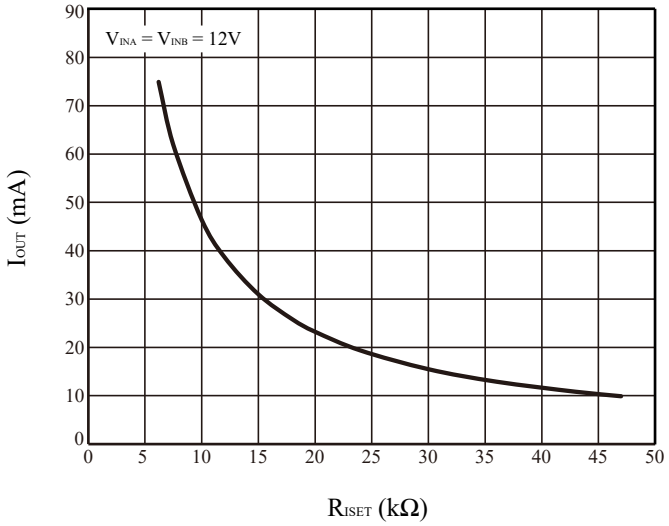


Figure 20 I_{OUT} vs. R_{ISET}

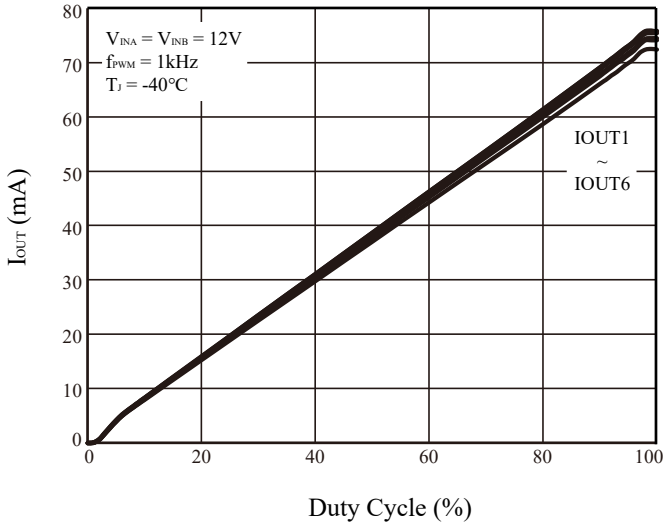


Figure 21 I_{OUT} vs. Duty Cycle

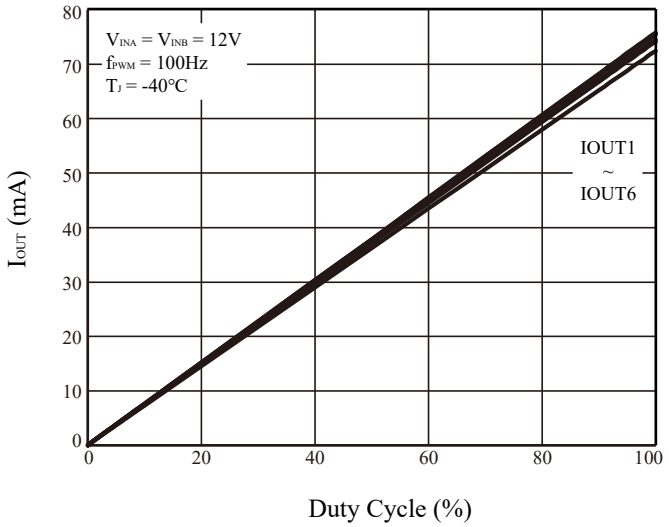


Figure 22 I_{OUT} vs. Duty Cycle

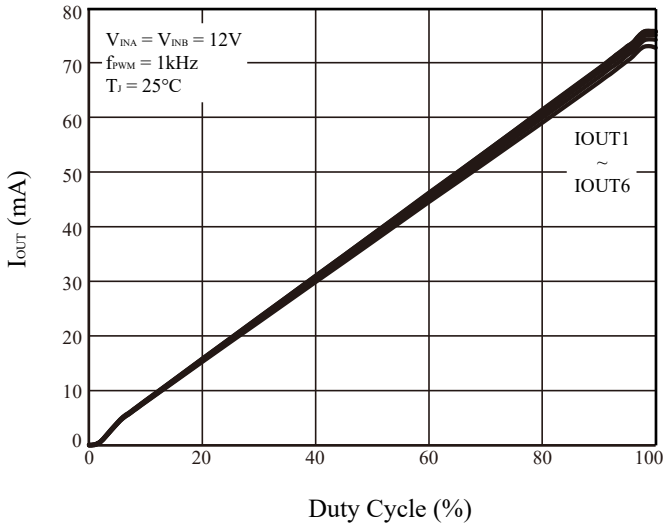


Figure 23 I_{OUT} vs. Duty Cycle

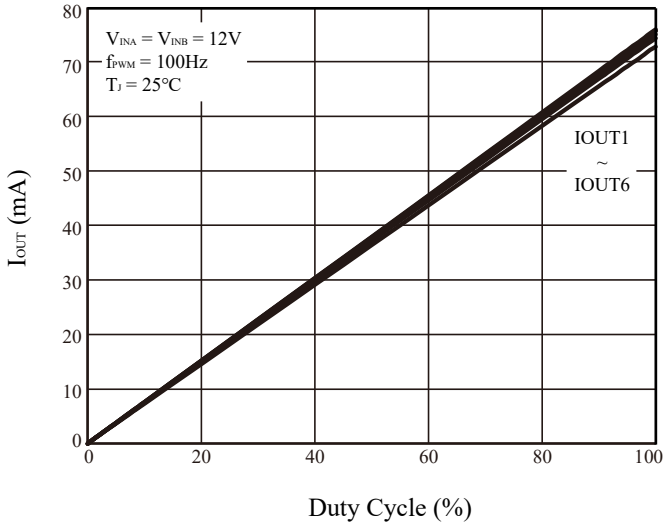


Figure 24 I_{OUT} vs. Duty Cycle

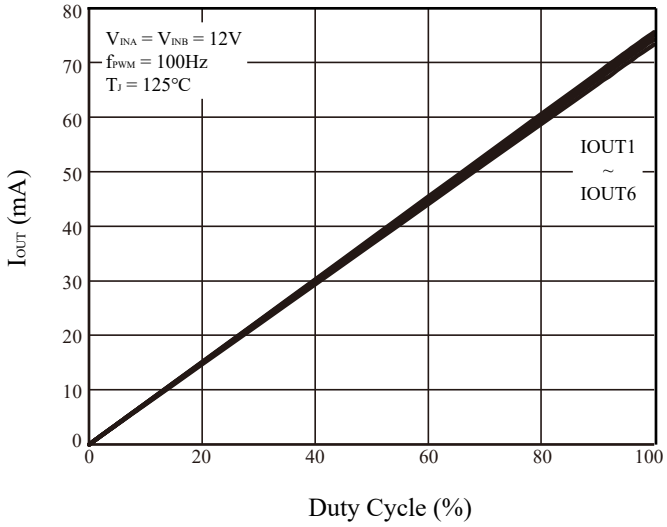


Figure 25 I_{OUT} vs. Duty Cycle

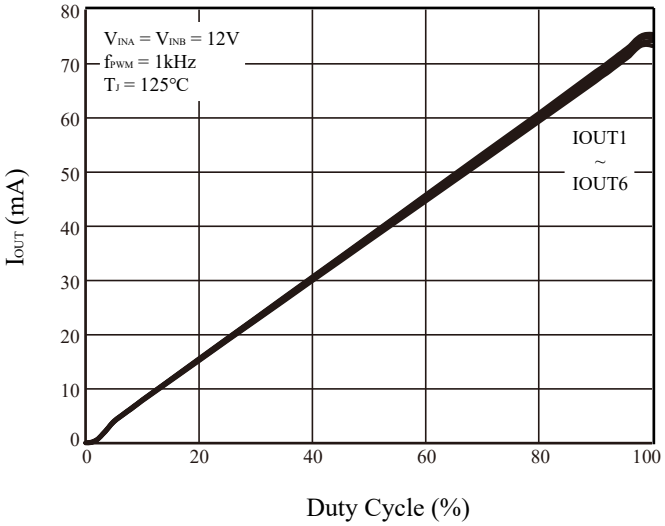


Figure 26 I_{OUT} vs. Duty Cycle

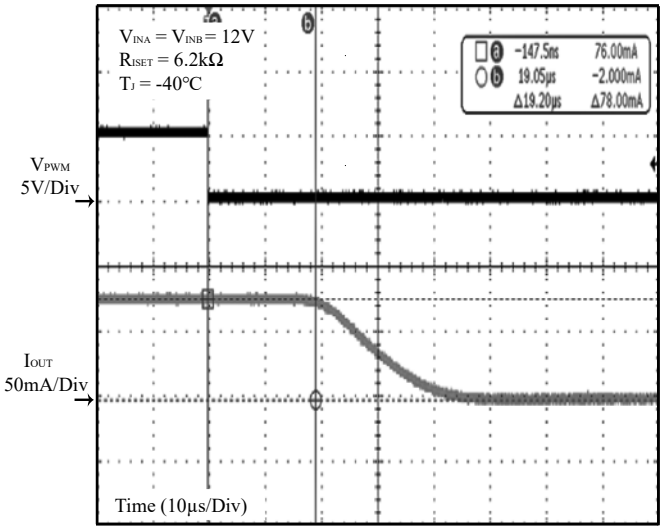


Figure 27 PWM Off

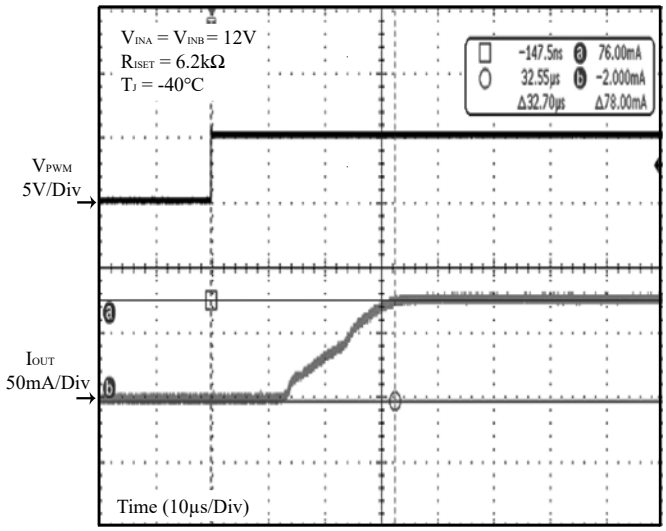


Figure 28 PWM On

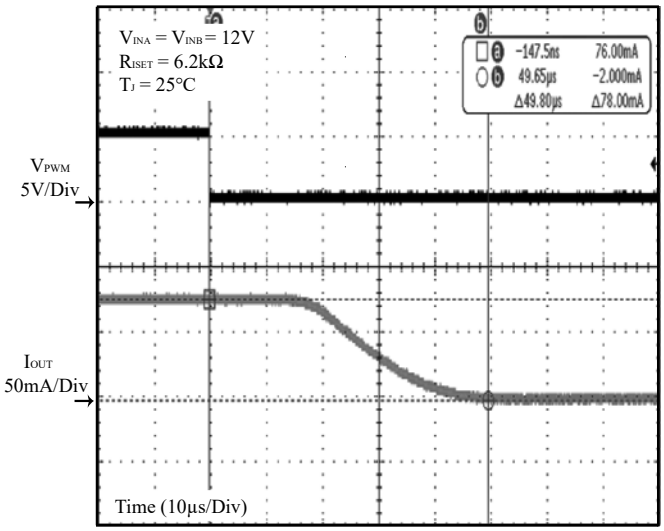


Figure 29 PWM Off

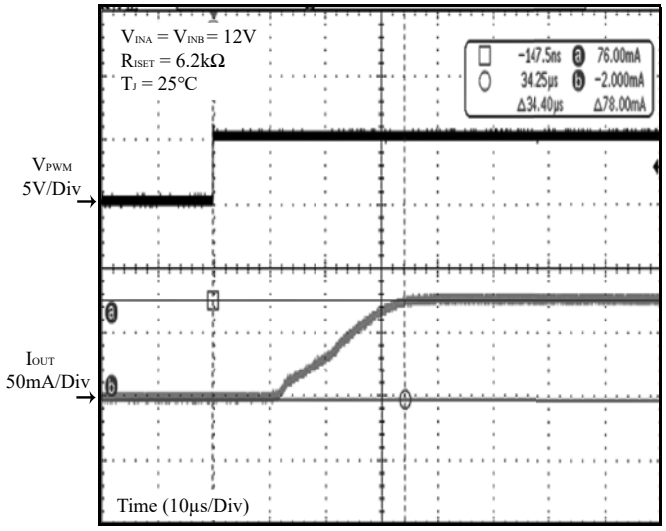


Figure 30 PWM On

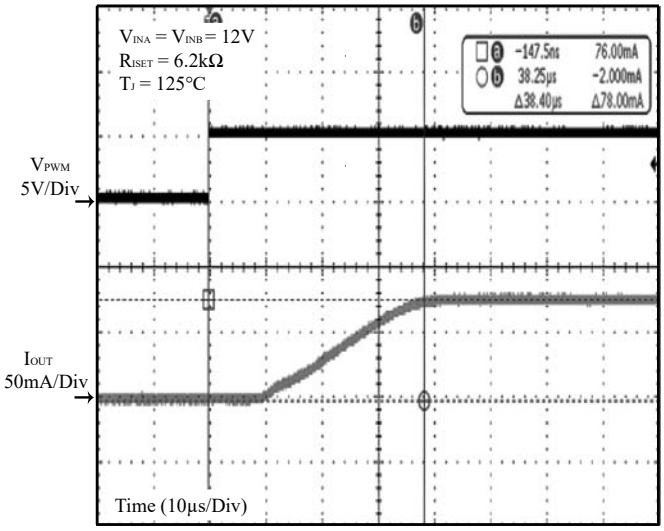


Figure 31 PWM On

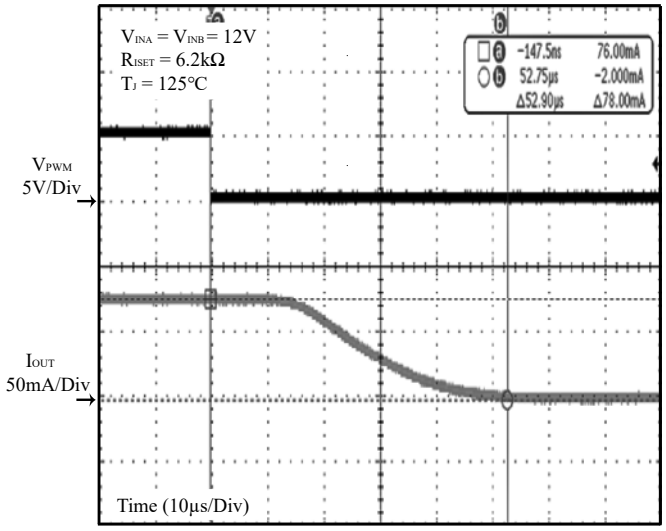


Figure 32 PWM Off

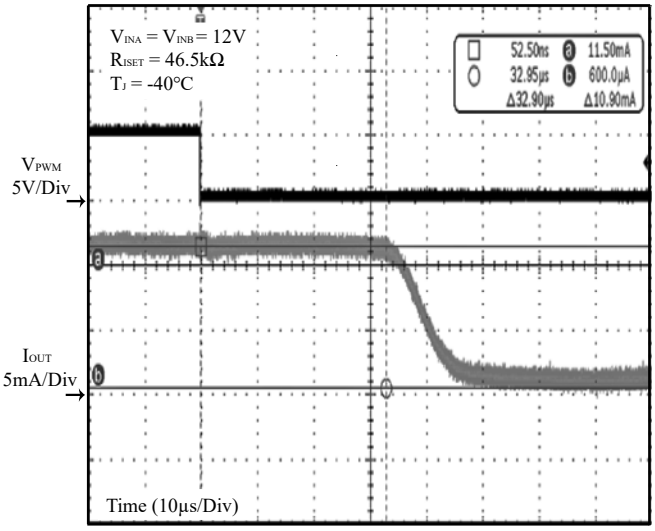


Figure 33 PWM Off

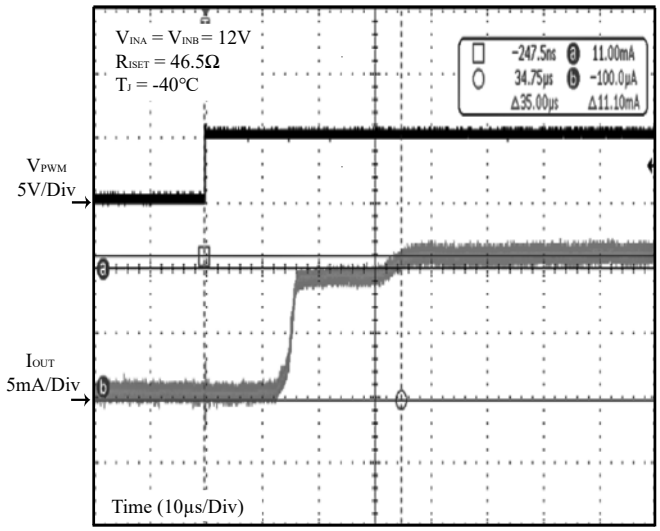


Figure 34 PWM On

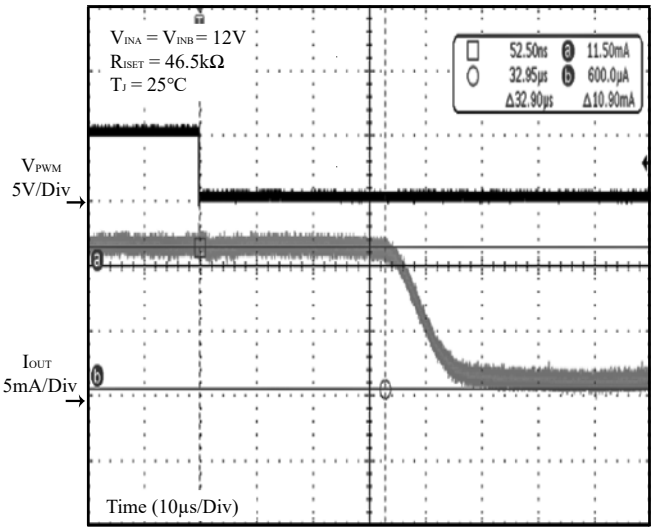


Figure 35 PWM Off

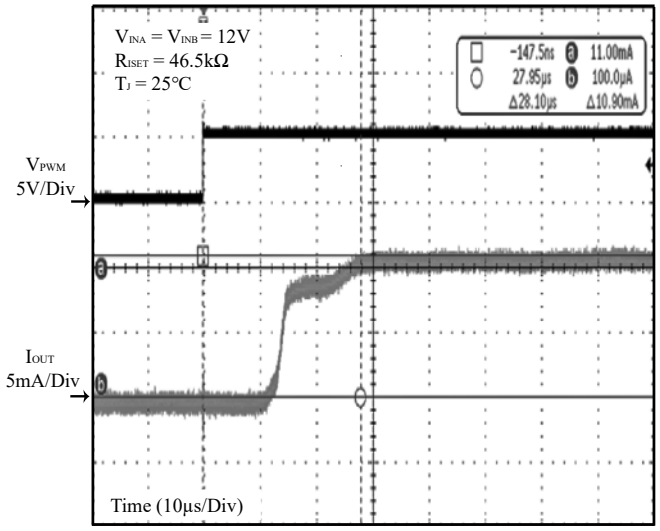


Figure 36 PWM On

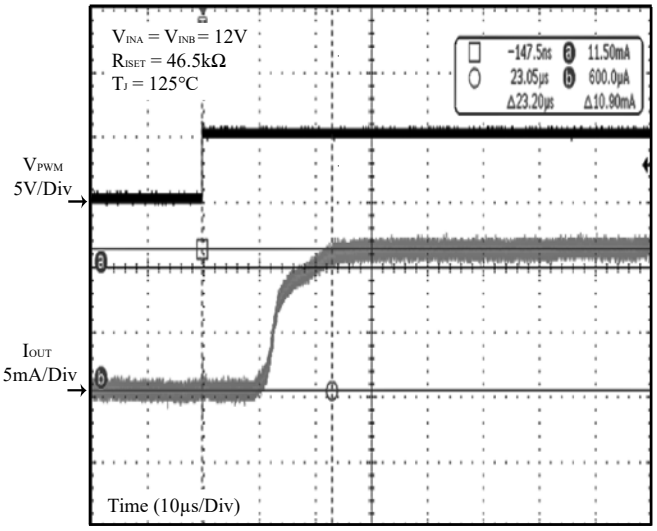


Figure 37 PWM On

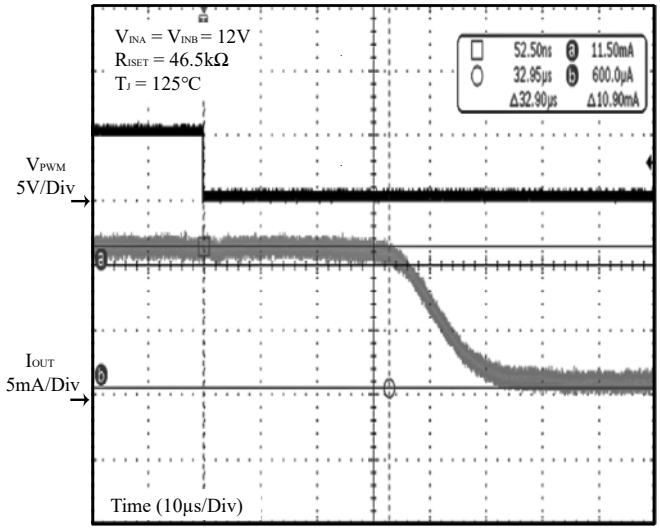
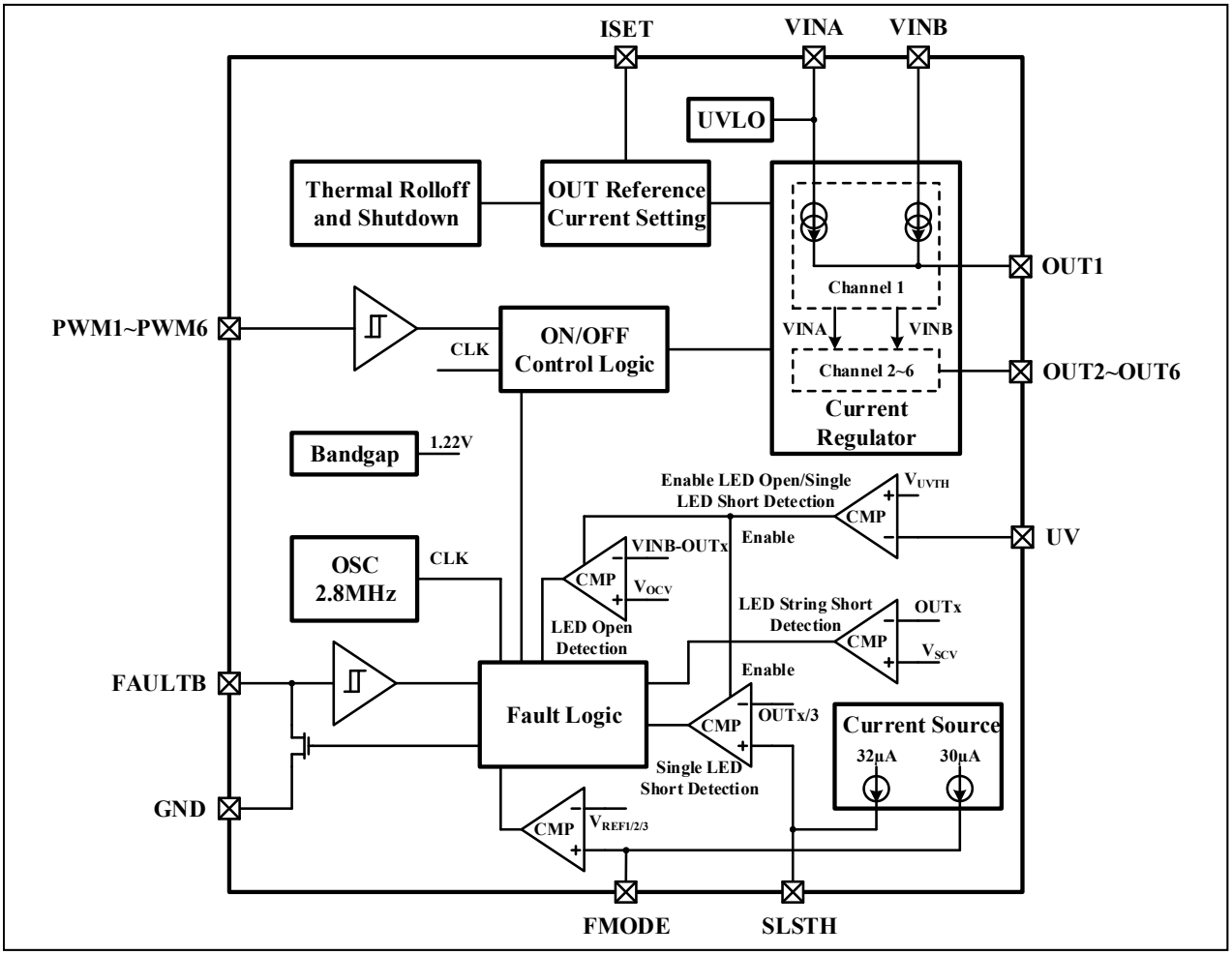


Figure 38 PWM Off

FUNCTIONAL BLOCK DIAGRAM



APPLICATION INFORMATION

The IS32LT3147 device is a six-channel linear LED driver with individual PWM dimming. A single resistor sets the output current for all six channels. Each channel has up to 75mA current capability, resulting in a 450mA current capability when paralleled. A current source output architecture allows LED common-cathode connection to ground. The thermal shunt mechanism helps to efficiently optimize the thermal stress on the driver.

UNDERVOLTAGE-LOCKOUT (UVLO)

IS32LT3147 features an undervoltage-lockout (UVLO) function on the VINA pin to prevent indeterminate operation at too low input voltages. UVLO threshold is an internally fixed value and cannot be adjusted. The device is enabled when the V_{INA} voltage exceeds V_{INA_UV} (Typ. 4.7V), and disabled when the V_{INA} voltage falls below (V_{INA_UV}-V_{INA_UVHY}) (Typ. 4.42V).

OUTPUT CURRENT SETTING

The regulated LED current (up to 75mA) per channel is set by a resistor (R_{ISET}) from ISET pin to GND. The programming resistor is computed using the following Equation:

$$R_{ISET} = \frac{V_{ISET}}{I_{OUT}} \times 404 \qquad (1)$$

(6.2kΩ ≤ R_{ISET} ≤ 46.5kΩ) and V_{ISET} = 1.15V (Typ.). Where, R_{ISET} is in Ω and I_{OUT} is the desired current of each channel in Amps.

It is recommended that R_{ISET} be a 1% accuracy resistor with good temperature characteristics to ensure a stable output current. The R_{ISET} resistor must be placed as close as possible to the ISET pin on PCB layout to avoid noise interference and ground bounce.

The device is protected from an output overcurrent condition caused by the R_{ISET} resistor. The output channel current is limited to an I_{OUT_L} value of 120mA (Typ.) should the ISET pin be shorted or if a low value resistor is connected to the ISET pin.

Unused channel(s) must have its corresponding PWM pin connected to GND to disable it and its corresponding OUTx pin connected to the VINB pin to avoid a false fault detection.

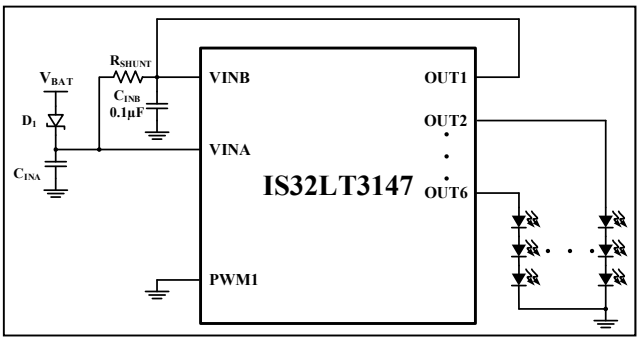


Figure 39 OUT1 Unused for Example

THERMAL SHUNT MECHANISM

For any linear constant current LED driver, the power dissipation on the driver always depends on the voltage drop on the driver and the output current.

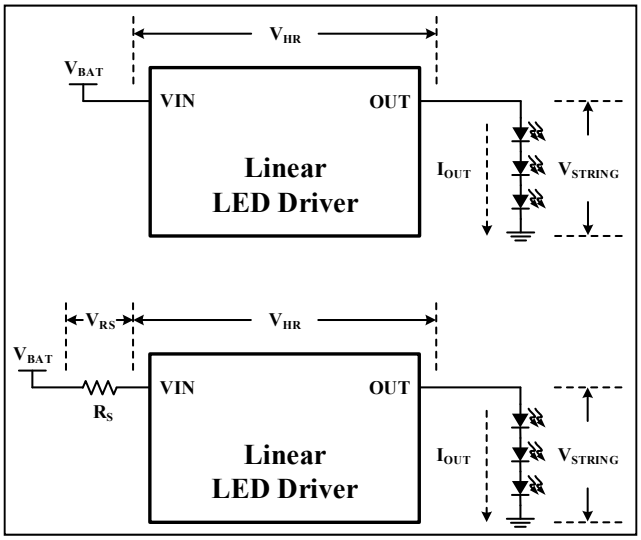


Figure 40 Linear LED Driver Power Dissipation

As Figure 40, the power dissipation on the driver can be calculated by following equation:

$$P_{DRIVER} = V_{HR} \times I_{OUT} = (V_{BAT} - V_{STRING}) \times I_{OUT} \qquad (2)$$

According to above equation, a higher input voltage will result in more power dissipation on the driver. A power resistor, R_S, can be added to shunt some power from the driver. The power dissipation on the driver becomes:

$$P_{DRIVER} = V_{HR} \times I_{OUT} = (V_{BAT} - R_S \times I_{OUT} - V_{STRING}) \times I_{OUT} \qquad (3)$$

Since the internal circuit current consumption of the linear LED driver is negligible compared to I_{OUT}, therefore I_{VIN} is equal to I_{OUT}.

A large R_S value is able to significantly lower the power dissipation on the driver for high voltage inputs. Note the automotive battery voltage range of 9V to 16V requires careful consideration of Rs value. A

large R_S will result in insufficient headroom operating voltage (V_{HR}) for the driver at the low input voltage causing a drop in the output current. To solve this, the IS32LT3147 features a thermal shunt mechanism of two current input paths, VINA pin and VINB pin. VINA is connected directly to the power supply and VINB is connected to the power supply via a thermal shunt resistor in series. As below Figure 41.

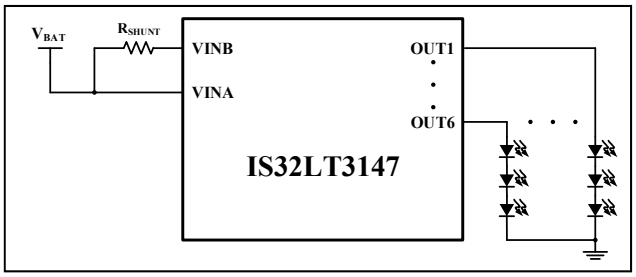


Figure 41 Thermal shunt Topology

The thermal shunt mechanism default current path is through the VINB pin. However, when the input voltage, V_{BAT}, is at the low level, the thermal shunt resistor R_{SHUNT} will limit the current through the VINB path so the majority of current will instead flow through the VINA path. Diverting current to the VINA path will ensure sufficient headroom operating voltage (V_{HR}) so the driver can maintain a constant output current. As the V_{BAT} input voltage increases, the device gradually diverts more input current from the VINA path to the VINB path. The resistor R_{SHUNT} can significantly shunt power from the driver at high input voltages to maintain the driver's junction temperature at a reasonable level. If the thermal shunt mechanism is not implemented, connect both VINA and VINB pins to the power supply.

As shown in Figure 42, the IS32LT3147 has different operating areas when using the thermal shunt mechanism. Within the Low Headroom Area, the input voltage is too low for current regulation. Even though all input current flows through the VINA path, the headroom voltage is insufficient to reach the operating value. So the power dissipation on the driver is minimal. When the input voltage rises above (V_{OUT_MAX}+V_{HR_MIN}), the transition voltage V_{TR} splits the operation into two areas: Thermal Shunt Area and Thermal Increasing Area.

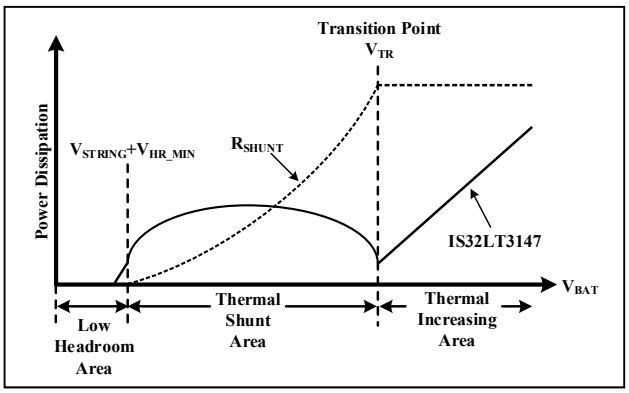


Figure 42 Power Dissipation Distribution

Thermal Shunt Area:

The IS32LT3147 channels operate in constant regulator mode when the input voltage rises above (V_{OUT_MAX}+V_{HR_MIN}). The majority of input current is gradually transferred from the VINA path to the VINB path. Therefore, the power dissipation on R_{SHUNT} increases and the power dissipation on the driver remains at a reasonable low level. The VINB path current can be calculated by:

$$I_{VINB} = \frac{V_{BAT} - V_{OUT\_MAX} - V_{HR\_MIN}}{R_{SHUNT}} \quad (4)$$

Where, V_{OUT_MAX} is the maximum voltage of all OUTx pins. V_{HR_MIN} is the minimum headroom voltage.

The VINA path current is:

$$I_{VINA} = (I_{OUT} \times N - I_{VINB}) + I_{IN} \quad (5)$$

Where, I_{IN} is the power supply quiescent current. N is the number of the channels in use.

The power dissipation on the R_{SHUNT} resistor is:

$$P_{SHUNT} = \frac{(V_{BAT} - V_{OUT\_MAX} - V_{HR\_MIN})^2}{R_{SHUNT}} \quad (6)$$

The power dissipation on the IS32LT3147 is:

$$P_{3147\_TSA} = V_{BAT} \times (I_{OUT} \times N + I_{IN}) - \frac{(V_{BAT} - V_{OUT\_MAX} - V_{HR\_MIN})^2}{R_{SHUNT}} - \sum_{X=1}^{N} (I_{OUT} \times V_{OUTx}) \quad (7)$$

Thermal Increasing Area:

When the input voltage is equal or greater than the Transition Voltage V_{TR}, all the input current flows through R_{SHUNT} into the VINB pin. The power dissipation on the R_{SHUNT} resistor is constant. And the power dissipation on the driver increases linearly. V_{TR} voltage point can be adjusted by the resistance value of R_{SHUNT}.

$$V_{TR} = R_{SHUNT} \times I_{OUT} \times N + V_{OUT\_MAX} + V_{ABTR} \quad (8)$$

To optimize the power dissipation on the driver, R_{SHUNT} value should be chosen to make sure the V_{TR} is equal to the maximum input voltage, typically 16V for 12V automotive system applications.

$$R_{SHUNT\_16V} = \frac{16V - V_{OUT\_MAX} - V_{ABTR}}{I_{OUT} \times N} \quad (9)$$

Where, R_{SHUNT_16V} is the thermal shunt resistor value to make V_{TR}=16V. V_{ABTR} is the voltage threshold of input current full transition from VINA path to VINB path. N is the number of the channels in use.

However, a large R_{SHUNT} value with low V_{INA} results in a low drop out voltage from the VINB pin to the OUTx pin. Since the LED string open protection is achieved by detecting this drop out (refer to the "LED STRING OPEN PROTECTION" section), a large R_{SHUNT} value could falsely trigger the LED string open protection at low input voltages. To prevent false triggering, the fault undervoltage-lockout voltage threshold V_{FLT_UVLO} should be set so the maximum OUTx voltage plus 1.5V margin is > than 9V (refer to the "UV PIN FUNCTION" section). Therefore, the maximum power shunt resister value is limited by the V_{FLT_UVLO} value. It can be calculated by:

$$R_{SHUNT\_MAX} = \frac{V_{FLT\_UVLO} - V_{OUT\_MAX}}{6mA \times N} \quad (10)$$

Where, 6mA is a typical output current level, below which the drop out voltage (V_{INB}-V_{OUTx}) would be too low and falsely trigger the LED string open fault protection. N is the number of the channels in use.

If the calculated R_{SHUNT_16V} is lower than the calculated R_{SHUNT_MAX}, the final R_{SHUNT} value should be R_{SHUNT_16V} otherwise choose R_{SHUNT_MAX}.

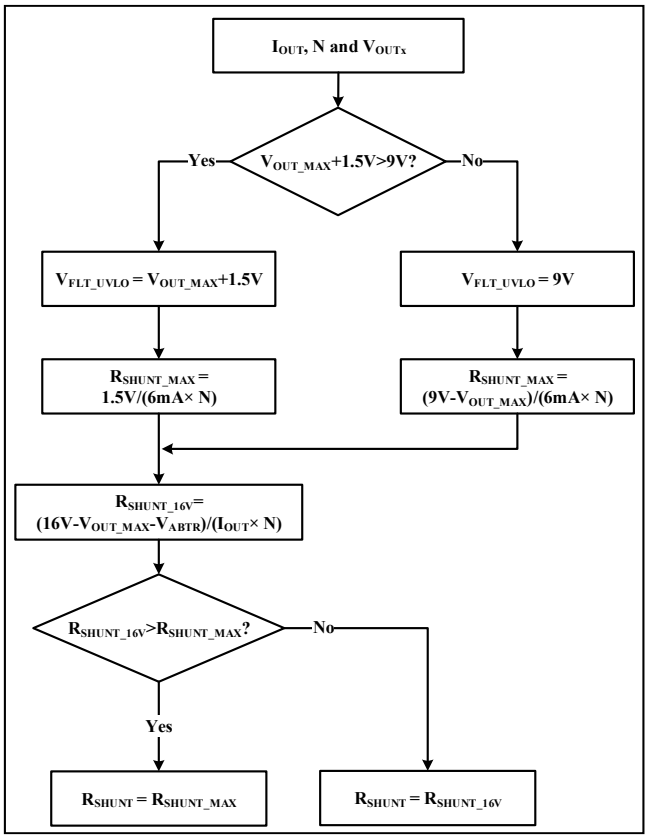


Figure 43 R_{SHUNT} and V_{FLT_UVLO} Calculation Flowchart

The power dissipation on IS32LT3147 is:

$$P_{3147\_TIA} = V_{BAT} \times (I_{OUT} \times N + I_{IN}) - R_{SHUNT} \times (I_{OUT} \times N)^2 - \sum_{X=1}^{N} (I_{OUT} \times V_{OUTx}) \quad (11)$$

The power dissipation on the R_{SHUNT} resistor is constant at maximum value which can be calculated by:

$$P_{SHUNT\_MAX} = R_{SHUNT} \times (I_{OUT} \times N)^2 \quad (12)$$

The power rating of R_{SHUNT} should be carefully considered. A single high wattage resistor or several small wattage resistors in parallel can be used to sustain the power dissipation.

DEVICE ENABLE AND SHUTDOWN

The device doesn't have a dedicated enable pin however pull all PWMx pins below V_{IL} to turn off all channels. Keep the PWMx pins low for longer than t_{SD} to force the device into shutdown mode with a low standby current. When any PWMx pin is pulled high (>V_{IH}), the device will be enabled.

PWM DIMMING

The device features a dedicated PWM pin for each output channel to control the current source. The voltage at the PWM pin should be higher than V_{IH} to enable the corresponding output channel and lower than V_{IL} to disable it.

An external PWM signal on the PWMx pins can be used to modulate the output current to dim the LED light output. The PWM dimming output current is based on the PWM signal's duty cycle and can be calculated by the following Equation:

$$I_{OUT\_PWM} = I_{OUT} \times D_{PWM} \quad (13)$$

Where D_{PWM} is the duty cycle of the PWM signal.

The recommended frequency range of the external PWM signal is 100Hz~1kHz and the duty cycle range can be from 0 to 100%. Due to the output current slew rate control for EMI consideration plus propagation delay time from PWM rising edge to the output activity, a lower frequency PWM will provide a better dimming linearity and contrast ratio.

All PWMx pins are high-voltage tolerant, however if the voltage applied on them is possibly higher than the VINA and VINB pins voltage at any time, a series resistor (recommended value is 10kΩ) for each PWM pin is required to limit the current flowing into it. Since the VINB pin voltage may be regulated down close to the LED string forward voltage by the thermal shunt mechanism, a series resistor for each PWM pin must be added in most applications. If the PWM dimming function of any channel is not implemented, connect its corresponding PWM pin to the VINA pin via a 10kΩ series resistor. As shown in Figure 44.

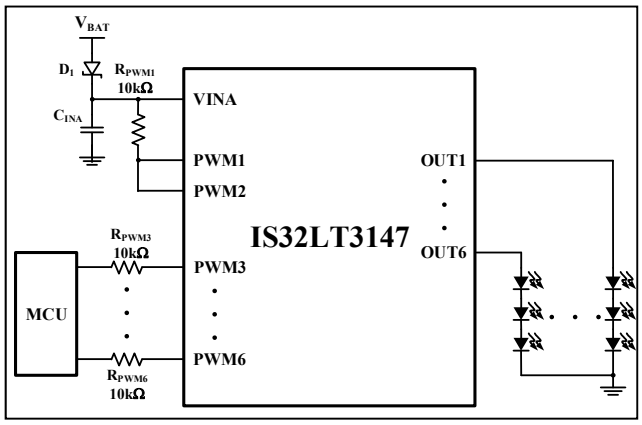


Figure 44 No PWM Dimming to OUT1/OUT2 (Fully On)

FAULT PROTECTION AND REPORTING

For robust system reliability, the IS32LT3147 integrates detection circuitry to protect various fault conditions and report the fault conditions on the FAULTB pin which can be monitored by an external host. The fault protections include LED string open/shorted, single LED shorted, ISET pin open/shorted, thermal roll-off (not reported) and thermal shutdown. The FAULTB pin will go low when the device detects a fault condition.

The FMODE is a fault action mode set pin. Connecting a proper value resistor, R_{FMODE}, from this pin to GND to select various modes of the action when a fault being detected. Refer to Table 1 ~ Table 3. If R_{FMODE} = 0Ω or 27kΩ, the fault action is in "One Fail All Fail" mode which means if any channel encounters a fault then all other normal channels will be turned off. In this mode, the FAULTB pin supports both input and output functions. If R_{FMODE} = 62kΩ or 150kΩ, the fault action is in "One Fail Other On" mode which means if any channel encounters a fault then all other normal channels will continue normal operation. In this mode, the FAULTB pin supports output function only.

Table 1 R_{FMODE} Resistance Versus Fault Actions

R_{FMODE}(kΩ)	Fault Action	Single LED Short
0	One Fail All Fail Mode	Retry Current in Faulty Channel
27		Latched Off Device
62	One Fail Other On Mode	Retry Current in Faulty Channel
150		Fully On

In the "One Fail All Fail" mode, the FAULTB pin supports both input and output functions. Externally pulling FAULTB pin low will disable all outputs, so the FAULTB pin is not allowed to float in this mode. An external resistor, R_{FAULTB}, must be added to pull up FAULTB pin above 2.3V for normal operation. The recommended resistor value is 47kΩ. For lighting systems with multiple IS32LT3147 drivers which requires the complete lighting system be shut down when a fault is detected, the FAULTB pin can be used in a parallel connection. A fault output by one device will pull low the FAULTB pins of the other parallel connected devices and simultaneously turn them all off. This satisfies the multiple devices "One Fail All Fail" operating requirement.

UV PIN FUNCTION

The UV pin with a resistor divider from VINA is to program an undervoltage-lockout threshold for LED string open and single LED shorted fault detections. This helps to prevent false fault detection due to the insufficient power supply voltage, such as caused by a power rail transient. The UV pin voltage must be higher than V_{UVTH} to enable fault detection and lower than (V_{UVTH}-V_{UVTH_HY}) to disable.

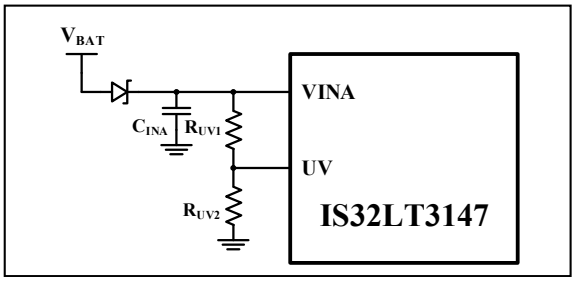


Figure 45 Externally UVLO for Fault Detection

The fault undervoltage-lockout threshold can be computed using the following:

$$V_{FLT\_UVLO} = V_{UVTH} \times \frac{R_{UV1} + R_{UV2}}{R_{UV2}} \qquad (14)$$

To prevent false fault triggering, the fault undervoltage-lockout threshold should be set at the larger of the maximum voltage of all OUTx pins plus 1.5V margin or the minimum input voltage (typically 9V for a 12V system):

$$V_{FLT\_UVLO} = \max\left\{\left(V_{OUT\_MAX} + 1.5V\right), 9V\right\} \qquad (15)$$

Where V_{OUT_MAX} is the maximum voltage of all OUTx pins.

LED STRING OPEN PROTECTION

The LED string open detection is enabled after VINA voltage rising above a setting fault undervoltage-lockout threshold, V_{FLT_UVLO}. If any LED string is open, the corresponding OUTx pin will be pulled up close to VINB by its internal current source. When V_{INA}>V_{FLT_UVLO} and the drop out voltage from the VINB pin to the OUTx pin, (V_{INB}-V_{OUTx}), falls below the LED string open detection voltage, V_{OCV}, and persists for longer than the fault reporting delay time t_{FBDEL} (2.5ms when PWM is 100% on or 8 continuous PWM cycles when the PWM dimming is implementing), the LED string open fault protection will be triggered and the FAULTB pin will go low to report the fault condition.

The faulty channel will reserve a retry current I_{RTR} for recovery detection. The R_{FMODE} value on the FMODE pin decides the fault action. If the R_{FMODE} = 0Ω or 27kΩ, the fault protection mode is “One Fail All Fail” mode, so all other normal channels will be turned off. If the R_{FMODE} = 62kΩ or 150kΩ, the fault protection mode is “One Fail Other On” mode which means that all other normal channels will keep normal operation. No matter in which fault protection mode, the device recovers to normal operation and the FAULTB pin will go back to high impedance once the open condition is removed, (V_{INB}-V_{OUTx}) rising above the LED string open detection voltage, (V_{OCV}+V_{OCV_HY}).

LED STRING SHORT PROTECTION

The LED string short condition is detected if any one of the OUTx pin voltage is lower than LED string short detection voltage, V_{SCV}. Once a short condition occurs and persists for longer than the fault reporting delay time t_{FBDEL} (2.5ms when PWM is 100% on or 8 continuous PWM cycles when the PWM dimming is implementing), the LED string short protection will be triggered and the FAULTB pin will go low to report the fault condition. The faulty channel will reserve a retry current I_{RTR} for recovery detection. The fault action is decided by the R_{FMODE} resistor as well. If the R_{FMODE} = 0Ω or 27kΩ, the fault protection mode is “One Fail All Fail” mode, so all other normal channels will be turned off. If the R_{FMODE} = 62kΩ or 150kΩ, the fault protection mode is “One Fail Other On” which means that all other normal channels will keep normal operation. No matter in which fault mode, the device will recover to normal operation and the FAULTB pin will go back to high impedance once the short condition is removed, the OUTx pin voltage rising above the LED string short detection voltage, (V_{SCV}+V_{SCV_HY}).

SINGLE LED SHORT DETECTION

The IS32LT3147 supports single LED short detection which is implemented by detecting the OUTx pins voltage. The detection is enabled/disabled by UV pin as well to prevent insufficient power supply VINA falsely triggering. The detection voltage is set by a resistor R_{SLSTH} connected from SLSTH pin to GND:

$$R_{SLSTH} = \frac{V_{SLSTH}}{3 \times I_{SLSTH}} \qquad (16)$$

Where V_{SLSTH} is desired single LED short detection voltage in Volt. The maximum V_{SLSTH} should not be set above 8.5V.

It is recommended that R_{SLSTH} be 1% accuracy resistor with good temperature characterization. The V_{SLSTH} should be properly chosen within:

$$N \times V_{f\_MIN} > V_{SLSTH} > (N-1) \times V_{f\_MAX} \qquad (17)$$

Where N is the number of LEDs used in the strings, V_{f_MAX} and V_{f_MIN} is the maximum and minimum forward voltage of LED used.

In case of V_{INA}>V_{FLT_UVLO} and any one of OUTx pins voltage drops blow V_{SLSTH} but above LED string short detection voltage, V_{SCV}, for longer than the fault reporting delay time t_{FBDEL} (2.5ms when PWM is 100% on or 8 continuous PWM cycles when the PWM dimming is implementing), the single LED short protection will be triggered and FAULTB pin will go low to report the fault condition. The fault action also is decided by the R_{FMODE} resistor. As Table 1.

In the “One Fail All Fail” mode, all other normal channels will be turned off. If the R_{FMODE} = 0Ω, the faulty channel will reserve a retry current I_{RTR} for recovery detection. If R_{FMODE} = 27kΩ, the device will latch in completely off state, including the faulty channel, until power cycle.

In the “One Fail Other On” mode, all other normal channels will keep normal operation. If the R_{FMODE} = 62kΩ, the faulty channel will reserve a retry current I_{RTR} for recovery detection as well. If the R_{FMODE} = 150kΩ, the faulty channel will be fully on that means all channels are fully on and report the fault condition only. Besides the latched off mode of R_{FMODE}=27kΩ, the device will recover to normal operation and the FAULTB pin will go back to high impedance once the single LED short condition is removed, V_{OUTx} rising above the single LED short detection voltage, (V_{SLSTH}+V_{SLSTH_HY}).

If the single LED short protection is unused, please connect the SLSTH pin to ground.

ISET PIN OPEN/SHORT PROTECTION

If the ISET pin is left open or a large value resistor (>R_{ISET_OC}) is connected to it, and persists for longer than fault detection deglitch time t_{FBDT}, the ISET pin open protection will be triggered. All channels will be turned off and the FAULTB pin will go low to report the fault condition.

The device is protected from an output overcurrent condition caused by R_{ISET} resistor. All output current is limited to an I_{OUT_L} value of 120mA in case of the ISET pin is shorted or too low value resistor (<R_{ISET_SC}) is connected to the ISET pin. If the condition persists for longer than t_{FBDT}, the ISET pin short protection will be triggered. All channels will be turned off and the FAULTB pin will go low to report the fault condition.

Once the resistance from the ISET pin to GND resumes to a normal range, all channels will recover to normal operation and the FAULTB pin will go back to high impedance.

THERMAL ROLL-OFF PROTECTION

The output current will be equal to the set value as long as the junction temperature of the IC remains below T_{RO} (Typ. 150°C). If the junction temperature

exceeds this threshold, the output current of all channels will begin to reduce at a rate of about 3.7%/°C until thermal shutdown protection following the junction temperature ramping up. Thermal roll-off protection won't be reported by the FAULTB pin.

THERMAL SHUTDOWN PROTECTION

In the event that the junction temperature exceeds T_{SD} (Typ. 175˚C), all channels will go to the "OFF" state and FAULTB pin will pull low to report the fault condition. At this point, the IC presumably begins to cool off. Any attempt to toggle the outputs back to the source condition before the IC cooled to below (T_{SD}-T_{SDHY}) (Typ. 155˚C) will be blocked and the IC will not be allowed to restart. The FAULTB pin will recover to high impedance once the IC has cooled down.

Table 2 "One Fail All Fail" Mode Fault Actions

R_{FMODE} = 0Ω or 27kΩ (ONE-FAIL-ALL-FAIL)					
UV Pin	**Fault Type**	**Fault Condition**	**Output State**	**FAULTB Pin (with Input Function)**	**Recovery**
V_{UV}<(V_{UVTH}-V_{UVTH_HY})	LED string open	Disabled			
	LED string short	V_{OUTx}<V_{SCV}	Faulty channel outputs I_{RTR} for recovery detection and other channels off	Pull low (If the FAULTB pins of multiple devices are tied together, all other devices will be off)	V_{OUTx}>(V_{SCV}+V_{SCV_HY})
	Single LED short	Disabled			
	ISET open	ISET pin to GND resistance> R_{ISET_OC}	All channels off	Pull low (If the FAULTB pins of multiple devices are tied together, all other devices will be off)	ISET pin to GND resistance resumes to normal range
	ISET short	ISET pin to GND resistance< R_{ISET_SC}	All channels off		ISET pin to GND resistance resumes to normal range
	Thermal shutdown	T_J>T_{SD}	All channels off		T_J<(T_{SD}-T_{SDHY})
	Thermal roll-off	T_J>T_{RO}	Output current of all channels linearly decreases toward zero following T_J increasing	High impedance (If the FAULTB pins of multiple devices are tied together, all other devices will be on)	T_J<T_{RO}
V_{UV}>V_{UVTH}	LED string open	(V_{INB}-V_{OUTx})<V_{OCV}	Faulty channel outputs I_{RTR} for recovery detection and other channels off	Pull low (If the FAULTB pins of multiple devices are tied together, all other devices will be off)	(V_{INB}-V_{OUTx})>(V_{OCV}+V_{OCV_HY})
	LED string short	V_{OUTx}<V_{SCV}	Faulty channel outputs I_{RTR} for recovery detection and other channels off		V_{OUTx}>(V_{SCV}+V_{SCV_HY})
	Single LED short	V_{OUTx}<V_{SLSTH}	R_{FMODE} = 0Ω: Faulty channel outputs I_{RTR} for recovery detection and other channels off		V_{OUTx}>(V_{SLSTH}+V_{SLSTH_HY})
			R_{FMODE} = 27kΩ: All channels latched off		Power cycle
	ISET open	ISET pin to GND resistance> R_{ISET_OC}	All channels off		ISET pin to GND resistance resumes to normal range
	ISET short	ISET pin to GND resistance< R_{ISET_SC}	All channels off		ISET pin to GND resistance resumes to normal range
	Thermal shutdown	T_J>T_{SD}	All channels off		T_J<(T_{SD}-T_{SDHY})
	Thermal roll-off	T_J>T_{RO}	Output current of all channels linearly decreases toward zero following T_J increasing	High impedance (If the FAULTB pins of multiple devices are tied together, all other devices will be on)	T_J<T_{RO}

Table 3 "One Fail Other On" Mode Fault Actions

R_{FMODE} = 62kΩ or 150kΩ (ONE-FAIL-OTHER-ON)					
UV Pin	**Fault Type**	**Fault Condition**	**Output State**	**FAULTB Pin (without Input Function)**	**Recovery**
V_{UV}<(V_{UVTH}-V_{UVTH_HY})	LED string open	Disabled			
	LED string short	V_{OUTx}<V_{SCV}	Faulty channel outputs I_{RTR} for recovery detection and other channels on	Pull low (If the FAULTB pins of multiple devices are tied together, all other devices will be on)	V_{OUTx}>(V_{SCV}+V_{SCV_HY})
	Single LED short	Disabled			
	ISET open	ISET pin to GND resistance> R_{ISET_OC}	All channels off	Pull low (If the FAULTB pins of multiple devices are tied together, all other devices will be on)	ISET pin to GND resistance resumes to normal range
	ISET short	ISET pin to GND resistance< R_{ISET_SC}	All channels off		ISET pin to GND resistance resumes to normal range
	Thermal shutdown	T_J>T_{SD}	All channels off		T_J<(T_{SD}-T_{SDHY})
	Thermal roll-off	T_J>T_{RO}	Output current of all channels linearly decreases toward zero following T_J increasing	High impedance (If the FAULTB pins of multiple devices are tied together, all other devices will be on)	T_J<T_{RO}
V_{UV}>V_{UVTH}	LED string open	(V_{INB}-V_{OUTx})<V_{OCV}	Faulty channel outputs I_{RTR} for recovery detection and other channels on	Pull low (If the FAULTB pins of multiple devices are tied together, all other devices will be on)	(V_{INB}-V_{OUTx})>(V_{OCV}+V_{OCV_HY})
	LED string short	V_{OUTx}<V_{SCV}	Faulty channel outputs I_{RTR} for recovery detection and other channels on		V_{OUTx}>(V_{SCV}+V_{SCV_HY})
	Single LED short	V_{OUTx}<V_{SLSTH}	R_{FMODE} = 62kΩ: Faulty channel outputs I_{RTR} for recovery detection and other channels on		V_{OUTx}>(V_{SLSTH}+V_{SLSTH_HY})
			R_{FMODE} = 150kΩ: All channels on		
	ISET open	ISET pin to GND resistance> R_{ISET_OC}	All channels off		ISET pin to GND resistance resumes to normal range
	ISET short	ISET pin to GND resistance< R_{ISET_SC}	All channels off		ISET pin to GND resistance resumes to normal range
	Thermal shutdown	T_J>T_{SD}	All channels off		T_J<(T_{SD}-T_{SDHY})
	Thermal roll-off	T_J>T_{RO}	Output current of all channels linearly decreases toward zero following T_J increasing	High impedance (If the FAULTB pins of multiple devices are tied together, all other devices will be on)	T_J<T_{RO}

THERMAL CONSIDERATIONS

The package thermal resistance, θ_{JA}, determines the amount of heat that can pass from the silicon die to the surrounding ambient environment. The θ_{JA} is a measure of the temperature rise created by power dissipation and is usually measured in degree Celsius per watt (°C/W). The junction temperature, T_J, can be calculated by the rise of the silicon temperature, ΔT, the power dissipation on IS32LT3147, P_{3147}, and the package thermal resistance, θ_{JA}, as in Equation (18):

$$T_J = T_A + \Delta T = T_A + P_{3147} \times \theta_{JA} \quad (18)$$

The P_{3147} is descripted in the "Thermal Shunt Mechanism" section.

When operating the chip at high ambient temperatures, or when the supply voltage is high, care must be taken to avoid exceeding the package power dissipation limits. The maximum power dissipation at T_A=25°C can be calculated using the following Equation (19):

$$P_{D(MAX)} = \frac{150°C - 25°C}{\theta_{JA}} \qquad (19)$$

So,

$$P_{D(MAX)} = \frac{150°C - 25°C}{31.8°C/W} \approx 3.93W$$

for eTSSOP-20 package.

Figure 46, shows the power derating of the IS32LT3147 on a JEDEC board (in accordance with JESD 51-5 and JESD 51-7) standing in still air.

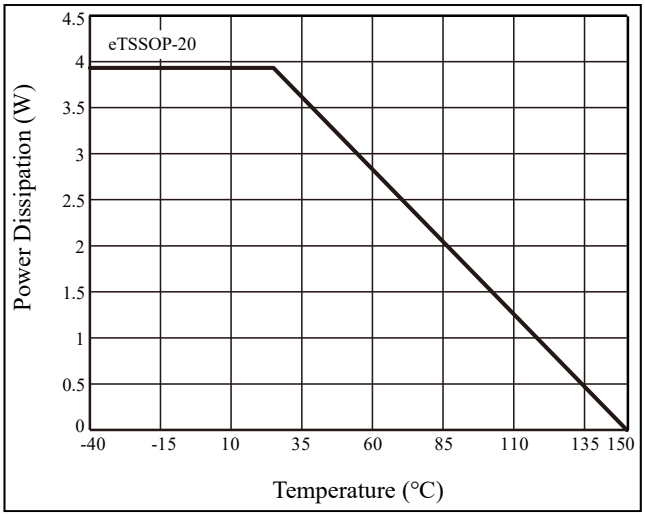


Figure 46 Dissipation Curve (eTSSOP-20)

In the thermal shunt application, the R_P will share quite a lot power dissipation; therefore its package power rating should be sufficient to prevent heat run away.

When designing the Printed Circuit Board (PCB) layout, double-sided PCB with a large copper area on each side of the board directly under the IS32LT3147 and the thermal shunt resistor. Multiple thermal vias, as shown in Figure 47, will help to conduct heat from the exposed pad of the IS32LT3147 and the thermal shunt resistor to the copper on each side of the board. To avoid the heat buildup, the thermal shunt resistor should be spread out on the PCB board with some distance from IS32LT3147.

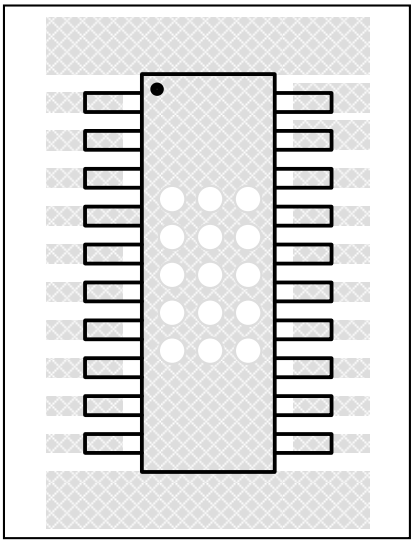


Figure 47 Board Via Layout For Thermal Dissipation

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

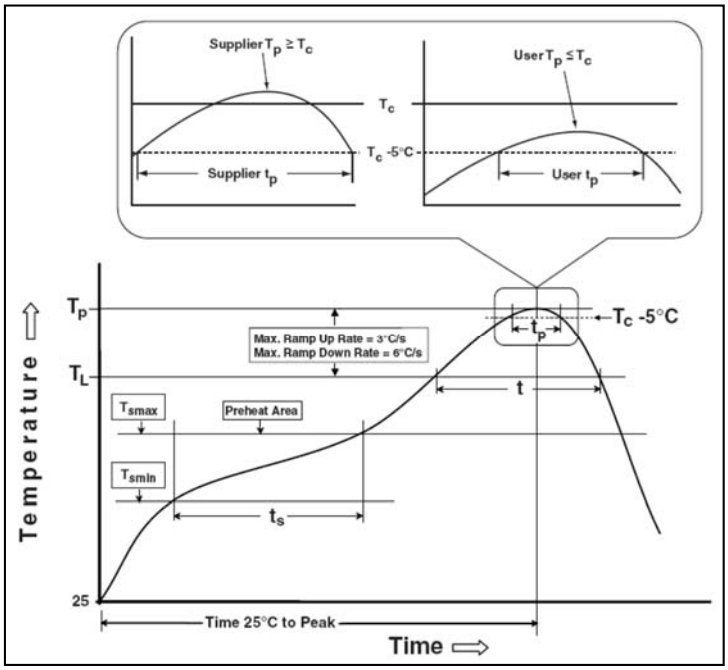
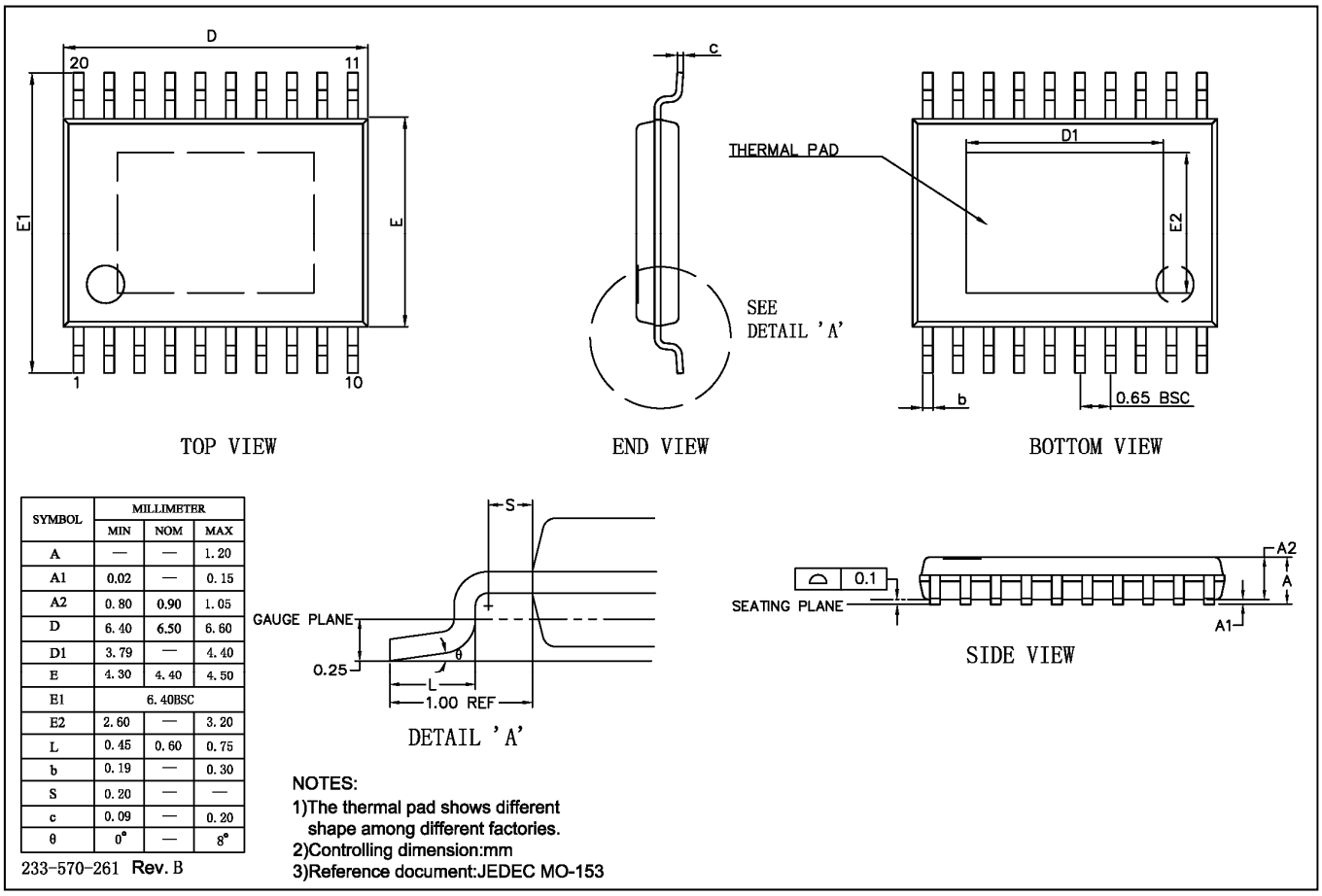


Figure 48 Classification Profile

PACKAGE INFORMATION

eTSSOP-20



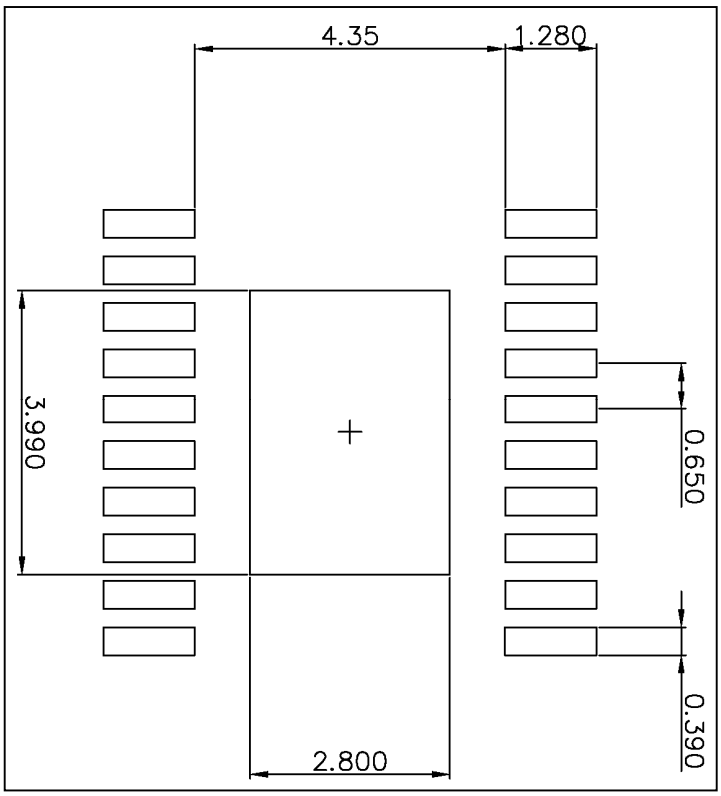
SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.02	—	0.15
A2	0.80	0.90	1.05
D	6.40	6.50	6.60
D1	3.79	—	4.40
E	4.30	4.40	4.50
E1	6.40BSC		
E2	2.60	—	3.20
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20	—	—
c	0.09	—	0.20
θ	0°	—	8°

233-570-261 Rev. B

NOTES:
1)The thermal pad shows different shape among different factories.
2)Controlling dimension:mm
3)Reference document:JEDEC MO-153

RECOMMENDED LAND PATTERN

eTSSOP-20



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release	2022.03.03