IS32AP2123

24W MONO AUTOMOTIVE CLASS-D AUDIO AMPLIFIER WITH LOAD DUMP AND I2C DIAGNOSTICS

October 2020

GENERAL DESCRIPTION

The IS32AP2123 is a Class-D audio amplifier for driving a mono speaker in BTL (Bridge-Tied-Load) configuration. It is capable of delivering 20W into 4Ω speaker at less than 1% THD+N from a 14.4V power supply.

It is a mono Class-D audio amplifier designed for automotive applications, such as emergency call (eCall), telematics, and instrument cluster, and infotainment applications. With a wide operating voltage range of 4.5V to 24V makes it ideal for start/stop or backup battery operation.

The IS32AP2123 comes with onboard load diagnostic hardware accessible via a standard I2C port. The internal diagnostics evaluate the output impedance to check for shorts across the outputs, to the battery, or to ground. The I2C interface allows the system to reads of diagnostic and protection device parameters.

The integrated 40V load-dump protection reduces external voltage clamp cost and size, for reliable automotive audio systems. The highly efficient (85%) IS32AP2123 comes in a thermally enhanced eTSSOP-16 package requiring no heatsink for typical operation.

APPLICATIONS

- Automotive emergency call (eCall)
- Telemetric systems
- Instrument cluster systems
- Infotainment audio

FEATURES

- 4.5V to 24V operating range
- Mono BTL digital power amplifier
- Differential analog input
- 24W output power at 10% THD+N into 4Ω
- 70dB power supply rejection ratio (PSRR)
- Up to 85% efficiency into 4Ω
- Support spread spectrum to optimize EMI
- I2C Interface
  - Query and set up critical device parameters
- Automatic load diagnostic functions during power up and after fault events:
  - Open and shorted output load
  - Output-to-power and -ground shorts
- Support AM avoidance (400 and 500kHz modulation frequency)
- AGC function with adjustable power limiter
- Protection and monitoring functions:
  - Short-circuit (to ground, VCC or output-to-output) protection
  - 40V load dump protection
  - Output DC level detection while music is playing
  - Over temperature protection
  - Over and under voltage protection
  - Dynamic temperature control to avoid thermal run away
- Thermally enhanced eTSSOP-16 package
- Designed for automotive EMC requirements
- AEC-Q100 Qualified
- -40°C to +125°C ambient operating temperature

TYPICAL APPLICATION CIRCUIT

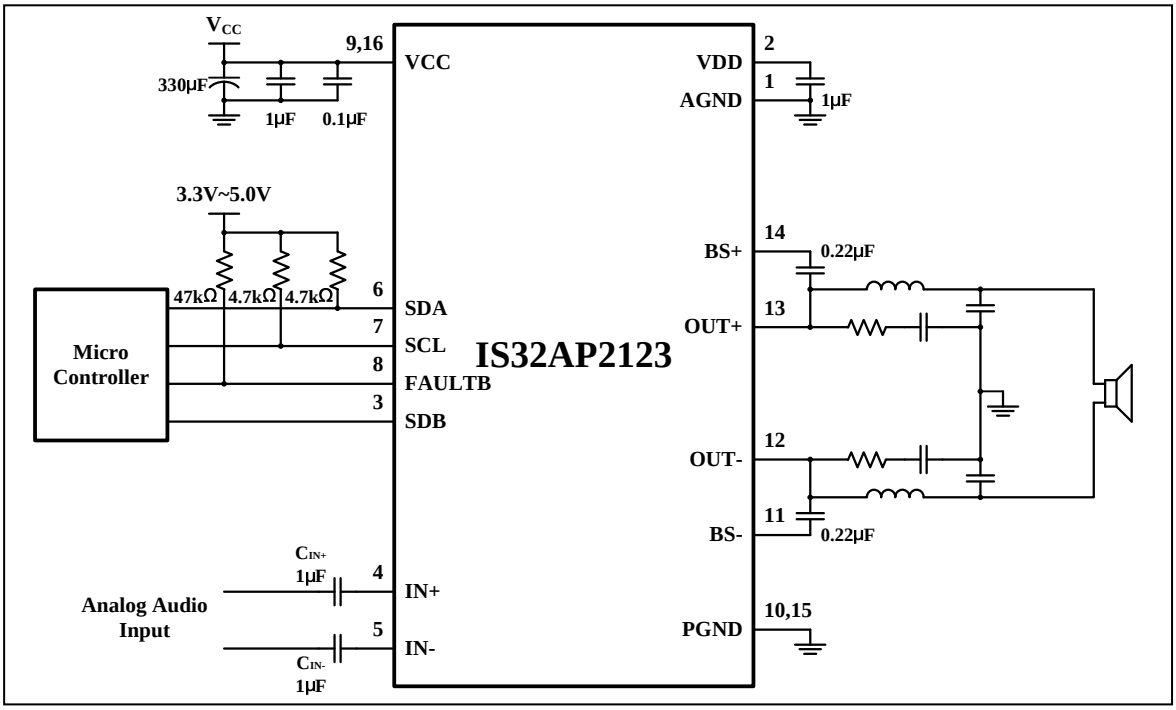
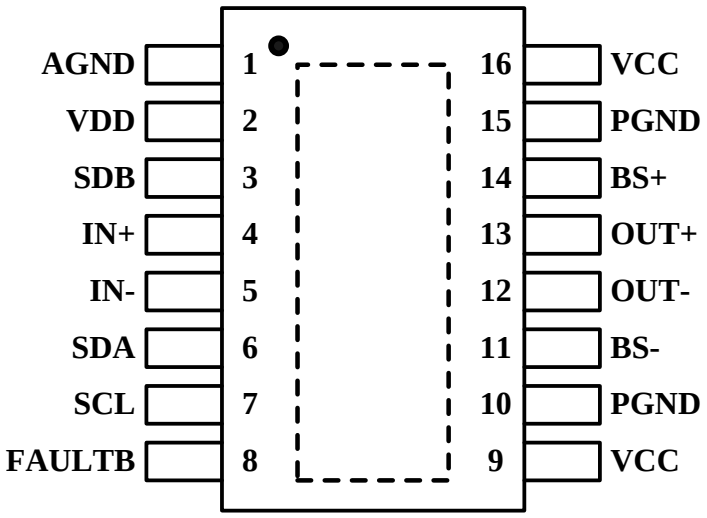


Figure 1 Typical Application Circuit

PIN CONFIGURATION

Package	Pin Configuration (Top View)
eTSSOP-16	

PIN DESCRIPTION

No.	Pin	Description
1	AGND	Ground.
2	VDD	Internal 6V voltage.
3	SDB	Active-low SDB pin (no internal pull-up or pull-down).
4	IN+	Non-inverting analog input.
5	IN-	Inverting analog input.
6	SDA	I2C serial data.
7	SCL	I2C serial clock.
8	FAULTB	Active-low open-drain output used to report faults.
9,16	VCC	Power supply.
10,15	PGND	Ground.
11	BS-	Bootstrap for negative-output high-side FET.
12	OUT-	Negative output for channel.
13	OUT+	Positive output for channel.
14	BS+	Bootstrap for positive-output high-side FET.
	Thermal Pad	Connect to GND.

ORDERING INFORMATION

Automotive Range: -40°C To +125°C

Order Part No.	Package	QTY
IS32AP2123-ZLA3-TR	eTSSOP-16, Lead-free	2500/Reel
IS32AP2123-ZLA3		96/Tube

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range (Unless otherwise noted) (Note 1).

Supply voltage, V_{CC} (Relative to GND)	-0.3V ~ +30V
Pulsed supply voltage range, V_{CC_MAX} (t≤400ms exposure)	-1.0V ~ +40V
Supply voltage ramp rate, V_{CC_RAMP}	15V/ms
For FAULTB pin (Relative to GND)	-0.3V ~ +30V
For SCL, SDA, SDB pins (Relative to GND)	-0.3V ~ +6.5V
For IN+, IN-, (Relative to GND)	-0.3V ~ +6.5V
Package thermal resistance, junction to ambient (4 layer standard test PCB based on JEDEC standard), θ_{JA}	47.2°C/W
Package thermal resistance, junction to thermal PAD (4 layer standard test PCB based on JESD 51-8), θ_{JP}	1.62°C/W
Operating temperature range, $T_A=T_J$	-40°C ~ +150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage range relative to GND. Includes AC transients, requires proper decoupling.	2Ω±20% load (or higher)	4.5	14.4	24	V
V_{SD_H}	SDB pin input voltage for logic-level high		2			V
V_{SD_L}	SDB pin input voltage for logic-level low				0.7	V
V_{I2C_H}	SCL/SDA pin input voltage for logic-level high	R_{I2C}=4.7kΩ, V_{CC}=3.3V or 5V	2.1		5.5	V
V_{I2C_L}	SCL/SDA pin input voltage for logic-level low		-0.5		1.1	V
R_L	Load impedance range	When using low impedance loads, do not exceed overcurrent limit.	2	4	16	Ω
R_{PU}	External pull-up resistor range (for FAULTB pin)	Resistor connected between open-drain logic output and pullup voltage supply		47		kΩ
C_{VDD}	External capacitor on the VDD pin, typical value ±10%			1		μF
C_{IN}	External capacitance to analog input pin in series with input signal			1		μF
C_{BSP}	External boostrap capacitor, typical value ±20%			220		nF

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 14.4V, R_L = 4Ω, P_O = 1W/CH, AES17 filter, default I2C settings (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Operating Current						
I_{CC}	VCC idle current	In play mode, no audio present		11		mA
I_{SD}	VCC shutdown current	SDB mode,		5	20	μA
Output Power						
P_O	Output power per channel	4Ω, THD≤1%,1kHz,T_A=75°C (Note 2)		20		W
		4Ω, THD=10%,1kHz,T_A=75°C (Note 2)		24		
η	Power efficiency	4Ω, P_O=22W (THD=10%) (Note 2)		85		%
Audio Performance						
V_{NO}	Noise voltage at output	Gain=20dB, zero input, and A-weighting (Note 2)		95		μV
CMRR	Common-mode rejection ratio	f=1kHz, 100mVrms referenced to GND, Gain=20dB (Note 2)		63		dB
PSRR	Power supply rejection ratio	V_{CC}=14.4VDC+1Vrms, f=1kHz (Note 2)		-70		dB
THD+N	Total harmonic distortion+noise	P_O=1W, f=1kHz (Note 2)		0.05		%
f_S	Switching frequency	Switching frequency selectable for AM interference avoidance		400		kHz
				500		
Gain	Voltage gain (V_{OUT}/V_{IN})	Source impedance=0Ω, P_O=1W	19	20	21	dB
			25	26	27	
			31	32	33	
			35	36	37	
Spread Spectrum Function						
f_{SS_P}	Spread spectrum pattern frequency	f_S= 400kHz (Note 2)		3.2		kHz
		f_S= 500kHz (Note 2)		2.5		
f_{SS_S}	Frequency span of spread spectrum	(Note 2)		±23		%

ELECTRICAL CHARACTERISTICS (CONTINUE)

T_A = 25°C, V_{CC} = 14.4V, R_L = 4Ω, P_O = 1W/CH, AES17 filter, default I2C settings (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
PWM Output Stage						
R_{DSON}	MOSFET ON-resistance	T_J=25°C		400		mΩ
V_{OFFSET}	Output offset voltage	Zero input signal, Gain=20dB			±25	mV
VCC Over Voltage Protection						
V_{OV_SET}	VCC over voltage shutdown set		30.4	32	33.6	V
V_{OV_HYS}	VCC over voltage shutdown hysteresis			0.9		V
VCC Under voltage Protection						
V_{UV_SET}	VCC under voltage shutdown set		3.6	4	4.4	V
V_{UV_HYS}	VCC under voltage shutdown hysteresis			0.25		V
AVDD						
V_{VDD}	VDD pin voltage		5.5	6.05	6.6	V
Over Temperature (OT) Protection						
T_{OT_SD}	Junction temperature for over temperature shutdown	(Note 2)		170		°C
T_{OT_HYS}	Junction temperature for over temperature hysteresis	(Note 2)		15		°C
T_{OT_W}	Junction temperature for the gain of amplifier will decrease	(Note 2)		155		°C
Over Current (OC) Shutdown Protection						
I_{MAX}	Maximum current (Peak output current)			5		A
SDB Pin						
I_{SDB}	SDB pin current			0.1	0.2	μA
DC Detect						
V_{DC}	DC detect threshold			2.9		V
t_{DC}	DC detect step response time				750	ms
Fault Report						
V_{OH_FAULT}	FAULTB pin output voltage for logic high	External 47kΩ pull up resistor to 3.3V	2.4			V
V_{OL_FAULT}	FAULTB pin output voltage for logic low				0.5	V

ELECTRICAL CHARACTERISTICS (CONTINUE)

T_A = 25°C, V_{CC} = 14.4V, R_L = 4Ω, P_O = 1W/CH, AES17 filter, default I2C settings (unless otherwise noted).

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
Load Diagnostics						
R_{DT}	Resistance to detect a short from OUT pin to VCC or ground				200	Ω
R_{OP}	Open circuit detection threshold	Including speaker wires	50	75	100	Ω
R_{ST}	Short circuit detection threshold		0.9	1.2	1.5	Ω
I2C						
V_{SDA_H}	SDA pin output voltage for logic high	R_{I2C}=4.7kΩ, V_{CC}=3.3V or 5V	2.4			V
V_{SDA_L}	SDA pin output voltage for logic low	3mA sink current			0.4	V
C_{I2C}	Capacitance for SCL and SDA pins	(Note 2)			10	pF

DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 2)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
I2C Interface						
f_{SCL}	Serial-clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μs
$t_{HD,\ STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU,\ STA}$	Repeated START condition setup time		0.6			μs
$t_{SU,\ STO}$	STOP condition setup time		0.6			μs
$t_{HD,\ DAT}$	Data hold time		-		-	μs
$t_{SU,\ DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs
t_R	Rise time of both SDA and SCL signals, receiving				300	ns
t_F	Fall time of both SDA and SCL signals, receiving				300	ns

Note 2: Guaranteed by design.

TYPICAL PERFORMANCE CHARACTERISTICS

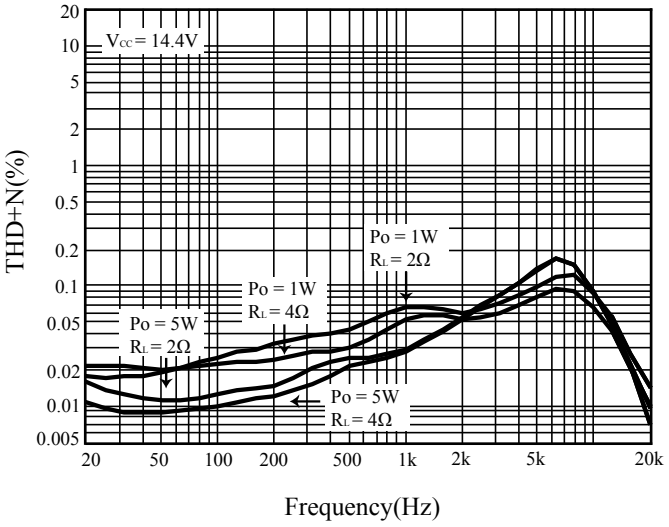


Figure 2 THD+N vs. Frequnecy

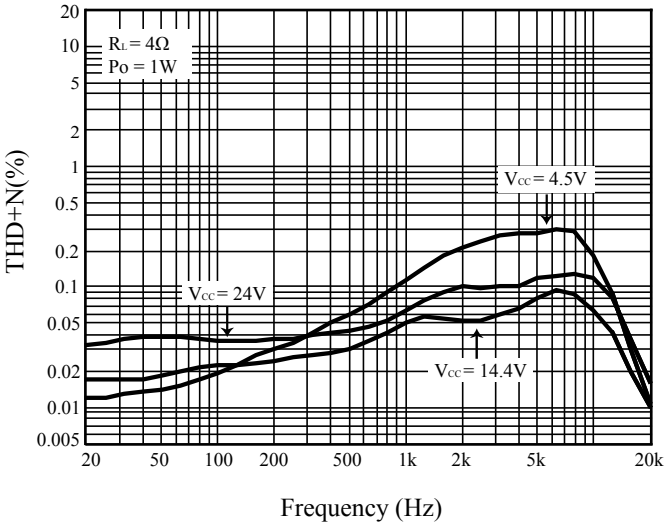


Figure 3 THD+N vs. Frequency

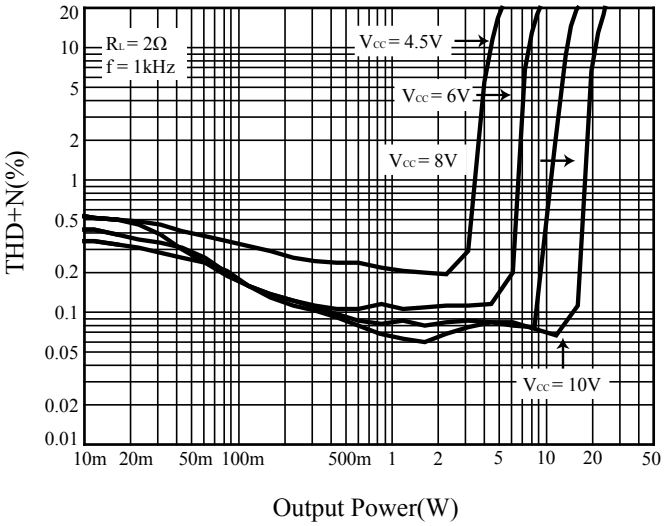


Figure 4 THD+N vs. Output Power

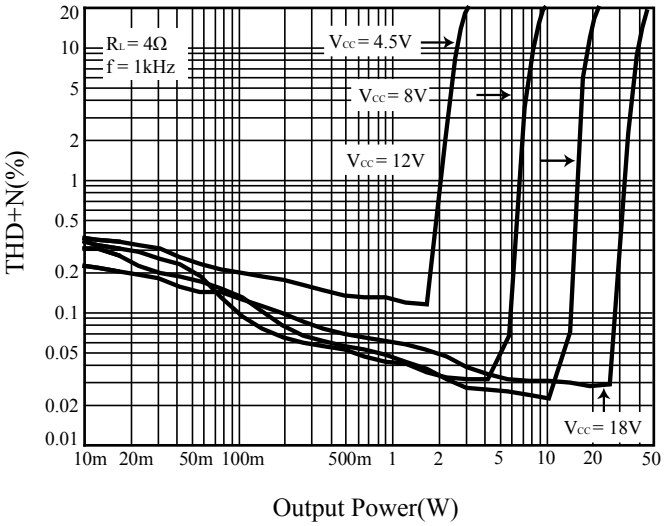


Figure 5 THD+N vs. Output Power

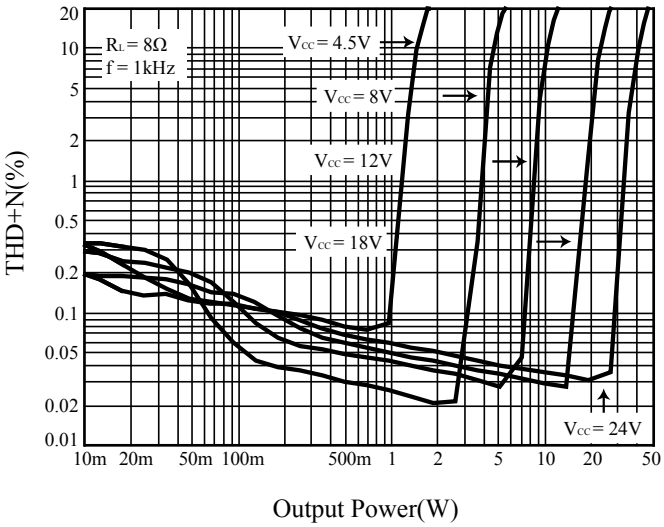


Figure 6 THD+N vs. Output Power

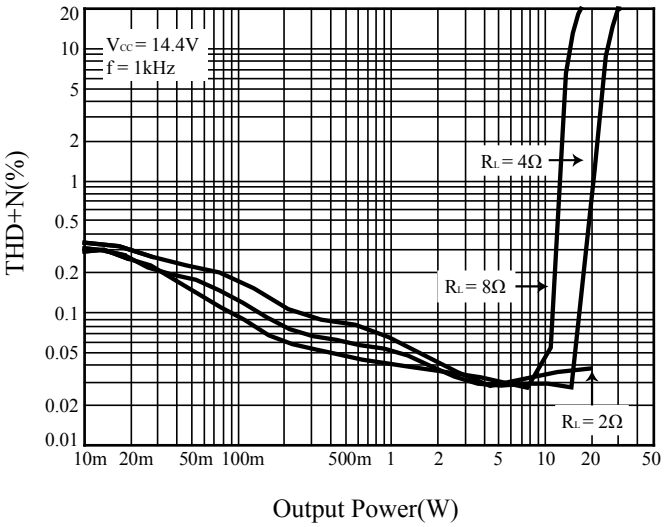


Figure 7 THD+N vs. Output Power

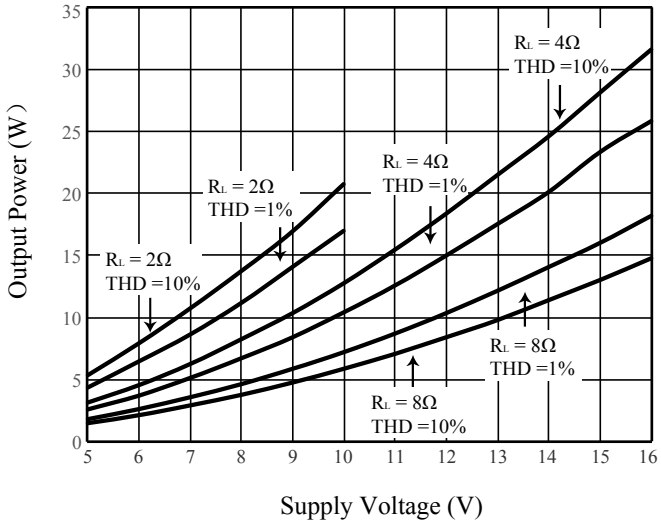


Figure 8 Output Power vs. V_{CC}

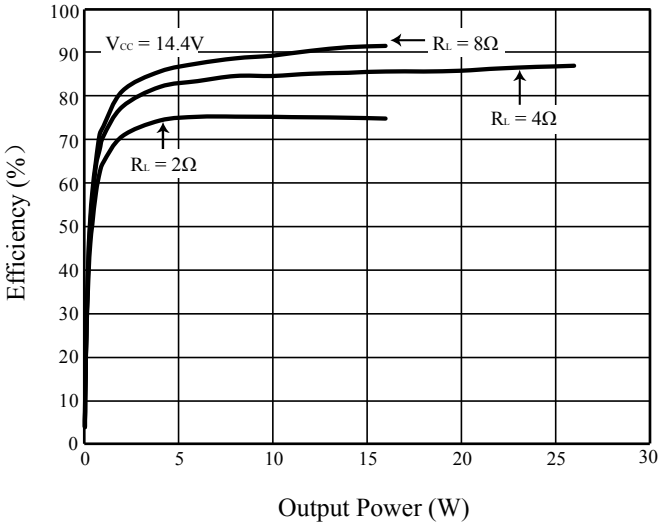


Figure 9 Efficiency vs. Output Power

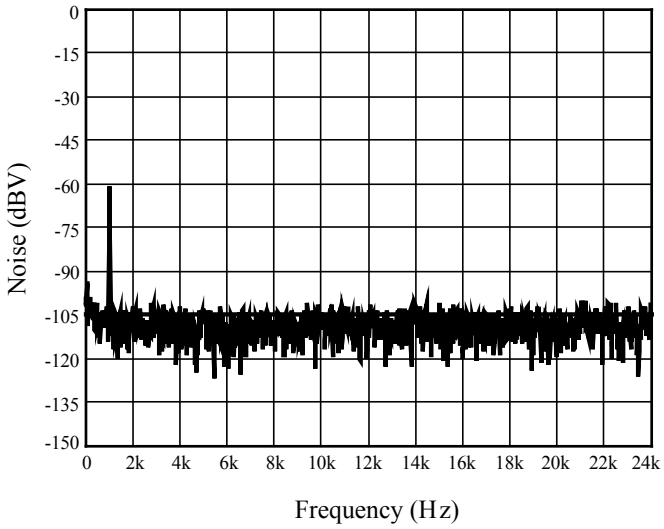


Figure 10 Noise FFT With -60dB Output

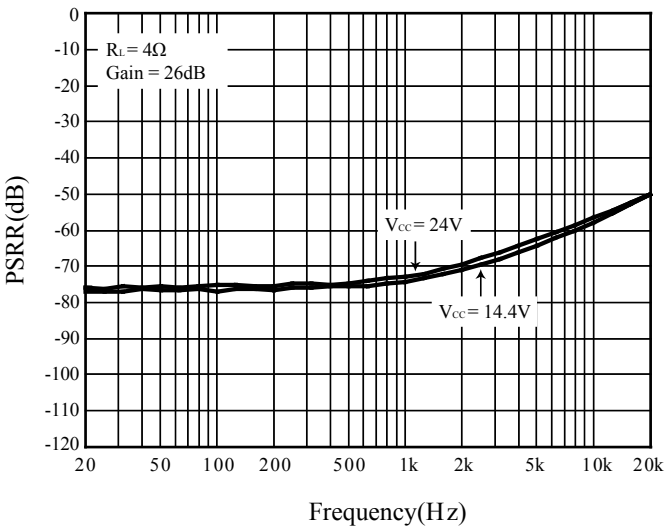
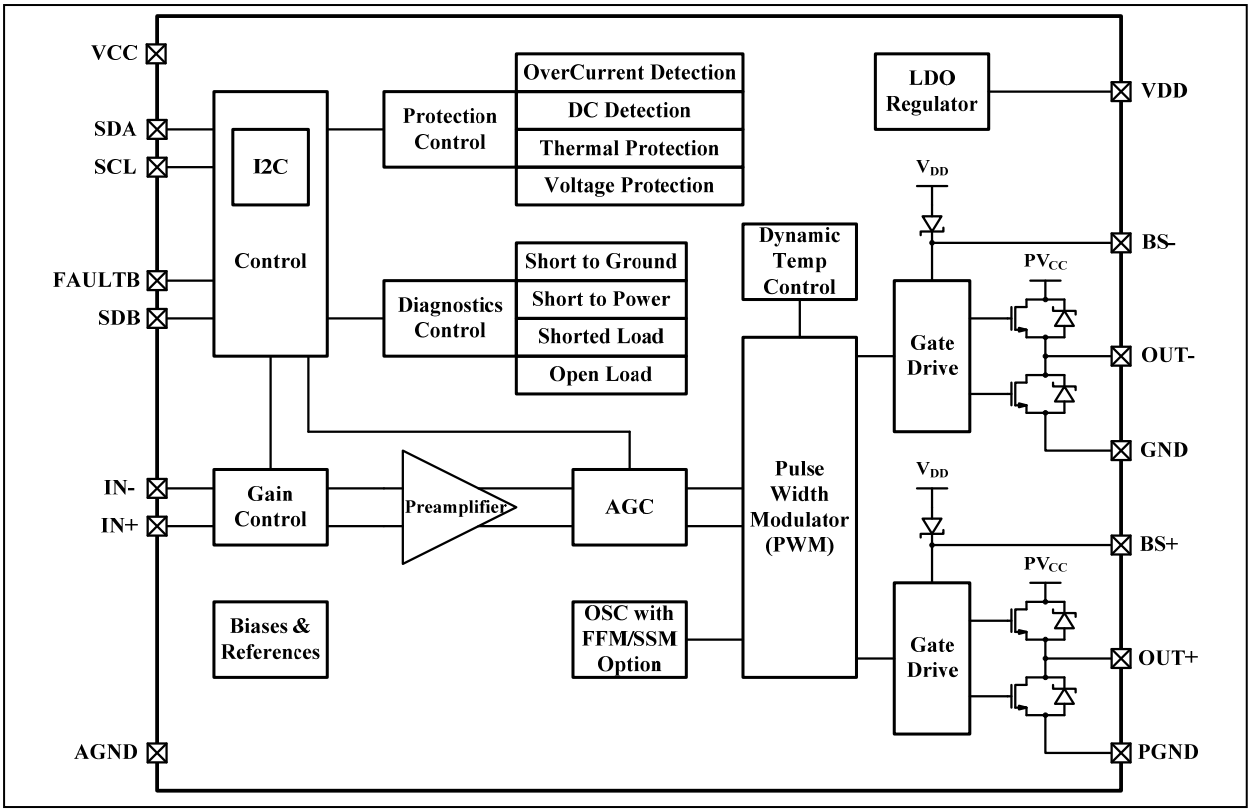


Figure 11 PSRR

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

The IS32AP2123 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS32AP2123 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The complete slave address is:

Table 1 Slave Address

Bit	A7:A1	A0
Value	1110 001	0/1

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS32AP2123.

The timing diagram for the I2C is shown in Figure 8. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS32AP2123's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS32AP2123 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS32AP2123, the register address byte is sent, most significant bit first. IS32AP2123 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS32AP2123 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

READING OPERATION

To read the register, after I2C start condition, the bus master must send the IS32AP2123 device address with the R/$\overline{W}$ bit set to "0", followed by the register address which determines which register is accessed. Then restart I2C, the bus master should send the IS32AP2123 device address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS32AP2123 to the master (Figure 15).

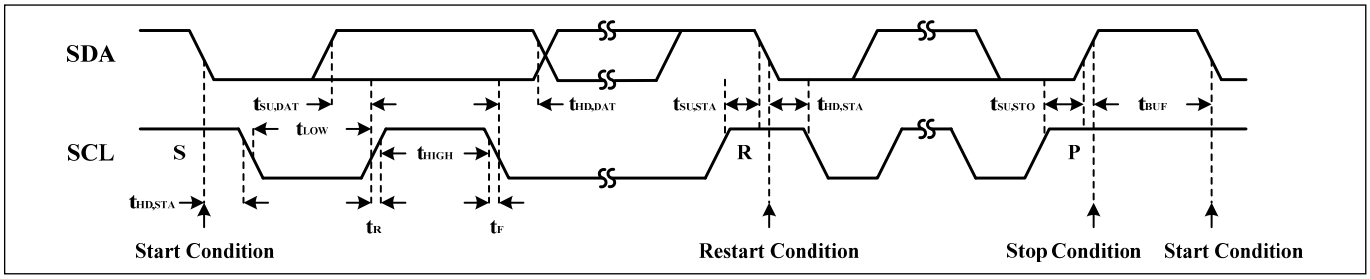


Figure 12 Interface Timing

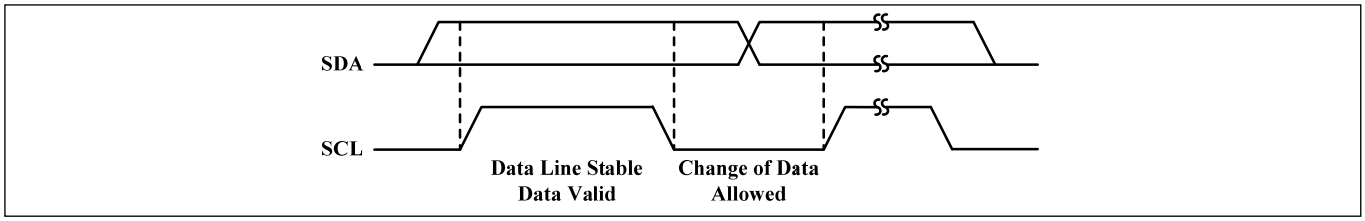


Figure 13 Bit Transfer

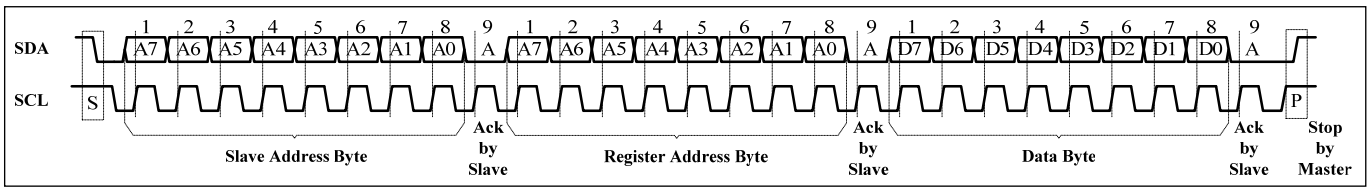


Figure 14 Writing to IS32AP2123 (Typical)

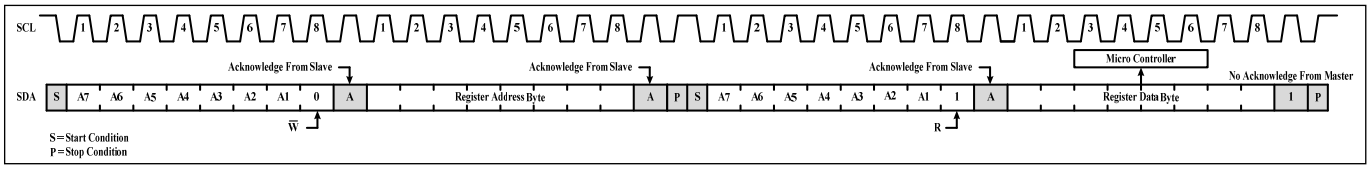


Figure 15 Reading from IS32AP2123

Table 2 Register Definitions

Address	Name	Function	R/W	Table	Default
10h	Status Register	Shows operating and load diagnostic state.	R	3	0000 0000
11h	Fault Register	Shows fault protection state		4	
12h	Load Diagnostics Register	Shows short/open state		5	0000 0000
13h	Control Register	Operating control setting	R/W	6	0111 1000
14h	Load Diagnostics Control Register	Load Diagnostics setting	R/W	7	0000 0000

Table 3 10h Status Register

Bit	D7	D6	D5	D4	D3:D0
Name	PM	MM	PLD	FT	-
Default	0	0	0	0	0000

The register shows operating and load diagnostic state.

PM Play Mode State
0 No
1 Occur

MM Mute Mode State
0 No
1 Occur

PLD Performing Load Diagnostics
0 No
1 Occur

FT Fault Condition State
0 No
1 Occur

Table 4 11h Fault Register

Bit	D7	D6	D5	D4
Name	OT	DCO	VOV	VUV
Default	0	0	0	0
Bit	D3	D2	D1:D0	
Name	OC	LDF	-	
Default	0	0	00	

Self-cleared when fault condition disappears and this register is read after that.

OT Over Temperature Shutdown State
0 No
1 Occur

DCO DC Offset Protection State
0 No
1 Occur

VOV VCC Over Voltage State
0 No
1 Occur

VUV VCC Under Voltage State
0 No
1 Occur

OC Over Current Shutdown State
0 No
1 Occur

LDF A Load-Diagnostics Fault State
0 No
1 Occur

Table 5 12h Load Diagnostics Register

Bit	D7	D6	D5	D4	D3:D0
Name	SL	OL	SG	SV	-
Default	0	0	0	0	0000

Self-cleared when fault condition disappears and this register is read after that.

SL Short Load Status
0 No
1 Occur

OL Open Load Status
0 No
1 Occur

SG Short to Ground
0 No
1 Occur

SV Short to VCC
0 No
1 Occur

Table 6 13h Control Register

Bit	D7:D6	D5:D3	D2	D1	D0
Name	GS	APLS	SM	SSM	SF
Default	01	111	0	0	0

GS Gain setting
00 20dB
01 26dB
10 32dB
11 36dB

APLS AGC Power Limit Setting
000 5.4V peak output
001 6.2V peak output
010 7.1V peak output
011 8.6V peak output
100 10V peak output
101 12V peak output
110 13.7V peak output
111 AGC Disable

SM Software Mute Setting
0 No Mute
1 Mute

SSM Spread-Spectrum Mode Setting
0 No Spread-spectrum
1 Spread-spectrum

SF Switching Frequency Setting
0 400kHz
1 500kHz

Table 7 14h Load Diagnostics Control Register

Bit	D7:D1	D0
Name	-	LDC
Default	0000 000	0

The Load Diagnostics Control Register controls the on or off of Load Diagnostics.

LDC Load Diagnostics State
0 Load Diagnostics enable
1 Load Diagnostics disable

TYPICAL APPLICATION INFORMATION

OVERVIEW

The IS32AP2123 is a Class-D audio amplifier for driving a mono speaker in BTL (Bridge-Tied-Load) configuration. It is capable of delivering 20W into 4Ω speaker at less than 1% THD+N from a 14.4V power supply.

It is a mono Class-D audio amplifier designed for automotive applications, such as emergency call (eCall), telematics, and instrument cluster, and infotainment applications. With a wide operating voltage range of 4.5V to 24V makes it ideal for start/stop or backup battery operation.

The IS32AP2123 comes with onboard load diagnostic hardware accessible via a standard I2C port. The internal diagnostics evaluate the output impedance to check for shorts across the outputs, to the battery, or to ground. The I2C interface allows the system to reads of diagnostic and protection device parameters.

The integrated 40V load-dump protection reduces external voltage clamp cost and size, for reliable automotive audio systems. And the onboard load diagnostics report the status of the speaker through I2C.

FEATURE DESCRIPTION

Analog Audio Input and Preamplifier

The differential preamplifier input stage serves to cancel common-mode noise that may appear on the inputs. For a differential audio source, connect the positive lead to IN+ and the negative lead to IN-. The inputs must be ac-coupled to minimize the output dc-offset and ensure correct ramping of the output voltages. For good transient performance, the impedance seen at each of the two differential inputs should be the same.

Programmable Gain Control

The IS32AP2123's 2-bit gain setting is programmed through the I2C interface (Table 6 13h Control Register). Changing the gain will impact the analog input impedance of the amplifier. The logic table shown in Table 8 highlights the amplifier gain settings in dB and the resulting input impedance.

Bootstrap Capacitors

The output stage uses dual NMOS transistors; therefore, the circuit requires bootstrap capacitors for the high side of each output to turn on correctly. The required capacitor connection is from BS+ to OUT+ and from BS- to OUT- as shown in Figure 1.

Analog Audio Input Filter

The circuit requires an input capacitor to allow biasing of the amplifier put to the proper dc level. The input capacitor and the input impedance of the amplifier form a high-pass filter with a -3dB corner frequency determined by the equation: $f = 1 / (2 \pi R_{IN} C_{IN})$, where R_{IN} is the input impedance of the device based on the gain setting and C_{IN} is the input capacitor value. Use a capacitor which matches the application need for the lowest frequency.

Table 8 Input Impedance and Gain

Gain	Input Impedance
20dB	60kΩ±20%
26dB	30kΩ±20%
32dB	15kΩ±20%
36dB	9kΩ±20%

Pulse-Width Modulator (PWM)

The PWM block converts the analog signal from the preamplifier into a switched signal of varying duty cycle. PWM is generated by comparing the differential audio signal with an internally generated high frequency sawtooth waveform. This internal modulator is an advanced design with high bandwidth, low noise, low distortion, and excellent stability.

The IS32AP2123 uses a pulse-width modulation scheme with each output switching from 0 to the supply voltage; this allows increased efficiency at low power.

The IS32AP2123 outputs OUT+ and OUT- are designed to switch from 0V to VCC. If there is no input, the OUT+ and OUT- pins are in phase with each other, so that there is little or no current in the speaker. When a positive signal is applied, the duty cycle of OUT+ is greater than 50% and OUT- is less than 50%. The duty cycle of OUT- is greater than 50% and that of OUT+ is less than 50% for negative output voltages. With this configuration, there is minimal to no current through the speaker most of the switching period and thus power losses are lowered.

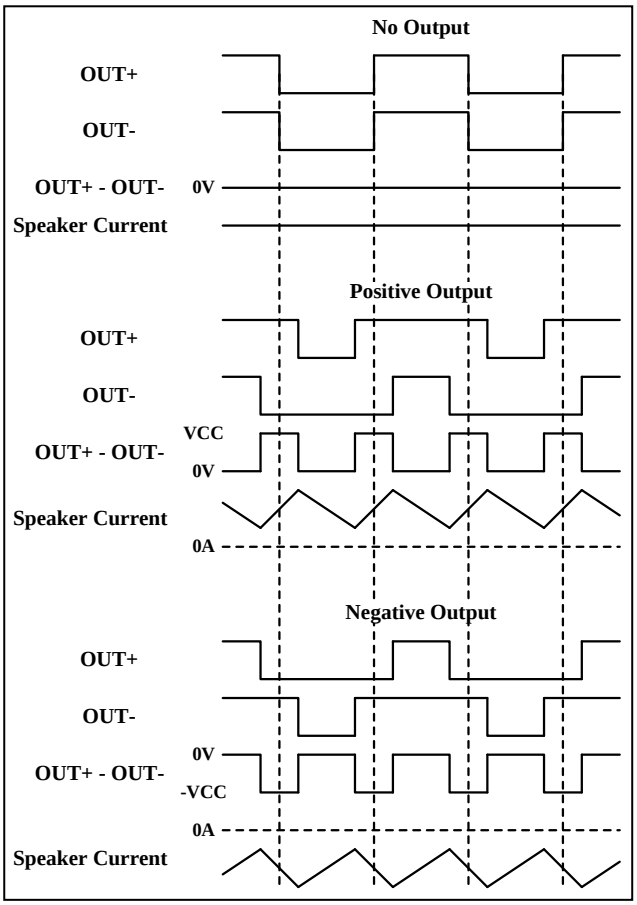


Figure 16 Output Modulation

Gate Drive

The gate driver accepts the low-voltage PWM signal and level shifts it to drive a high-current, full-bridge, power FET stage. The device implements a controlled rising/falling gate drive to optimize EMI and audio performance.

AM Avoidance

In order to assure EMC in an AM, AP2123 provides a special function. By means of I2C interface, a suitable switching frequency (400kHz or 500kHz) can be set depending on the AM station selected by the tuner.

Power FETs

The BTL output comprises four matched N-channel FETs for high efficiency and maximum power transfer to the load. By design, the FETs withstand large voltage transients during a load-dump event.

Load Diagnostics

The device incorporates load diagnostic circuitry designed for detecting and determining the status of output connections. The device supports the following diagnostics:

- Short to GND
- Short to VCC
- Short across load
- Open load

The device reports the presence of any of the short or open conditions to the system via I2C register read. And enable or disable this function by LDC bit of 14h register. Note that the result is only valid when power supply is 7.5V~24V.

Load Diagnostics - The load diagnostic function runs at start-up or when the device is in a fault state (DC detect, overcurrent, overvoltage, undervoltage, and overtemperature). During this test, the outputs are in a Hi-Z state. The device determines whether the output is a short to GND, short to VCC, open load, or shorted load. The load diagnostic biases the output, which therefore requires limiting the capacitance value for proper functioning; see the Recommended Operating Conditions. The load diagnostic test takes approximately 260ms to run. Note that the check phase repeats if a fault is present or a large capacitor to GND is present on the output. On detection of an open load, the output still operates. On detection of any other fault condition, the output goes into a Hi-Z state, and the device checks the load continuously until removal of the fault condition. After detection of a normal output condition, the audio output starts. The load diagnostics run after every other overvoltage (OV) event.

The device performs load diagnostic tests as shown in Figure 17.

Figure 18 illustrates how the diagnostics determine the load based on output conditions (OL is R_{OP} and SL is R_{ST}).

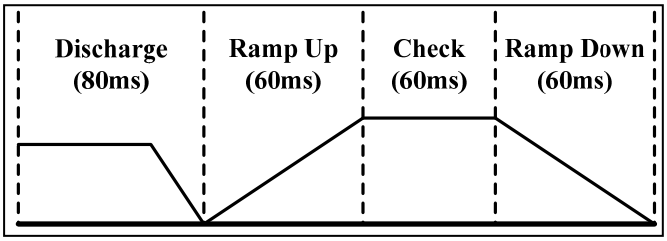


Figure 17 Load Diagnostics Sequence of Events

	Output Conditions	Load Diagnostics
OL Max.	Open Load	Open Load Detected
OL Min.	Open Load (OL) Detection Threshold	Normal or Open Load May Be Detected
SL Max.	Normal Load	Play Mode
SL Min.	Shorted Load (SL) Detection Threshold	Normal or Shorted Load May Be Detected
	Shorted Load	Shorted Load Detected

Figure 18 Load Diagnostic Reporting Thresholds

Faults During Load Diagnostics - If the device detects a fault (overtemperature, overvoltage, undervoltage) during the load diagnostics test, the device exits the load diagnostics, which may result in a pop or click on the output.

Protection and Monitoring

The IS32AP2123 is fully protected against undervoltages, overvoltages, overcurrents, DC input and thermal overloads as explained here.

Overcurrent Shutdown (OCSD) - If the output current exceeds the value for I_{MAX} the overcurrent protection is activated which forces the outputs to the high-impedance state. Periodically, the device attempts to restart. If the overcurrent condition is still present then the OCSD remains active. The device asserts LOW the FAULTB pin and updates the I2C register.

DC Detect - This circuit checks for a DC offset continuously during normal operation at the output of the amplifier. If a DC offset occurs, the device asserts the FAULTB pin and updates the I2C register. Note that the DC detection threshold follows VCC changes.

Dynamic Temperature Control (DTC) - the DTC function is designed to protect the IC from overheating. As the junction temperature is higher than T_{OT_W}, the gain of amplifier will decrease. Finally, as the junction temperature is around T_{OT_W}, the attenuated gain steps will be released when junction temp falls below T_{OT_W}. If DTC can't suppress the temperature and the temperature reach to the T_{OT_SD} trip point (170°C), the amplifier will be shutdown. Typically, T_{OT_W} is 155°C.

Overtemperature Shutdown (OTSD) - If the die junction temperature, T_J, reaches 170°C (T_{OT_SD}), the device shuts down, the outputs are forced to the high-impedance state, the FAULTB pin is pulled LOW and the I2C register is updated. Recovery is automatic when the temperature returns to a safe level.

Undervoltage (UV) - If the supply voltage drops below the value for V_{UV_SET} given in the Electrical specifications table, the undervoltage protection is activated which forces the outputs to the high-impedance state. In the event of an undervoltage condition, the device asserts the FAULTB pin and resets the I2C register.

Overvoltage (OV) and Load Dump - If the supply voltage exceeds the value for V_{OV_SET} the overvoltage protection is activated which forces the outputs to the high-impedance state. If VCC reaches the overvoltage threshold, the device asserts LOW the FAULTB pin and updates the I2C register. The device can withstand 40V load-dump voltage spikes. When the supply voltage falls back to within the operating range the device restarts and FAULTB pin returns to a HIGH state.

Adjacent-Pin Shorts - The device design is such that shorts between adjacent pins do not cause damage.

AGC (Automatic Gain Control) Control Function

This is the function to limit the output power to fit different models of speaker, to protect the speakers from over stress of power. When output power goes over selected power limit level, AGC control function will be activated, the gain of amplifier will decrease to bring output power back under the limit. Different to simple output power limit function, AGC control function of IS32AP2123 can limit power while not causing any clipping at the differential signal output. The sound quality will not be hurt when the AGC is activated.

The power limit of the AGC can be selected through I2C.

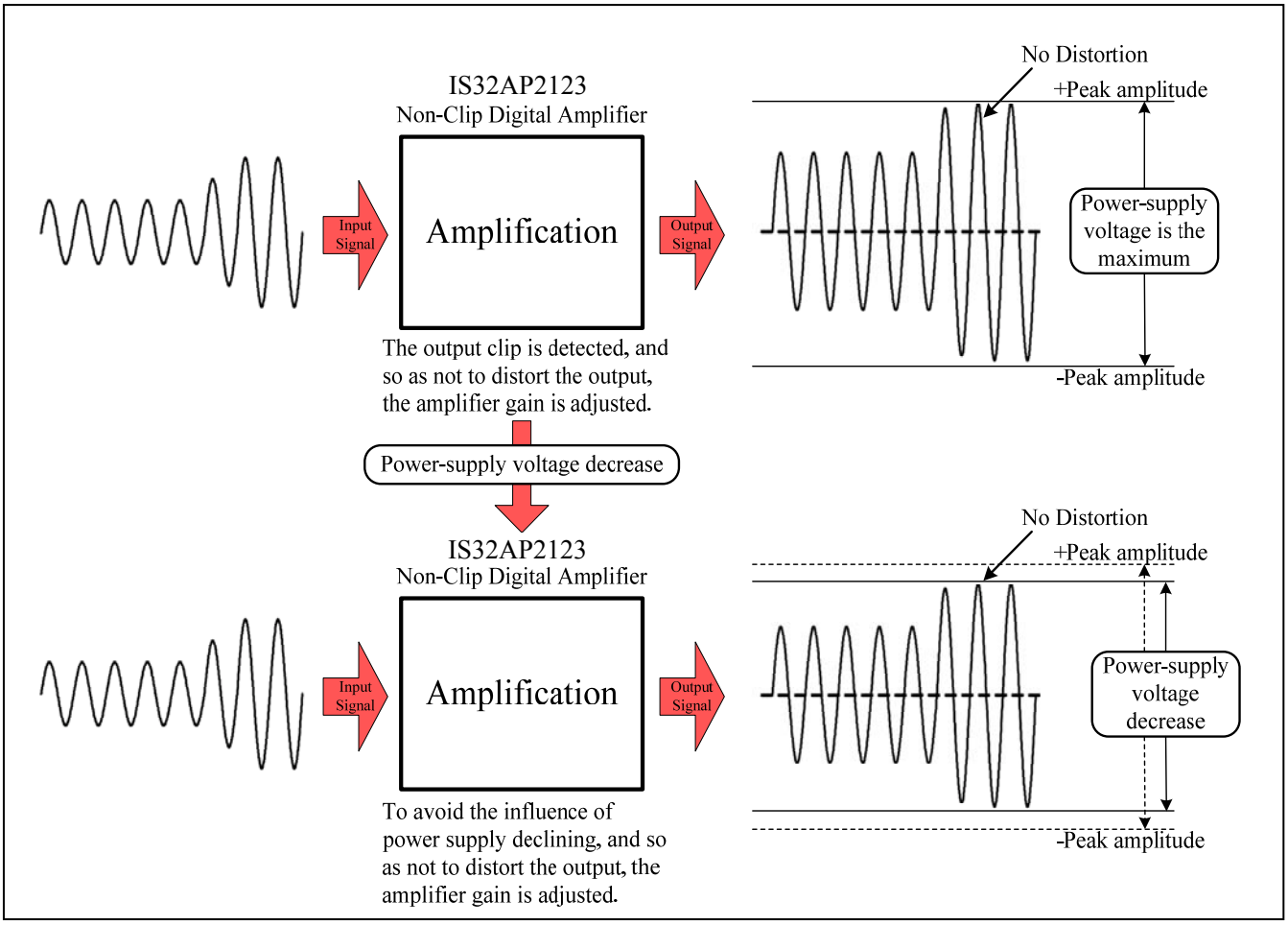


Figure 19 Operation Outline of AGC Control Function

To eliminate any possible interruption to the music, the adjustment of gain is not a steep jumping from default value to target value. It is a step by step adjustment with digitalized tiny step size and fixed interval. The attack time, which is the transition period from default gain to attenuated gain, is about 55ms. The release time, which is the recovery period from attenuated gain back to default gain, is about 1.5s. Both attack and release time vary with the input value and selected output limit.

Assuming no limitation by the power supply, the audio output signal would be as in Figure 20.

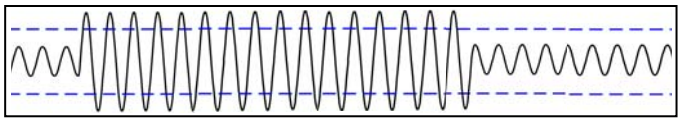


Figure 20 Assuming no Restriction from Power Supply, the Audio Output Signal

In normal operation without the AGC, the output is distorted because of the restriction from power supply, as shown in Figure 21.

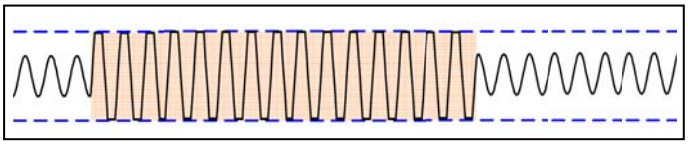


Figure 21 AGC Function Off

With the AGC function of IS32AP2123, the optimum output power can be obtained along with the minimal distortion. The Figure 22 shows the outcome of AGC function.

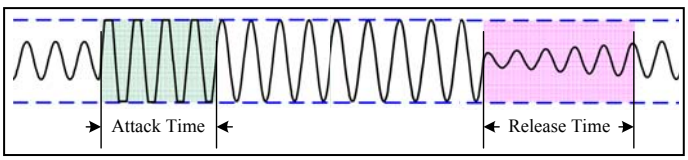


Figure 22 AGC Function On

DEVICE FUNCTIONAL MODES

Hardware Control Pins

There are two discrete hardware pins for real-time control and indication of device status.

FAULTB pin: This active-low open-drain output pin indicates the presence of a fault condition which requires the device to go into the high impedance

mode. On assertion of this pin, the device has protected itself and the system from potential damage. The system can read the exact nature of the fault via I2C.

SDB pin: Assertion of this active-low pin sends the device into a complete shutdown, limiting the current draw.

EMI Considerations

Automotive-level EMI performance depends on both careful integrated-circuit design and good system-level design. Controlling sources of electromagnetic interference (EMI) was a major consideration in all aspects of the design.

The design has minimal parasitic inductances due to the short leads on the package. This dramatically reduces the EMI that results from current passing from the die to the system PCB. The design incorporates circuitry that optimizes output transitions that cause EMI. To help minimize EMI, the PWM switching frequency can be set to either 400kHz or 500kHz by programming the switch frequency register in Table 6 13h Control Register.

Spread Spectrum Function - To optimize the EMI performance, the IS32AP2123 includes a spread spectrum feature. In spread spectrum mode, the switching frequency keeps changing around a central frequency of 400kHz/500kHz, reducing the wideband spectral contend, improving EMI emissions radiated by the speaker and associated cables and traces. Where a fixed frequency Class-D exhibits large amounts of spectral energy at multiples of the switching frequency, the spread spectrum architecture of the IS32AP2123 spreads that energy over a larger bandwidth. The cycle-to-cycle variation of the switching period does not affect the audio reproduction, efficiency, or PSRR.

Operating Modes and Faults

The following tables list operating modes and faults.

Table 9 Operating Mode

State Name	Output	Oscillator	I2C
Shutdown	Hi-Z	Stopped	Stopped
Load diagnostic	DC biased	Active	Active
Fault and mute	Hi-Z	Active	Active
Play	Switching with audio	Active	Active

Table 10 Faults and Actions

Fault/Event	Monitoring Modes	Reporting Method	Action Result (Output)	Clearing
UV or OV	Hi-Z, mute, play	I2C+FAULTB pin	Hi-Z (Note 8)	Self-clearing
OTSD	Hi-Z, mute, play		Hi-Z (Note 9)	
OC fault	Play			
DC detect				
Load diagnostic-short	Hi-Z		Hi-Z (Note 9), re-run diagnostics	
Load diagnostic-open		I2C	None	

Note 8: Hi-Z impedance is about 500kΩ to ground.
Note 9: Hi-Z impedance is about 48kΩ to ground.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

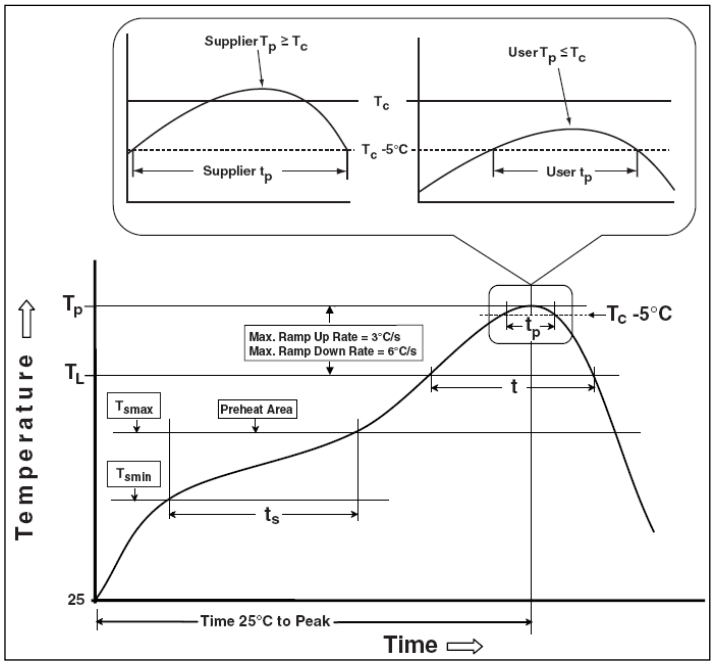
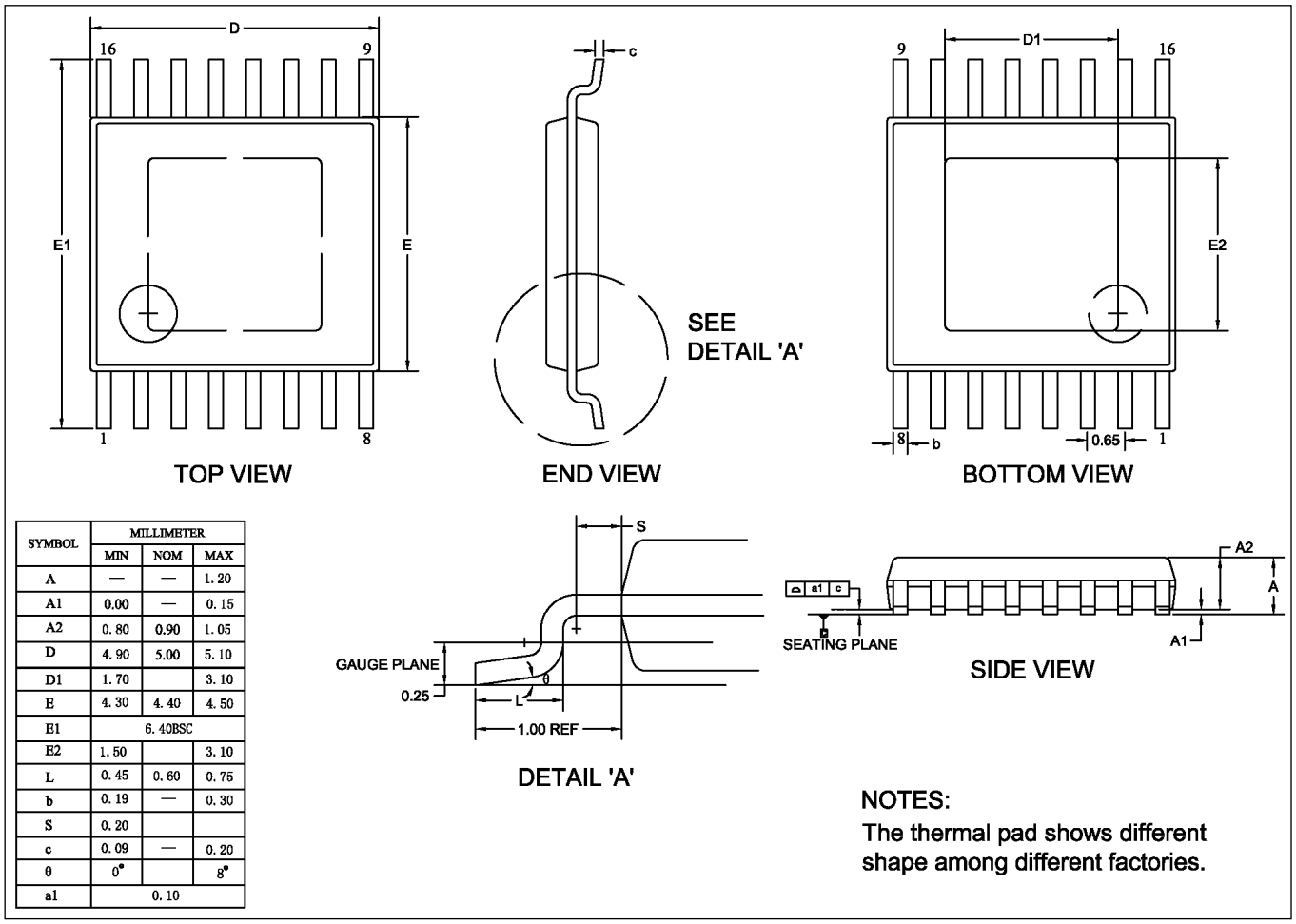


Figure 23 Classification Profile

PACKAGE INFORMATION

eTSSOP-16

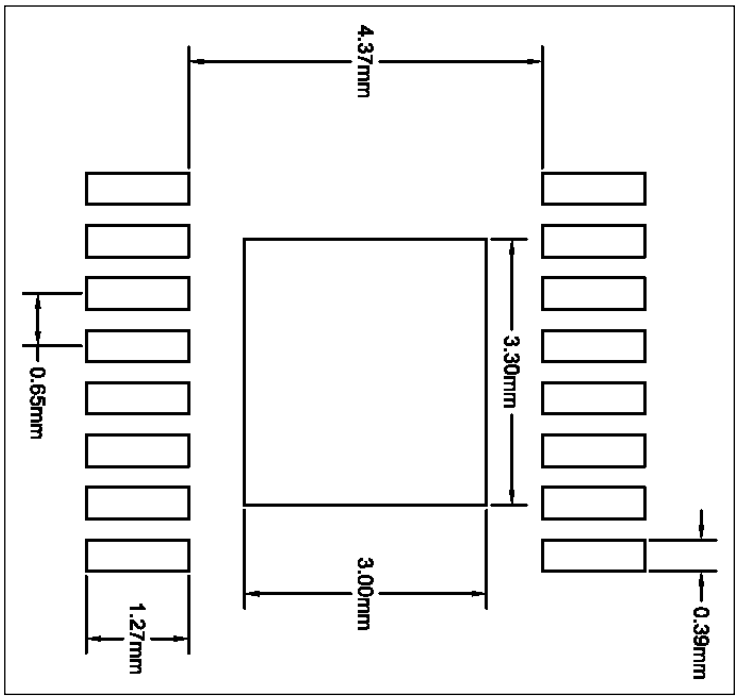


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.20
A1	0.00	—	0.15
A2	0.80	0.90	1.05
D	4.90	5.00	5.10
D1	1.70		3.10
E	4.30	4.40	4.50
E1	6.40BSC		
E2	1.50		3.10
L	0.45	0.60	0.75
b	0.19	—	0.30
S	0.20		
c	0.09	—	0.20
θ	0°		8°
a1	0.10		

NOTES:
The thermal pad shows different shape among different factories.

RECOMMENDED LAND PATTERN

eTSSOP-16



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. user's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
0A	Initial release.	2019.09.02
A	Update to final version and update land pattern	2020.07.07