IS31SE5114

15-CH PROGRAMMABLE CAPACITIVE TOUCH SENSOR

September 2019

GENERAL DESCRIPTION

The IS31SE5114 is an ultra-low power, fully integrated 15-channel solution for capacitive touch-buttons applications. The chip allows electrodes to project sense fields through any dielectric such as glass or plastic. On-chip calibration logic continuously monitors the environment and automatically adjusts on-and-off threshold levels to prevent false sensor activation.

The IS31SE5114 supports the 400kHz I²C serial bus data protocol and includes a field programmable slave address. An INTB is generated when a button event (touched or released) occurs, triggered and cleared condition could be configured by setting the interrupt register.

The built-in LCD controller can support up to 8 common and 28 segment output with ½ , ⅓ or ¼ bias. When configured as LED controller, it supports a direct-drive mode that can drive up to 8 SEG by 15 digits with 64-level brightness control.

Many peripheral functions are also embedded in the chip such as UART, EUART with LIN capability, one I2C master/slave and two I2C pure slave controllers, one SPI master/slave controller, PWMs, GPIOs, etc. Unused touch key and/or LED/LCD pins can be programmed for selected I/O function. User can refer to the Technical Reference Manual, TRM-5114_R1 for detail.

IS31SE5114 is available in LQFP-64 package. It operates from 2.7V to 5.5V over the temperature range of -40°C to +105°C.

FEATURES

- Fifteen sensors capacitive touch controller with readable key value through shared GPIO
- Individual sensitivity threshold setting for each key
- Optional multiple-key function
- Press and hold function
- Automatic calibration
- Individual key calibration
- Interrupt output with auto-clear and repeating
- Auto sleep mode for extremely low power
- Keys wake up from sleep mode
- 400kHz fast-mode I²C interface
- One SPI master/slave controllers
- One 8051 UART
- One full-duplex LIN-capable EUART2
- LCD Controller
  - 32 x 4, 31 x 5, 30 x 6, 29 x 7, 28 x 8
  - ½ , ⅓ or ¼ bias and 8 brightness
- LED Controller
  - Up to 8 SEG x 15 DIGIT common cathode direct drive
  - Up to 8 COM x 28 SEG external drive
  - Programmable 64 brightness
- Operating temperature is -40°C ~ +105°C
- LQFP-64 package

APPLICATIONS

- Home appliance control keys
- Industrial touch keys

TYPICAL APPLICATION CIRCUIT (LQFP-64)

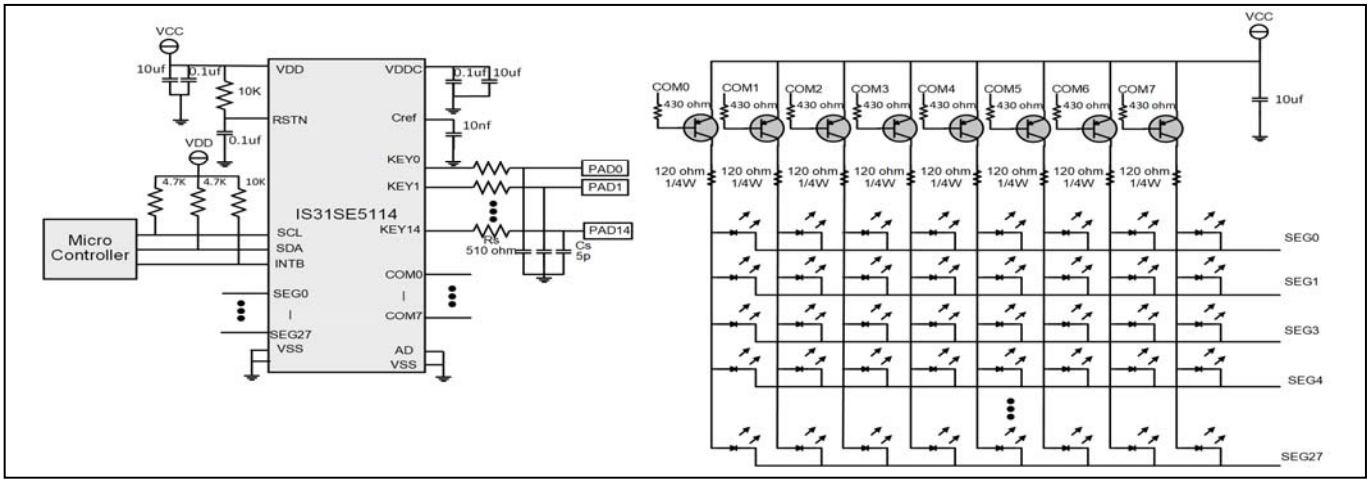
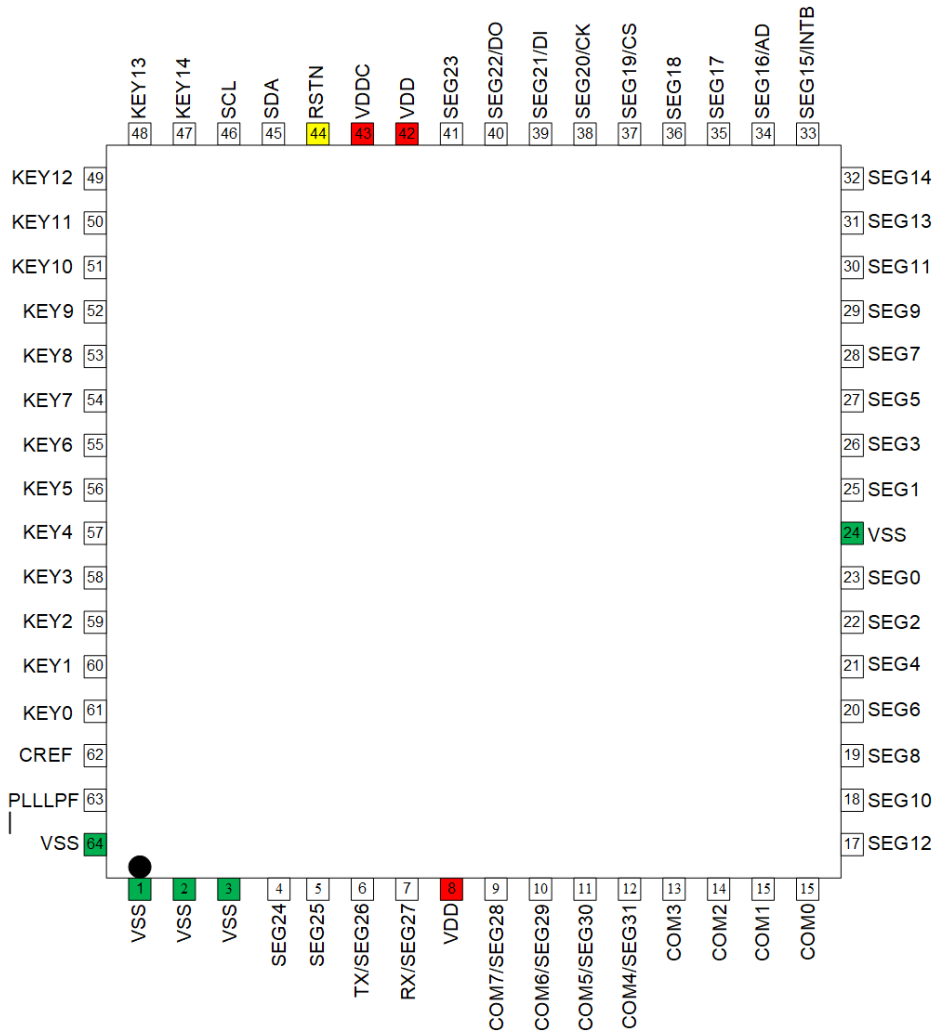


Figure 1 Typical Application Circuit (LQFP-64)

Note 1: The IC should be placed far away from the noise points in order to prevent the EMI.

Note 2: The R_S and C_S should place as close to IC as possible to reduce EMI.

PIN CONFIGURATION

Package	Pin Configuration (Top View)
LQFP-64	

PIN DESCRIPTION

No.	Pin	Description
8, 42	VCC	Power supply.
4 – 7	SEG24 – SEG27	These pins can be configured as LED/LCD SEG driver.
9 – 12	SEG28 – SEG31 / COM7 -COM4	These pins can be configured as LED/LCD SEG driver. These pins can be configured as LED/LCD COM driver.
13 – 16	COM3 – COM0	These pins can be configured as LED/LCD COM driver.
17 – 23	SEG12, SEG10, …, SGE0	These pins can be configured as LED/LCD SEG driver.
25 – 31	SEG 1, SEG3, …, SEG13	These pins can be configured as LED/LCD SEG driver.
32 – 41	SEG14 – SEG23	These pins can be configured as LED/LCD SEG driver.
44	RSTN	Reset Low Active.
62	Cref	External Capacitor.
46	SCL	I2C serial clock.

33	INTB	Interrupt output, active low.
34	AD	I2C address setting.
45	SDA	I2C serial data
61 – 47	KEY0 – KEY14	Input sense channel 0 - 14
24, 64	GND	Ground.
43	VDDC	Typical decoupling capacitors of 0.1μF and 10μF should be connected between VDDC and GND.

ORDERING INFORMATION
Industrial Range: -40°C to +105°C

Order Part No.	Package	QTY
IS31SE5114-LQLS3	LQFP-64, Lead-free	250/Tray

ABSOLUTE MAXIMUM RATINGS

Supply voltage, V_{CC}	-0.3V ~ +6.0V
Voltage at any input pin	-0.3V ~ V_{CC}+0.3V
Maximum junction temperature, T_{JMAX}	+150°C
Storage temperature range, T_{STG}	-65°C ~ +150°C
Operating temperature range, T_A=T_J	-40°C ~ +105°C
Junction Package thermal resistance, junction to ambient (4 layer standard test PCB based on JESD 51-2A), θ_{JA}	53.84°C/W
ESD (HBM) ESD (CDM)	±2kV ±750V

Note 3: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other condition beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, V_{CC} = 2.7V ~ 5.5V, unless otherwise noted. Typical value are T_A = 25°C, V_{CC} = 3.6V.

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{CC}	Supply voltage		2.7		5.5	V
I_{CC}	Quiescent power supply current	V_{CC} = 5.5V		100		μA
I_{SD}	Shutdown current	V_{CC} = 5.5V		15		μA
ΔC_S	Minimum detectable capacitance	C_S = 5pF (Note 4)		0.2		pF
Logic Electrical Characteristics						
V_{IL}	Logic "0" input voltage	V_{CC} = 2.7V			0.4	V
V_{IH}	Logic "1" input voltage	V_{CC} = 5.5V	1.4			V
I_{IL}	Logic "0" input current	V_{INPUT} = 0V (Note 4)		5		nA
I_{IH}	Logic "1" input current	V_{INPUT} = V_{CC} (Note 4)		5		nA

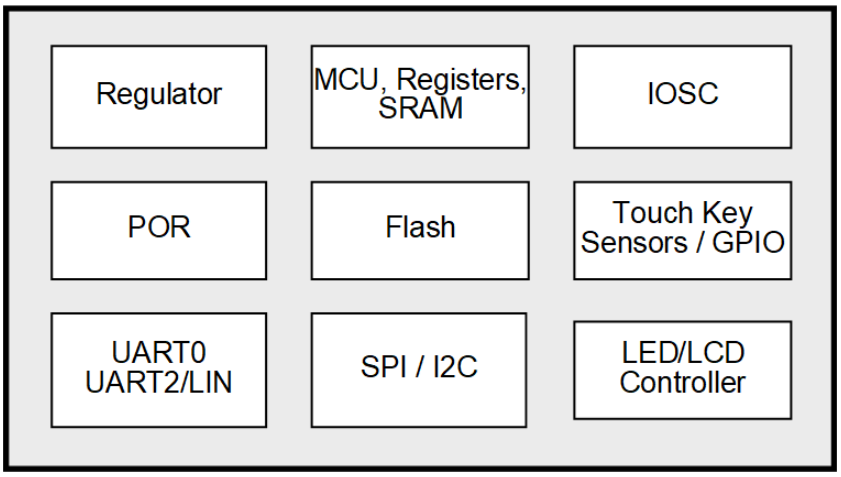
DIGITAL INPUT SWITCHING CHARACTERISTICS (Note 4)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
f_{SCL}	Serial-Clock frequency				400	kHz
t_{BUF}	Bus free time between a STOP and a START condition		1.3			μs
$t_{HD, STA}$	Hold time (repeated) START condition		0.6			μs
$t_{SU, STA}$	Repeated START condition setup time		0.6			μs
$t_{SU, STO}$	STOP condition setup time		0.6			μs
$t_{HD, DAT}$	Data hold time				0.9	μs
$t_{SU, DAT}$	Data setup time		100			ns
t_{LOW}	SCL clock low period		1.3			μs
t_{HIGH}	SCL clock high period		0.7			μs
t_R	Rise time of both SDA and SCL signals, receiving	(Note 5)		20+0.1C_b	300	ns
t_F	Fall time of both SDA and SCL signals, receiving	(Note 5)		20+0.1C_b	300	ns

Note 4: Guaranteed by design.

Note 5: C_b = total capacitance of one bus line in pF. I_{SINK} ≤ 6mA. t_R and t_F measured between 0.3 × V_{CC} and 0.7 × V_{CC}.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

I2C INTERFACE

The IS31SE5114 uses a serial bus, which conforms to the I2C protocol, to control the chip's functions with two wires: SCL and SDA. The IS31SE5114 has a 7-bit slave address (A7:A1), followed by the R/W bit, A0. Set A0 to "0" for a write command and set A0 to "1" for a read command. The value of bits A1 and A2 are decided by the connection of the AD pin.

The complete slave address is:

Table 1 Slave Address

Bit	A7:A3	A2:A1	A0
Value	01111	AD	1/0

AD connected to GND, AD = 00;
AD connected to VCC, AD = 11;
AD connected to SCL, AD = 01;
AD connected to SDA, AD = 10;

The SCL line is uni-directional. The SDA line is bi-directional (open-collector) with a pull-up resistor (typically 4.7kΩ). The maximum clock frequency specified by the I2C standard is 400kHz. In this discussion, the master is the microcontroller and the slave is the IS31SE5114.

The timing diagram for the I2C is shown in Figure 2. The SDA is latched in on the stable high level of the SCL. When there is no interface activity, the SDA line should be held high.

The "START" signal is generated by lowering the SDA signal while the SCL signal is high. The start signal will alert all devices attached to the I2C bus to check the incoming address against their own chip address.

The 8-bit chip address is sent next, most significant bit first. Each address bit must be stable while the SCL level is high.

After the last bit of the chip address is sent, the master checks for the IS31SE5114's acknowledge. The master releases the SDA line high (through a pull-up resistor). Then the master sends an SCL pulse. If the IS31SE5114 has received the address correctly, then it holds the SDA line low during the SCL pulse. If the SDA line is not low, then the master should send a "STOP" signal (discussed later) and abort the transfer.

Following acknowledge of IS31SE5114, the register address byte is sent, most significant bit first. IS31SE5114 must generate another acknowledge indicating that the register address has been received.

Then 8-bit of data byte are sent next, most significant bit first. Each data bit should be valid while the SCL level is stable high. After the data byte is sent, the IS31SE5114 must generate another acknowledge to indicate that the data was received.

The "STOP" signal ends the transfer. To signal "STOP", the SDA signal goes high while the SCL signal is high.

READING PORT REGISTERS

To read the device data, the bus master must first send the IS31SE5114 address with the R/$\overline{W}$ bit set to "0", followed by the command byte, which determines which register is accessed. After a restart, the bus master must then send the IS31SE5114 address with the R/$\overline{W}$ bit set to "1". Data from the register defined by the command byte is then sent from the IS31SE5114 to the master (Figure 5).

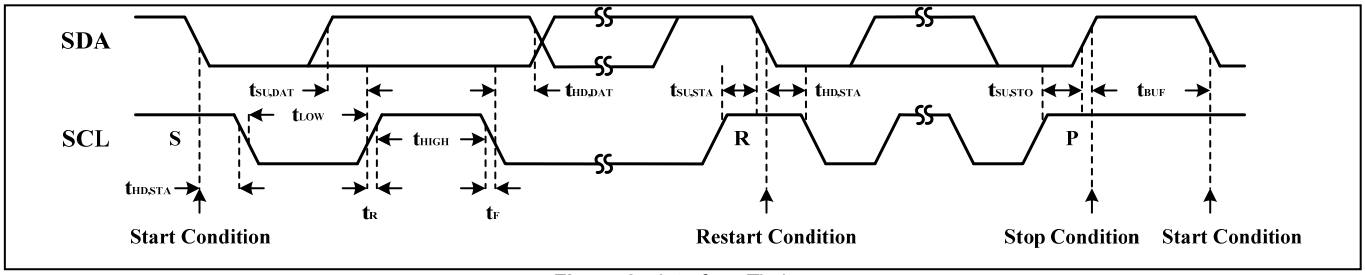


Figure 2 Interface Timing

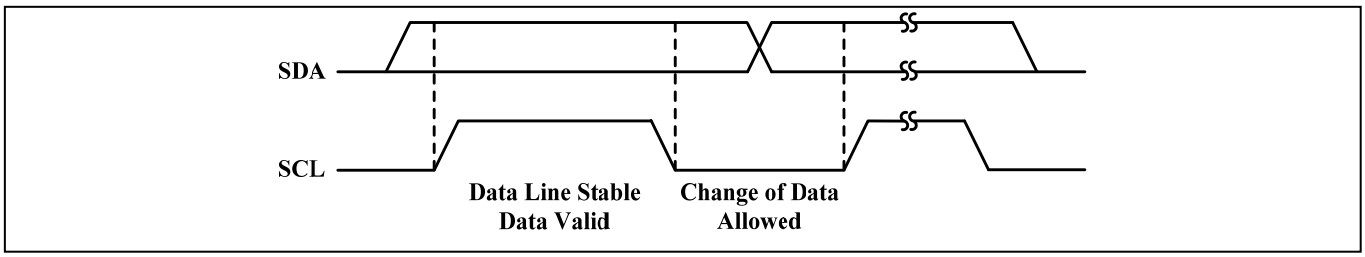


Figure 3 Bit Transfer

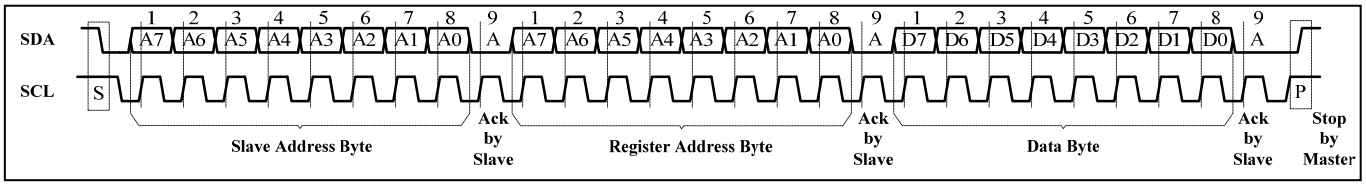


Figure 4 Writing to IS31SE5114

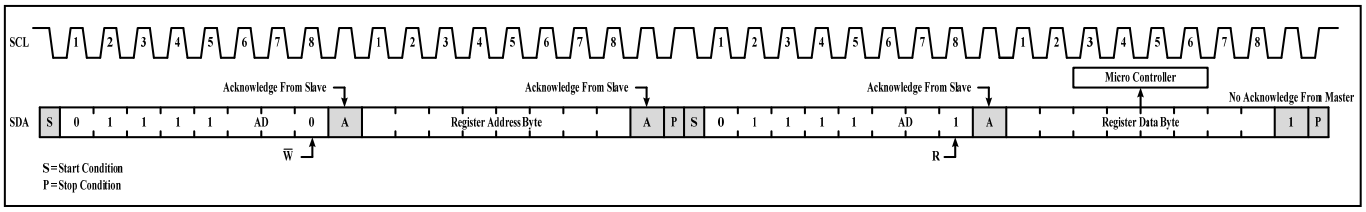
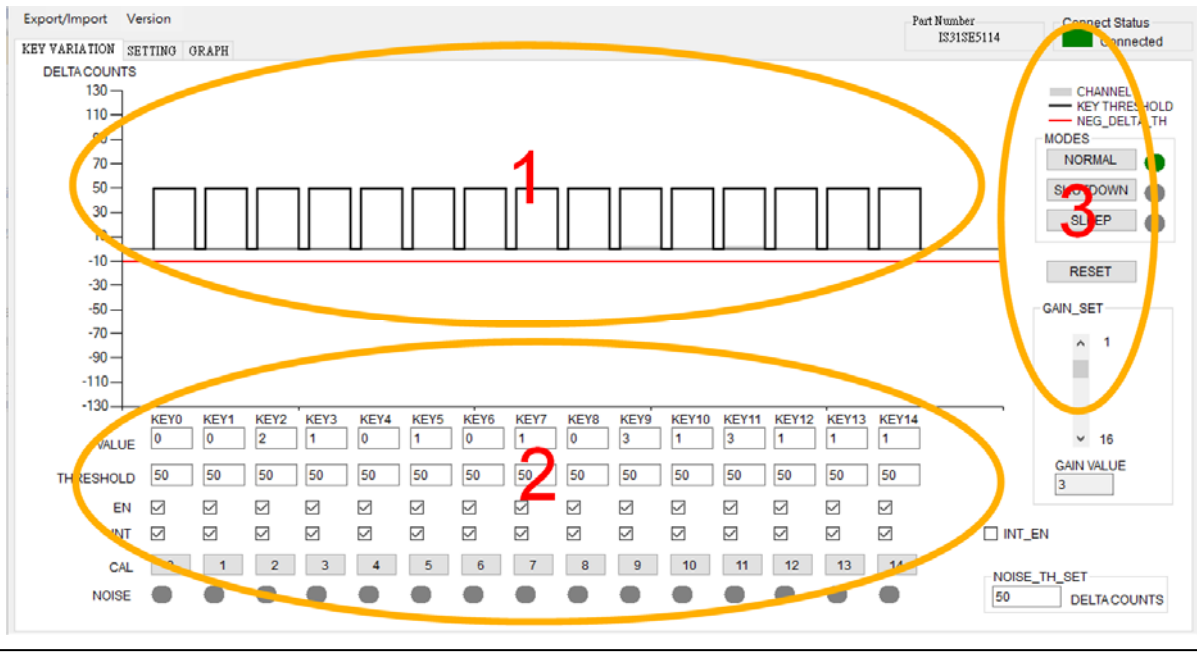


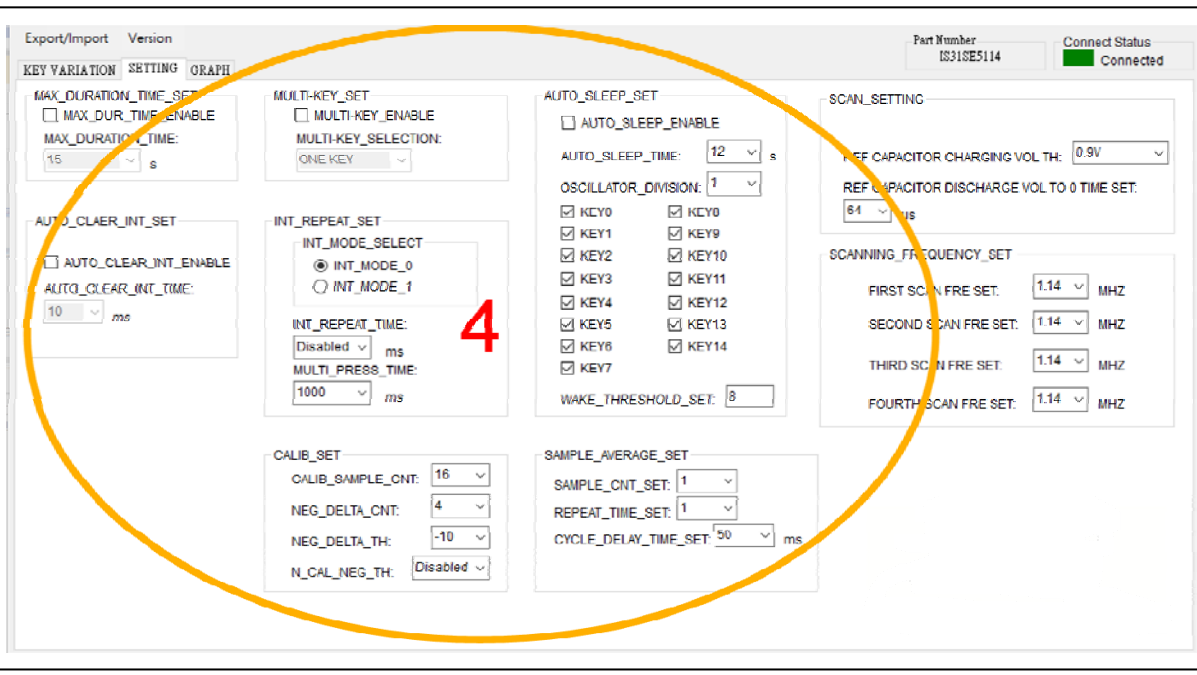
Figure 5 Reading from IS31SE5114

IS31SE5114 GUI

IS31SE5114 GUI is a windows-based Integrated Design Environment (IDE). User can use it to develop touch key applications without firmware coding. With the GUI user can design the touch key system easily. With the GUI you can:

1. Monitor the Key value
2. Set touch threshold and enable keys
3. Switch the operating modes
4. Tune System parameters





FUNCTIONAL DEFINITOIN of KEY PERIPHRALS

The IS31SE5114 is a capacitive touch-sensing controller with MCU. The MCU is based on 1-T 8051 core. Embedded in the MCU core are also a full-duplex UART port, an enhanced EUART port with LIN capability, one I2C master/slave and two I2C pure slave controllers, one SPI marter/slave controller, up to 20 GPIO pins

GPIO

Each GPIO is controlled by two registers. One is IOCFGPx.y (I/O Configuration) and the other is MFCFGPx.y (Multifunction Configuration).

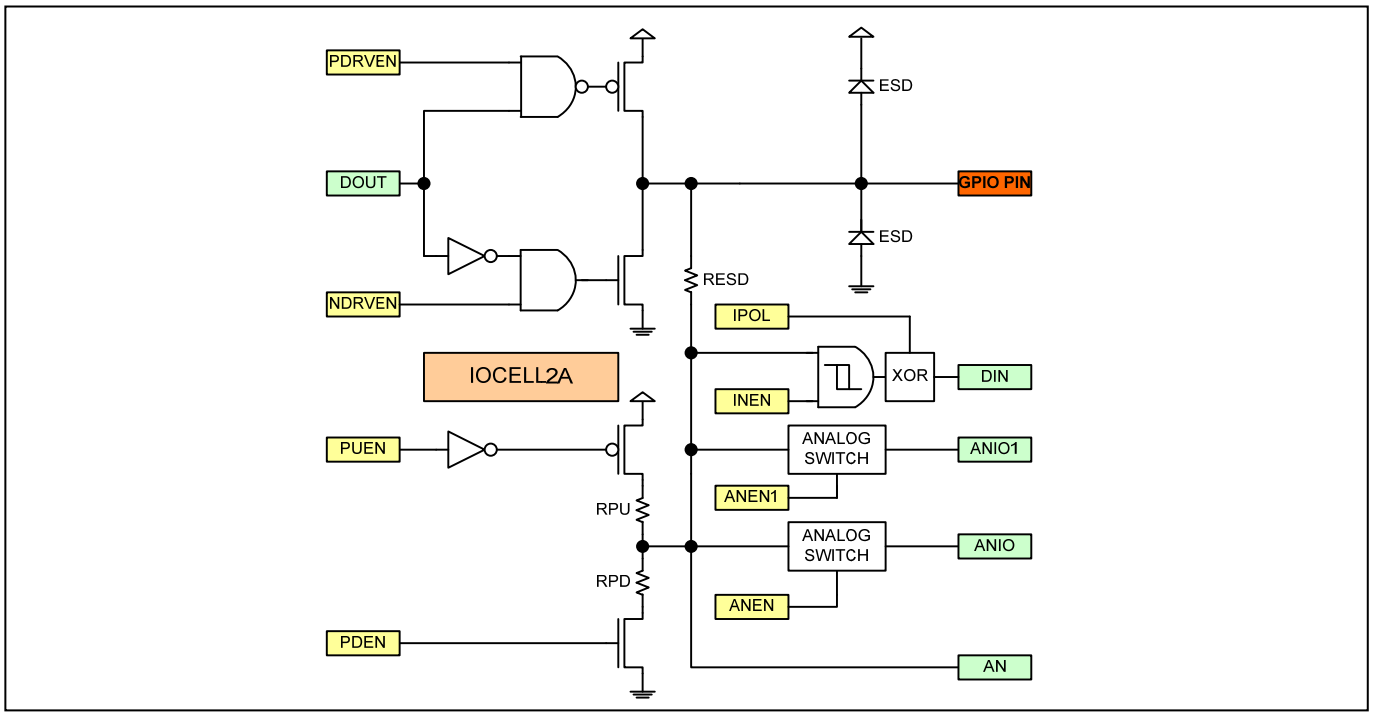


Figure 6 I/O Configuration

Figure 6 shows that there are 7 control bits for the IOCFGPx.y register, and these registers are located at XFR 0xA040 – 0xA047 for P0.0 to P0.7, 0xA048 – 0xA04F for P1.0 to P1.7, 0xA060 – 0xA063 for P2.0 to P2.3.

GPIO Port Multi-Function

Each signal pin is multi-functional and the pin configuration is specified by MFCFGP register. There are 7 control bits for the MFCFGPx.y register, and these registers are located at XFR 0xA050 – 0xA057 for P0.0 to P0.7, 0xA058 – 0xA05F for P1.0 to P1.7, and 0xA070 – 0xA073 for P2.0 to P2.3.

The touch keys and GPIO mapping table are as follows:

Touch KEY No.	GPIO Port
KEY0	P0.1
KEY1	P0.2
KEY2	P0.3
KEY3	P0.4
KEY4	P0.5
KEY5	P0.6
KEY6	P0.7
KEY7	P1.0
KEY8	P1.1
KEY9	P1.2

KEY10	P1.3
KEY11	P1.4
KEY12	P1.5
KEY13	P1.6
KEY14	P1.7

Serial Port – UART0

UART0 is full duplex and fully compatible with the standard 8052 UART. The receive path of UART0 is double-buffered that can commence reception of second byte before previously received byte is read from the receive register. Writing to SBUF0 loads the transmit register while reading SBUF0, reads a physically separate receive register. The UART0 can operate in four modes.

The touch keys related function and UART0 pins mapping table are as follows:

Touch KEY No.	GPIO Port
KEY4	P0.5/RX0
KEY5	P0.6/TX0

To use UART0 function, IOCFGP0.4, IOCFGP0.5, MFCFGP0.4, and MFCFGP0.5 should be defined in advance to enable UART0.

MFCFGP0.5 (0xA055h) GPIO P0.5 Function Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	RXD0EN	-	-	-	GPIOEN
WR	-	-	-	RXD0EN	-	-	-	GPIOEN

RXD0EN RXD0EN=1 uses this pin as RXD input for UART0

GPIOEN GPIO Function Enable Bit. Set this bit to enable GPIO function. DISABLE is the default value.

MFCFGP0.6 (0xA056h) GPIO P0.6 Function Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	TXD0EN	-	-	-	GPIOEN
WR	-	-	-	TXD0EN	-	-	-	GPIOEN

TXD0EN TXD0EN=1 uses this pin as TXD output for UART0

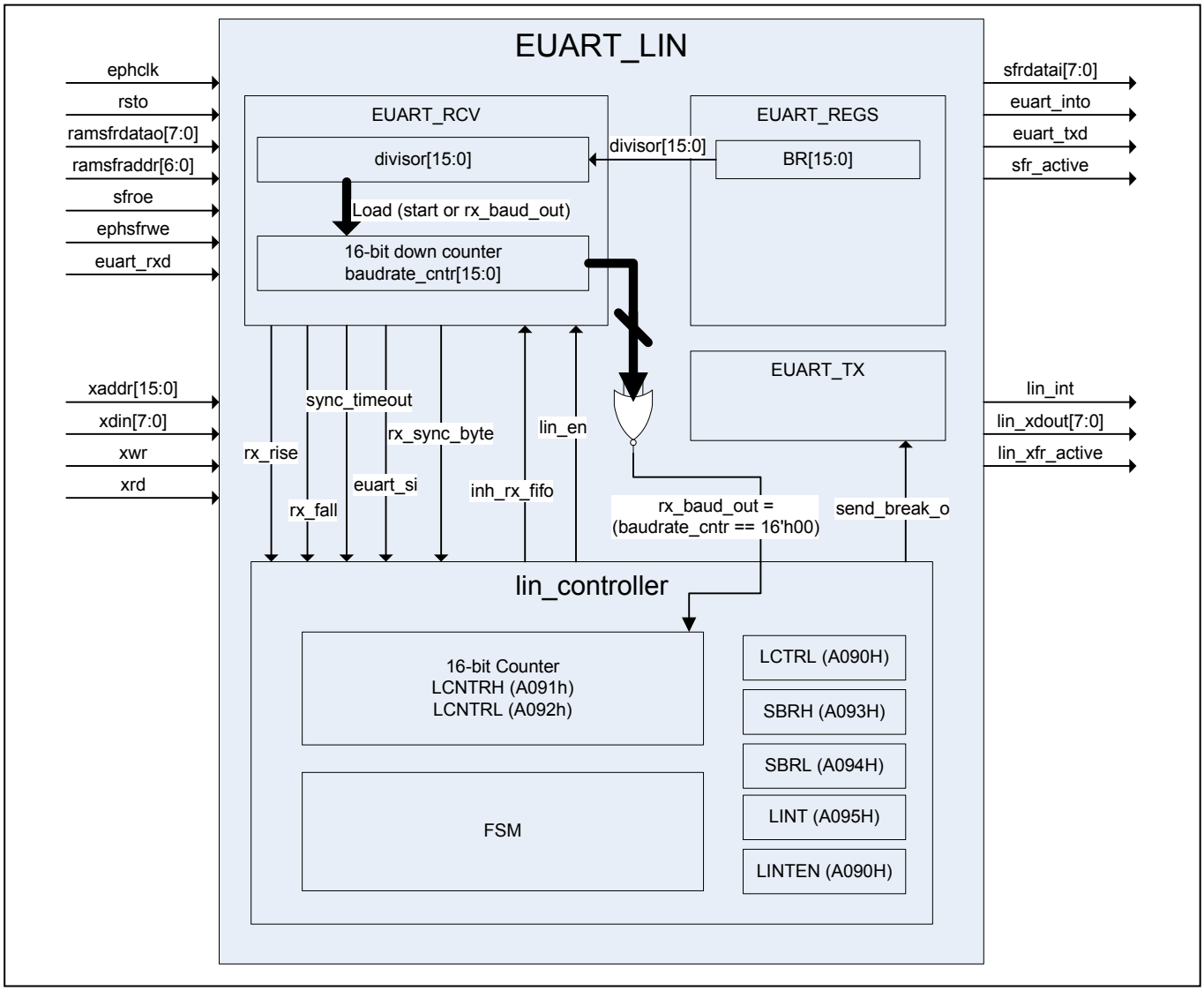
GPIOEN GPIO Function Enable Bit. Set this bit to enable GPIO function. DISABLE is the default value.

To enable UART0, four GPIO related configuration registers, the setting is as follows:

Register Name	Value
IOCFGP0.4	0xA0 (input only)
IOCFGP0.5	0x06 (output pin)
MFCFGP0.4	0x10
MFCFGP0.5	0x10

EUART2 with LIN Controller (EUART2)

LIN-capable 16550-like EUART2 is an enhanced UART controller (EUART) with separate transmit and receive FIFOs. Both transmit and receive FIFOs are 15-bytes deep and can be parameterized for interrupt triggering. The addition of FIFO significantly reduces the CPU load to handle high-speed serial interface. Transmit FIFO and receive FIFO have respective interrupt trigger levels that can be set based on optimal CPU performance adjustment. EUART2 also has dedicated 16-bit Baud Rate generator and thus provides accurate baud rate under wide range of system clock frequency. EUART2 also provides LIN extensions that incorporate message handling and baud-rate synchronization. The block diagram of EUART2 is shown in the following.



EUART2 can be configured to add LIN capability. The major enhancement of LIN includes master/slave configurations, auto baud-rate synchronization, and frame-based protocol with header. Under LIN extension mode, all EUART2 registers and functions are still effective and operational. LIN is a single-wire bus and it requires external components to combine RX and TX signals externally. LIN is frame based and consists of message protocols with master/slave configurations.

The touch keys related function and UART2/LIN pins mapping table are as follows:

Touch KEY No.	GPIO Port
KEY5	P0.6/RX2
KEY6	P0.7/TX2

To use UART2 function, IOCFGP0.5, IOCFGP0.6, MFCFGP0.5, and MFCFGP0.6 should be defined in advance to enable UART2.

MFCFGP0.6 (0xA056h) GPIO P0.6 Function Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	RXD2EN	-	-	GPIOEN
WR	-	-	-	-	RXD2EN	-	-	GPIOEN

RXD2EN RXD2EN=1 use this pin as RXD input for EUART2

GPIOEN GPIO Function Enable Bit. Set this bit to enable GPIO function. DISABLE is the default value.

MFCFGP0.7 (0xA057h) GPIO P0.7 Function Configuration Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	-	-	-	-	TXD2EN	-	-	GPIOEN
WR	-	-	-	-	TXD2EN	-	-	GPIOEN

TXD2EN TXD2EN=1 uses this pin as TXD output for EUART2

GPIOEN GPIO Function Enable Bit. Set this bit to enable GPIO function. DISABLE is the default value.

To enable EUART2/LIN, four GPIO related configuration registers, the setting is as follows:

Register Name	Value
IOCFGP0.5	0xA0 (input only)
IOCFGP0.6	0x06 (output pin)
MFCFGP0.5	0x08
MFCFGP0.6	0x08

Serial Peripheral Interface (SPI)

The Serial Peripheral Interface (SPI) is an enhanced synchronous serial hardware which is compatible with Motorola's SPI specifications. The SPI Controller includes a 4-byte FIFO for both transmit and receive. SPI Interface uses Master-Out-Slave-In (MOSI), Master-In-Slave-Out (MISO), Serial Clock (SCK) and Slave Select (SSN) for interface. SSN is low active and only meaningful in slave mode.

The touch keys related function and SPI pins mapping table are as follows:

Touch KEY No.	GPIO Port
SDA, INTB	P2.1, P3.3 (MISO)
SCL, AD	P2.0, P3.2 (MOSI)
KEY5, KEY14	P0.6, P1.7 (SCK)
CREF	P0.0 (SSN)

LED/LCD controller

The LCD/LED Controller supports up to maximum 240 dots with 8 COM and 30 SEG. Driving duty cycle methods include static, ½, 1/3, ¼, 1/5, 1/6, 1/7, 1/8, and programmable ½, ⅓ and ¼ bias with 12-level brightness control. The clock sources of LCD/LED controller can be selected either from RTC or from SIOSC, and support display frame rate down to 1Hz. When configured in LED mode, it supports either direct-driving or external-driving modes. In LCD mode, the LCD controller can be left running during STOP or SLEEP mode. The current consumption of LCD controller is about 10uA.

LCDCSL (A120h) LCD Controller Pixel Clock Divider Low Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	CSL[7-0]							
WR	CSL[7-0]							

LCDCSH (A121h) LCD Controller Pixel Clock Divider High Register R/W (0x00)

	7	6	5	4	3	2	1	0
RD	LCDCSEL	MODE[1:0]		LCDBRT[2]	CSL[11-8]			
WR	LCDCSEL	MODE[1:0]		LCDBRT[2]	CSL[11-8]			

CLKSEL LCD Controller Clock Selection
CLKSEL=0 uses RTC as LCD controller clock LCDCLK.
CLKSEL=1 uses SIOSC as LCD controller clock LCDCLK.
In LED modes, the clock is forced to use SYSCLK

MODE[1-0] LCD/LED Mode Setting
00 – Disabled
01 – LCD Mode
10 – LED External Drive Mode
11 – LED Direct Drive Digit Mode

LCDBRT[2] LCD Bias Mode Setting

LCDCS[11-0] LCDCS[11-0] defines the pixel rate of the LCD/LED
In LCD mode, (RTC or SIOSC)/(CSL[11-0]+1)
In LED modes, SYSCLK/256/(CSL[11-0]+1)

LCDCFGA (A122h) LCD configure register AR/W (0x00)

	7	6	5	4	3	2	1	0
RD	ENCOM7	ENCOM6	ENCOM5	ENCOM4	DISPOFF	-	INTEN	INTF
WR	ENCOM7	ENCOM6	ENCOM5	ENCOM4	DISPOFF	-	INTEN	INTF

ENCOM7 Enable COM7 Output
ENCOM7=0, enables SEG28 as output
ENCOM7=1, enables COM7 as output

ENCOM6 Enable COM6 Output
ENCOM6=0, enables SEG29 as output
ENCOM6=1, enables COM6 as output

ENCOM5 Enable COM5 Output
ENCOM5=0, enables SEG30 as output
ENCOM5=1, enables COM5 as output

ENCOM4 Enable COM4 Output
ENCOM4=0, enables SEG31 as output
ENCOM4=1, enables COM4 as output

DISPOFF LCD/LED Display Control
DISPOFF = 0 for normal display
DISPOFF =1 turn off all segments and common outputs to disable display. The internal logic is still in operation.

INTEN Interrupt Enable for Display Frame

INTF Interrupt Flag for Display Frame
This bit is set by hardware at display frame.
This bit must be cleared by software. Write 0 to clear INTF at next display clock rising edge

** A Display Frame is defined as a completion of a scan cycle. In other words, in LCD or LED external drive

mode, it it's the clock/duty. In LED direct drive mode, it is clock * (# of active digits).

LCDCFGB (A123h) LCD configure register BR/W (0x00)

	7	6	5	4	3	2	1	0
RD	BIAS[1-0]		LCDBRT[1-0]		LEDDIG[3-0]/LCDDUTY[2-0]			
WR	BIAS[1-0]		LCDBRT[1-0]		LEDDIG[3-0]/LCDDUTY[2-0]			

BIAS[1-0] LCD Bias Mode Setting
00 = Reserved
01 = ½ Bias
10 = 1/3 Bias
11 = ¼ Bias

LCDBRT[2-0] LCD Bias Mode Setting
In LCD mode, there are 8 brightness levels. Only LCDBRT[2-0] are used from 000 to 111.

LCDDUTY[2-0] LCD Display Duty Cycle Setting
For LCD Display Mode and for LED external drive mode
0000 = Static
0001 = ½ Duty
0010 = 1/3 Duty
0011 = ¼ Duty
0100 = 1/5 Duty
0101 = 1/6 Duty
0110 = 1/7 Duty
0111 = 1/8 Duty

LEDDIG[3-0] LED Active Digit Count
LEDDIG[3-0] + 1 defines the number of active digits. Please note the active digit must start from SEG0 and continuously on.

LCDCFGC (A124h) LED configure register CR/W (0x00)

	7	6	5	4	3	2	1	0
RD	SEGPOL	COMPOL	LEDBRT[5-0]/LCDRAC[3-0]					
WR	SEGPOL	COMPOL	LEDBRT[5-0]/LCDRAC[3-0]					

SEGPOL Segment Output Polarity in LED external drive mode
SEGPOL= 0, high active
SEGPOL= 1, low active

COMPOL Common Output Polarity in LED external drive mode
COMPOL= 0, high active
COMPOL= 1, low active

LEDBRT[5-0] LED Brightness Control
In LED mode, there are 64 brightness levels. LEDBRT[5-0] from 000000 to111111.

LCDRAC[3-0] Reference Acceleration Control
0000 = Disable Reference Acceleration
LCDRAC[3-0]+1 defines the number LCDCLK cycles for acceleration. Please note the higher LCDRAC will result higher power consumption.

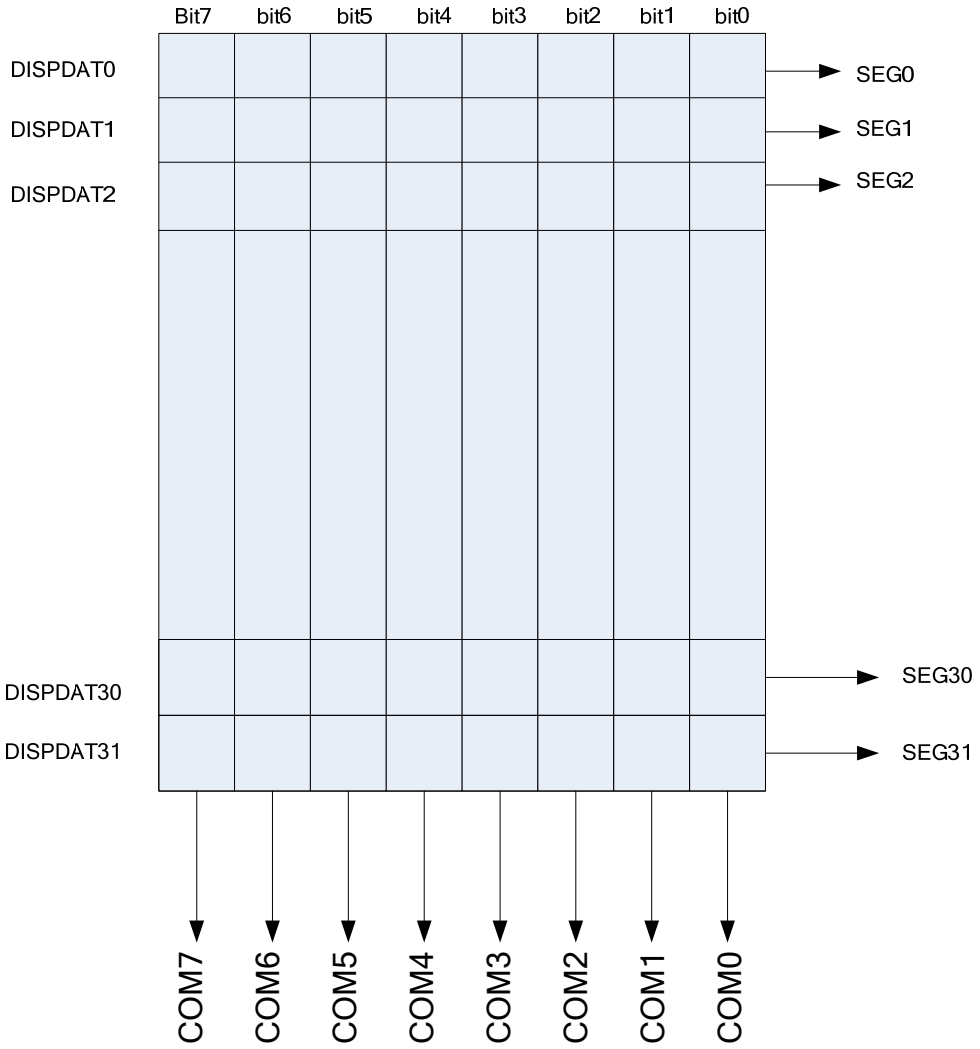
The display data are stored in DISPDAT[31-0] registers. In LCD and LED external drive mode, the data are scanned out through SEG output pins. In LED direct drive mode, the data are scanned out through COM output pins.

DISPDAT[31-0] (A100h - A11Fh) Display Data Register 0 – 31 R/W (0x00)

	7	6	5	4	3	2	1	0
RD	DISPDAT[I][7-0]							
WR	DISPDAT[I][7-0]							

LCD Drive Mode

DSIPDAT /SEG Mapping

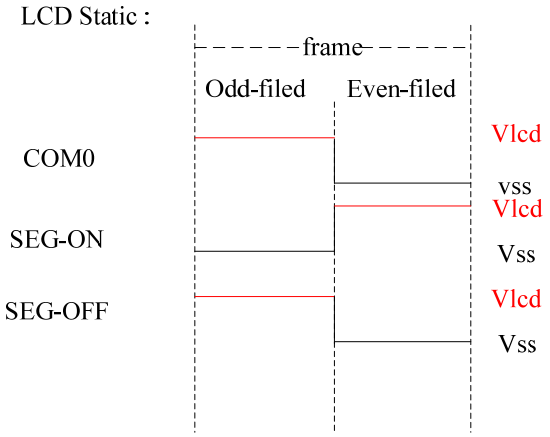


DISPDAT00~31 provide SEG00~31 output contents , output sequence follows COMx timing ,
The COMx output sequence : COM0(T0)-> COM1(T1)->COM2(T2)->COM3(T3)…->COMN(TN) -> COM0(T0)
The N value defined by Duty setting , N=0 for static, N=1 for 1/2duty, N=2 for 1/3duty, N=3 for 1/4 duty ..
And Max N=7 for 1/8 duty.
Example DISPDAT0=8'b0100_1010, DISPLAY1=8'b0011_0001, 1/4duty
COM0 timing , SEG0 output related to DISPDAT0-bit0 ("0" , output off-level waveform)
SEG1 output related to DISPDAT1-bit0 ("1" , output on-level waveform)
COM1 timing , SEG0 output related to DISPDAT0-bit1 ("1" , output on-level waveform)
SEG1 output related to DISPDAT1-bit1 ("0" , output off-level waveform)
COM2 timing , SEG0 output related to DISPDAT0-bit2 ("0" , output off-level waveform)
SEG1 output related to DISPDAT1-bit2 ("0" , output off-level waveform)

COM3 timing , SEG0 output related to DISPDAT0-bit3 (“1” , output on-level waveform)
SEG1 output related to DISPDAT1-bit3 (“0” , output off-level waveform)
Repeat to COM0 timing …, COM4~COM7 not used.
COMx output waveform refer to duty and bias definition .

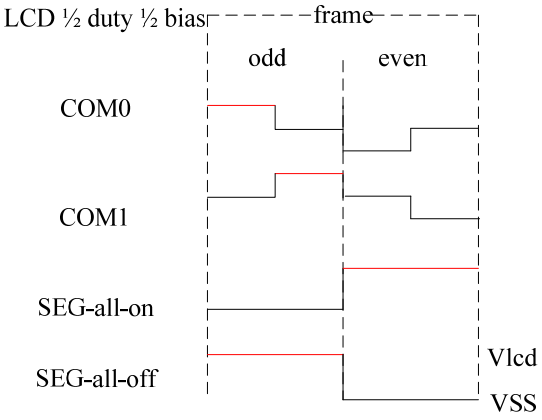
Static mode

frame rate =30Hz
sysclk = 16Mhz,
T2M=0 , div-12
timer2-value = 16*2^20 /12/30/2
= 23302
{TP2H,TP2L}=2^16-23302 = 16'hA4FA



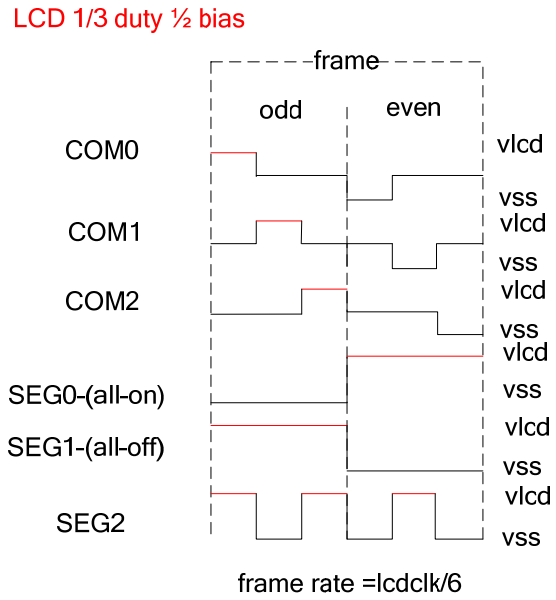
frame rate =lcdclk/2

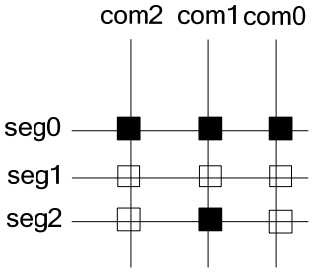
½ Duty ½ Bias



frame rate =lcdclk/4

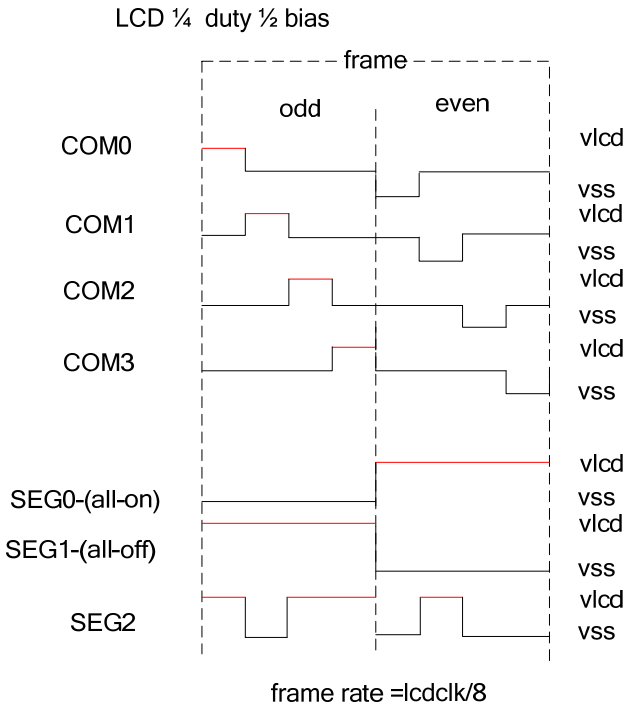
1/3 Duty ½ Bias

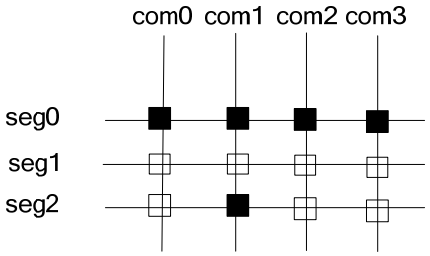




Reg_Seg0=3'b111
Reg_Seg1=3'b000
Reg_seg2=3'b010

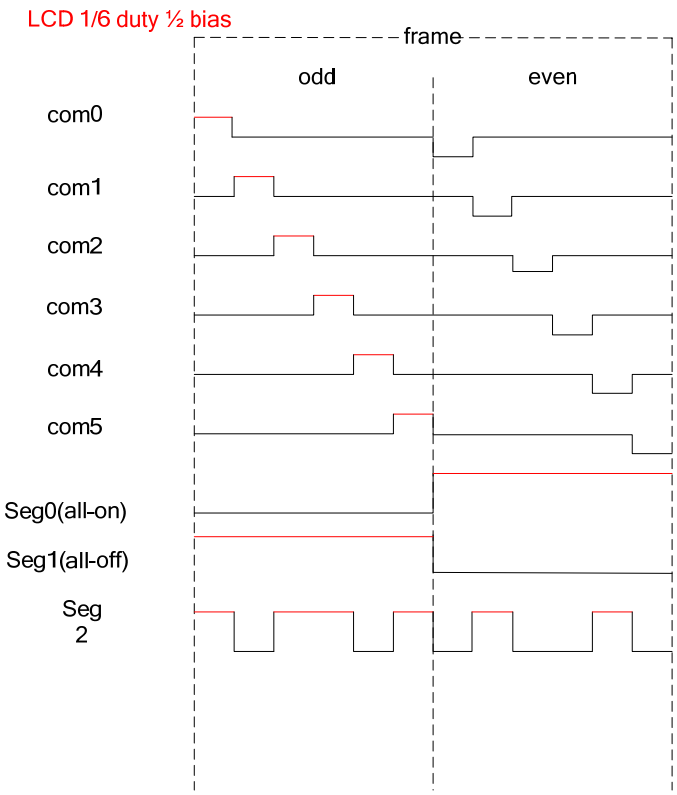
¼ Duty ½ Bias

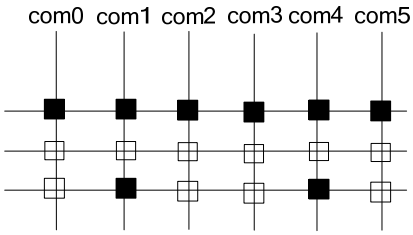




DISPDAT0=4'b1111
DISPDAT1=4'b0000
DISPDAT2=4'b0010

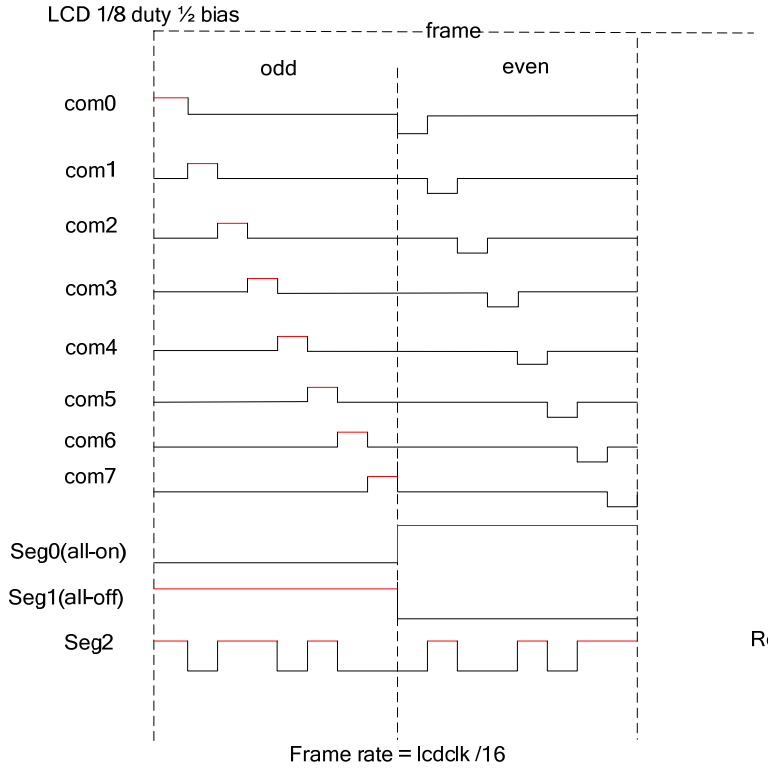
1/6 Duty ½ Bias



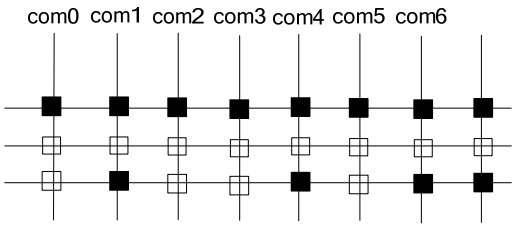


Reg_Seg={com7,com6,com5,com4,com3,com2,com1,com0}
DISPDAT0=6'b111111
DISPDAT1=6'b000000
DISPDAT2=6'b010010

1/8 Duty ½ Bias

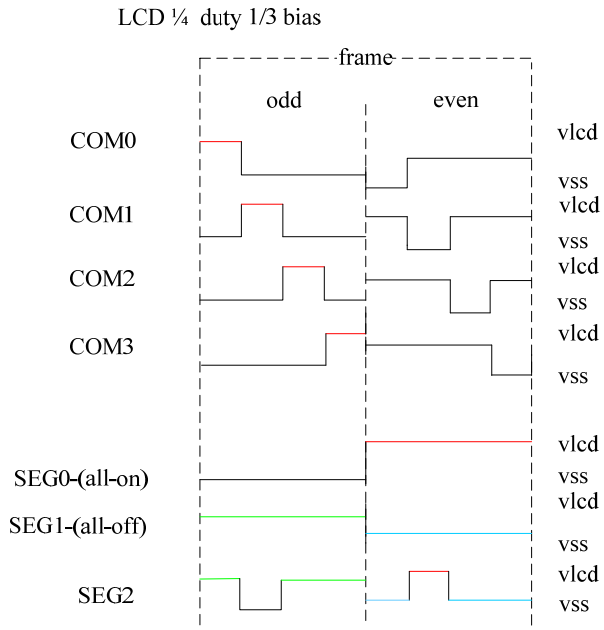


Frame rate = lcdclk /16

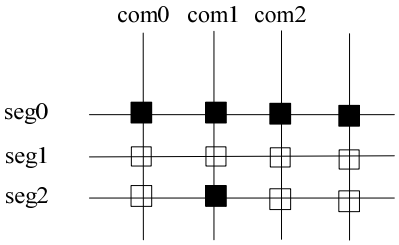


Reg_Seg={com7,com6,com5,com4,com3,com2,com1,com0}
DISPDAT0=8'b11111111
DISPDAT1=8'b00000000
DISPDAT2=8'b11010010

¼ Duty 1/3 Bias

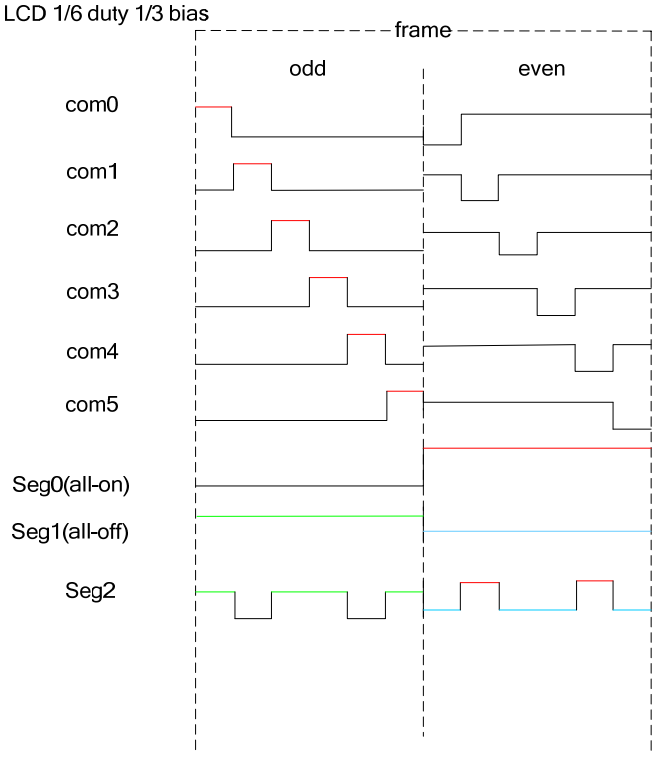


frame rate =lcdclk/8

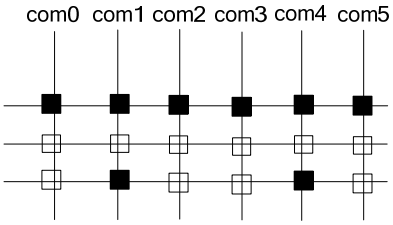


DISPDAT0=4'b1111
DISPDAT1=4'b0000
DISPDAT2=4'b0010

1/6 Duty 1/3 Bias

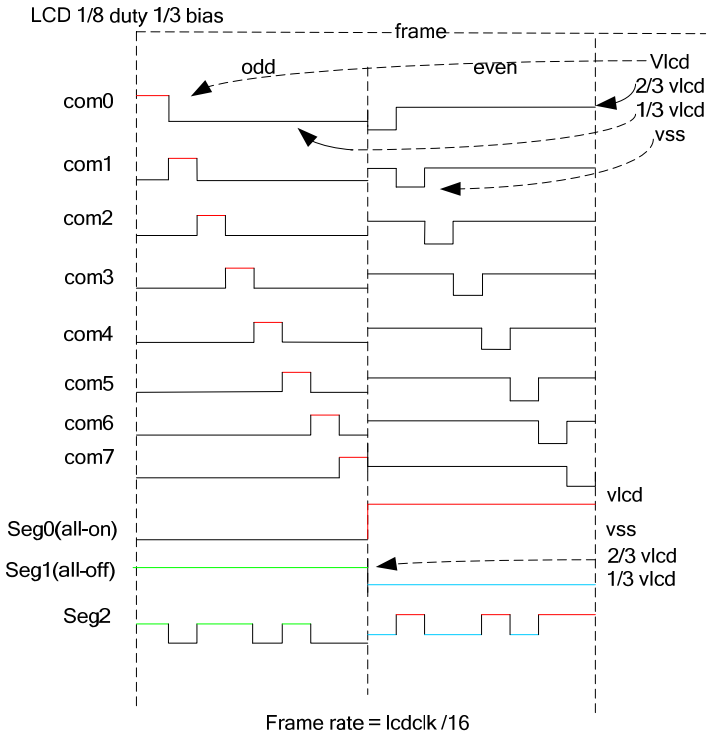


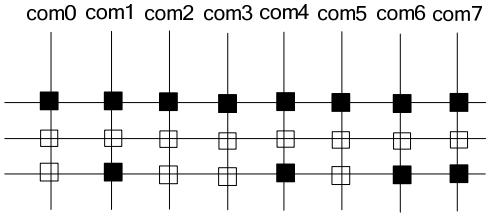
Frame rate = lcdclk /12



Reg_Seg={com7,com6,com5,com4,com3,com2,com1,com0}
DISPDAT0=6'b111111
DISPDAT1=6'b000000
DISPDAT2=6'b010010

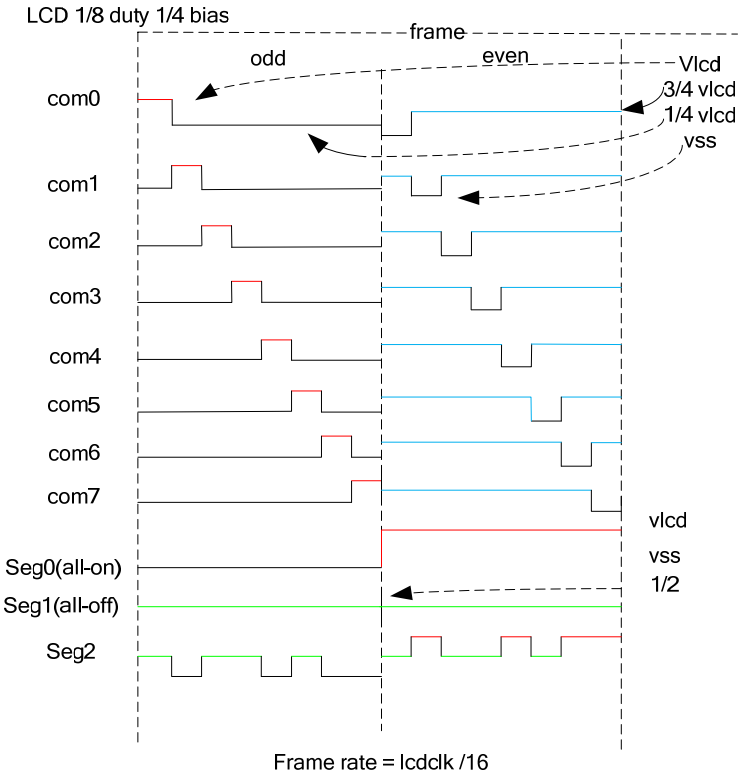
1/8 Duty 1/3 Bias

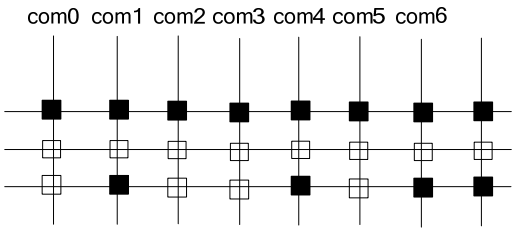




Reg_Seg={com7,com6,com5,com4,com3,com2,com1,com0}
DISPDAT0=8'b11111111
DISPDAT1=8'b00000000
DISPDAT2=8'b11010010

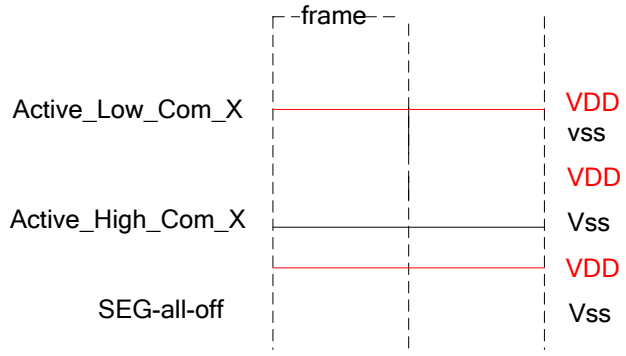
1/8 Duty 1/4 Bias





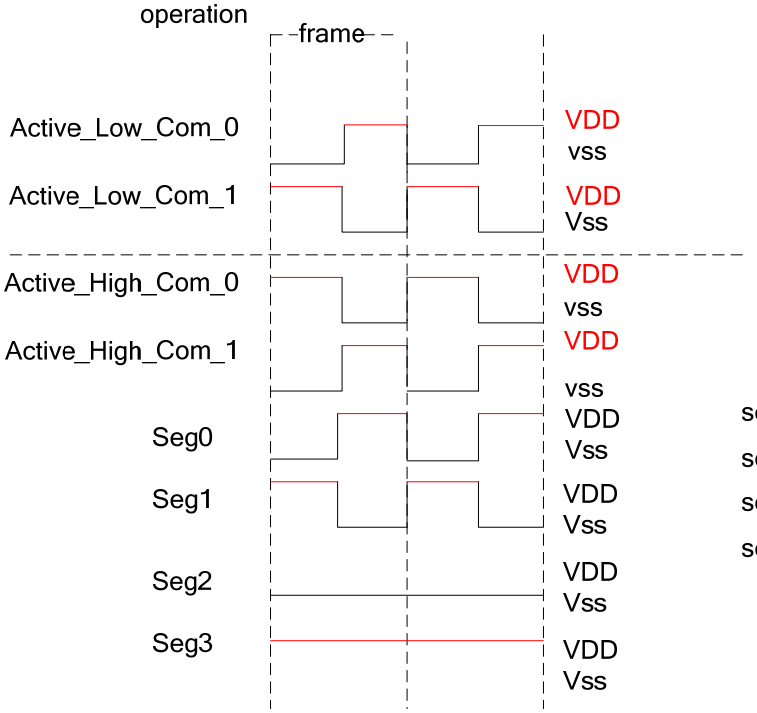
Reg_Seg={com7,com6,com5,com4,com3,com2,com1,com0}
DISPDAT0=8'b11111111
DISPDAT1=8'b00000000
DISPDAT2=8'b11010010

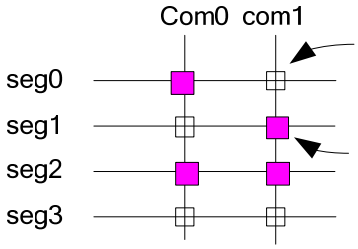
LCD ½ duty : display off



frame rate =lcdclk/2

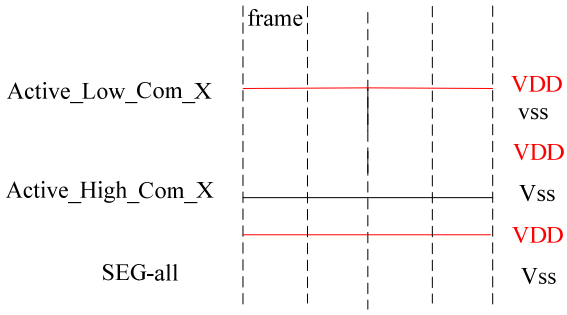
LCD ½ duty : display normal operation





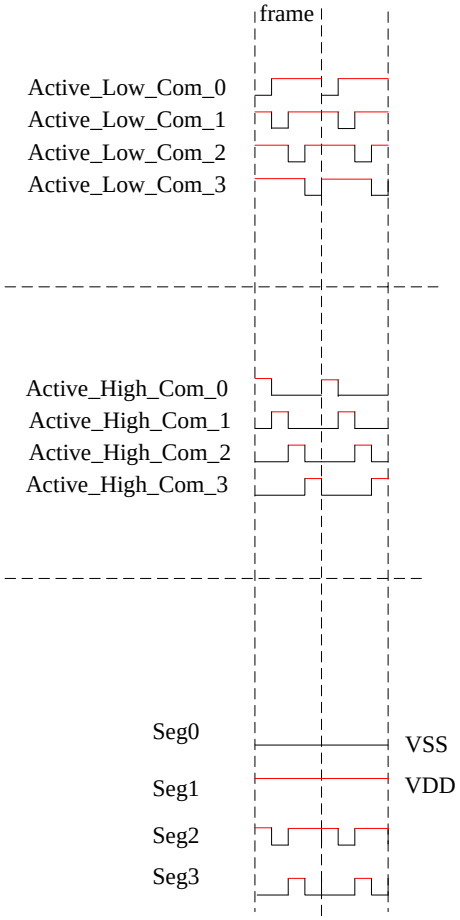
frame rate =lcdclk/2

LCD 1/4 duty : display off

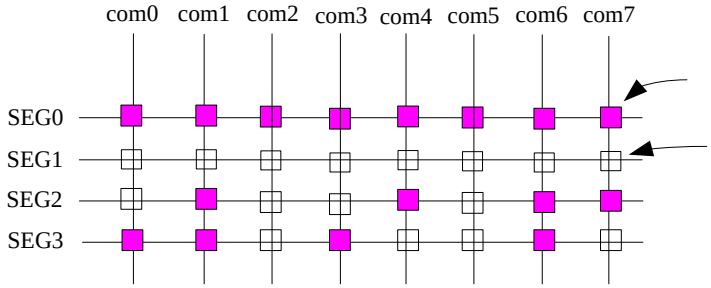


frame rate =lcdclk/4

LCD 1/4 duty ：display normal operation



frame rate =lcdclk/4



Reg_Seg={com7,com6,com5,com4,com3,com2,com1,com0}

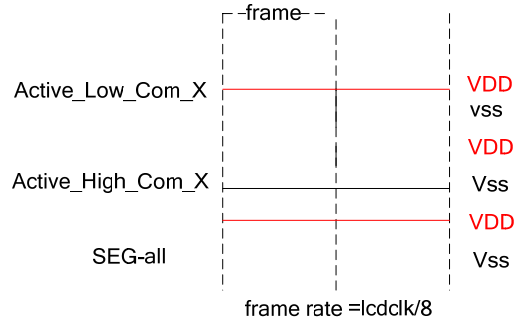
DISPDAT0=8'b11111111

DISPDAT1=8'b00000000

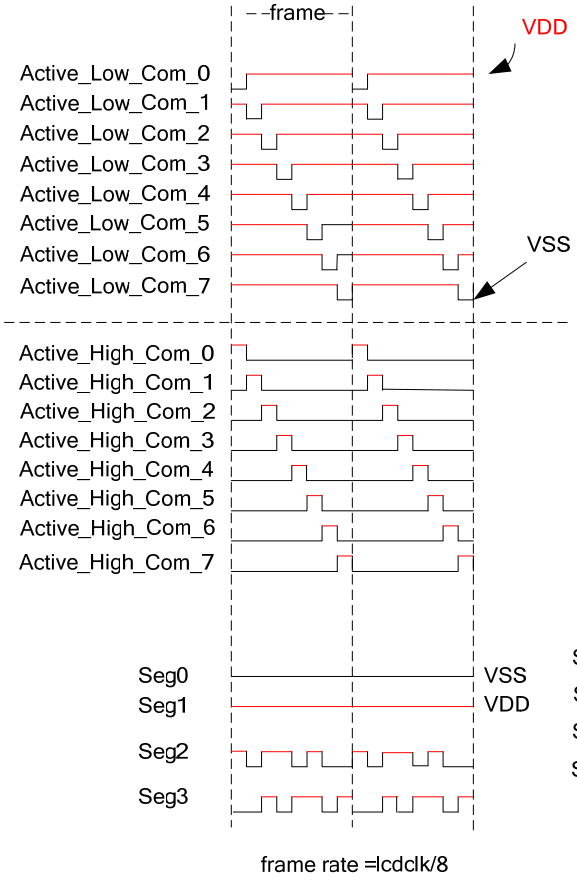
DISPDAT2=8'b11010010

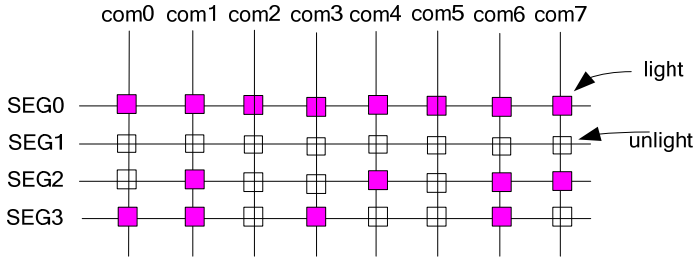
DISPDAT3=8'b01001011

LCD 1/8 duty : display off



LCD 1/8 duty : display normal operation





Reg_Seg={com7,com6,com5,com4,com3,com2,com1,com0}
DISPDAT0=8'b11111111
DISPDAT1=8'b00000000
DISPDAT2=8'b11010010
DISPDAT3=8'b01001011

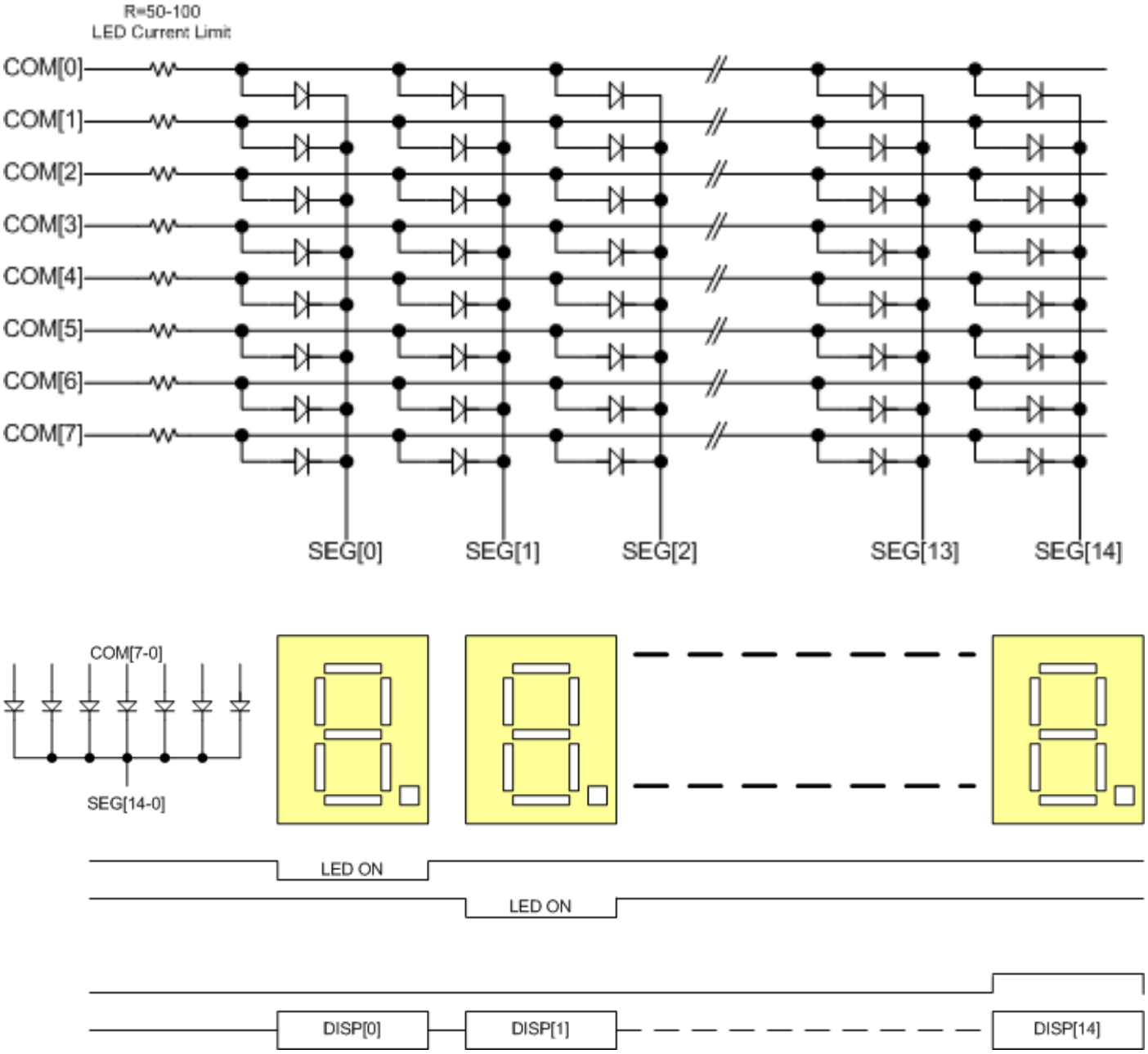
LED Drive Mode

Direct Drive Mode

SE5114 support LED direct drive with common-cathode LED driving without external transistors. This mode is enabled by setting MODE[1-0]=11 in LCDCSH register. The LED is configured as 8-segment digit display and up to 15 digits. The display data are stored in DISPDAT[15-0]. These are scanned out on COM[7-0] and SEG[0-14] are enabled scanned sequentially. The resulting duty cycle of the LED is thus 1/SEG[0-14] depending on the number of SEG enabled.

The COM outputs are used to drive the segments and the SEG outputs are used to drive the digits. COM outputs have high PMOS drive (up to 25mA source current with RDSON of 20Ohm for 85C, and up to 20mA for

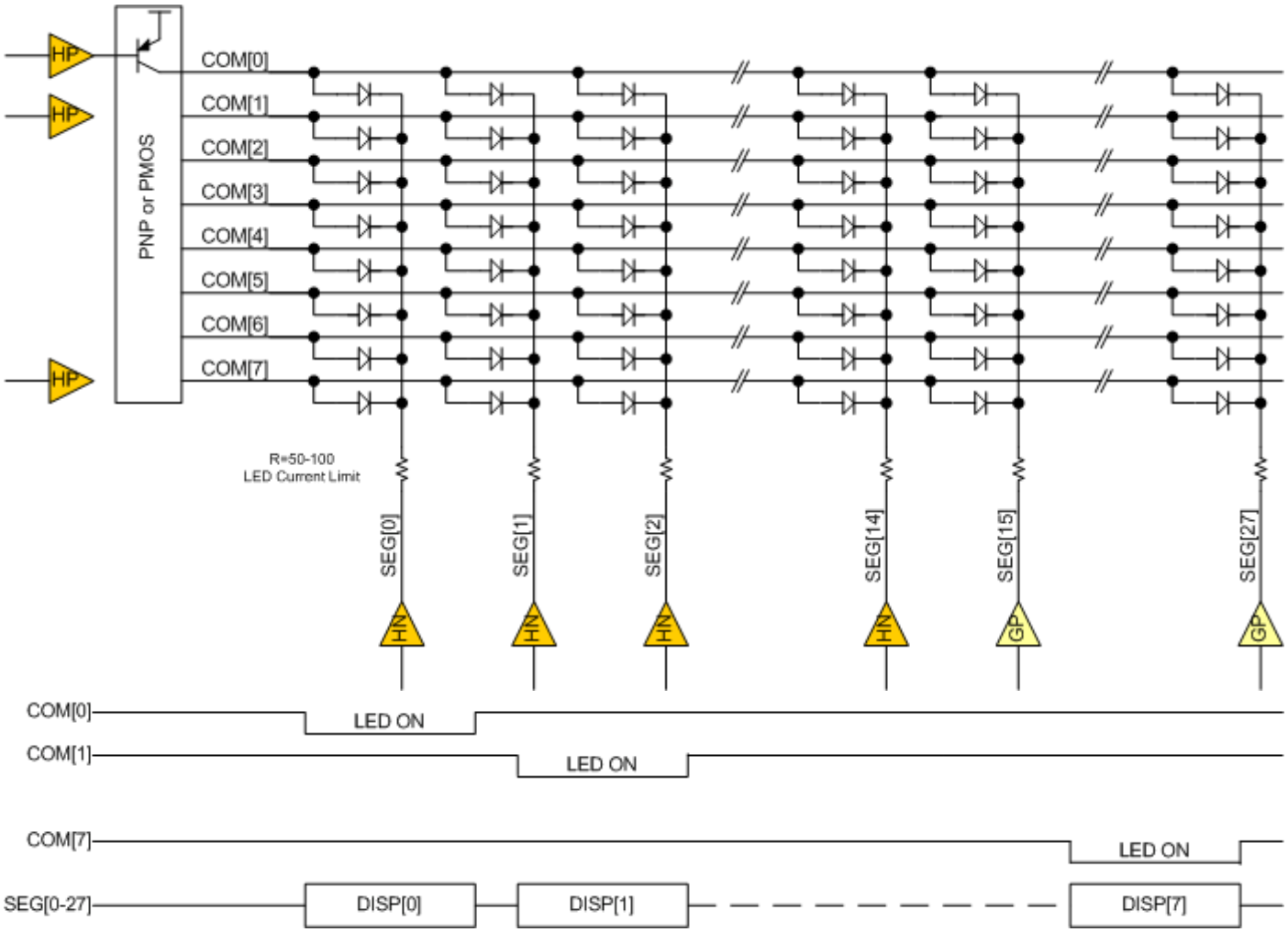
110C) and SEG outputs have high NMOS drive (up to 125mA sink current with RDSON of 8 Ohm for 85C, and up to 125mA for 110C), thus is suited to drive common-cathode LED arrays. A typical application circuit showing the LED array and associated scanning waveform is shown in the following diagram.



Since each SEG output needs to sink up to 8 LED if all COM output is enabled, the total sink current must be less than 8 x of COM source current. For sink current up to 125mA, the LED current thus should be limited to 125mA/8 = 16mA. Then the average LED current can be derived as 16mA x Duty Cycle. For example, total 10 digits are enabled then the average LED current is 1.6mA.

External Drive Mode

For higher LED brightness requirement, SE5114 also supports external drive mode to increase the average LED current. In this mode, COM[0-7] is scanned and enabled sequentially while SEG output are output accordingly. As the result, the on duty cycle of LED is 1/COM[0-7] depending on the number of enabled COM outputs. This is set by LCDDTY[2-0] and ranges from 0 (static) to $1/8^{th}$. This mode can support up to 4 x 32 or 8 x 28 LED matrix array. This mode is enabled by setting MODE[1-0]=10 in LCDCSH register. The application circuits and corresponding scan timing of external drive mode is shown in the following diagram.



In the example, COM output is connected to external PNP or PMOS transistor to supply LED current. In this case, COM output polarity must be set in order to obtain correct driving signals. When PNP is used, maximum LED brightness should be set to 63/64 in order to avoid ghosting due to PNP extended turn-off delay. Alternatively, NPN transistors can also be used. NPN transistor can also serve as high voltage blocking function for LED array.

External drive mode can provide significant higher LED average current for several reasons. First, source current limitation is removed. Secondly, scanning COM makes the effective duty on cycle higher (static to $1/8^{th}$). The sink current is determined by the maximum drive capability of SEG driver (up to 125mA for SEG[14-0] output driver), and GPIO driver (up to 50mA for SEG[15-31]) if total segment count is more than 15. And the maximum current for PNP/PMOS drive is the number of the segments times the LED on current. Using an 8 by 27 array as an example, the maximum LED on current is then 50mA. And the PNP/PMOS maximum current is 50mA * 27 = 1.35A. And because the duty cycle $1/8^{th}$, the effective LED average current is 50mA/8 = 6.25mA. For another 8 x 14 array example, the LED on current is then 125mA, and the PNP/PMOS current is 125mA * 14 = 1.68A. And the effective LED average current is 128mA/8 = 15.6mA.

Table 2 Register Function

Address	Name	Function	R/W	Table	Default
00h	Main Control Register	Controls general power states and power dissipation	W	3	0000 0000
01h	INT Configuration Register	Interrupt configuration	R/W	4	
02h	Key Status Register 1	KEY0~Key7 status bits	R	5-1	
03h	Key Status Register 2	Key8~KEY14 status bits		5-2	
04h	Interrupt Enable Register 1	KEY0~key7 Enables Interrupts associated with capacitive touch sensor inputs	R/W	6-1	1111 1111
05h	Interrupt Enable Register 2	Key8~KEY14 Enables Interrupts associated with capacitive touch sensor inputs		6-2	
06h	Key Enable Register 1	KEY0~key7 sets the channels enable		7-1	
07h	Key Enable Register 2	Key8~KEY14 sets the channels enable		7-2	
08h	Multiple Touch Key Configure Register	Multiple touch key function setting		8	0000 0000
09h	Auto-Clean Interrupt Register	Set auto-clean interrupt time and enable		9	
0Ah	Interrupt Repeat Time Register	Set repeat cycle for pressing key interrupt		10	0000 1111
0Bh	Auto-SLEEP Mode Register	Set auto enter SLEEP Mode time		11	
0Ch	Exit SLEEP Mode Register 1	Set press KEY0~Key7 to exit SLEEP Mode		12-1	1111 1111
0Dh	Exit SLEEP Mode Register 2	Set press Key8~KEY14 to exit SLEEP Mode		12-2	
0Eh	Gain and Press Time Setting Register	Set gain and pressing trigger time		13	0010 1111
0Fh	Key Touch Sampling Configure Register	Set sampling times and cycle time		14	0
10h	Calibration Configure Register	Set auto-calibration cycle and negative value trigger setting		15	0011 0000
11h	Key Calibration Register 1	KEY0~Key7 compel calibrate enable set		16-1	0
12h	Key Calibration Register 2	Key8~KEY14 compel calibrate enable set		16-2	
13h	Noise Threshold Register	Set noise threshold value		17	0011 0010
14h	Noise Indication Register 1	KEY0~Key7 noise indication		18-1	0
15h	Noise Indication Register 2	Key8~KEY14 noise indication		18-2	
17h	Negative Threshold Register	Set negative threshold and compel calibration threshold		20	0000 1000
18h	Wake Up Threshold Register	Set wake up threshold		21	0000 1000
19h	Scan Voltage Register	Set scanning voltage		19	0
20h~2Fh	Variation Value Register	Keys value setting	R/W	22	0
30h~3Fh	Threshold Set Register	Keys threshold setting		23	0011 0010
40h,42h … 5Ch,5Eh	Calibration Low Bit Register	Internal calibration low 8-bit for KEY0~KEY14	R	24-1	0000 0000

41h,43h … 5Dh,5Fh	Calibration High Bit Register	Internal calibration high 8-bit for KEY0~KEY14		24-2	

Table 3 00h Main Control Register (Write Only)

Bit	D7	D6	D5	D4	D3	D2:D0
Name	SR	-	SDM	SP	-	-
Default	0	0	0	0	0	000

SR System Reset
0 Normal Mode
1 System Reset

SDM Shutdown Mode
0 Normal Mode
1 Shutdown Mode

SP Sleep Mode
0 Normal Mode
1 SLEEP Mode

Table 4 01h Interrupt Configuration Register

Bit	D7:D4	D3	D2	D1	D0
Name	-	MDEN	INM	INE	-
Default	0000	0	0	0	0

MDEN Maximum Duration Time Enable
0 Disable
1 Enable

Maximum press function is used to prevent key pressing all the time by accident. When maximum press function is enabled, once key keep pressing at programmed time the key calibration value will be updated.

INM Interrupt Mode
0 Interrupt Mode 0(Touch key trigger once interrupt)
1 Interrupt Mode 1(Touch key trigger repeated interrupt)

INM bit sets interrupt time for once or multiple. Multiple interrupt is used for key pressing detection.

INE Interrupt Function Enable
0 Enable
1 Disable

Table 5-1 02h Key Status Register 1 (Read only)

Bit	D7:D0
Name	KS[7:1]
Default	0000 0000

Table 5-2 03h Key Status Register 2 (Read only)

Bit	D6:D0
Name	KS[15:8]
Default	000 0000

KSx KEY0~KEY14 Status
0 No action
1 Press or release keys

If the value of KSx is detected over programmed threshold, the corresponding bit will be set to “1”.

Table 6-1 04h Interrupt Enable Register 1

Bit	D7:D0
Name	KINT[7:1]
Default	1111 1111

Table 6-2 05h Interrupt Enable Register 2

Bit	D6:D0
Name	KINT[15:8]
Default	111 1111

The Interrupt Enable Register determines whether a sensor pad touch or release (if enabled) causes the interrupt pin to be asserted.

KINTx Key Interrupt Enable
0 Disable
1 Enable

The default value for Interrupt Enable Registers is interrupt enable. Only set INE bit of Interrupt Configuration Register (01h) to “0”, INTB pin will generate interrupt signal.

Table 7-1 06h Key Enable Register 1

Bit	D7:D0
Name	KEN[7:1]
Default	1111 1111

Table 7-2 07h Key Enable Register 2

Bit	D6:D0
Name	KEN[15:8]
Default	111 1111

KENx	Touch Key Enable Setting
0	Disable
1	Enable

Table 8 08h Multiple Touch Key Configure Register

Bit	D7:D3	D2	D1:D0
Name	-	MKEN	MTK
Default	0000 0	0	00

MKEN	Multi- Key Enable
0	Disable
1	Enable

MTK	Multi -Key Selection
01	Allow one key triggered at same time
10	Allow two keys triggered at same time
11	Allow three keys triggered at same time

Table 9 09h Auto-Clear Interrupt Register

Bit	D7:D4	D3	D2:D0
Name	-	ACEN	ACT
Default	0000	0	000

ACEN	Auto-Clear Interrupt Enable
0	Disable
1	Enable

ACT	Auto-Clear Interrupt Time
000	10ms
001	20ms
010	30ms
011	40ms
100	50ms
101	100ms
110	150ms
111	200ms

When ACEN=0, the INTB will keep low until MCU read 02h and 03h registers. When ACEN=1, if MCU don't read 02h and 03h registers within programmed time (ACT=10ms~200ms), INTB pin will be release automatically.

Table 10 0Ah Interrupt Repeat Time Register

Bit	D7:D4	D3:D0
Name	INTRT	MPT
Default	0000	0000

INTRT	Interrupt Repeat Time
0000	Close
0001	50ms
0010	100ms
0011	150ms
0100	200ms
0101	250ms
0110	300ms
0111	350ms
1000	400ms
1001	450ms
1010	500ms
1011	600ms
1100	700ms
1101	800ms
1110	900ms
1111	1s

MPT	Multi-key Press Time
0000	Close
0001	50ms
0010	100ms
0011	150ms
0100	200ms
0101	250ms
0110	300ms
0111	350ms
1000	400ms
1001	450ms
1010	500ms
1011	600ms
1100	700ms
1101	800ms
1110	900ms
1111	1s

When set the INM as 1 and several keys are pressed, it will generate the second interrupt until M_PRESS_TIME after the first interrupt. Then wait for INT_RPT_TIME to trigger the third interrupt. After all of these if the keys are still pressing, wait for INT_RPT_TIME to trigger others interrupt until keys release.

Table 11 0Bh Auto-SLEEP Mode Register

Bit	D7	D6:D4	D3:D0
Name	ASEN	OSCD	AST
Default	0	000	0000

ASEN	**Auto-SLEEP Enable**
0	Disable
1	Enable

OSCD	**Auto-Sleep Oscillator Division**
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

AST	**Auto-SLEEP Time**
0000	0.5s
0001	1s
0010	1.5s
0011	2s
0100	2.5s
0101	3s
0110	3.5s
0111	4s
1000	4.5s
1001	5s
1010	6s
1011	7s
1100	8s
1101	9s
1110	10s

When ASEN=1 and no actions on touch key and I2C interface, the IC will enter into SLEEP Mode after programmed time (AST).

Table 12-1 0Ch Exit SLEEP Mode Register 1

Bit	D7:D0
Name	ESMEN[7:1]
Default	0000 0000

Table 12-2 0Dh Exit SLEEP Mode Register 2

Bit	D6:D0
Name	ESMEN[14:8]
Default	000 0000

ESMENx	**Exit Sleep Mode Enable**
0	Touch key can't trigger exiting SLEEP Mode
1	Touch key trigger exiting SLEEP Mode

When IC is in Normal Mode and ASEN=1, set ESMENx=1 will exit from SLEEP Mode by pressing the corresponding key.

Table 13 0Eh Gain and Press Time Setting Register

Bit	D7:D4	D3:D0
Name	GAIN	MDT
Default	00000	0000

GAIN	**Gain Control**
0000	1X
0001	2X
0010	3X
0011	4X
0100	5X
0101	6X
0110	7X
0111	8X
1000	9X
1001	10X
1010	11X
1011	12X
1100	13X
1101	14X
1110	15X
1111	16X

The GAIN bits are used to set the gain factor. Internal count will count the final value and put it into KEYx_ΔCOUNT.

MDT	Max Duration Time
0000	0.5s
0001	1s
0010	2s
0011	3s
0100	4s
0101	5s
0110	6s
0111	7s
1000	8s
1001	9s
1010	10s
1011	11s
1100	12s
1101	13s
1110	14s
1111	15s

MPT bits set the pressing time. When key pressed continue over the programmed time (MDT), system will force to calibrate the pressed key. Set MDEN to "1" will enable this function.

Table 14 0Fh Key Touch Sampling Configure Register

Bit	D7:D4	D3:D2	D1:D0
Name	SC	ST	CDS
Default	0000	00	00

SC	Touch Key Sampling Count Setting
0000	1
0001	2
0010	3
0011	4
0100	5
0101	6
0110	7
0111	8
1000	9
1001	10
1010	11
1011	12
1100	13
1101	14
1110	15
1111	16

SC is used to set average sampling times for each channel. Higher SC value will increase stability and anti-interference ability, but decrease reaction speed.

ST	Sampling Time (Single Channel)
00	0.5ms
01	1ms
10	2ms
11	3ms

CDS	Cycle Delay Time
00	50ms
01	100ms
10	200ms
11	300ms

Sampling 16 channels is for one cycle.

Table 15 10h Calibration Configure Register

Bit	D7	D6:D4	D3:D2	D1:D0
Name	-	CSC	-	NDC
Default	0	000	00	00

CSC	Calibrate Sample Count
000	2
001	4
010	8
011	16
100	32
101	64
110	128
111	256

If there is no action on keys, environmental capacitance will be calibrated after CSC times.

NDC	Negative Delta Count
00	4
01	8
10	16
11	32

If channel detects the value over negative threshold (NDTH) for NDC times, it will be calibrated forcibly.

Table 16-1 11h Individual Force Calibration Register 1

Bit	D7:D0
Name	FCK7:FCK1
Default	0000 0000

Table 16-2 12h Individual Force Calibration Register 2

Bit	D6:D0
Name	FCK14:FCK8
Default	000 0000

FCKx Individual Force Calibrate Key

0 Close

1 Enable

When enable FCKx, the corresponding bit will be set to “0”.

Table 17 13h Noise Threshold Register

Bit	D7:D0
Name	NTH
Default	0000 0000

The noise threshold is from 0~127. It is invalid if NTH>127.

If difference value between samplings is over the programmed threshold, the corresponding noise bit will be set to “1”.

Table 18-1 14h Noise Indication Register 1

Bit	D7:D0
Name	NK7:NK1
Default	0000 0000

Table 18-2 15h Noise Indication Register 2

Bit	D6:D0
Name	NK14:NK8
Default	000 0000

NKx Noise Indication

0 No noise

1 Noise

Table 19 19h Scan Voltage Register

Bit	D7	D6:D4	D3
Name	VTH	ZERO_Time [2:0]	REFSEL
Default	0	000	0

VTH Scan Voltage

If REFSEL = 0

0 Cref charges to 0.9V

1 Cref charges to 1.35V

If REFSEL = 1

0 Cref charges to VDDH/2

1 Cref charges to VDDH*3/4

ZERO_Time [2:0] Discharge time of Cref

000 8 us

001 16 us

010 24 us

011 32 us

100 40 us

101 48 us

110 56 us

111 64 us

REFSEL Cref charges source selection

0 The Cref charging source is 1.8V

1 The Cref charging source is VDDH

Table 20 17h Negative Threshold Register

Bit	D7:D4	D3:D0
Name	NCTH	NDTH
Default	0000	0000

NCTH Negative Calibrate Threshold Setting

0000 Disabled

0001 -10

0010 -20

0011 -30

0100 -40

0101 -50

0110 -60

0111 -70

1000 -80

1001 -90

1010 -100

1011 -110

1100 -120

1101 Not available

1110	Not available
1111	Not available

NDTH	Negative Delta Threshold Setting
0000	-1
0001	-2
0010	-3
0011	-4
0100	-5
0101	-6
0110	-7
0111	-8
1000	-9
1001	-10
1010	-11
1011	-12
1100	-13
1101	-14
1110	-15
1111	-16

When negative value is over the programmed threshold (NCTH), the channel will be calibrated forcibly.
If negative value is detected over threshold for NDTH times continually, the channel will be calibrated forcibly.

Table 21 18h Wake Up Threshold Register

Bit	D7	D6:D0
Name	-	WTH[6:0]
Default	0	111 1111

Table 22 20h~2Eh KEY0~KEY14 Variation Value Register

Bit	D7	D6:D0
Name	SIGN	KEYx_ΔCOUNT
Default	0	000 0000

SIGB	Sign bit
0	Positive
1	Negative

KEYx_ΔCOUNT Key Value Count

Table 23 30h~3Eh KEY0~KEY14 Threshold Set Register

Bit	D7	D6:D0
Name		KEYx_TH
Default	1	111 1111

KEYx_TH Key Threshold
0~127

Table 24-1 40h, 42h … 5Ah, 5Ch KEY0~KEY14 Calibration Low Byte Register (Read Only)

Bit	D7:D0
Name	KEY0_CAL_L
Default	0000 0000

Table 24-2 41h, 43h … 5Bh, 5Dh KEY0~KEY14 Calibration High Byte Register (Read only)

Bit	D7:D0
Name	KEY0_CAL_H
Default	0000 0000

TYPICAL APPLICATION INFORMATION

GENERAL DESCRIPTION

The IS31SE5114 is an ultra low power, fully integrated 15-channel solution for capacitive touch-buttons applications. The chip allows electrodes to project sense fields through any dielectric such as glass or plastic.

SENSITIVITY ADJUSTING

Sensitivity can be adjusted by the external capacitor

or internal register.

The value of capacitor is higher the sensitivity is lower; value of capacitor is lower the sensitivity is higher.

INTERRUPTION

The changing of action can be signed by the INTB pin. The INTB pin will be pulled low when sensitivity channel is pressed or released.

SHUTDOWN MODE

Shutdown mode can be used as a means of reducing power consumption. During shutdown mode all registers retain their data.

Software Shutdown

By setting SDM bit of the Configuration Register (00h) to “1”, the IS31SE5114 will operate in software shutdown mode.

CLASSIFICATION REFLOW PROFILES

Profile Feature	Pb-Free Assembly
Preheat & Soak Temperature min (Tsmin) Temperature max (Tsmax) Time (Tsmin to Tsmax) (ts)	150°C 200°C 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3°C/second max.
Liquidous temperature (TL) Time at liquidous (tL)	217°C 60-150 seconds
Peak package body temperature (Tp)*	Max 260°C
Time (tp)** within 5°C of the specified classification temperature (Tc)	Max 30 seconds
Average ramp-down rate (Tp to Tsmax)	6°C/second max.
Time 25°C to peak temperature	8 minutes max.

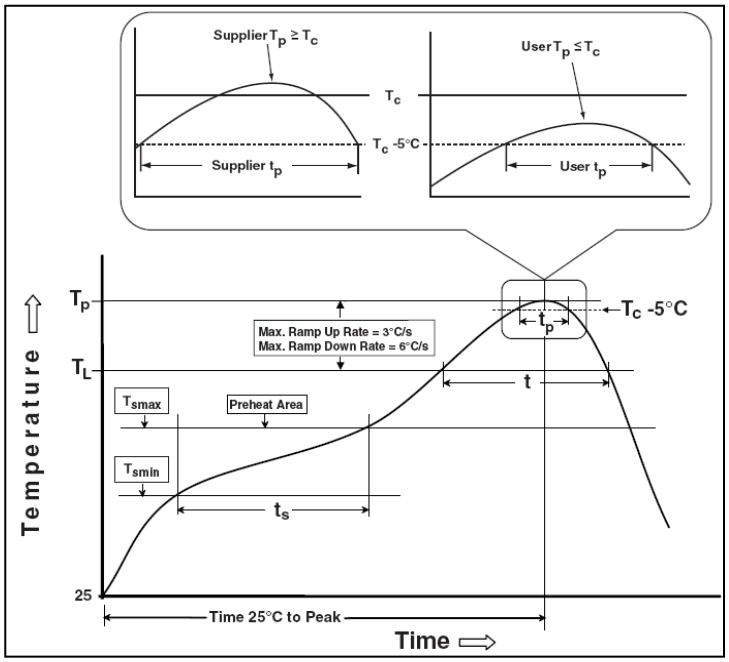
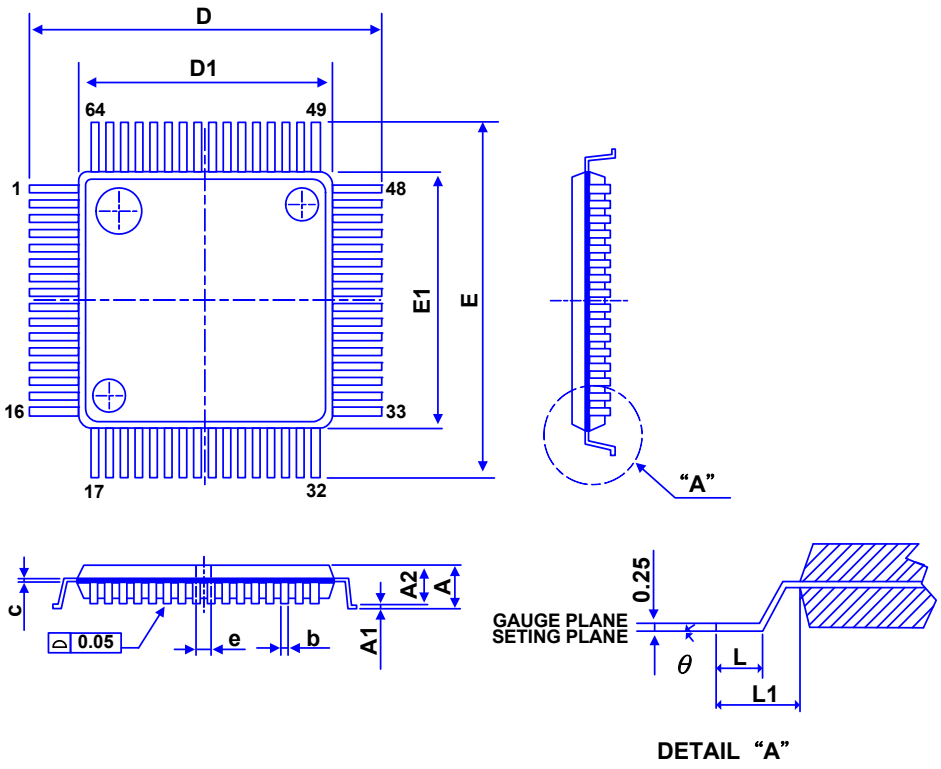


Figure 6 Classification Profile

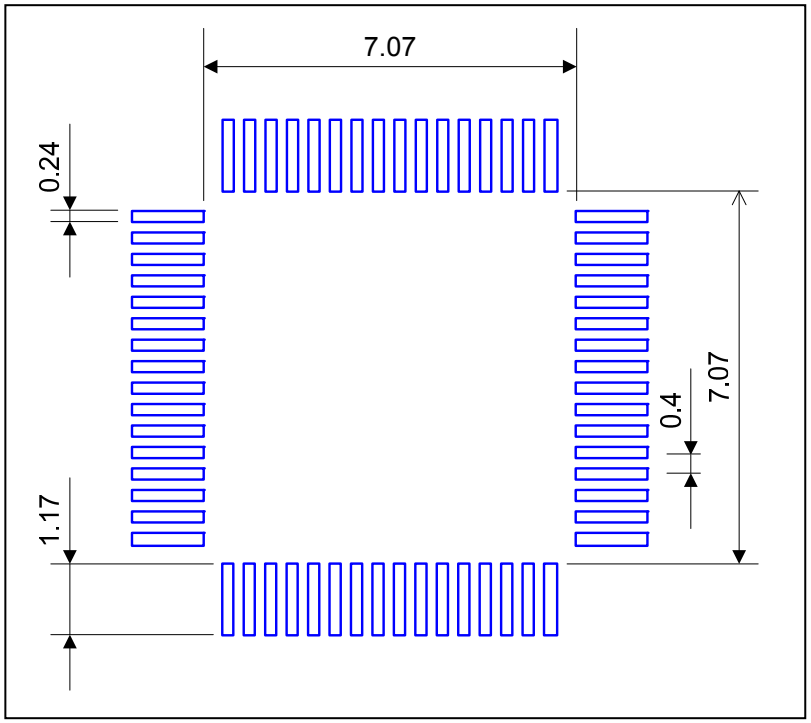
PACKAGE INFORMATION
LQFP-64



SYMBOL	DIMENSIONS IN MILLIMETERS		
	MIN.	NOM.	MAX.
A	-	-	1.60
A1	0.05	-	0.15
A2	1.35	1.40	1.45
D		9.00 BSC	
E		9.00 BSC	
E1		7.00 BSC	
D1		7.00 BSC	
L1		1.00 REF	
L	0.45	0.60	0.75
c	0.09	-	0.20
e		0.40 BSC	
B	0.13	0.18	0.24
θ°	0°	3.5°	7°

Notes:
1.CONTROLLING DIMENSION: MM
2.REFERENCE DOCUMENT: JEDEC MS-026

RECOMMENDED LAND PATTERN



Note:

1. Land pattern complies to IPC-7351.
2. All dimensions in MM.
3. This document (including dimensions, notes & specs) is a recommendation based on typical circuit board manufacturing parameters. Since land pattern design depends on many factors unknown (eg. User's board manufacturing specs), user must determine suitability for use.

REVISION HISTORY

Revision	Detail Information	Date
A	Initial release.	2019.09.04