HV56264

Quad High Voltage Amplifier Array

Features

- Four Independent High Voltage Amplifiers
- 219V Output Voltage Swing
- 11 V/μs Output Slew Rate
- 410 μA Maximum Operating Current for High Voltage Supply
- Wide Operating Close Loop Gain Range: 50 to 100V/V
- 150 kHz, -3 dB Bandwidth with 15 pF Load
- AEC-Q100 Qualified
- TSSOP and TFBGA Packages

Application

- Tunable Laser
- Micro-Electromechanical Systems (MEMS) Driver
- Test Equipment
- Piezoelectric Transducer Driver

General Description

The HV56264 is an AEC-Q100 rated, Quad High Voltage Amplifier Array integrated circuit. The device operates on a 225V high voltage supply and a 5.0V low voltage supply. Amplifiers input voltage range from 0V to 3.3V and output swing ranges from 1.0V to VPP – 6V with a 3 mA sink/source current capability.

The HV56264 is designed for maximum performance with minimal high voltage current. The high voltage current for each amplifier is typically less than 75 μA.

Related Devices

HV264

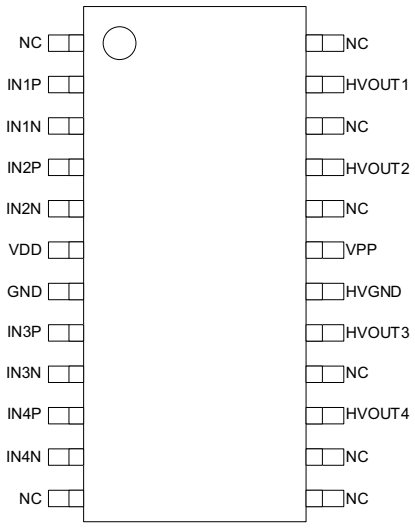
Packages

- TSSOP 24L
- TFBGA 60-Ball

Package Types

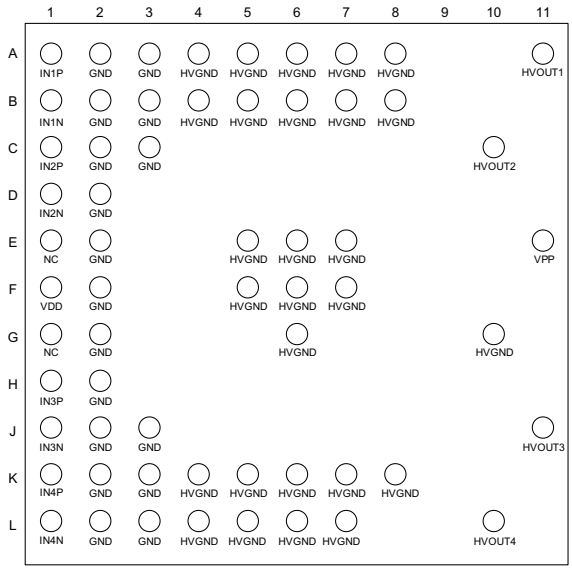
24-Lead TSSOP

TOP VIEW

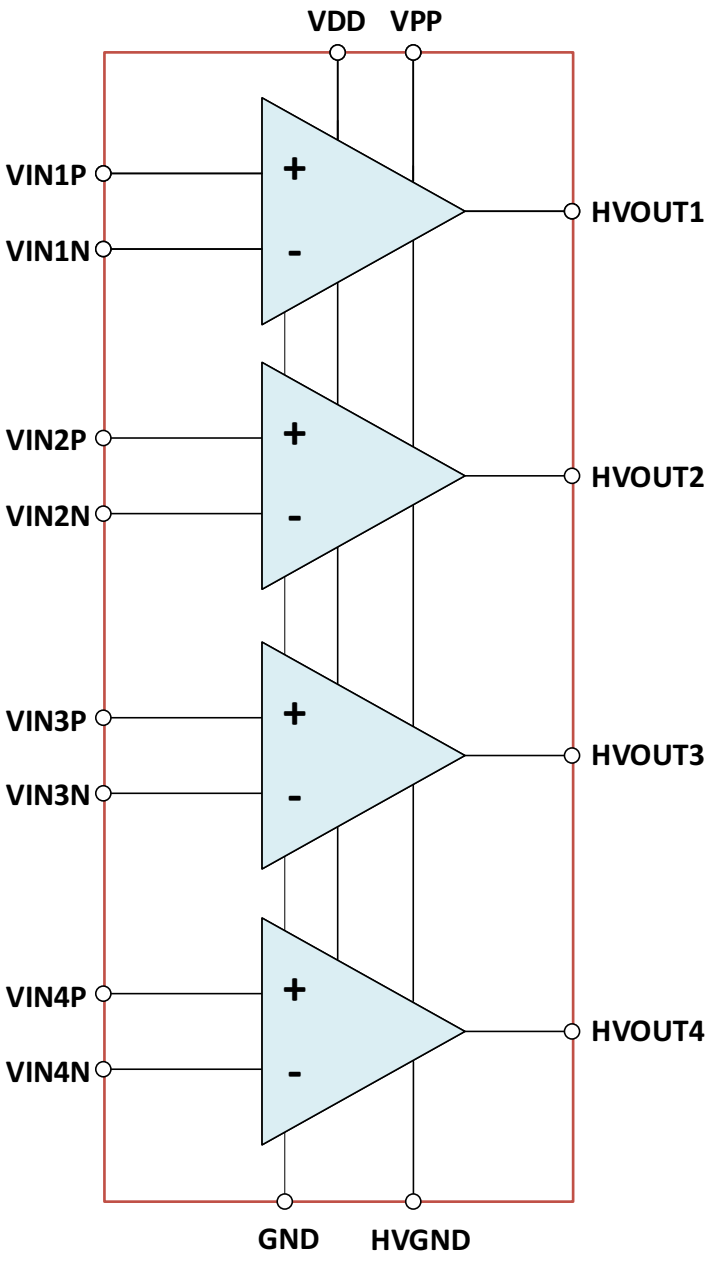


60-Ball TFBGA

TOP VIEW
SEE THROUGH



Block Diagram



1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

$VIN_{XP,N}$ High Voltage Amplifiers Inputs.....–0.3V to 5.5V
V_{DD} Low Output Voltage Supply.....–0.3V to 5.5V
V_{PP} High Voltage Supply for Op-Amps.....–0.5V to 250V
Storage Temperature.....–55°C to +150°C
Operating Junction Temperature.....–40°C to +125°C
ESD Rating HBM High Voltage Pins.....1kV
ESD Rating HBM Low Voltage Pins.....2kV
ESD Rating CDM Corner Pins..... 750V
ESD Rating CDM all Other Pins..... 500V

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: RECOMMENDED OPERATING RATINGS

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
High Voltage Supply	V_{PP}	50	—	225	V	
Low Voltage Supply	V_{DD}	4.5	5	5.5	V	
Inputs for Amplifiers	$VIN_{XP,N}$	0	—	3.3	V	

POWER SEQUENCE

Power-Up Sequence

1. Connect Ground
2. Apply VDD
3. Set all inputs to ground
4. Apply VPP

Power-Down Sequence

Reverse order of Power-Up Sequence

DC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, V_{DD} = 5.0V, V_{PP} = 225V, T_A= T_J= +25°C.
Boldface specifications apply over the full operating temperature range of T_A= T_J = -40°C to 125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
V_{PP} Supply Current	I_{PP}	—	—	300	µA	All inputs at 0V, RF = 5.36 MΩ R1 = 79.6 kΩ VDD = 5.5V
		—	—	**410**		
V_{DD} Supply Current	I_{DD}	—	—	6.6	mA	All inputs at 0V, RF = 5.36 MΩ R1 = 79.6 kΩ VDD = 5.5V
		—	—	**8.3**		
HV_{OUT} VOH1 Voltage Swing	VOH1	**VPP-3**	—	—	V	VIN = 3.3V RF = 536 kΩ R1 = 7.97 kΩ (Note 1)
HV_{OUT} VOH2 Voltage Swing	VOH2	**VPP-6**	—	—		VIN = 3.3V RF = 5.36 MΩ R1 = 79.6 kΩ
HV_{OUT} VOL1 Voltage Swing	VOL1	—	—	**1**		VIN = 0V RF = 536 kΩ R1 = 7.97 kΩ (Note 1)
HV_{OUT} VOL2 Voltage Swing	VOL2	—	—	**1.7**		VIN = 0V RF = 5.36 MΩ R1 = 79.6 kΩ
Input Voltage Range	$V_{INXP,N}$	0		VDD-1.5	V	Note 2
Input Current into $V_{INXP,N}$ pins	I_{IN}	—	—	50	nA	VIN = 1V (Note 1)
High Voltage Output Offset Voltage	HV_{OS}	**–1.9**	—	**1.9**	V	

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Design guidance only.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: Unless otherwise specified, V_{DD} = 5.0V, V_{PP} = 225V, T_A= T_J = +25°C, RF = 5.36 MΩ, R1 = 79.6 kΩ
Boldface specifications apply over the full operating temperature range of T_A= T_J = -40°C to 125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
HV_{OUT} Slew Rate-Rising Edge	SR	4	11	20	V/µs	Load = 15 pF 10%-90% VIN = 0 to 3.3V Square Wave
HV_{OUT} Slew Rate-Falling Edge		4	11	20		
Total External Feedback Resistance	FB	700k	—	7M	Ω	External Resistor Network RFB= RF+RI (Note 2)
Bandwidth (–3dB)	BW	150	—	—	kHz	Load = 15pF VIN= 1.5V DC + 150 mV AC (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Design guidance only.
3: Excluding package parasitic capacitance.

AC ELECTRICAL CHARACTERISTICS (CONTINUED)

Electrical Specifications: Unless otherwise specified, V_{DD} = 5.0V, V_{PP} = 225V, T_A= T_J = +25°C, RF = 5.36 MΩ, R1 = 79.6 kΩ
Boldface specifications apply over the full operating temperature range of T_A= T_J = -40°C to 125°C.

Parameters	Sym.	Min.	Typ.	Max.	Units	Conditions
Closed Loop Gain Range	A_V	50	—	100	V/V	External Resistor Network (Note 2)
HV_{OUT} Capacitive Load	C_{LOAD}	0	—	15	pF	(Note 2) (Note 3)
Output Referred Noise	V_N	—	—	10	mV_{rms}	Measured at HVOUT, VIN = 0.2V (Note 1)
VDD Power Supply Rejection Ratio	PSRR1	40	—	—	dB	VDD = 4.5V to 5.5V VPP = 225V, VIN = 0.1V, DC Measurement (Note 1)
VPP Power Supply Rejection Ratio	PSRR2	60	—	—	dB	VDD = 5V VPP = 50 to 225V, VIN = 0.1V DC Measurement (Note 1)
Crosstalk	Xtalk	—	—	-80	dB	Output Referred. VIN 0 to 3.3V sine wave at 100 Hz with CL = 15 pF (Note 1)

Note 1: Specification is obtained by characterization and is not 100% tested.
2: Design guidance only.
3: Excluding package parasitic capacitance.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: Unless otherwise specified, V_{DD} = 5.0V, V_{PP} = 225V						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Junction Temperature	T_J	–40	—	125	°C	
Storage Temperature	T_S	–55	—	150	°C	
Package Thermal Resistances						
Thermal Resistance - TSSOP	θ_{JC}	—	11.8	—	°C/W	Note 1
	θ_{JA}	—	55	—	°C/W	
Thermal Resistance - TFBGA	θ_{JC}	—	12.4	—	°C/W	
	θ_{JA}	—	47	—	°C/W	

Note 1: 4 Layers FR4 4”X4” PCB

2.0 TYPICAL PERFORMANCE CURVES

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: VDD = 5.0V, VPP = 225V, VIN = 0V, RF = 5.36 MΩ, RI = 79.6 kΩ, C_{LOAD} = 15 pF.

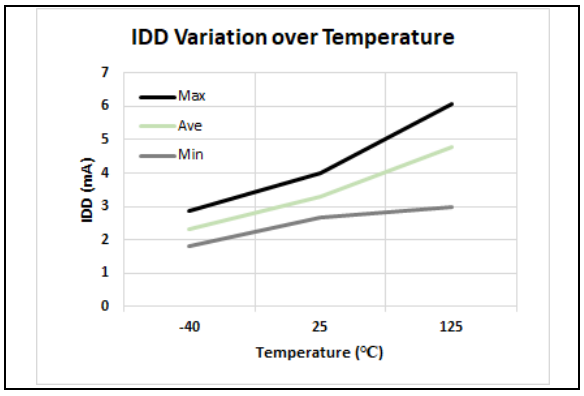


FIGURE 2-1: *I_{DD} Variation Over Temperature.*

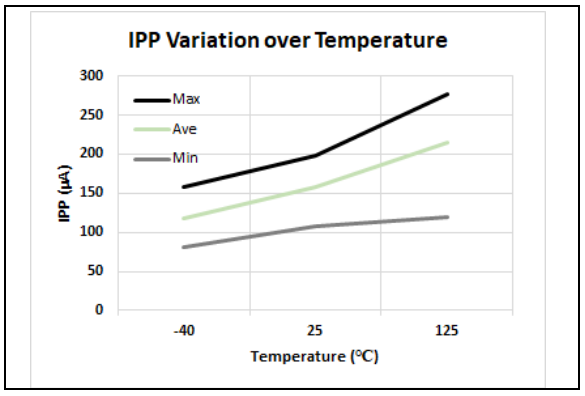


FIGURE 2-4: *I_{PP} Variation Over Temperature.*

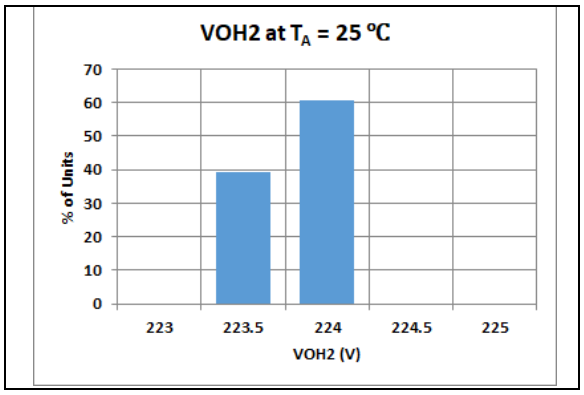


FIGURE 2-2: *VOH2 Distribution at T_A = 25°C.*

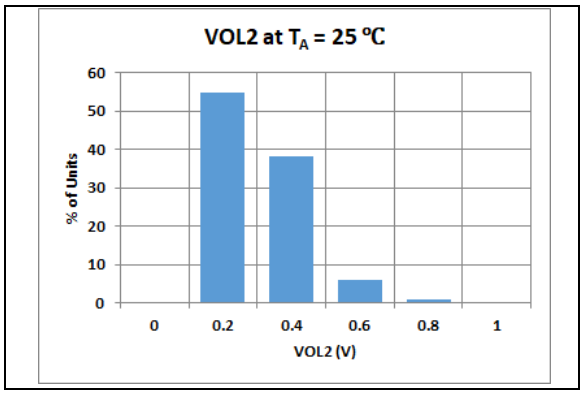


FIGURE 2-5: *VOL2 Distribution at T_A = 25°C.*

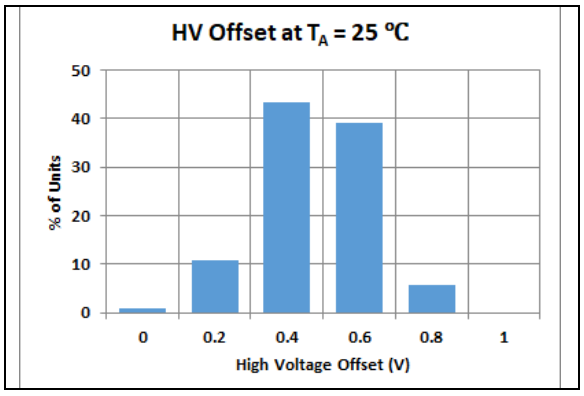


FIGURE 2-3: *HV_{OS} Distribution at T_A = 25°C.*

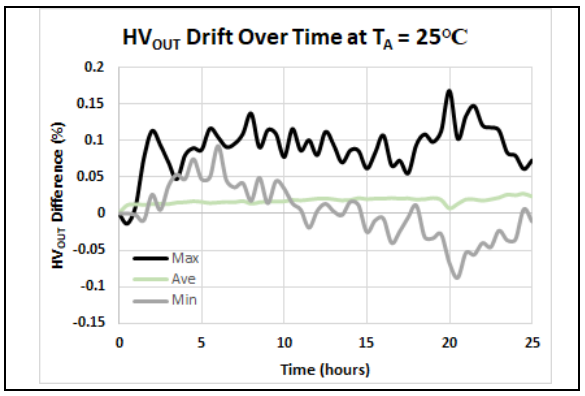


FIGURE 2-6: *HV_{OUT} Drift Over Time at T_A = 25 °C (VIN = 0.2V).*

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: VDD = 5.0V, VPP = 225V, VIN = 0V, RF = 5.36 MΩ, RI = 79.6 kΩ, C_{LOAD} = 15 pF.

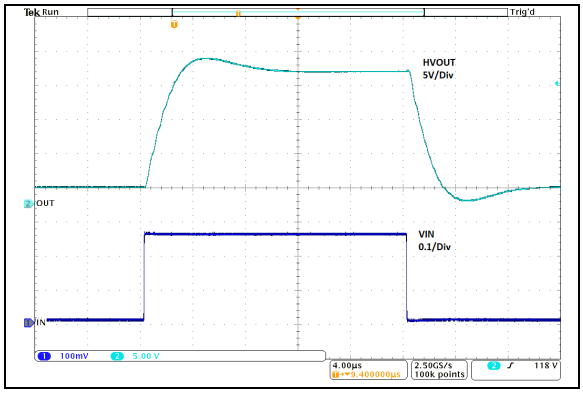


FIGURE 2-7: *Typical Small Signal Pulse Response (VIN = 1.5V to 1.75V, RF = 5.36 MΩ, RI = 79.6 kΩ).*

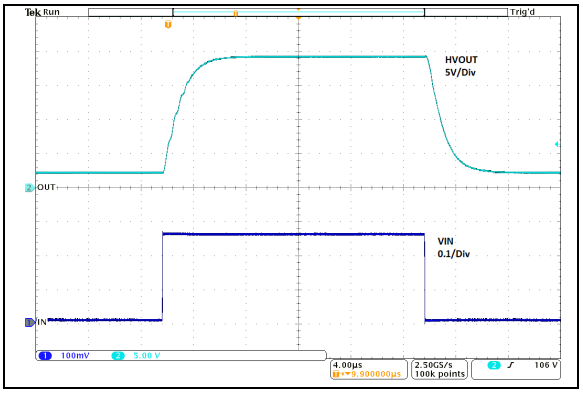


FIGURE 2-10: *Typical Small Signal Pulse Response (VIN = 1.5V to 1.75V, RF = 536 kΩ, RI = 7.97 kΩ).*

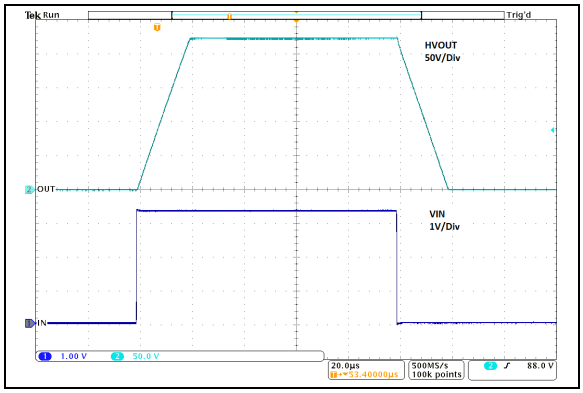


FIGURE 2-8: *Typical Small Signal Pulse Response (VIN = 0V to 3.3V, RF = 5.36 MΩ, RI = 79.6 kΩ).*

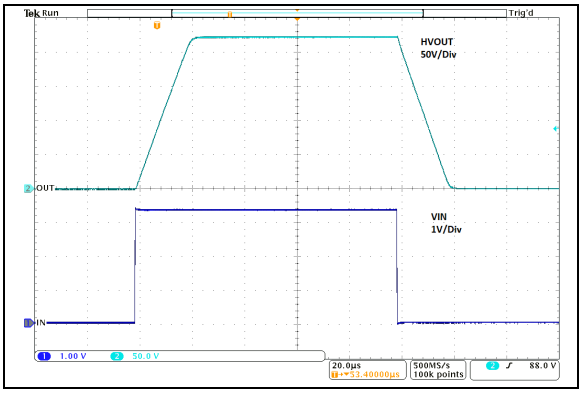


FIGURE 2-11: *Typical Small Signal Pulse Response (VIN = 0V to 3.3V, RF = 536 kΩ, RI = 7.97 kΩ).*

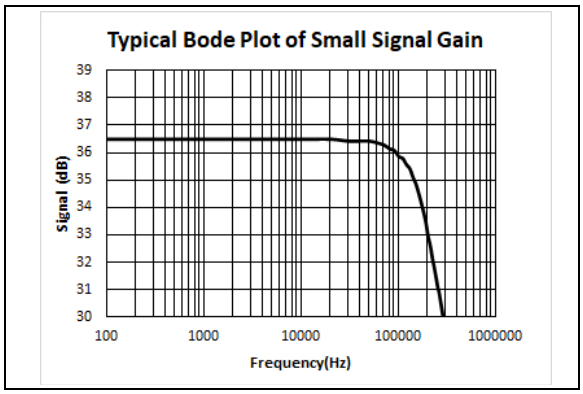


FIGURE 2-9: *Typical Bode Plot of Small Signal Gain (VIN = 1.5V + 0.2AC).*

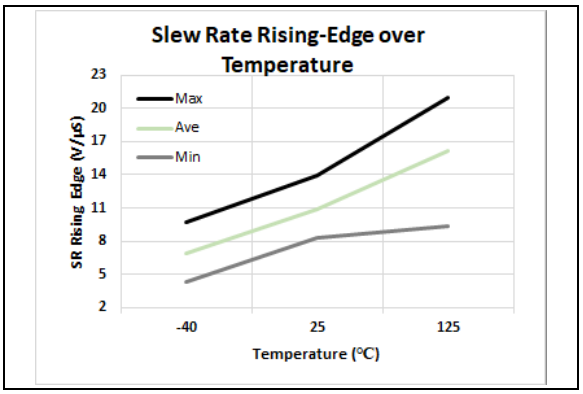


FIGURE 2-12: *Slew Rate Rising-Edge Variation Over Temperature.*

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated: VDD = 5.0V, VPP = 225V, VIN = 0V, RF = 5.36 MΩ, RI = 79.6 kΩ, C_{LOAD} = 15 pF.

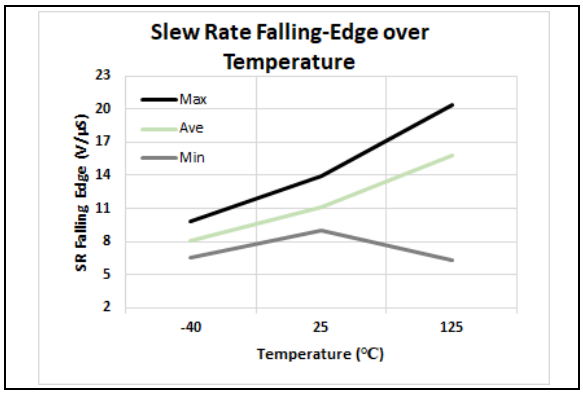


FIGURE 2-13: *Slew Rate Falling-Edge Variation Over Temperature.*

FIGURE 2-15: *PSRR1-VDD (VDD = 5.0V + 0.1 V AC).*

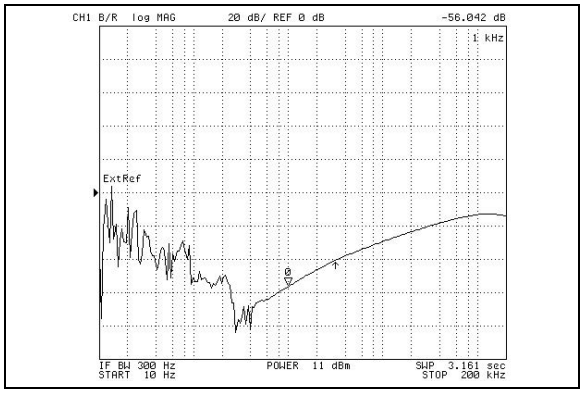


FIGURE 2-14: *PSRR2-VPP (VPP = 225V + 1V AC).*

3.0 PACKAGE PIN CONFIGURATION AND DESCRIPTION

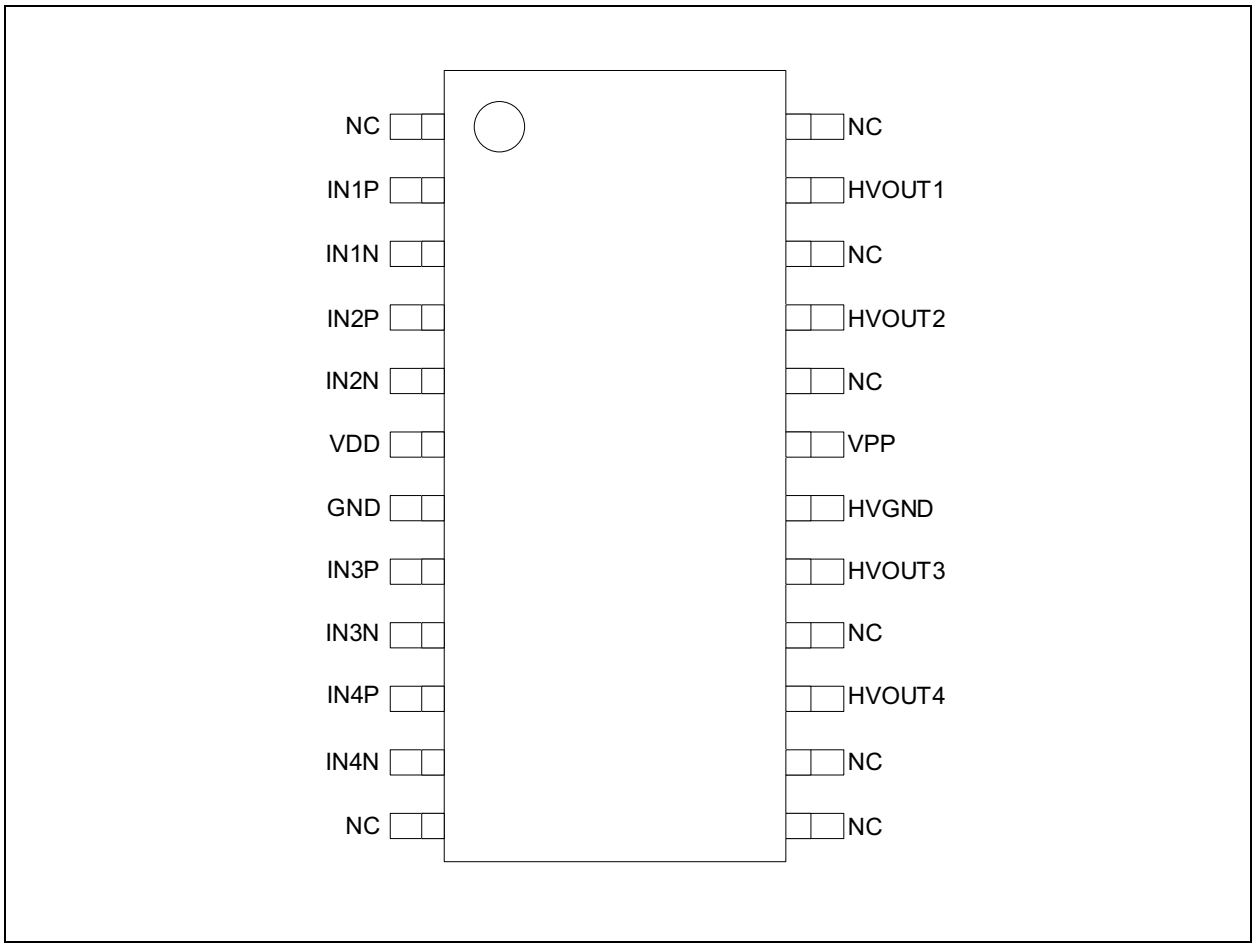


FIGURE 3-1: *TSSOP Pinout.*

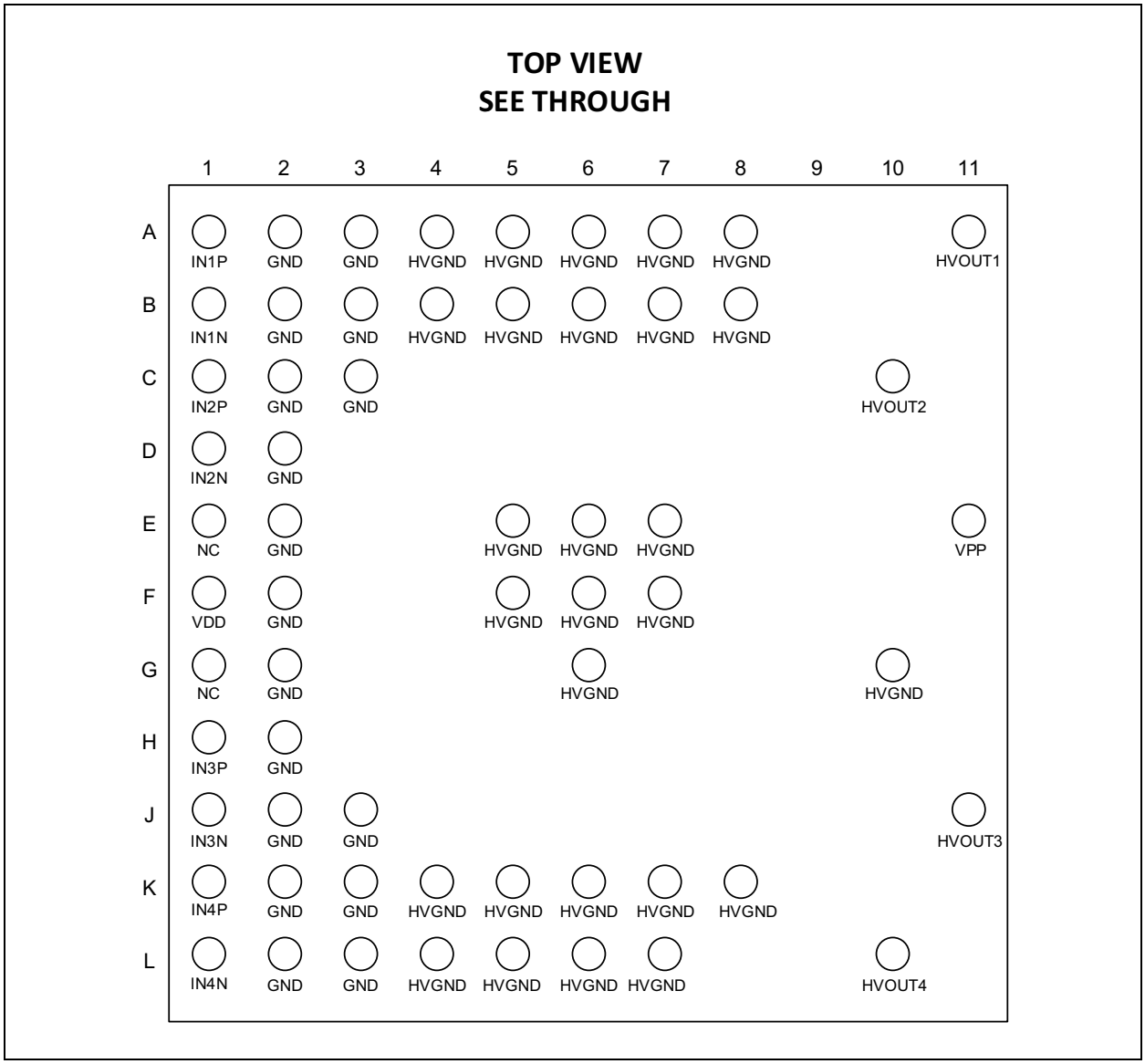


FIGURE 3-2: *TFBGA Pinout.*

TABLE 3-1: PINOUT CONFIGURATION

TSSOP PIN #	TFBGA PIN #	NAME	FUNCTION
1,12,13,14,16,20,22,24	E1,G1	NC	No Connection
2	A1	IN1P	Amplifier 1 Non-inverting Input
3	B1	IN1N	Amplifier 1 Inverting Input
4	C1	IN2P	Amplifier 2 Non-inverting Input
5	D1	IN2N	Amplifier 2 Inverting Input
6	F1	VDD	Low Voltage Supply
7	A2,A3,B2,B3,C2,C3,D2,E2, F2,G2,H2,J2,J3,K2,K3,L2,L3	GND	Ground
8	H1	IN3P	Amplifier 3 Non-inverting Input
9	J1	IN3N	Amplifier 3 Inverting Input
10	K1	IN4P	Amplifier 4 Non-inverting Input
11	L1	IN4N	Amplifier 4 Inverting Input
15	L10	HVOUT4	Amplifier 4 Output
17	J11	HVOUT3	Amplifier 3 Output
18	A4,A5,A6,A7,A8,B4,B5,B6,B7,B8, E5,E6,E7,F5,F6,F7,G6,G10, K4,K5,K6,K7,K8,L4,L5,L6,L7	HVGND	High Voltage Ground
19	E11	VPP	High Voltage Positive Supply
21	C10	HVOUT2	Amplifier 2 Output
23	A11	HVOUT1	Amplifier 1 Output

3.1 IN1P, IN1N, IN2P, IN2N, IN3P, IN3N, IN4P, IN4N Input pins

Input pins for the amplifiers.

3.2 Low Voltage Supply Input Pin (VDD)

Low voltage supply input pin for the amplifiers.

3.3 High Voltage Positive Supply Input Pin (VPP)

High voltage supply input pin for the amplifiers.

3.4 High Voltage Ground (HVGND)

Ground reference pins for the high voltage amplifiers.

3.5 High Voltage Amplifiers Outputs (HVOUT4, HVOUT3, HVOUT2, HVOUT1)

Amplifiers output pins.

3.6 Ground (GND)

Ground reference for input signals and low voltage supplies.

4.0 FUNCTIONAL DESCRIPTION

The HV56264 is a Quad High Voltage Amplifier Array that can operate up to 225V with a source/sink capability of 3 mA. Amplifiers are designed to deliver a 11 V/μs typical output slew rate and sustain a 150 kHz –3 dB Bandwidth for a 15 pF capacitive load.

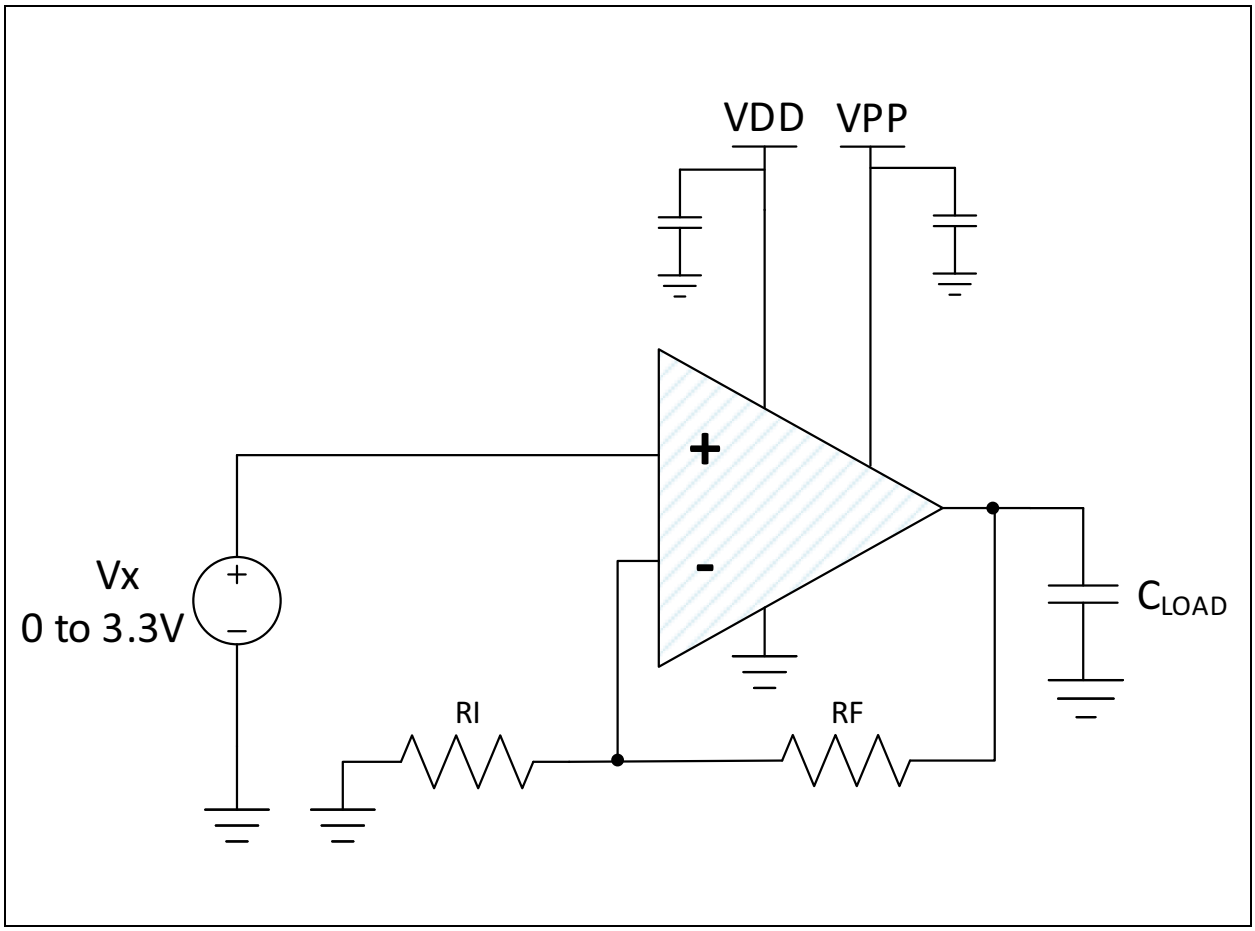
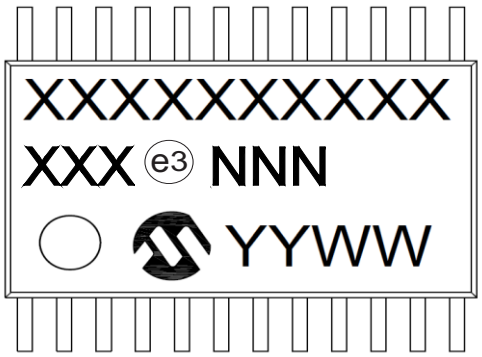


FIGURE 4-1: *Functional Block Diagram.*

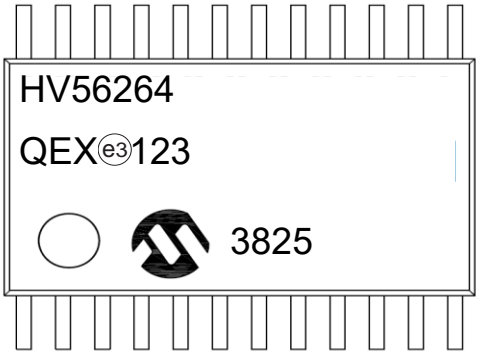
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

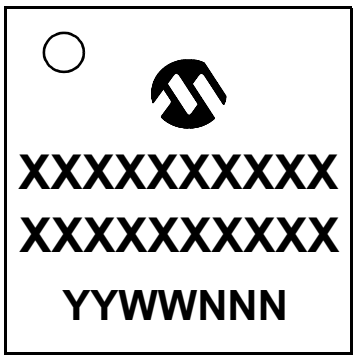
24-Lead TSSOP



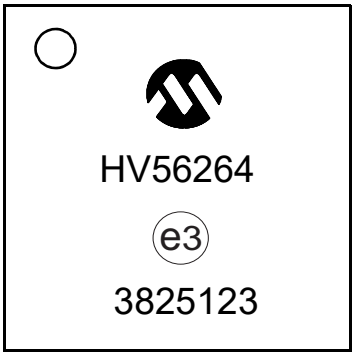
Example



60-Lead TFBGA (6 x 6 mm)



Example

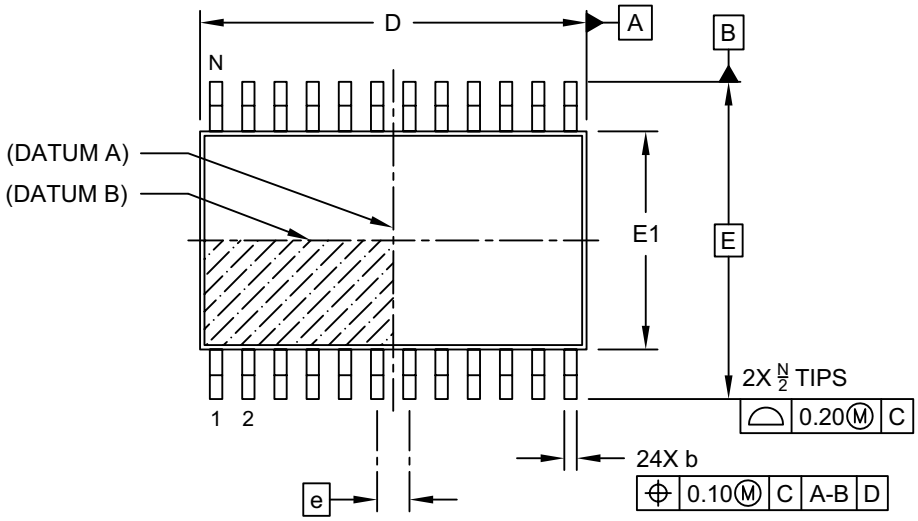


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

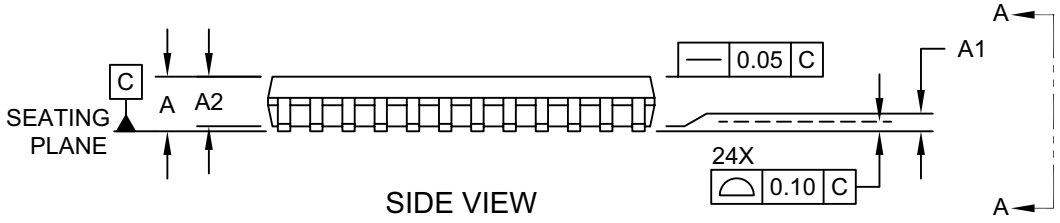
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

24-Lead Thin Shrink Small Outline Package (QE) - 4.40 mm Body [TSSOP]
Supertex Legacy & Micrel Legacy Package

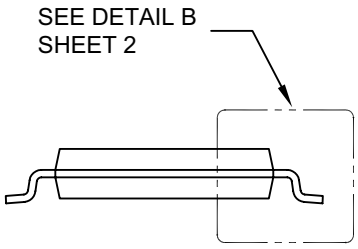
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

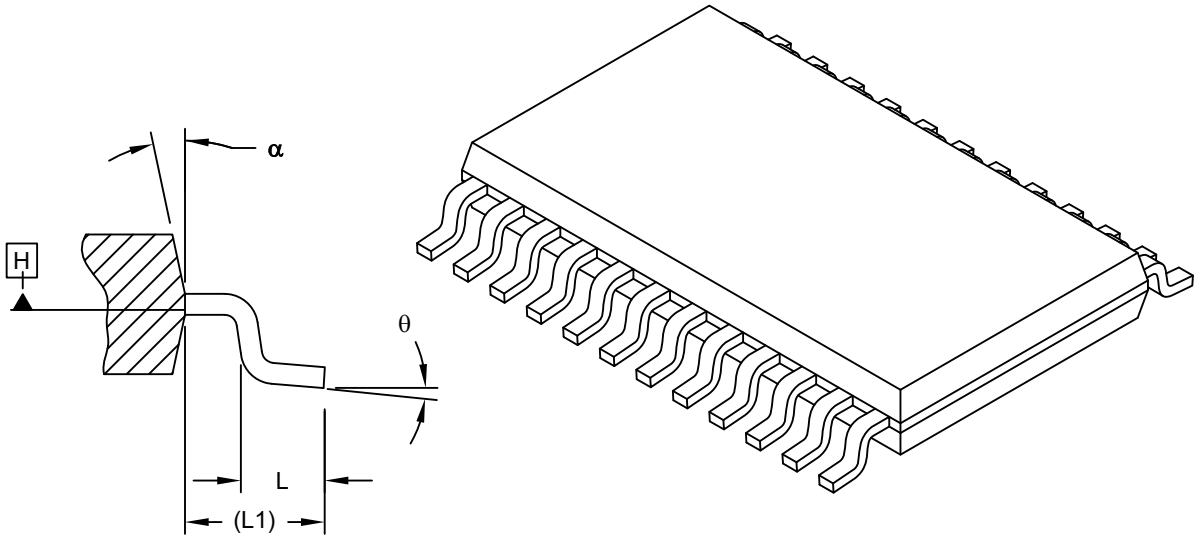


VIEW A-A

Microchip Technology Drawing C04-284A Sheet 1 of 2

24-Lead Thin Shrink Small Outline Package (QE) - 4.40 mm Body [TSSOP]
Supertex Legacy & Micrel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		24	
Lead Pitch	e		0.65 BSC	
Overall Height	A	0.85	-	1.20
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	0.80	1.00	1.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	4°	8°
Overall Width	E		6.40 BSC	
Overall Length	D	7.70	7.80	7.90
Molded Package Width	E1	4.30	4.40	4.50
Lead Width	b	0.19	-	0.30
Mold Draft Angle Top	α		12° REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

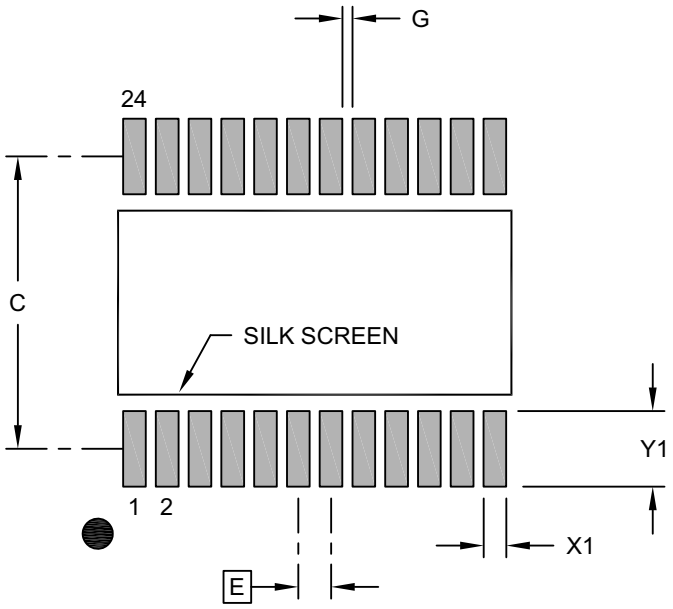
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-284A Sheet 2 of 2

24-Lead Thin Shrink Small Outline Package (QE) - 4.40 mm Body [TSSOP]
Supertex Legacy & Micrel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.80	
Contact Pad Width (X24)	X1			0.45
Contact Pad Length (X24)	Y1			1.50
Contact Pad to Center Pad (X20)	G1	0.20		

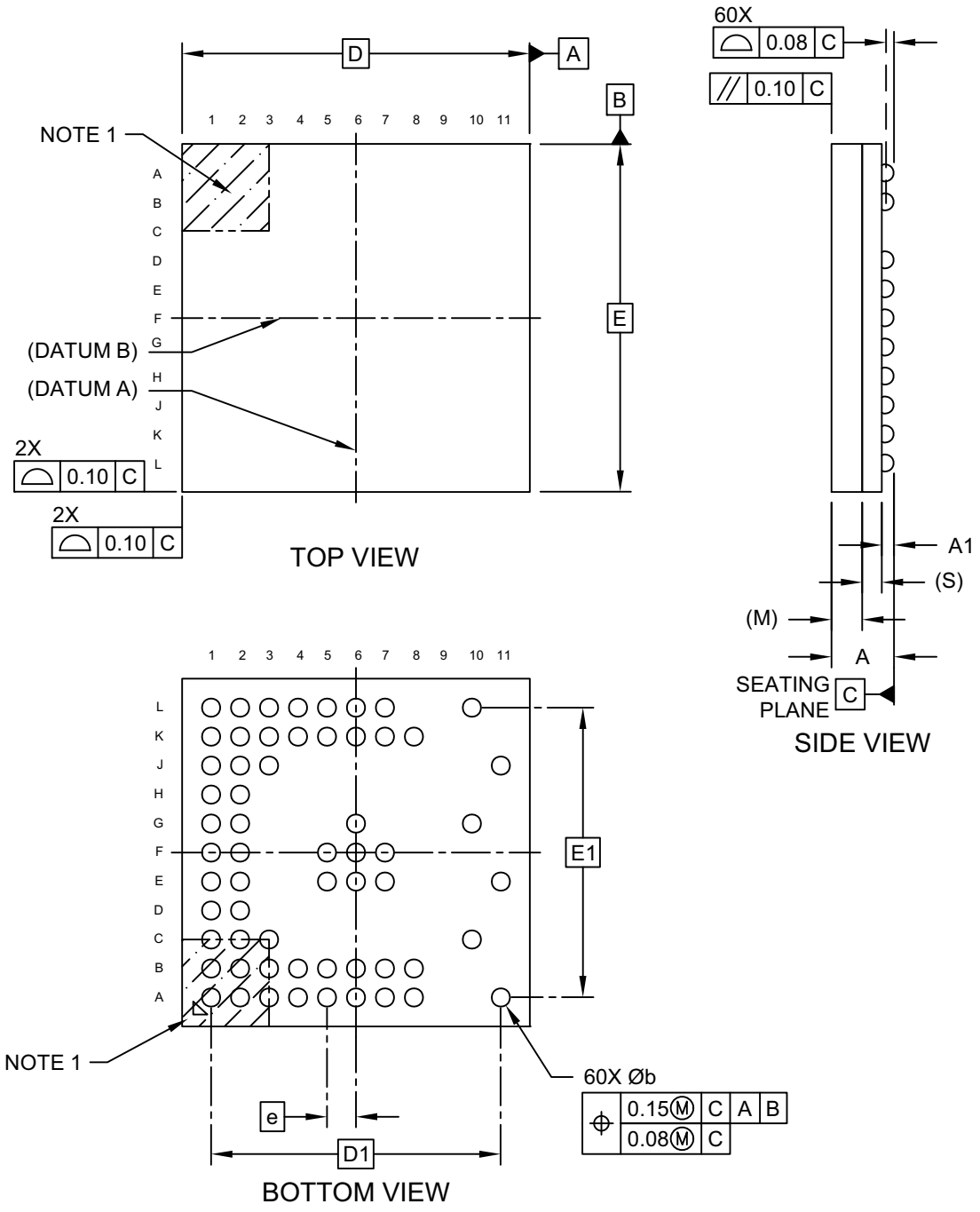
Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2284A

60-Ball Thin Fine-Pitch Ball Grid Array (AKA) - 6x6x1.20 mm Body [TFBGA]

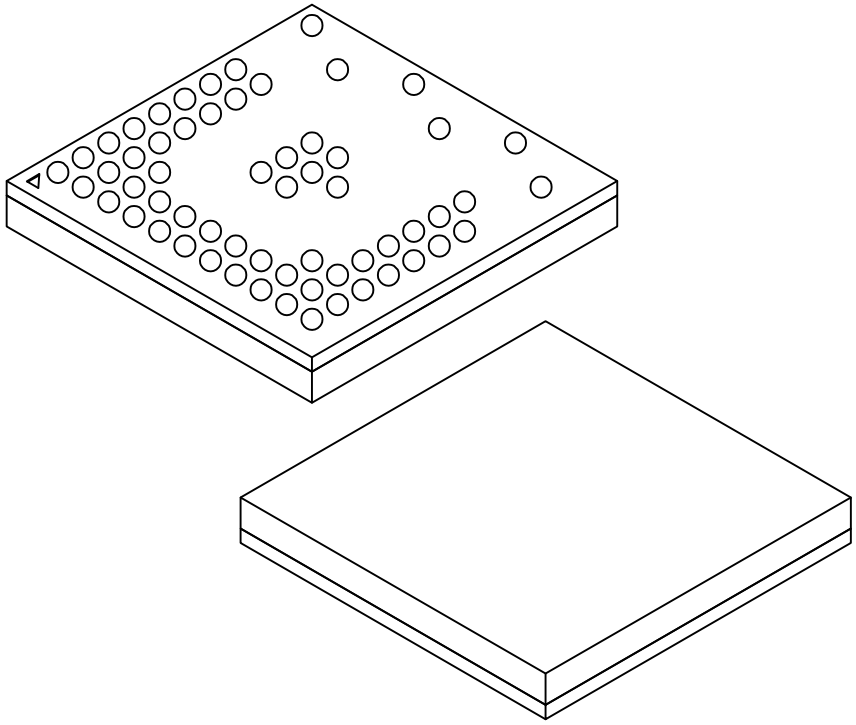
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-1277 Rev A Sheet 1 of 2

60-Ball Thin Fine-Pitch Ball Grid Array (AKA) - 6x6x1.20 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Terminals	N		60	
Pitch	e		0.50 BSC	
Overall Height	A	–	–	1.20
Ball Height	A1	0.16	–	0.26
Mold Thickness	M		0.53 REF	
Substrate Thickness	S		0.248 REF	
Overall Length	D		6.00 BSC	
Ball Array Length	D1		5.00 BSC	
Overall Width	E		6.00 BSC	
Ball Array Width	E1		5.00 BSC	
Ball Width	b	0.27	0.30	0.37

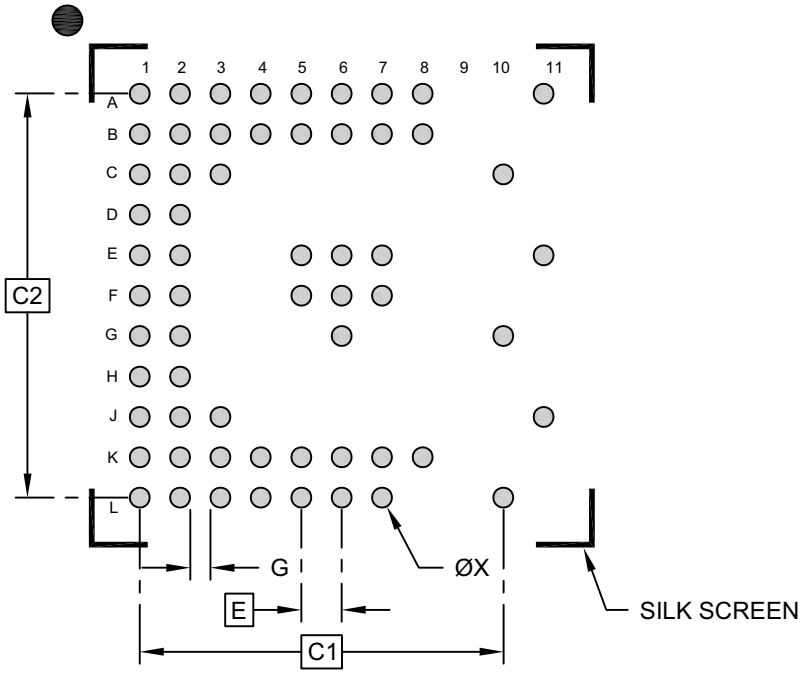
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-1277 Rev A Sheet 2 of 2

60-Ball Thin Fine-Pitch Ball Grid Array (AKA) - 6x6x1.20 mm Body [TFBGA]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.50 BSC	
Contact Pad Spacing	C1		5.00 BSC	
Contact Pad Spacing	C2		5.00 BSC	
Contact Pad Width (X60)	X			0.25
Space Between Contact Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-3277 Rev A

APPENDIX A: REVISION HISTORY

Revision B (January 2021)

The following is the list of modifications:

- Updated the DC Electrical Characteristics table.
- Minor typographical and layout edits.

Revision A (December 2020)

- Initial Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X[(1)]	-X	/XXX	-XXX
Device	Tape and Reel Option	Temperature Range	Package	Option

Device:	HV56264: Quad High Voltage Amplifier Array
Media Type	T = 2500/Reel for QEX Package = 3000/Reel for AKA Package
Temperature Range:	E = -40°C to +125°C (Extended) RoHS Compliant
Package:	QEX = 24LD TSSOP 6.4x4.4 mm AKA = 60-Ball Count TFBGA 6x6x1.2 mm
Option	VAO = Automotive Grade

Examples:

a) HV56264T-E/QEX-VAO: Quad High-Voltage Amplifier Array, Automotive Grade, 24-Lead TSSOP package, 2500 Reel

b) HV56264T-E/AKA-VAO: Quad High-Voltage Amplifier Array, Automotive Grade, 60-Terminal Count TFBGA package, 3000/Reel

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

NOTES:

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specifications contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is secure when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods being used in attempts to breach the code protection features of the Microchip devices. We believe that these methods require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Attempts to breach these code protection features, most likely, cannot be accomplished without violating Microchip's intellectual property rights.
- Microchip is willing to work with any customer who is concerned about the integrity of its code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of its code. Code protection does not mean that we are guaranteeing the product is "unbreakable". Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

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