HV265

4-Channel, 205V, High-Voltage Amplifiers Array

Features

- Four Independent High Voltage Amplifiers
- Up to +205 V Output Voltage
- Gain of 82 V/V with Internal Feedback Resistors
- 0.02 V/µs Minimum Output Slew Rate
- Less than 10 ms Settling Time
- Less than 1 kΩ Output Impedance
- Up to 200 pF Output Load
- 30 kHz Gain Bandwidth Product
- 24-lead TSSOP Package

Application

- MEMS Driver

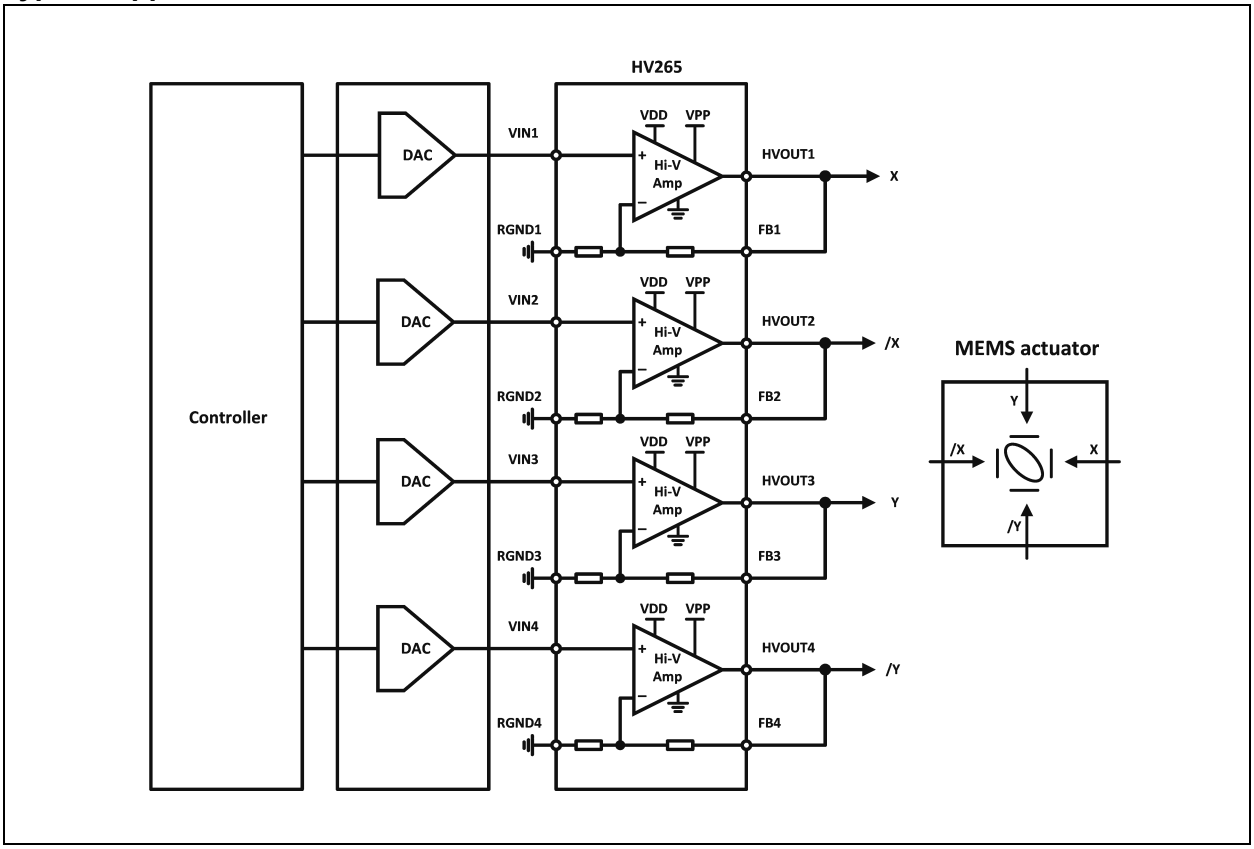
General Description

The HV265 device is a 4-channel high-voltage operational amplifier array with an optional internal feedback resistor network.

The amplifier array IC operates on a 225 V high-voltage supply and a 5 V low-voltage supply. Each channel has its independent input and output ports. When the internal feedback resistor network is used, the closed-loop gain is set to 82 V/V. High value SiCr resistors are used for internal feedback networks to minimize the power consumption. The input accepts voltage in the range of 0.05V and 2.5V.

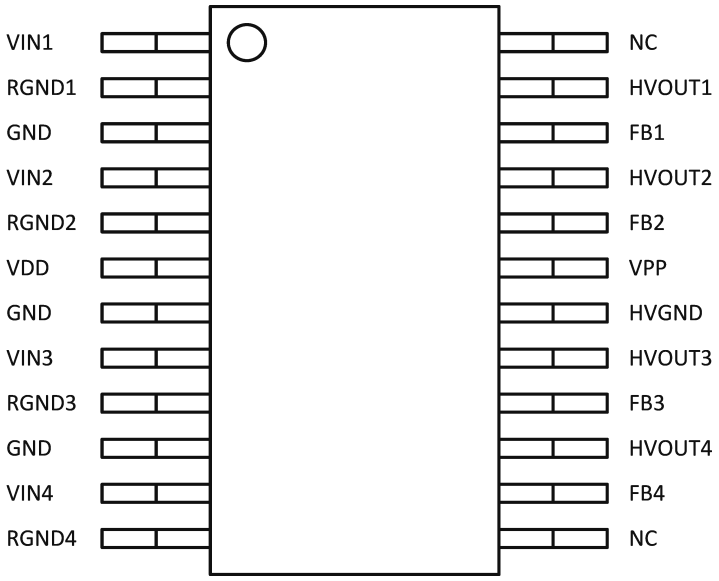
The output impedance of the amplifier is less than 1 kΩ and the output can drive a capacitive load up to 200 pF. The amplifier is designed to have good temperature stability and low output drift.

Typical Application Circuit



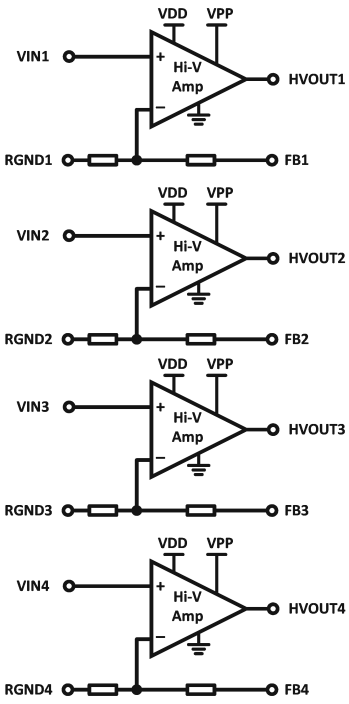
Package Types (Top View)

HV265
24-Lead TSSOP



See Table 2-1.

Block Diagram



NOTES:

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings †

Low supply voltage (V_{DD}) ..... -0.5V to 6.5V
High supply voltage (V_{PP}) ..... -0.5V to 250V
Input analog voltage (V_{IN}) ..... - 0.3V to V_{DD}
Maximum junction temperature ..... +125°C
Storage temperature ..... -65°C to +150°C
ESD Rating low voltage pins ..... 2 kV HBM, 500 V CDM, 750 V CDM corner lead
ESD Rating high voltage pins ..... 500 V HBM, 500 V CDM, 750 V CDM corner lead

† Notice: Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

TABLE 1-1: OPERATING SUPPLY VOLTAGES

Electrical Specifications: Unless otherwise specified: T_A = +25°C. **Boldface** specifications apply over the T_A range of -40 to +85°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
High Voltage Supply	V_{PP}	50	—	225	V	Note 1
Low Voltage Supply	V_{DD}	4.5	5.0	5.5	V	

Note 1: Specification is obtained by characterization and is not 100% tested.

ELECTRICAL CHARACTERISTICS

Electrical Specifications: unless otherwise specified, V_{DD} = 5.0V, V_{PP} = 225V, T_A = +25°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Conditions
Input Ground Range	R_{GND}	0	0	V_{DD}	V	
Input Analog Voltage	V_{IN}	0	—	3.3	V	
Quiescent V_{PP} Supply Current	$I_{PP}Q$	—	300	500	µA	V_{IN} = 0 or 5V
Quiescent V_{DD} Supply Current	$I_{DD}Q$	—	3	5	mA	V_{IN}= 0 or 5V
V_{PP} Supply Current	I_{PP}	—	—	**500**	µA	V_{IN}= $2V_{P-P}$ 100 Hz sine, C_L = 200 pF
V_{DD} Supply Current	I_{DD}	—	—	**5**	mA	V_{IN}= $2V_{P-P}$ 100 Hz sine, C_L = 200 pF
HV_{OUT} Output Voltage Range	HV_{OUT}	**1.85**		**V_{PP} - 10**	V	C_L = 200 pF
HV_{OUT} Sink Current	I_{SINK}	3			mA	C_L = 200 pF
HV_{OUT} Source Current	I_{SOURCE}	3			mA	C_L = 200 pF
HV_{OUT} High Level Output	V_{OH}	204.8			V	C_L = 200 pF, V_{IN}= 2.7V
HV_{OUT} Input DC Offset	HV_{OS}			±16	mV	Note 3 C_L = 200 pF
HV_{OUT} Drift Over Time (Room Temperature)	Drift		±30		mV	Note 3 C_L = 200 pF, V_{IN}= 2.5V
HV_{OUT} Temperature Coefficient (Drift Over Temperature)	Temp.		±115		mV	Note 3 C_L = 200 pF, V_{IN}= 2.5V T_J = -40°C to 85°C

Note 1: Recommended Operating Conditions: V_{IN}=0V, V_{DD}=5.0V, V_{PP}=+225V unless noted. Tj=25°C
2: Design guidance only.
3: Specification is obtained by characterization and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

Electrical Specifications: unless otherwise specified, V_{DD} = 5.0V, V_{PP} = 225V, T_A = +25°C.						
Parameter	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
HV_{OUT} Output Impedance	Z_{OUT}			1000	Ω	**Note 3** V_{IN}= 1.25 V_{DC} Test Frequency = 100 Hz C_L = 200 pF
Gain Bandwidth Product	GBWP	30			kHz	**Note 3** C_L = 200 pF
Slew Rate (HV_{OUT} from 10% to 90% and from 90% to 10%)	SR	**0.02**	-	-	V/µs	C_L = 200 pF
Settling Time (Within 1% of final HV_{OUT})	t_{ST}			10	ms	**Note 3** C_L = 200 pF, V_{IN}= 0 to 2.4 V
Feedback Impedance R_f + R_i	R_{FB}	4.9	7.0	-	MΩ	**Note 2**
Closed Loop Gain (dVo/dVin) (Internal Feedback Resistor Network)	A_V	**75.4**	**82**	**88.4**	V/V	C_L = 200 pF
HV_{OUT} Capacitive Load	C_L	0		200	pF	**Note 2**
Output Referred Noise	V_N			10	mV_{RMS}	**Note 3** Noise from 1 Hz to 10 kHz.
V_{DD} Power Supply Rejection	PSRR1	30			dB	**Note 3** 1 kHz
V_{PP} Power Supply Rejection	PSRR2	50			dB	**Note 3** 1 kHz
Crosstalk Rejection	Xtalk	80			dB	**Note 3** V_{IN}= 0 to 2.5V 100 Hz sine, C_L = 200 pF

Note 1: Recommended Operating Conditions: V_{IN}=0V, V_{DD}=5.0V, V_{PP}=+225V unless noted. Tj=25°C

2: Design guidance only.

3: Specification is obtained by characterization and is not 100% tested.

TEMPERATURE SPECIFICATIONS

Electrical Specifications: unless otherwise specified, V_{DD} = 5.0V, V_{PP} = 225V						
Parameters	**Sym.**	**Min.**	**Typ.**	**Max.**	**Units**	**Conditions**
Temperature Ranges						
Operating Junction Temperature Range	T_J	-40	—	+85	°C	
Maximum Junction Temperature	$T_{J(MAX)}$	—	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Package Thermal Resistances						
Thermal Resistance, 24L-TSSOP	θ_{JA}	—	87	—	°C/W	

1.1 Typical Performance Curves

Note: The graphs and tables provided below are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

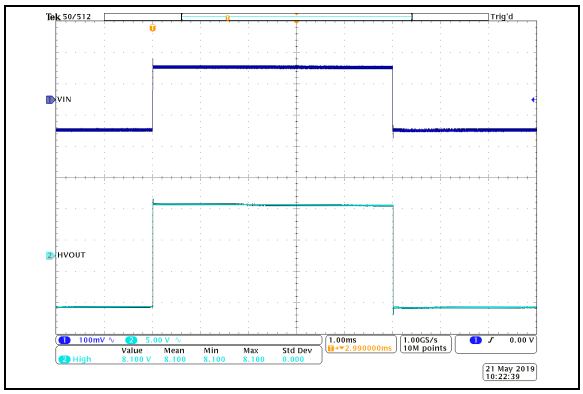


FIGURE 1-1: *Typical Small-Signal Pulse Response (VIN=0.9~1.1V pulse 100 Hz. CL=200 pF).*

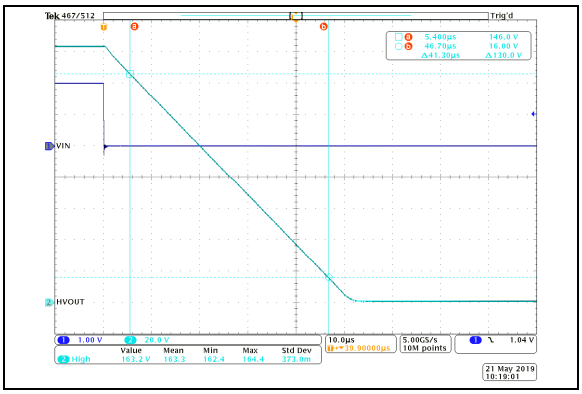


FIGURE 1-4: *Typical Fall Time (VIN = 0~2V Pulse 100 Hz. CL=200 pF).*

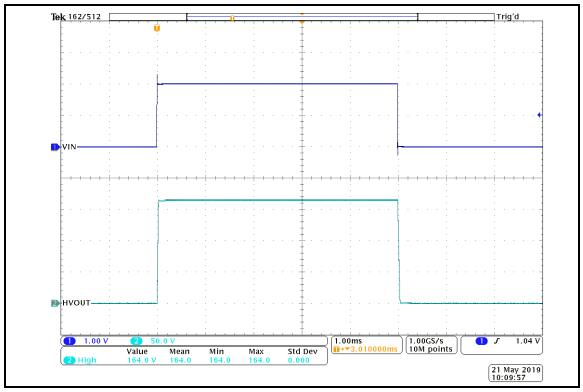


FIGURE 1-2: *Typical Large-Signal Pulse Response (VIN = 0~2V pulse 100 Hz. CL=200 pF).*

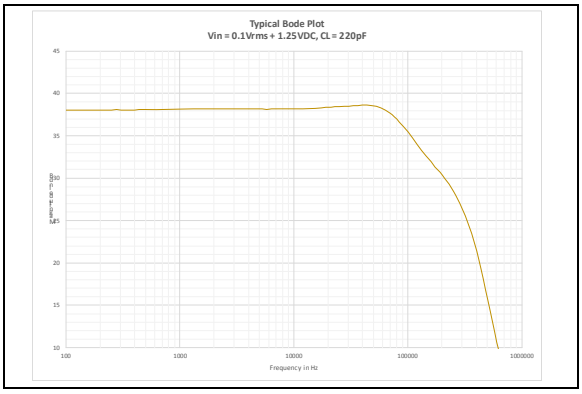


FIGURE 1-5: *Typical Bode Plot of Small Signal Input (VIN=100 mVp-p with 1.25 VDC).*

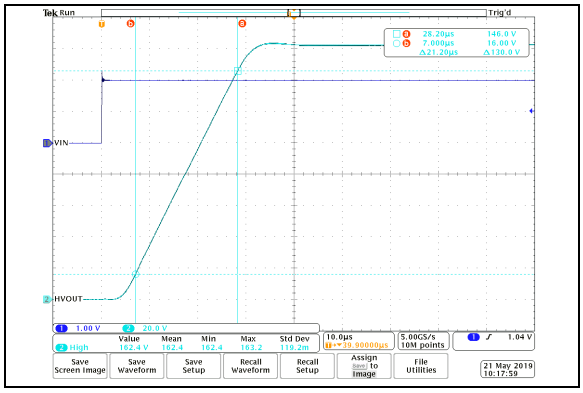


FIGURE 1-3: *Typical Rise Time (VIN = 0~2V Pulse 100 Hz. CL=200 pF).*

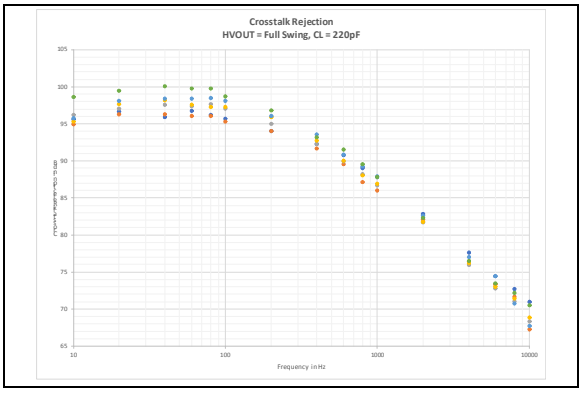


FIGURE 1-6: *Typical Crosstalk Rejection vs Frequency.*

Note: The graphs and tables provided below are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g. outside specified power supply range) and therefore outside the warranted range.

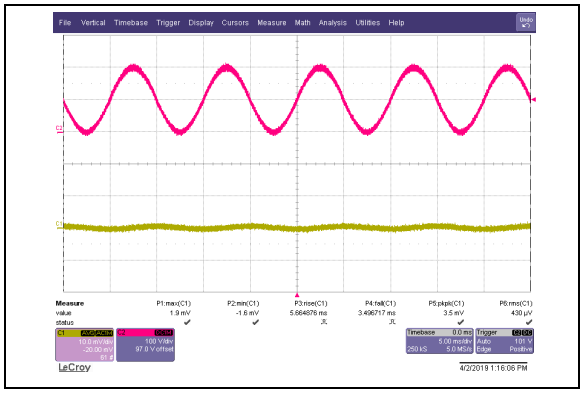


FIGURE 1-7: *Typical Crosstalk Rejection in Time Domain (Source VIN = 0~2.5V Sine).*

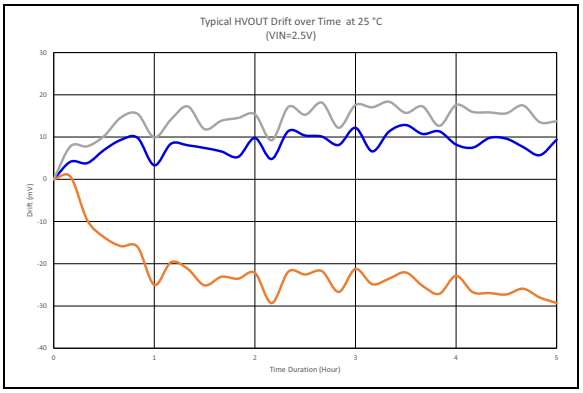


FIGURE 1-10: *Typical HV_{OUT} Drift Over Time. V_{PP}=225V,V_{DD}=5.0V,V_{IN}=2.5V@T_A=25°C.*

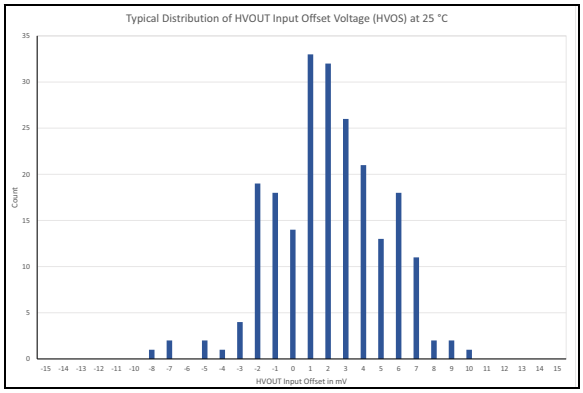


FIGURE 1-8: *Distribution of Input Offset at T_A = 25°C.*

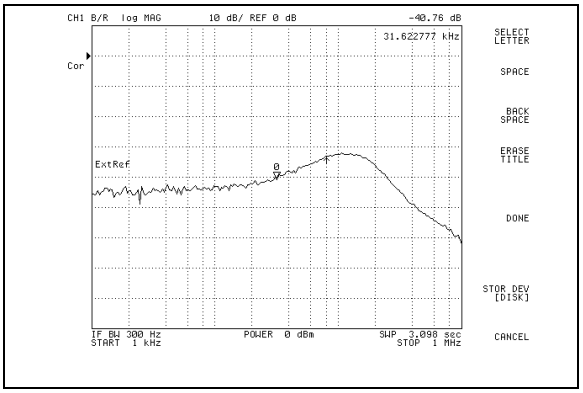


FIGURE 1-11: *Typical Power Supply Rejection from V_{DD} vs Frequency.*

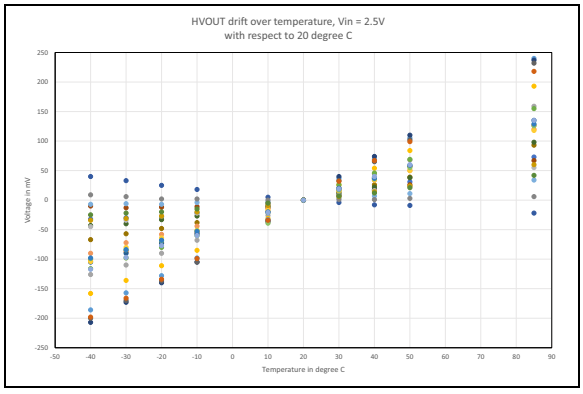


FIGURE 1-9: *Distribution of Typical HV_{OUT} Drift Over Temperature (VIN = 2.5VDC in Reference to T_A = 20°C.*

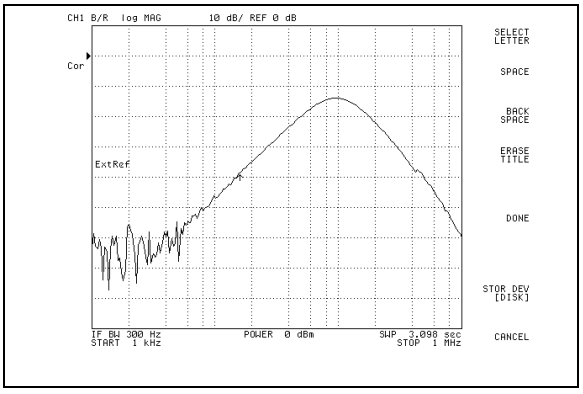


FIGURE 1-12: *Typical Power Supply Rejection from V_{PP} vs Frequency.*

NOTES:

2.0 PIN DESCRIPTION

The descriptions of the pins are listed in Table 2-1.

TABLE 2-1: PIN FUNCTION TABLE

Pin Number	Symbol	Description
1	$V_{IN}1$	Amplifier Input 1
2	RGND1	Resistor Ground 1. Typically grounded.
3	GND	Low Voltage Ground
4	$V_{IN}2$	Amplifier Input 2
5	RGND2	Resistor Ground 2. Typically grounded.
6	VDD	Positive Low Voltage Supply
7	GND	Low Voltage Ground
8	$V_{IN}3$	Amplifier Input 3
9	RGND3	Resistor Ground 3. Typically grounded.
10	GND	Low Voltage Ground
11	$V_{IN}4$	Amplifier Input 4
12	RGND4	Resistor Ground 4. Typically grounded.
13	NC	No Connection
14	FB4	Feedback Input 4
15	$HV_{OUT}4$	High Voltage Output 4
16	FB3	Feedback Input 3
17	$HV_{OUT}3$	High Voltage Output 3
18	HVGND	High Voltage Ground
19	VPP	Positive High Voltage Supply
20	FB2	Feedback Input 2
21	$HV_{OUT}2$	High Voltage Output 2
22	FB1	Feedback Input 1
23	$HV_{OUT}1$	High Voltage Output 1
24	NC	No Connection

3.0 DEVICE DESCRIPTION

3.1 Power-On/Power-Off Sequence

The device can be damaged by an improper power-up/down sequence. The acceptable power-on/off sequences are shown in Table 3-1 and Table 3-2. The user may add an external diode across V_{PP} and V_{DD} for additional protection. The anode of the diode is connected to V_{DD} and the cathode is connected to V_{PP}. Any low-current high-voltage diode such as a 1N4004 is adequate.

TABLE 3-1: ACCEPTABLE POWER-ON SEQUENCES

Option 1		Option 2	
Steps	**Description**	**Steps**	**Description**
1	V_{DD}	1	V_{DD}
2	V_{PP}	2	Inputs
3	Inputs	3	V_{PP}

TABLE 3-2: ACCEPTABLE POWER-OFF SEQUENCES

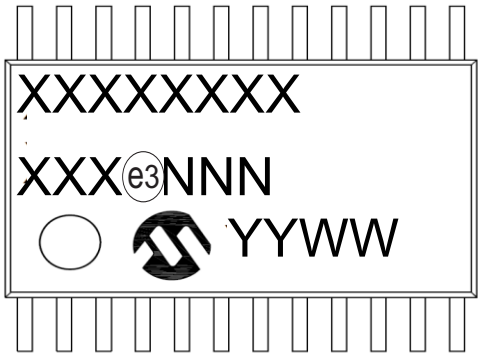
Option 1		Option 2	
Steps	**Description**	**Steps**	**Description**
1	Inputs	1	V_{PP}
2	V_{PP}	2	Inputs
3	V_{DD}	3	V_{DD}

NOTES:

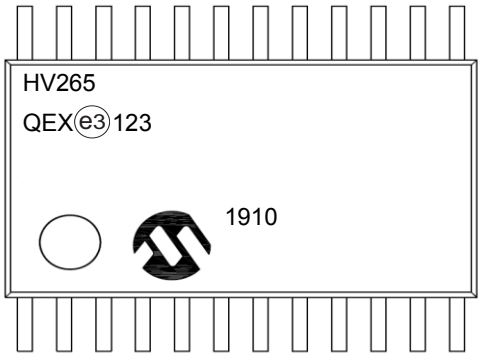
4.0 PACKAGING INFORMATION

4.1 Package Marking Information

24-Lead TSSOP



Example

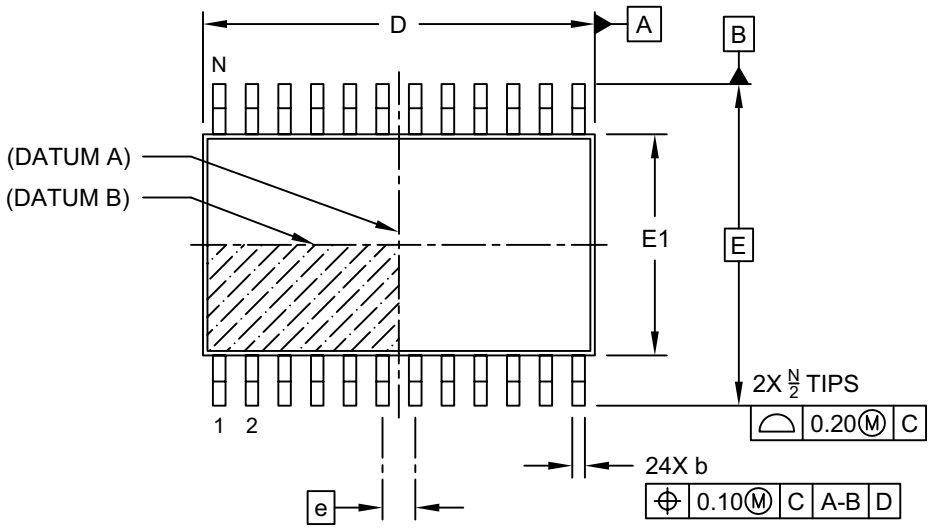


Legend:	XX...X	Product Code or Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

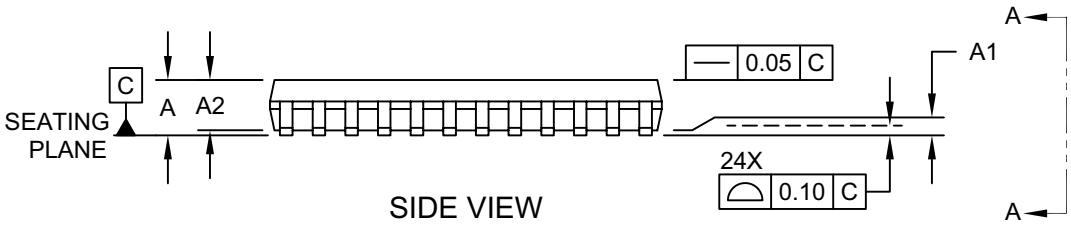
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information. Package may or may not include the corporate logo.

24-Lead Thin Shrink Small Outline Package (QE) - 4.40 mm Body [TSSOP]
Supertex Legacy & Micrel Legacy Package

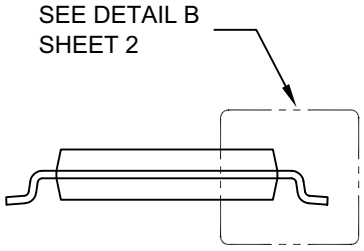
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

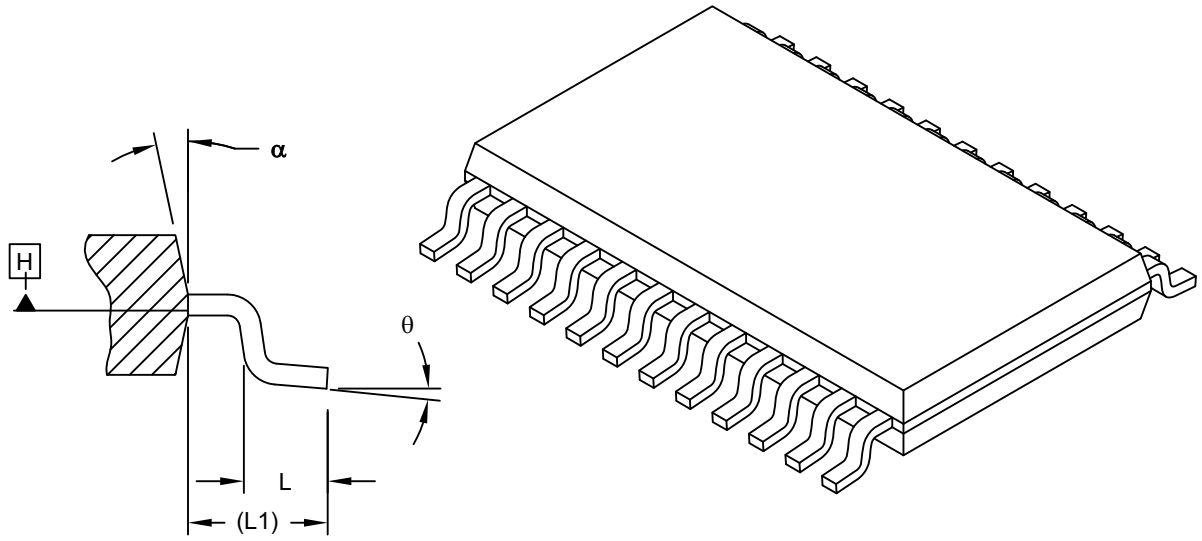


VIEW A-A

Microchip Technology Drawing C04-284A Sheet 1 of 2

24-Lead Thin Shrink Small Outline Package (QE) - 4.40 mm Body [TSSOP]
Supertex Legacy & Micrel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL B

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		24	
Lead Pitch	e		0.65 BSC	
Overall Height	A	0.85	-	1.20
Standoff	A1	0.05	0.10	0.15
Molded Package Thickness	A2	0.80	1.00	1.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	θ	0°	4°	8°
Overall Width	E		6.40 BSC	
Overall Length	D	7.70	7.80	7.90
Molded Package Width	E1	4.30	4.40	4.50
Lead Width	b	0.19	-	0.30
Mold Draft Angle Top	α		12° REF	

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M

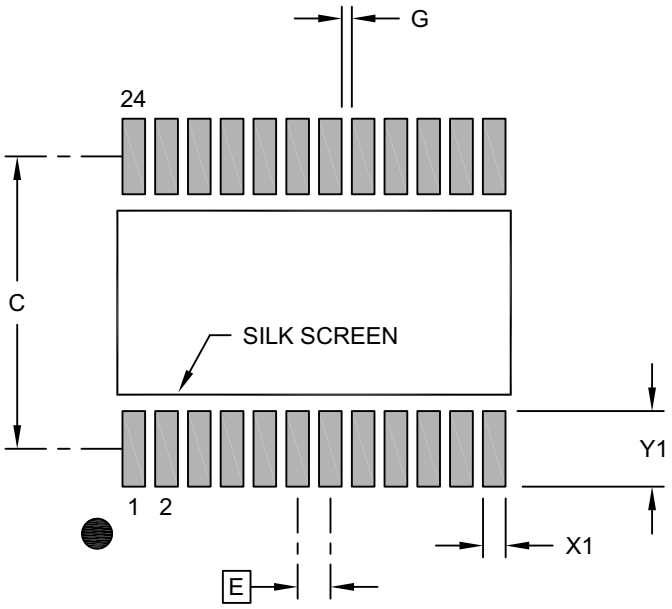
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-284A Sheet 2 of 2

24-Lead Thin Shrink Small Outline Package (QE) - 4.40 mm Body [TSSOP]
Supertex Legacy & Micrel Legacy Package

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		5.80	
Contact Pad Width (X24)	X1			0.45
Contact Pad Length (X24)	Y1			1.50
Contact Pad to Center Pad (X20)	G1	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
2. For best soldering results, thermal vias, if used, should be filled or tented to avoid solder loss during reflow process

Microchip Technology Drawing C04-2284A

APPENDIX A: REVISION HISTORY

Revision A (July 2019)

- Original release of this document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	-X	/XX
Device	Temperature Range	Package

Device:	HV265: 4-Channel, 205V, High-Voltage Amplifiers Array
Temperature Range:	I = -40°C to +85°C
Package:	QE = 24LD TSSOP 4.4mm

Example:

a) HV265-I/QE: 4-Channel 205V High-Voltage Amplifier Array, -40°C to +85°C, 24LD TSSOP package

NOTES:

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