

# DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

## **HEF4069UB** **gates** **Hex inverter**

Product specification  
File under Integrated Circuits, IC04

January 1995

# Hex inverter

# HEF4069UB gates

### DESCRIPTION

The HEF4069UB is a general purpose hex inverter. Each of the six inverters is a single stage.

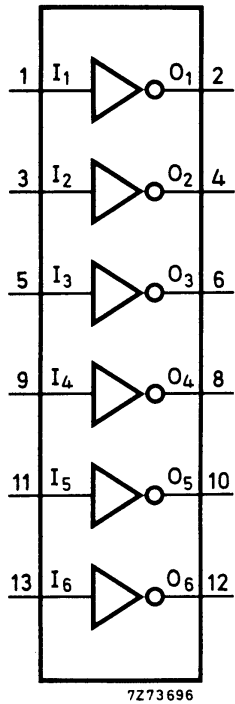


Fig.1 Functional diagram.

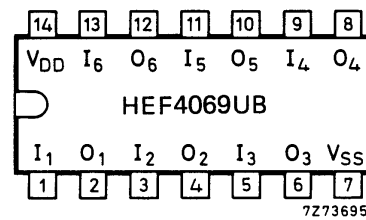


Fig.2 Pinning diagram.

- HEF4069UBP(N): 14-lead DIL; plastic (SOT27-1)
- HEF4069UBD(F): 14-lead DIL; ceramic (cerdip) (SOT73)
- HEF4069UBT(D): 14-lead SO; plastic (SOT108-1)
- ( ): Package Designator North America

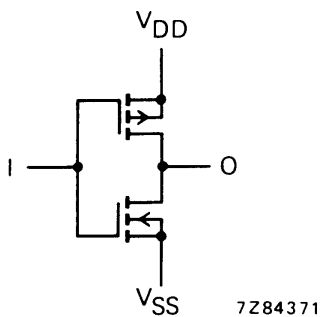


Fig.3 Schematic diagram (one inverter).

### FAMILY DATA, I<sub>DD</sub> LIMITS category GATES

See Family Specifications for V<sub>IH</sub>/V<sub>IL</sub> unbuffered stages

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**AC CHARACTERISTICS**

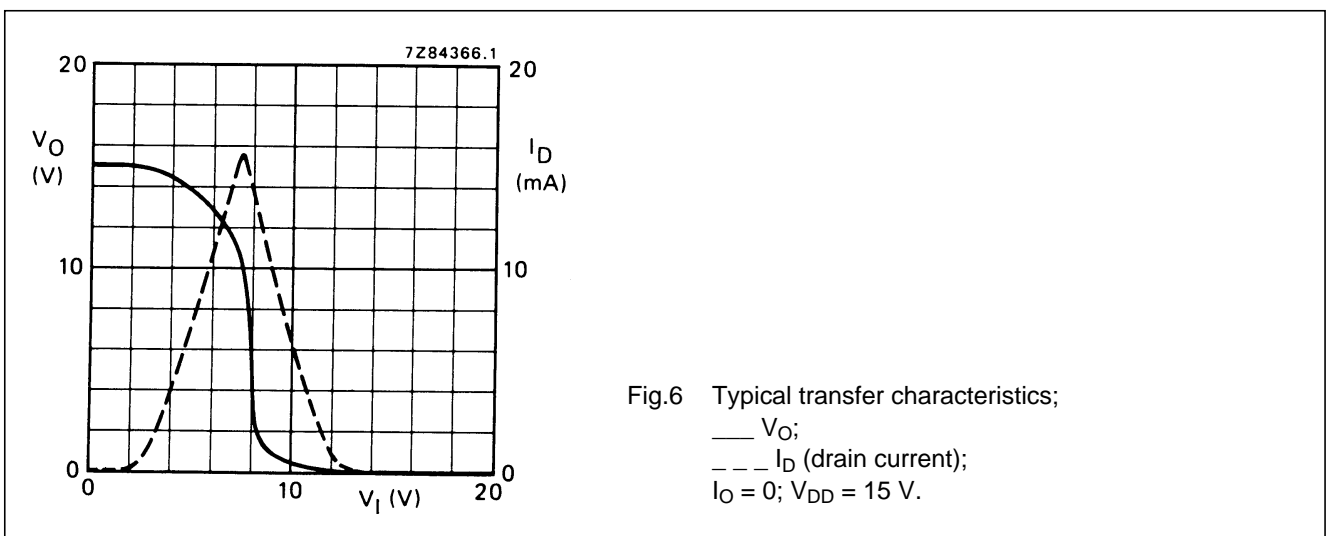
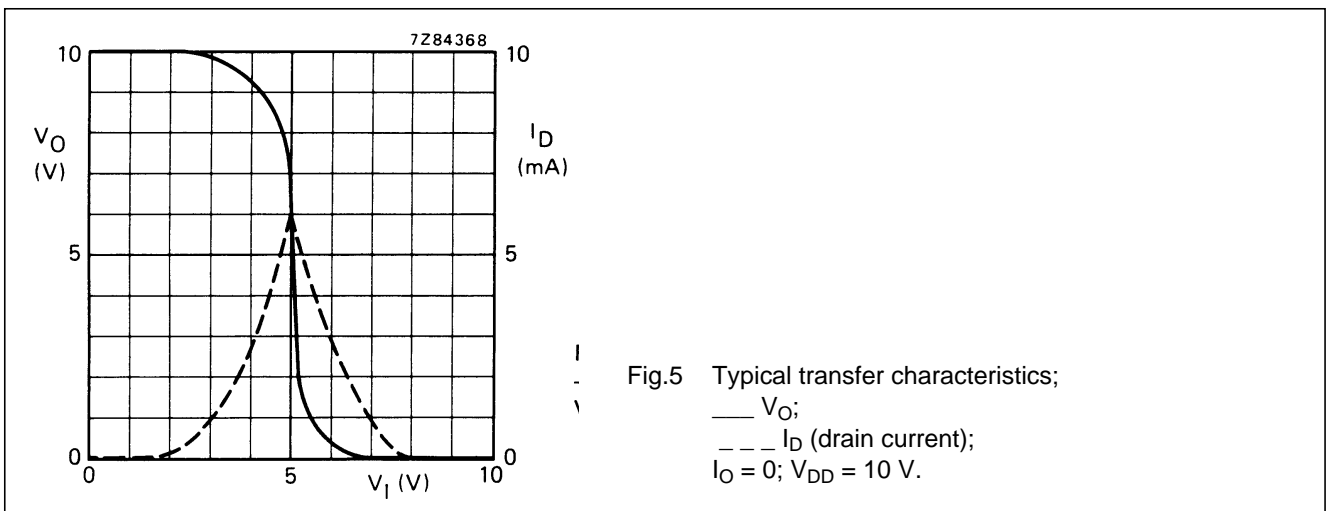
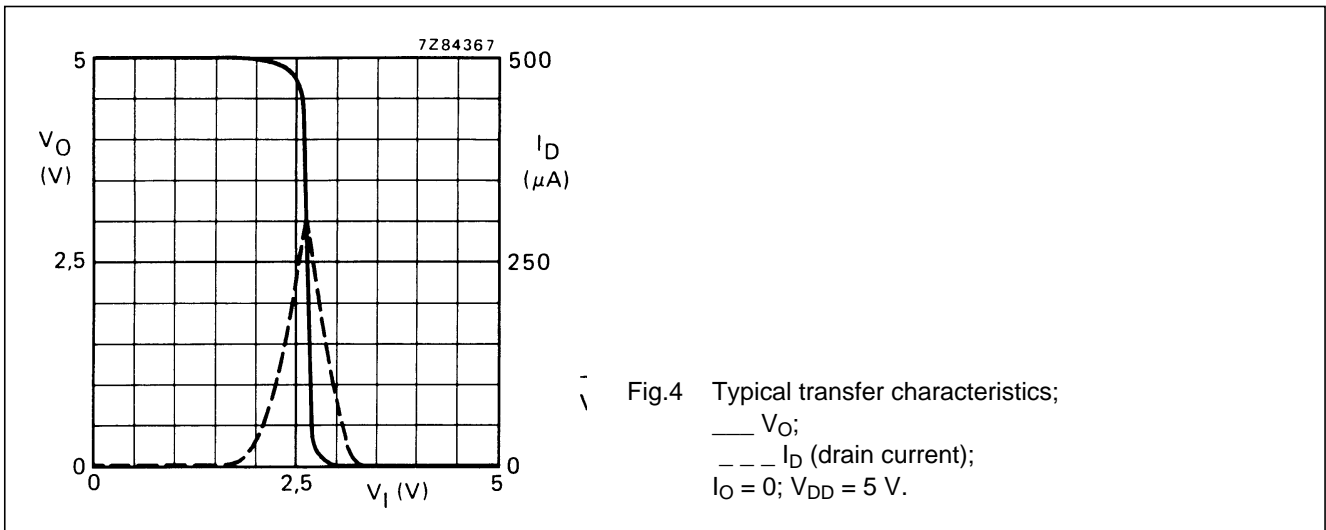
$V_{SS} = 0\text{ V}$ ;  $T_{amb} = 25\text{ }^\circ\text{C}$ ;  $C_L = 50\text{ pF}$ ; input transition times  $\leq 20\text{ ns}$

	$V_{DD}$ V	SYMBOL	TYP.	MAX.	TYPICAL EXTRAPOLATION FORMULA
Propagation delays $I_n \rightarrow O_n$ HIGH to LOW  LOW to HIGH	5	$t_{PHL}$	45	90 ns	18 ns + (0,55 ns/pF) $C_L$
	10		20	40 ns	9 ns + (0,23 ns/pF) $C_L$
	15		15	25 ns	7 ns + (0,16 ns/pF) $C_L$
	5	$t_{PLH}$	40	80 ns	13 ns + (0,55 ns/pF) $C_L$
	10		20	40 ns	9 ns + (0,23 ns/pF) $C_L$
	15		15	30 ns	7 ns + (0,16 ns/pF) $C_L$
Output transition times HIGH to LOW  LOW to HIGH	5	$t_{THL}$	60	120 ns	10 ns + (1,0 ns/pF) $C_L$
	10		30	60 ns	9 ns + (0,42 ns/pF) $C_L$
	15		20	40 ns	6 ns + (0,28 ns/pF) $C_L$
	5	$t_{TLH}$	60	120 ns	10 ns + (1,0 ns/pF) $C_L$
	10		30	60 ns	9 ns + (0,42 ns/pF) $C_L$
	15		20	40 ns	6 ns + (0,28 ns/pF) $C_L$

	$V_{DD}$ V	TYPICAL FORMULA FOR P ( $\mu\text{W}$ )	
Dynamic power dissipation per package (P)	5	$600 f_i + \sum (f_o C_L) \times V_{DD}^2$	where $f_i$ = input freq. (MHz) $f_o$ = output freq. (MHz) $C_L$ = load capacitance (pF) $\sum (f_o C_L)$ = sum of outputs $V_{DD}$ = supply voltage (V)
	10	$4\ 000 f_i + \sum (f_o C_L) \times V_{DD}^2$	
	15	$22\ 000 f_i + \sum (f_o C_L) \times V_{DD}^2$	

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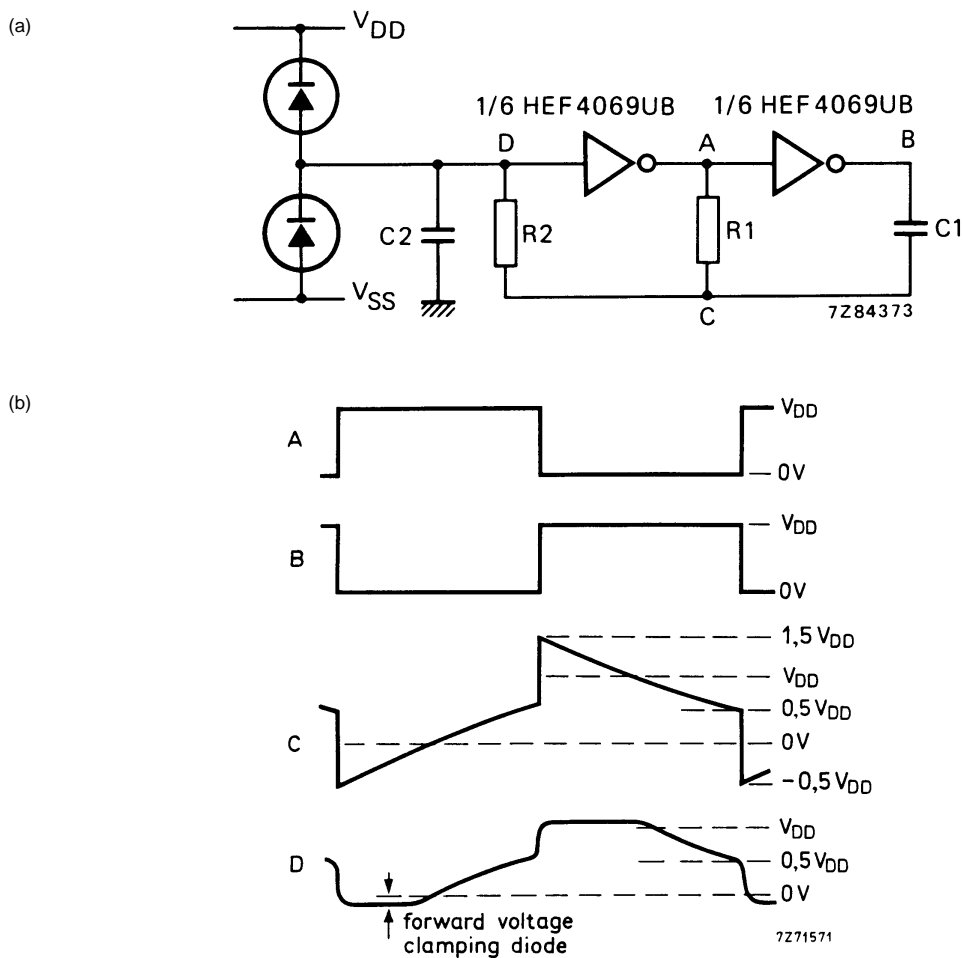
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APPLICATION INFORMATION

Some examples of applications for the HEF4069UB are shown below.

In Fig.7 an astable relaxation oscillator is given. The oscillation frequency is mainly determined by R1C1, provided  $R1 \ll R2$  and  $R2C2 \ll R1C1$ .



The function of R2 is to minimize the influence of the forward voltage across the protection diodes on the frequency; C2 is a stray (parasitic) capacitance. The period  $T_p$  is given by  $T_p = T_1 + T_2$ , in which

$$T_1 = R1C1 \ln \frac{V_{DD} + V_{ST}}{V_{ST}} \text{ and } T_2 = R1C1 \ln \frac{2V_{DD} - V_{ST}}{V_{DD} - V_{ST}} \text{ where}$$

$V_{ST}$  is the signal threshold level of the inverter. The period is fairly independent of  $V_{DD}$ ,  $V_{ST}$  and temperature. The duty factor, however, is influenced by  $V_{ST}$ .

Fig.7 (a) Astable relaxation oscillator using two HEF4069UB inverters; the diodes may be BAW62; C2 is a parasitic capacitance. (b) Waveforms at the points marked A, B, C and D in the circuit diagram.

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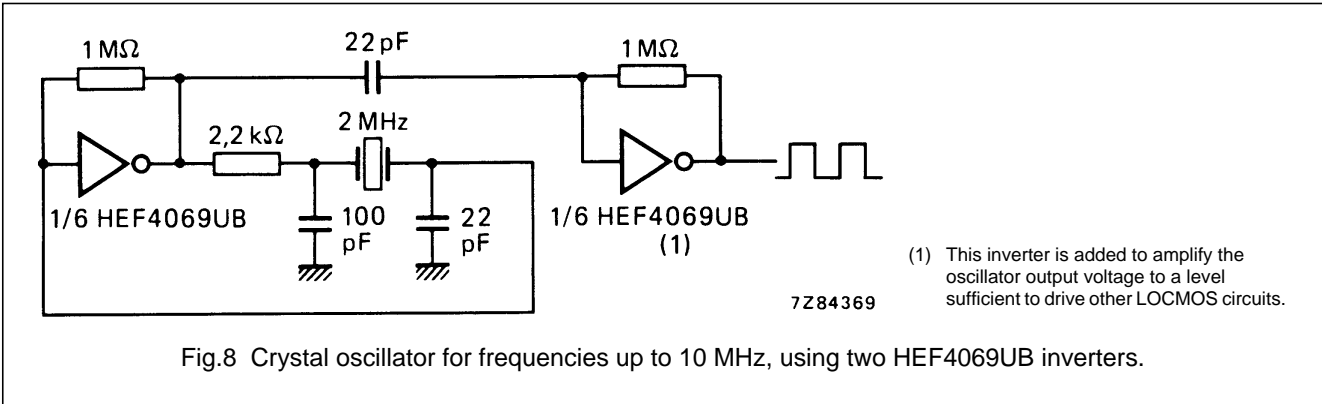


Fig.8 Crystal oscillator for frequencies up to 10 MHz, using two HEF4069UB inverters.

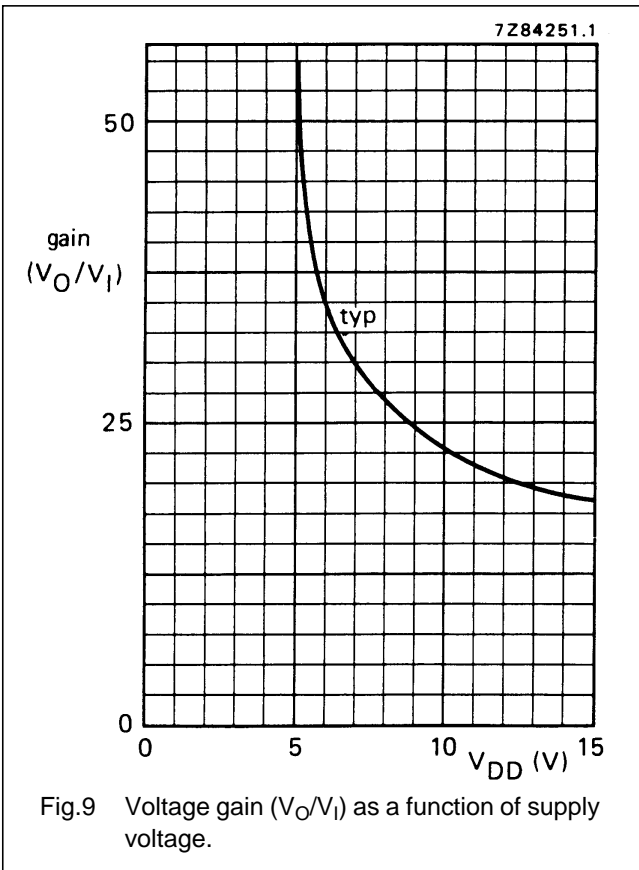


Fig.9 Voltage gain ( $V_O/V_I$ ) as a function of supply voltage.

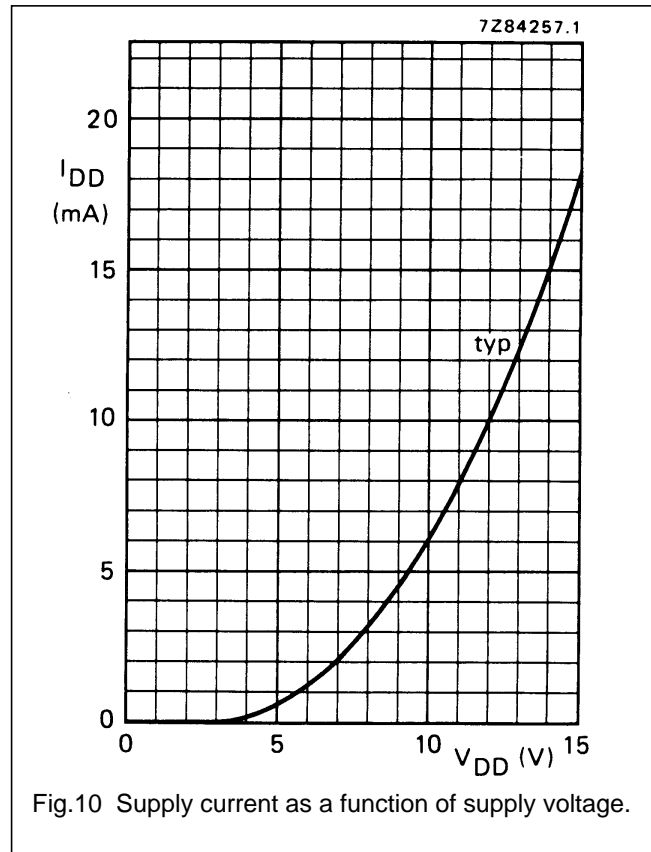


Fig.10 Supply current as a function of supply voltage.

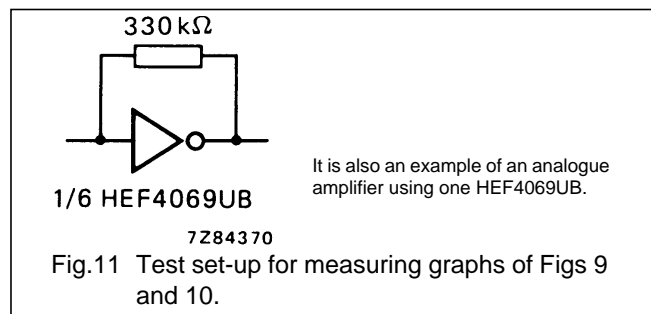


Fig.11 Test set-up for measuring graphs of Figs 9 and 10.

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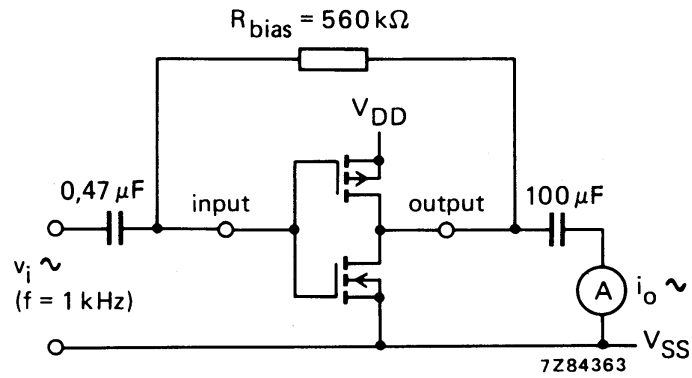


Fig.12 Test set-up for measuring forward transconductance  $g_{fs} = di_o/dv_i$  at  $v_o$  is constant (see also graph Fig.13).

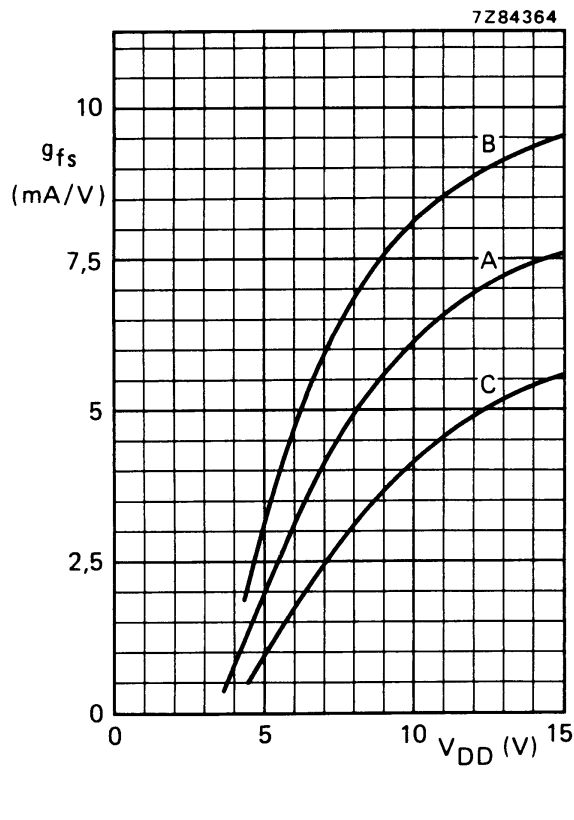


Fig.13 Typical forward transconductance  $g_{fs}$  as a function of the supply voltage at  $T_{amb} = 25\text{ }^\circ\text{C}$ .