

N and P Channel Enhancement Mode Power MOSFET

Description

The G1K2C10S2 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge. It can be used in a wide variety of applications.

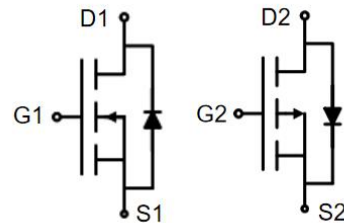
General Features

- NMOS
- V_{DS} 100V
- I_D (at $V_{GS} = 10V$) 3A
- $R_{DS(ON)}$ (at $V_{GS} = 10V$) < 130m Ω
- $R_{DS(ON)}$ (at $V_{GS} = 4.5V$) < 145m Ω
- 100% Avalanche Tested
- RoHS Compliant

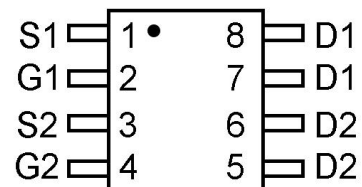
- PMOS
- V_{DS} -100V
- I_D (at $V_{GS} = -10V$) -3.5A
- $R_{DS(ON)}$ (at $V_{GS} = -10V$) < 200m Ω
- $R_{DS(ON)}$ (at $V_{GS} = -4.5V$) < 215m Ω
- 100% Avalanche Tested
- RoHS Compliant

Application

- Power switch
- DC/DC converters



Schematic diagram



pin assignment



SOP-8 Dual

Ordering Information

Device	Package	Marking	Packaging
G1K2C10S2	SOP-8 Dual	G1K2C10D	4000pcs/Reel

Absolute Maximum Ratings $T_C = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	V_{DS}	100	-100	V
Continuous Drain Current	I_D	3	-3.5	A
Pulsed Drain Current (note1)	I_{DM}	12	-14	A
Gate-Source Voltage	V_{GS}	± 20	± 20	V
Power Dissipation	P_D	2	3.1	W
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 To 150	-55 To 150	$^\circ\text{C}$

Thermal Resistance

Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	R_{thJA}	62.5	40	$^\circ\text{C/W}$

NMOS Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 100V, V_{GS} = 0V$	--	--	1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	--	--	± 100	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1	1.5	2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 5A$	--	110	130	m Ω
		$V_{GS} = 4.5V, I_D = 5A$	--	120	145	
Forward Transconductance	g_{FS}	$V_{GS} = 5V, I_D = 5A$	--	4	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = 50V,$ $f = 1.0\text{MHz}$	--	668	--	pF
Output Capacitance	C_{oss}		--	25	--	
Reverse Transfer Capacitance	C_{rss}		--	16	--	
Total Gate Charge	Q_g	$V_{DD} = 50V,$ $I_D = 5A,$ $V_{GS} = 10V$	--	22	--	nC
Gate-Source Charge	Q_{gs}		--	3	--	
Gate-Drain Charge	Q_{gd}		--	6	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 50V,$ $I_D = 5A,$ $R_G = 2.5\Omega$	--	11	--	ns
Turn-on Rise Time	t_r		--	7	--	
Turn-off Delay Time	$t_{d(off)}$		--	35	--	
Turn-off Fall Time	t_f		--	9	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	3	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = 5A, V_{GS} = 0V$	--	--	1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = 5A, V_{GS} = 0V$ $di/dt = 100A/\mu s$	--	27	--	nC
Reverse Recovery Time	T_{rr}		--	26	--	ns

Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



NMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

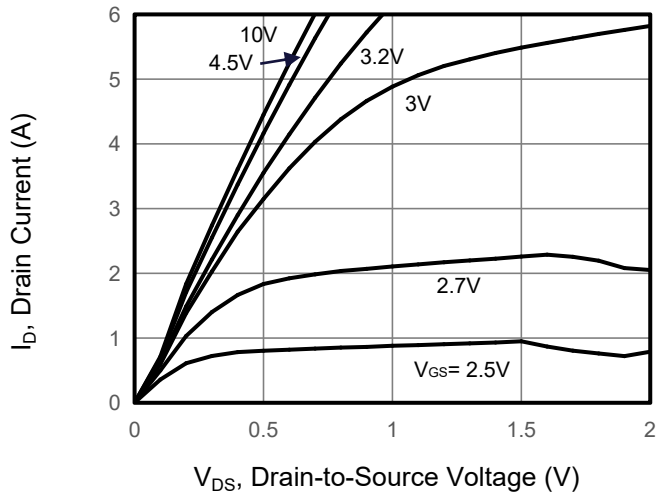


Figure 2. Transfer Characteristics

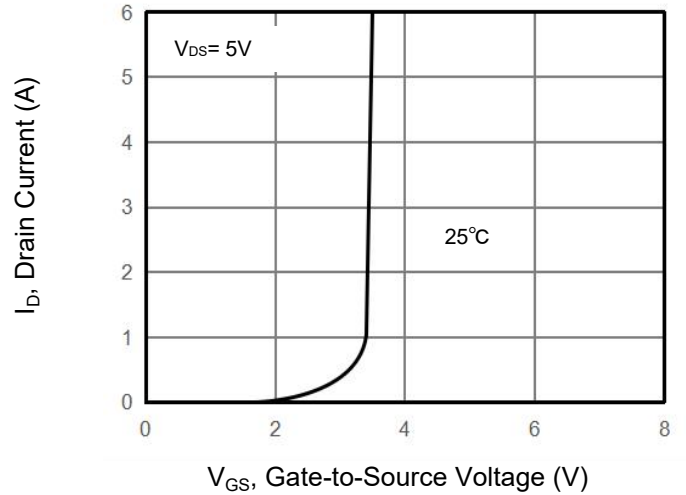


Figure 3. Drain Source On Resistance

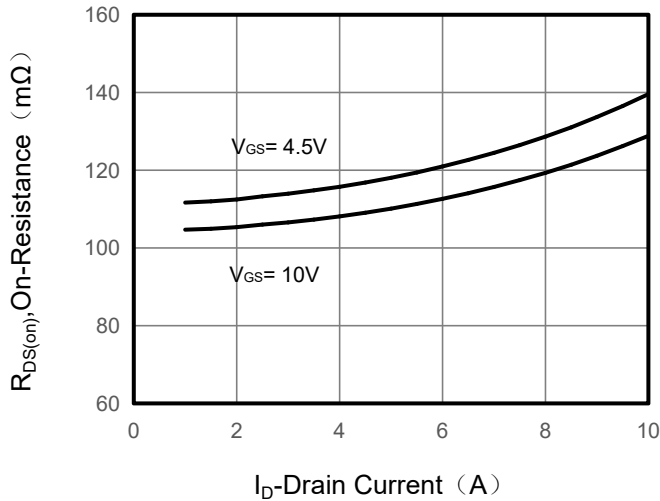


Figure 4. Gate Charge

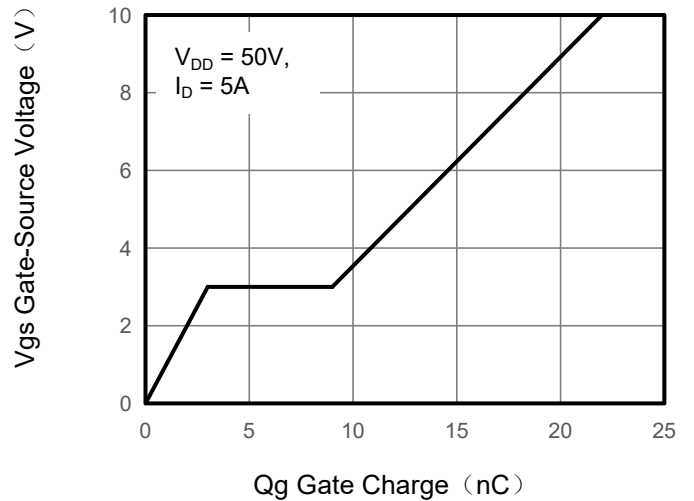


Figure 5. Capacitance

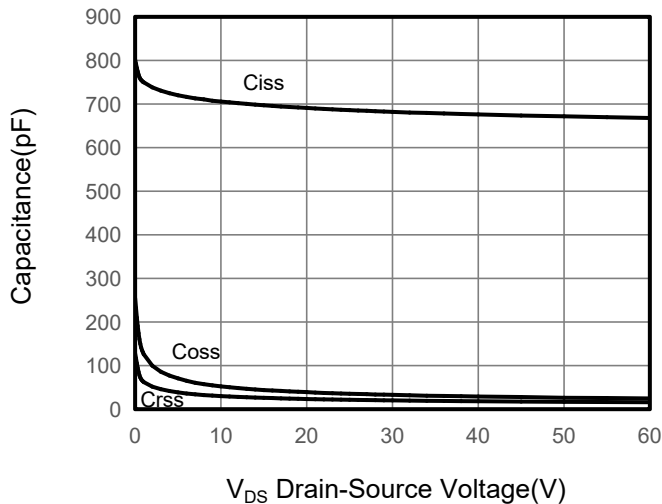
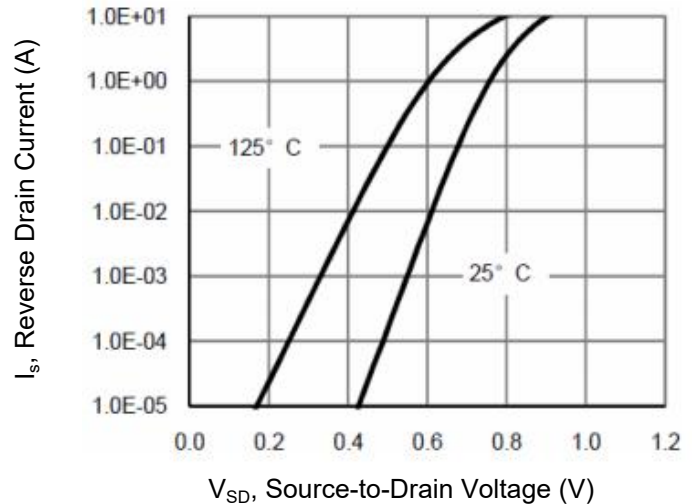


Figure 6. Source-Drain Diode Forward



NMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

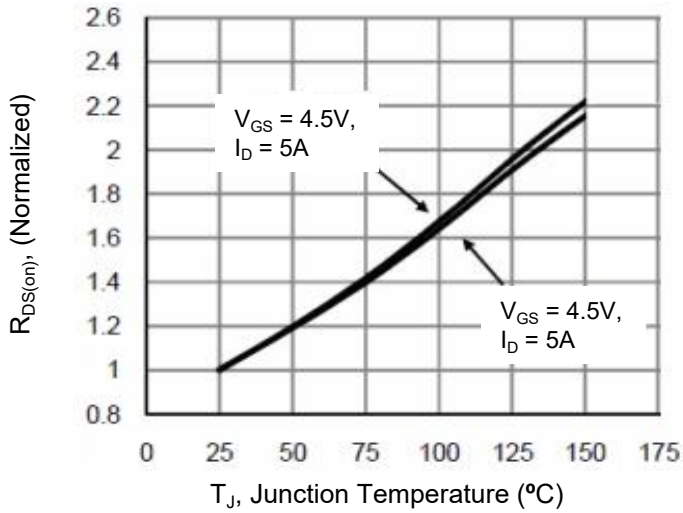


Figure 8. Safe Operation Area

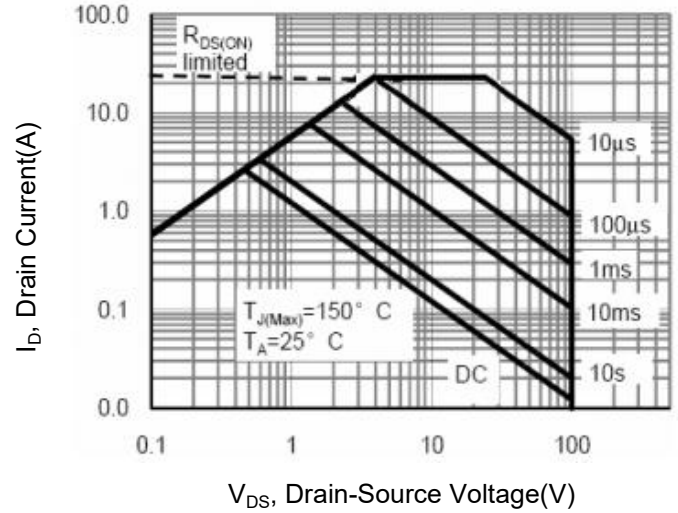
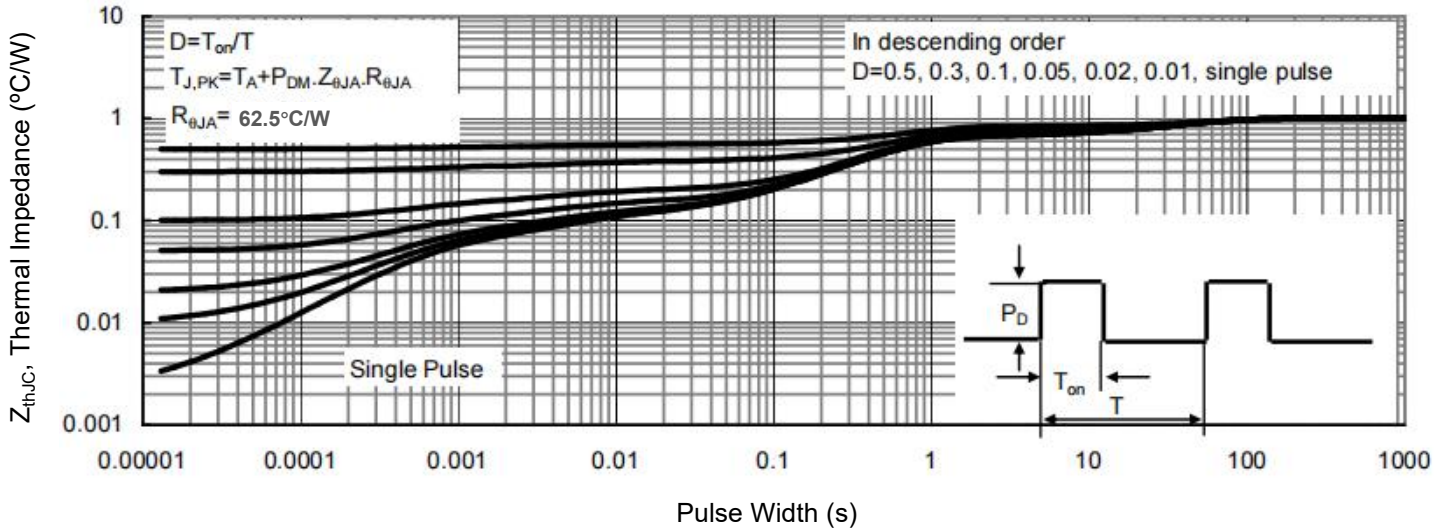


Figure 9. Normalized Maximum Transient Thermal Impedance

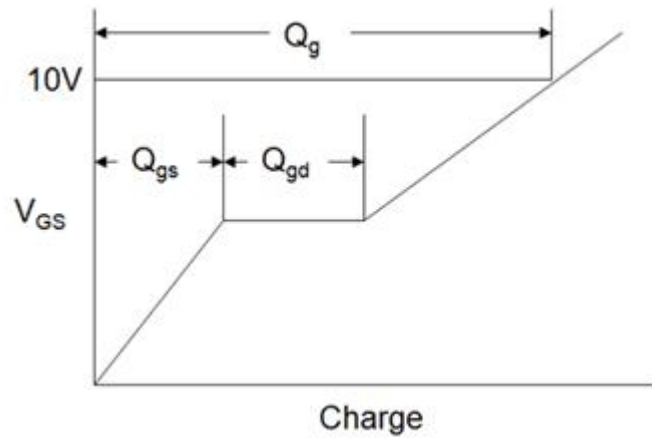
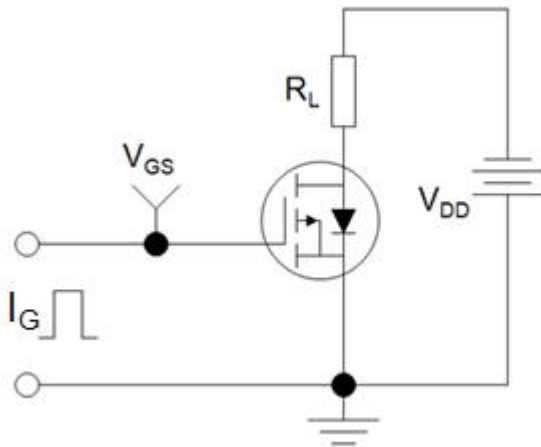


PMOS Specifications $T_J = 25^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
Static Parameters						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu A$	-100	--	--	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -100V, V_{GS} = 0V$	--	--	-1	μA
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20V$	--	--	± 10	μA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu A$	-1	-1.8	-2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -3A$	--	165	200	m Ω
		$V_{GS} = -4.5V, I_D = -2A$	--	175	215	
Forward Transconductance	g_{FS}	$V_{DS} = -5V, I_D = -3A$	--	8	--	S
Dynamic Parameters						
Input Capacitance	C_{iss}	$V_{GS} = 0V,$ $V_{DS} = -50V,$ $f = 1.0MHz$	--	1732	--	pF
Output Capacitance	C_{oss}		--	47	--	
Reverse Transfer Capacitance	C_{rss}		--	45	--	
Total Gate Charge	Q_g	$V_{DD} = -50V,$ $I_D = -3A,$ $V_{GS} = -10V$	--	23	--	nC
Gate-Source Charge	Q_{gs}		--	4.2	--	
Gate-Drain Charge	Q_{gd}		--	5.2	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -50V,$ $I_D = -3A,$ $R_G = 3\Omega$	--	24	--	ns
Turn-on Rise Time	t_r		--	5	--	
Turn-off Delay Time	$t_{d(off)}$		--	19	--	
Turn-off Fall Time	t_f		--	11	--	
Drain-Source Body Diode Characteristics						
Continuous Body Diode Current	I_S	$T_C = 25^\circ\text{C}$	--	--	-3.5	A
Body Diode Voltage	V_{SD}	$T_J = 25^\circ\text{C}, I_{SD} = -3A, V_{GS} = 0V$	--	--	-1.2	V
Reverse Recovery Charge	Q_{rr}	$I_F = -3A, V_{GS} = 0V$ $di/dt = -100A/\mu s$	--	22	--	nC
Reverse Recovery Time	T_{rr}		--	29	--	ns

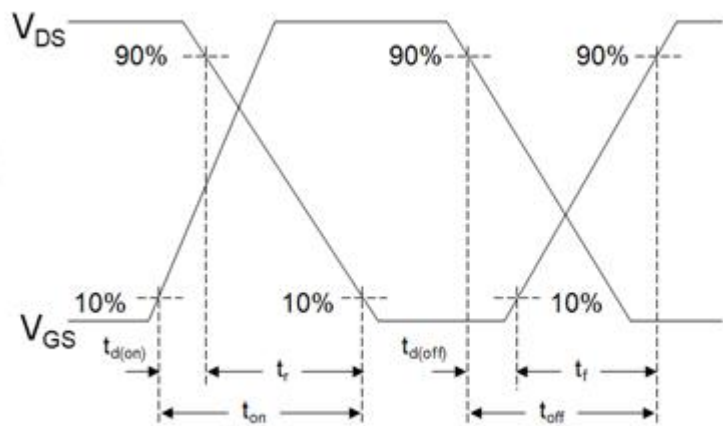
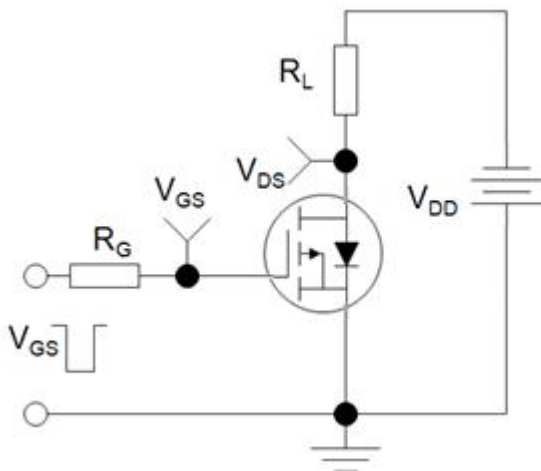
Notes

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical R_G

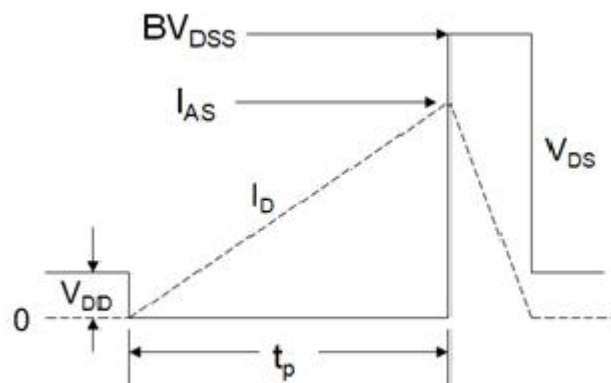
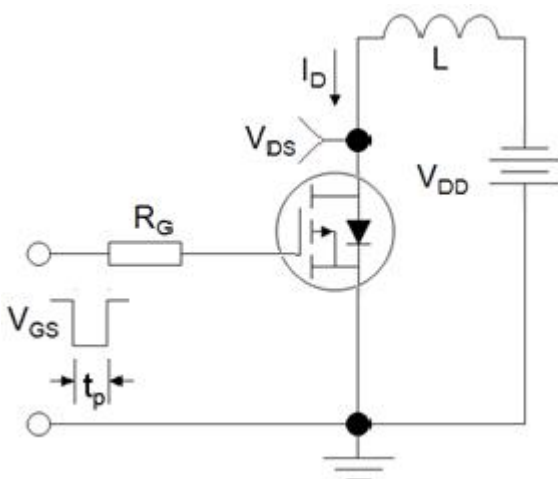
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



PMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 1. Output Characteristics

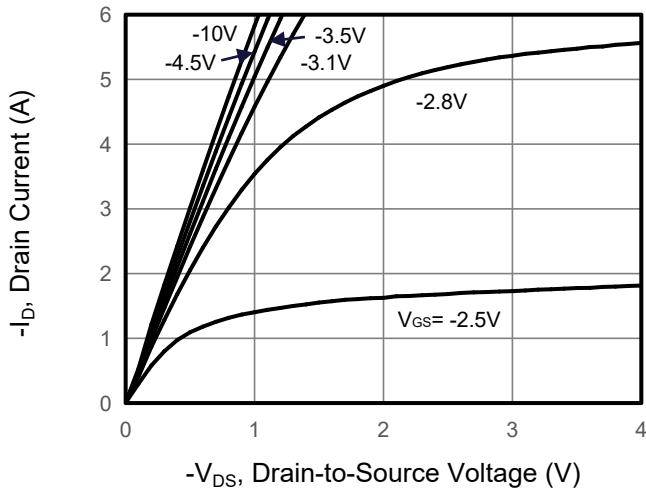


Figure 2. Transfer Characteristics

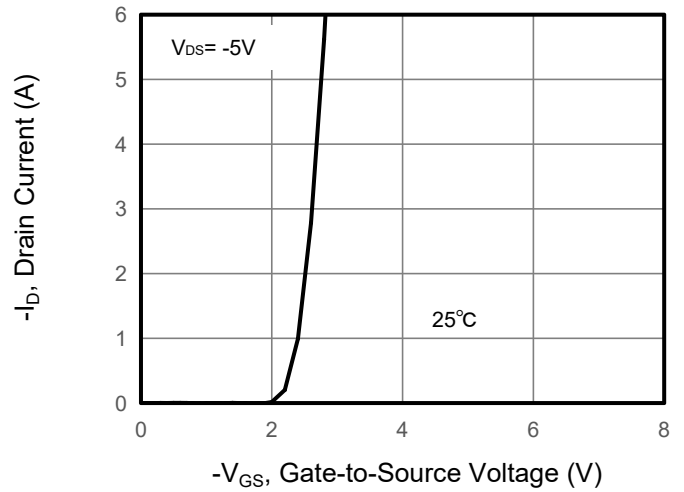


Figure 3. Drain Source On Resistance

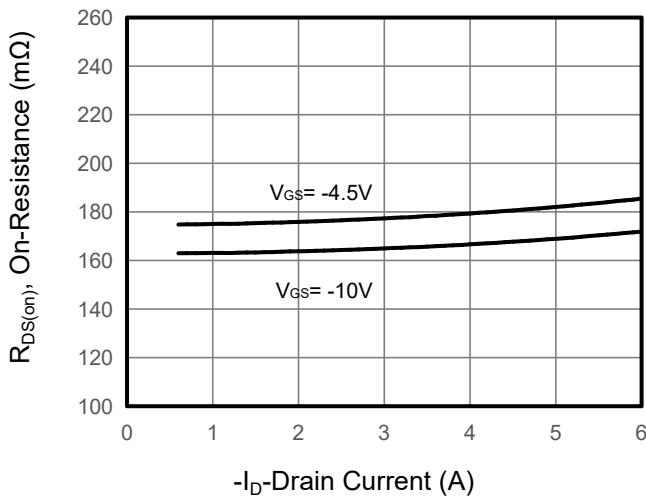


Figure 4. Gate Charge

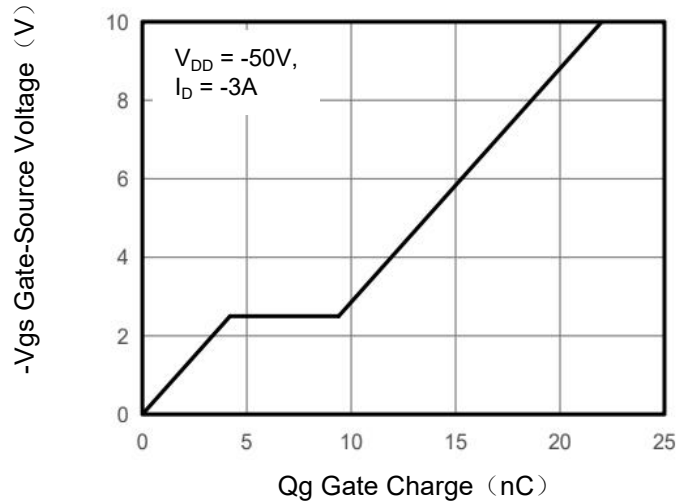


Figure 5. Capacitance

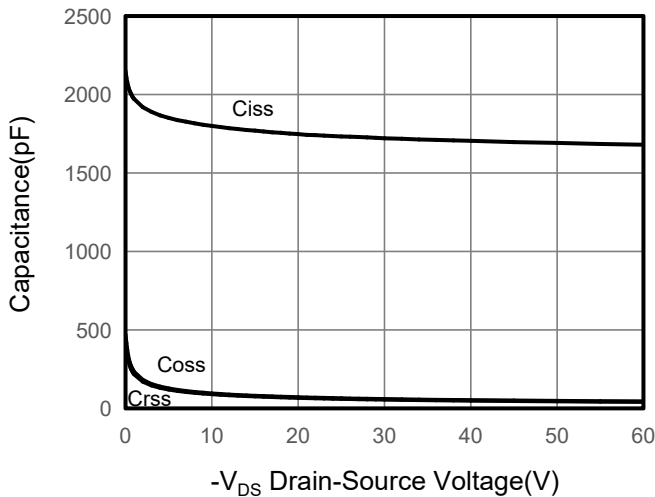
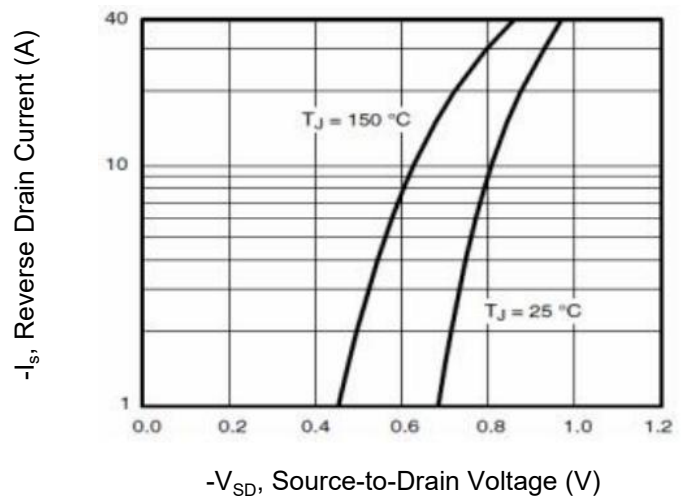


Figure 6. Source-Drain Diode Forward



PMOS Typical Characteristics $T_J = 25^\circ\text{C}$, unless otherwise noted

Figure 7. Drain-Source On-Resistance

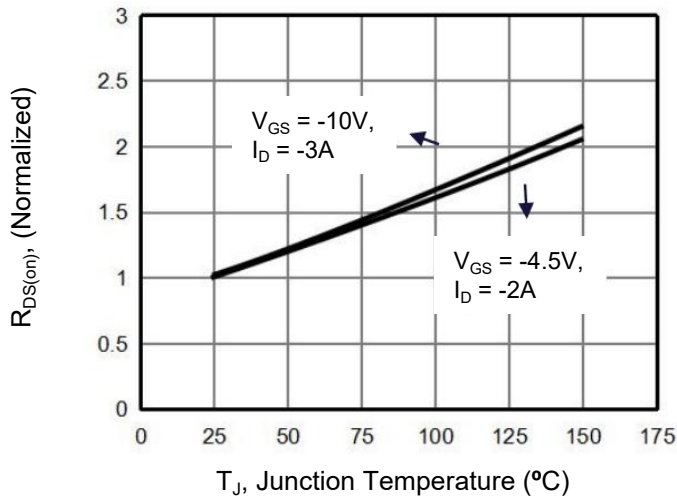


Figure 10. Safe Operation Area

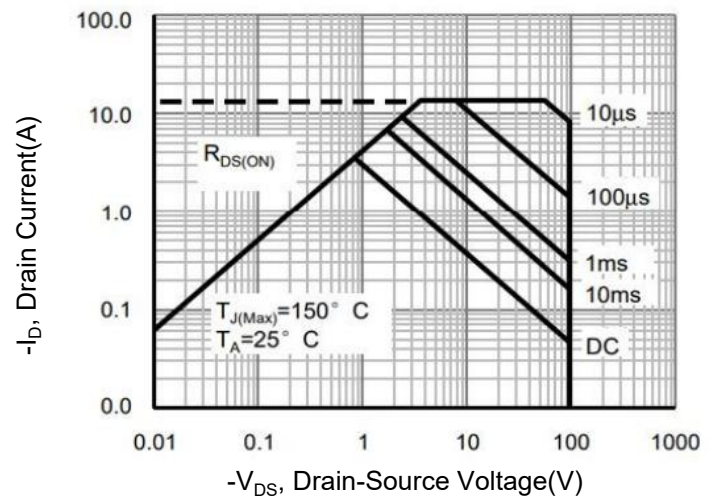
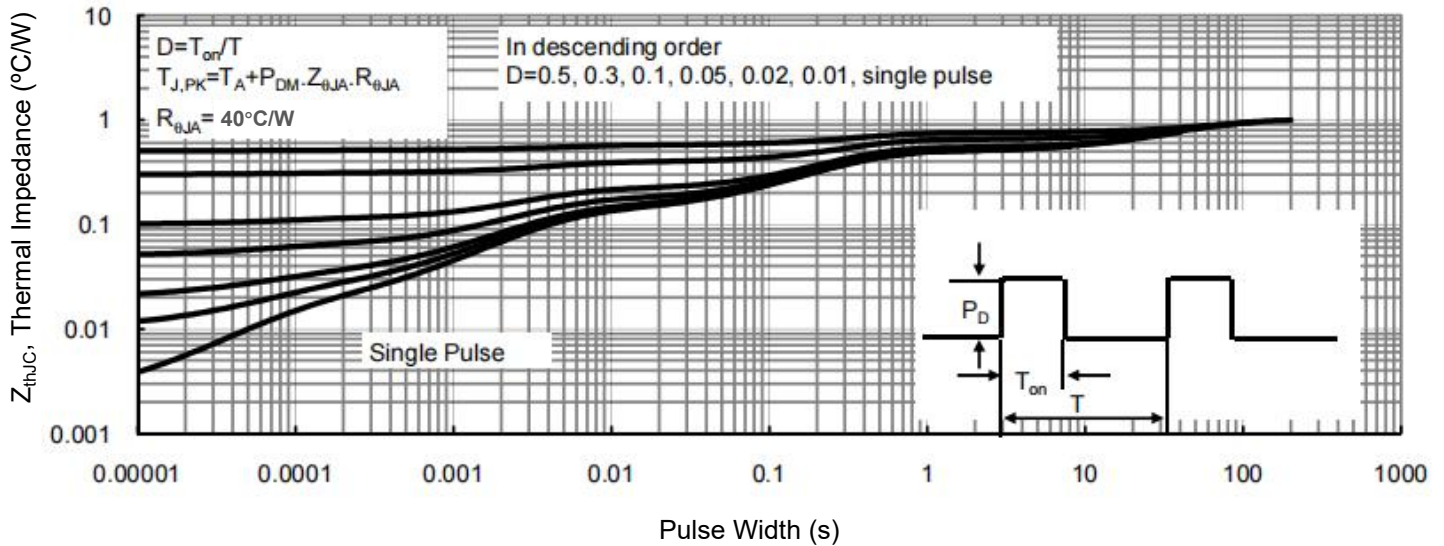
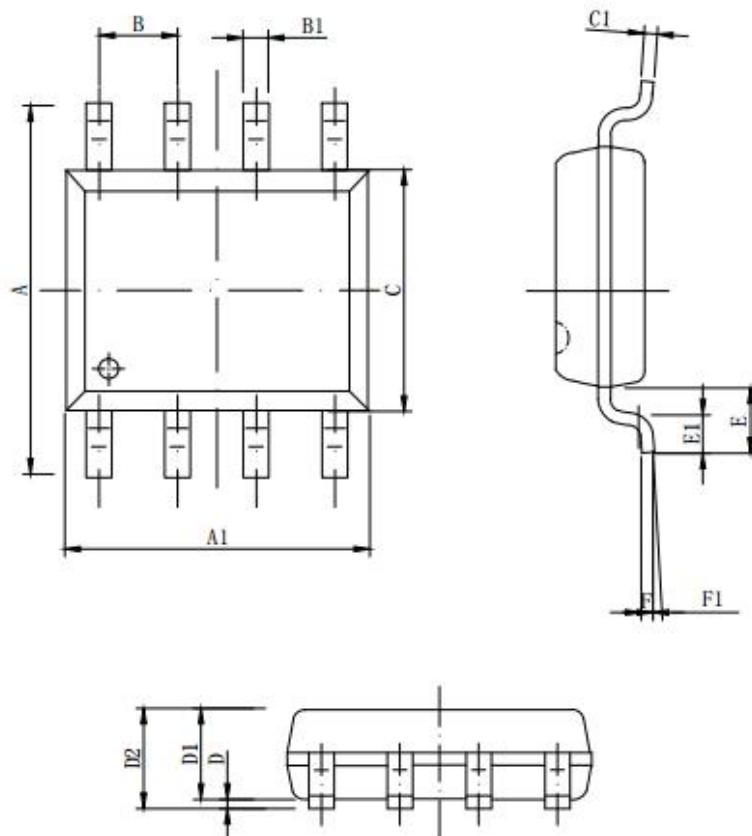


Figure 9. Normalized Maximum Transient Thermal Impedance



SOP-8 Dual Package Information



Symbol	Dimensions in Millimeters		
	MIN.	NOM.	MAX.
A	5.800	6.000	6.200
A1	4.800	4.900	5.000
B	1.270BSC		
B1	0.35 ^{8x}	0.40 ^{8x}	0.45 ^{8x}
C	3.780	3.880	3.980
C1	--	0.203	0.253
D	0.050	0.150	0.250
D1	1.350	1.450	1.550
D2	1.500	1.600	1.700
D2	1.500	1.600	1.700
E	1.060REF		
E1	0.400	0.700	0.100
F	0.250BSC		
F1	2°	4°	6°