SPECIFICATIONS

CUSTOMER : _____

MODEL NO. : GFOC1602AA-YG

VERSION : A

DATE : 2023.02.23

CERTIFICATION : ROHS

Customer Sign	Approved By	Prepared By	Prepared By
	GIFAR 2023.02.23 Sidney	GIFAR 2023.02.23 Roger	GIFAR 2023.02.23 Hazel

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Revision Record

Data(y/m/d)	Ver.	Description	page
2023.02.23	A	Specification released	

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Contents

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1. Basic Specifications

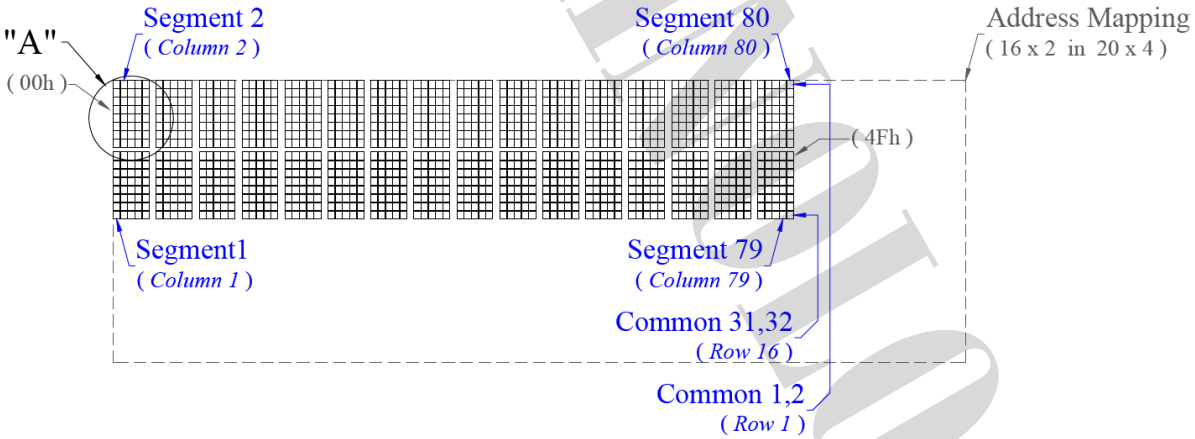
1.1 Display Specifications

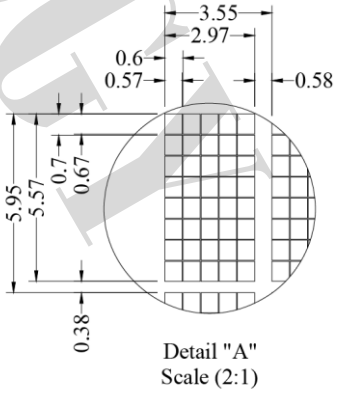
1) Display Mode: Passive Matrix
2) Display Color: Monochrome (Yellow)
3) Drive Duty: 1/16 Duty

1.2 Mechanical Specifications

1) Outline Drawing	: According to the annexed outline drawing
2) Number of Characters	: 16 Characters (5 × 8) × 2 Lines
3) Module Size	: 98.64 × 16.70 × 2.00 (mm)
4) Panel Size	: 66.10 × 16.70 × 2.00 (mm) including “Anti-Glare” Polarizer
5) Active Area	: 56.22 × 11.52 (mm)
6) Character Pitch	: 3.55 × 5.95 (mm)
7) Character Size	: 2.97 × 5.57 (mm)
8) Pixel Pitch	: 0.60 × 0.70 (mm)
9) Pixel Size	: 0.57 × 0.67 (mm)
10) Weight	: 4.59 (g) ± 10%

1.3 Active Area / Address Mapping & Character Construction





Address Mapping

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Line 1	00h	01h	02h	03h	04h	05h	06h	07h	08h	09h	0Ah	0Bh	0Ch	0Dh	0Eh	0Fh
Line 2	40h	41h	42h	43h	44h	45h	46h	47h	48h	49h	4Ah	4Bh	4Ch	4Dh	4Eh	4Fh

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1.4 Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
10	VCC	O	**Logic Power Output** This is a voltage supply pin which is supplied externally or regulated internally. A capacitor should be connected between this pin and GND under all circumstances. When VDD1 = 2.2~3.5V, VCC output voltage VDD1. When VDD1 = 3.5~5.5V, VCC output voltage 2.8V.
11	VDD1	P	**Power Supply for Logic Circuit** This is a voltage supply pin. It should match with the MCU interface voltage level and must be connected to external source
17, 21, 35	GND	P	**Ground of OEL System** This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.
8	VPP	P	**Power Supply for OEL Panel** This is the most positive voltage supply pin of the chip. A capacitor should be connected between this pin and GND.
DC/DC Converter			
5	VDD2	P	**Power Supply for DC/DC Converter Circuit** This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be connected to external source when the converter is used. It should be kept floating when the DC/DC converter is not used.
1 / 2 3 / 4	C1N / C1P C2P / C2N	I	**Positive Terminal of the Flying Inverting Capacitor** **Negative Terminal of the Flying Boost Capacitor** The charge-pump capacitors are required between the terminals. They must be floated when the converter is not used.
Driver			
6	IREF	I	**Current Reference for Brightness Adjustment** This pin is segment current reference pin. A resistor should be connected between this pin and GND. Set the current at 18.75μA.
7	VCOMH	P	**Voltage Output High Level for COM Signal** This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and GND.
9	VSL	P	**Voltage Output Low Level for SEG/COM Signal** This is Segment/Common voltage reference pin. This pin should be connected to GND externally.
External IC Communication			
12	GPIO	I/O	**General Purpose Input/Output** This pad is used to indicate the Display ON/OFF status. When Display On, this pin output voltage VDD1. When Display Off, this pin output voltage GND.
Configuration			
16	V1_OPT	I	**I/O Voltage Regulator Configuration** This is the VDD1 supply voltage select pin. V1_OPT = "H": Power should supply "3.5~5.5V" to VDD1. V1_OPT = "L": Power should supply "2.2~3.5V" to VDD1.
18 19	FT0 FT1	I	**Built-in Character ROM Selection** These pins are used to manage the character number of character generator. See the following table & Section 4.6:

FT1	FT0	Font Table
0	0	ENGLISH_JAPANESE CHARACTER FONT TABLE
0	1	WESTERN EUROPEAN CHARACTER FONT TABLE-I
1	0	ENGLISH_RUSSIAN CHARACTER FONT TABLE
1	1	WESTERN EUROPEAN CHARACTER FONT TABLE-II

20	VPPS	I	**DC/DC Converter Circuit Control** This Pin is used to control internal DC/DC Converter Circuit ON or OFF. VPPS = "H", Internal DC/DC Converter Circuit ON. VPPS = "L", Internal DC/DC Converter Circuit OFF.

1.4 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
Interface			
13 14 15	IM0 IM1 IM2	I	**Communicating Protocol Selection** These pins are MCU interface selection input. See the following table: IM2 / IM1 / IM0 8-bit 68XX Parallel: 0 0 0 8-bit 80XX Parallel: 0 0 1 4-wire SPI: 0 1 0 I^2C: 0 1 1 4-bit 68XX Parallel: 1 0 0 4-bit 80XX Parallel: 1 0 1 3-wire SPI: 1 1 0 I^2C: 1 1 1
22	CSB	I	**Chip Select** This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.
23	RESB	I	**Power Reset for Controller and Driver** This pin is reset signal input. When the pin is low, initialization of the chip is executed. Keep this pin pull high during normal operation.
24	RS	I	**Data/Command Control** This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 will be interpreted as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. In I^2C mode, this pin acts as SA0 for slave address selection. When serial interface mode is selected, this pin must be connected to GND. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
25	WRB	I	**Read/Write Select or Write** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low. When serial or I^2C mode is selected, this pin must be connected to GND.
26	RDB	I	**Enable or Read** This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low. When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low. When serial or I^2C mode is selected, this pin must be connected to GND.
27~34	D0~D7	I/O	**Host Data Input/Output Bus** When 8-bit bus mode, D0-D7 are used as bi-directional data bus that connects to an 8-bit MPU data bus. When 4-bit bus mode, D4-D7 are used as bi-directional data bus that connects to a 4-bit MPU data bus. And in this case D0-D3 pins are not used and set to HZ. When the serial interface is select, then D1 serves as the serial data input terminal (SI/SDA) and D0 serves as the serial clock input terminal (SCL). At this time, D7 to D2 are set to HZ. When the chip select is inactive, D0 to D7 are set to HZ.

2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage for Logic	V_{DD1}	-0.3	5.6	V	1, 2
Supply Voltage for I/O Pins	V_{DD2}	-0.3	5.6	V	1, 2
Supply Voltage for Display	Vpp	0	14.5	V	1, 2
Operating Temperature	T_{OP}	-40	85	°C	3
Storage Temperature	T_{STG}	-40	90	°C	3
Life Time (120 cd/m^2)		80,000	-	hour	4
Life Time (100 cd/m^2)		100,000	-	hour	4

Note 1: All the above voltages are on the basis of “GND = 0V”.

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. “Optics & Electrical Characteristics”. If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

Note 3: The defined temperature ranges do not include the polarizer. The maximum withstood temperature of the polarizer should be 80°C.

Note 4: V_{DD1}= V_{DD2}= 5.0V, V_{PP} generated by internal DC/DC convertor. T_a = 25°C, 50% Checkerboard. Software configuration follows Section 4.5 Initialization.
End of lifetime is specified as 50% of initial brightness reached. The average operating lifetime at room temperature is estimated by the accelerated operation at high temperature conditions.

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3. Optics & Electrical Characteristics

3.1 Optics Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	Note 8	100	120	-	cd/m2
C.I.E. (Yellow)	(x) (y)	C.I.E. 1931	0.46 0.45	0.50 0.49	0.54 0.53	
Dark Room Contrast	CR		>10,000:1			
Viewing Angle			-	Free	-	degree

* Software configuration follows Section 4.5 Initialization.

3.2 DC Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage for Logic	V_{DD1}	V1_OTP set “H”	3.5	-	5.5	V
		V1_OTP set “L”	2.2	-	3.5	V
Supply Voltage for Analog	V_{DD2}		2.7	-	5.5	V
Supply Voltage for Display	V_{PP}	Note 5	11.2	12.0	12.5	V
High Level Input	V_{IH}		0.7×VDD1	-	VDD1	V
Low Level Input	V_{IL}		0	-	0.3×VDD1	V
High Level Output	V_{OH}	IOH=-0.5mA	0.7×VDD1	-	VDD1	V
Low Level Output	V_{OL}	IOL=0.5mA	0	-	0.3×VDD1	V
Operating Current for VDD1	I_{DD1}		-	-	200	μA
Operating Current for VDD2	I_{DD2}	Note 6	-	18.4	23.0	mA
		Note 7	-	27.7	34.6	mA
		Note 8	-	47.3	59.1	mA
Sleep Mode Current for VDD1	$I_{DD1, SLEEP}$		-	-	10	μA
Sleep Mode Current for VDD2	$I_{DD2, SLEEP}$		-	-	10	μA

Note 5: Brightness (L_{br}) and Supply Voltage for Display (V_{pp}) are subject to the change of the panel characteristics and the customer’s request.

Note 6: V_{DD1}= V_{DD2}= 5.0V, V_{PP} generated by internal DC/DC convertor, 30% Display Area Turn on.

Note 7: V_{DD1}= V_{DD2}= 5.0V, V_{PP} generated by internal DC/DC convertor, 50% Display Area Turn on.

Note 8: V_{DD1}= V_{DD2}= 5.0V, V_{PP} generated by internal DC/DC convertor, 100% Display Area Turn on.

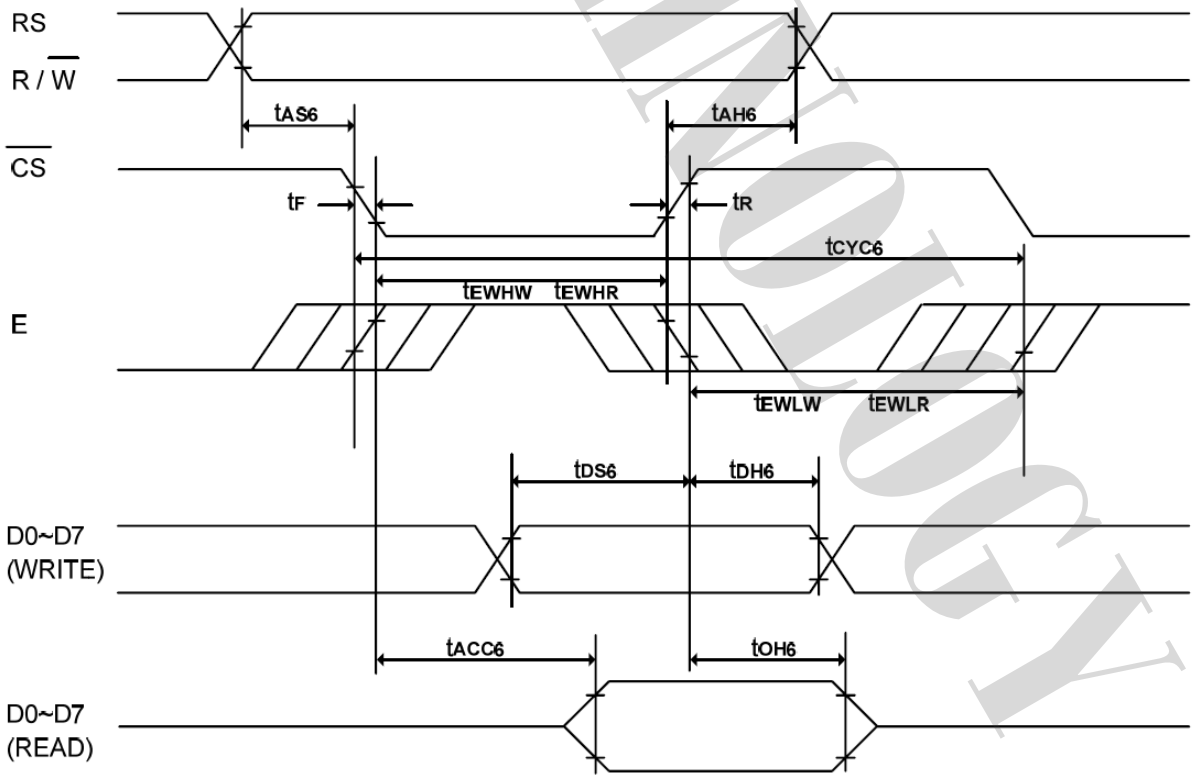
* Software configuration follows Section 4.5 Initialization.

3.3 AC Characteristics

3.3.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{CYC6}	System cycle time	500	-	ns
t_{AS6}	Address setup time	0	-	ns
t_{AH6}	Address hold time	0	-	ns
t_{DS6}	Data setup time	66	-	ns
t_{DH6}	Data hold time	25	-	ns
t_{OH6}	Output disable time (C_L = 100pF)	16	140	ns
t_{ACC6}	Access time (C_L = 100pF)	-	280	ns
t_{EWHW}	Enable H pulse width (Write)	166	-	ns
t_{EWHR}	Enable H pulse width (Read)	200	-	ns
t_{EWLW}	Enable L pulse width (Write)	166	-	ns
t_{EWLR}	Enable L pulse width (Read)	166	-	ns
t_R	Rise time	-	25	ns
t_F	Fall time	-	25	ns

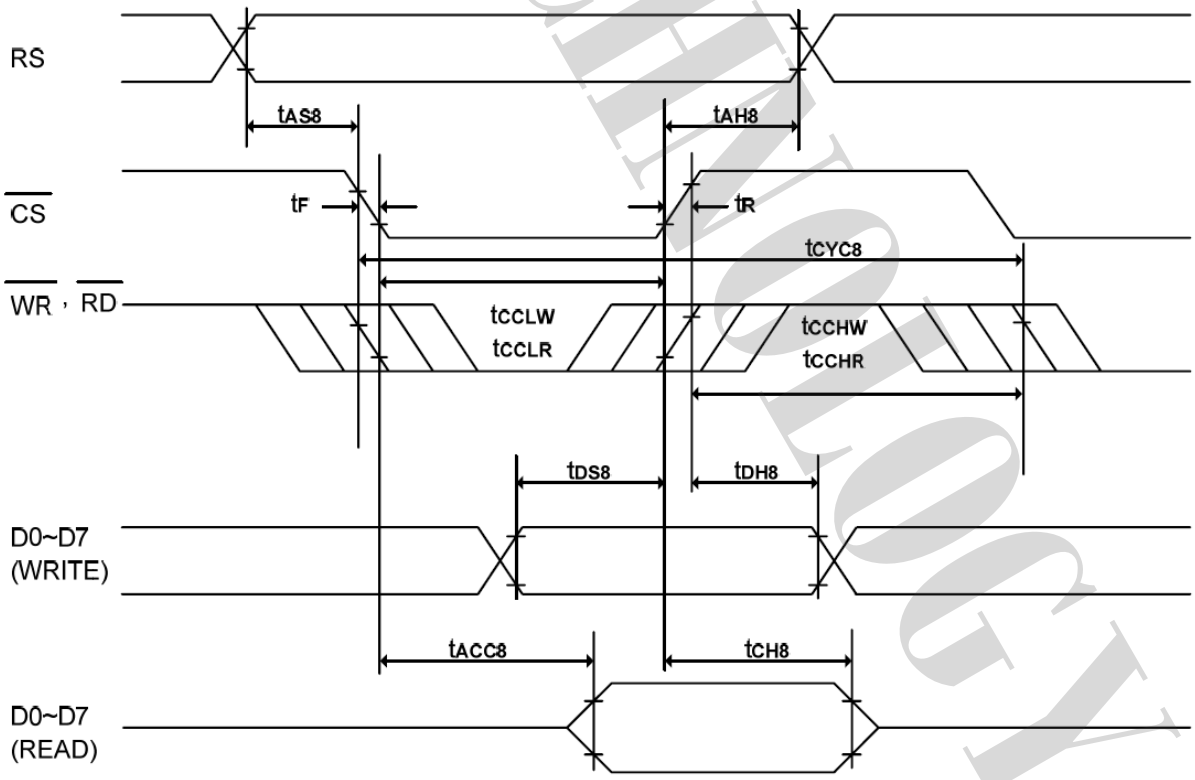
* (V_{DD1} = 2.2 – 5.5V, TA = +25°C)



3.3.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{CYC8}	System cycle time	500	-	ns
t_{AS8}	Address setup time	0	-	ns
t_{AH8}	Address hold time	0	-	ns
t_{DS8}	Data setup time	66	-	ns
t_{DH8}	Data hold time	25	-	ns
t_{CH8}	Output disable time(C_L = 100pF)	16	110	ns
t_{ACC8}	$\overline{RD}$ access time (C_L = 100pF)	-	230	ns
t_{CCLW}	Control L pulse width (WR)	166	-	ns
t_{CCLR}	Control L pulse width (RD)	200	-	ns
t_{CCHW}	Control H pulse width (WR)	166	-	ns
t_{CCHR}	Control H pulse width (RD)	166	-	ns
t_R	Rise time	-	25	ns
t_F	Fall time	-	25	ns

* (V_{DD1} = 2.2 – 5.5V, TA = +25°C)



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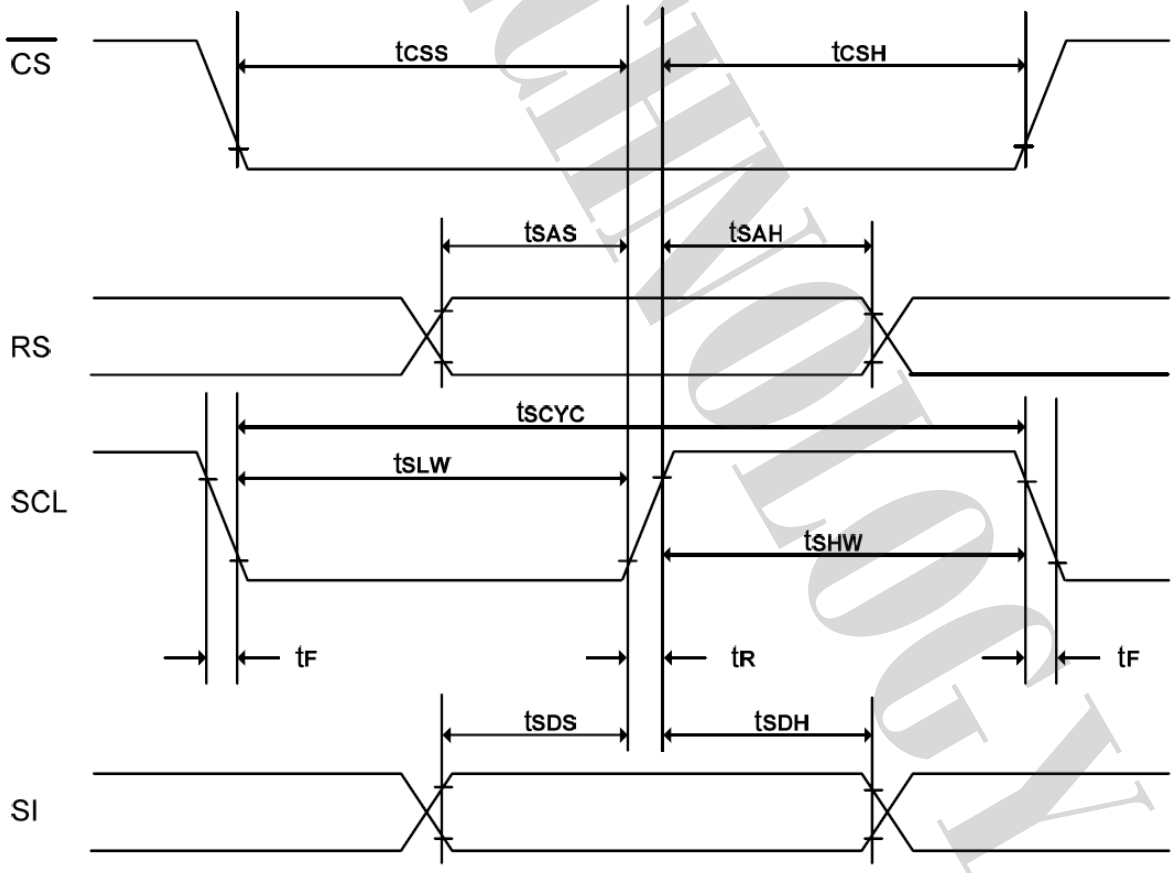
3.3.3 4- wire Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{SCYC}	Serial clock cycle	500	-	ns
t_{SAS}	Address setup time	300	-	ns
t_{SAH}	Address hold time	300	-	ns
t_{SDS}	Data setup time	200	-	ns
t_{SDH}	Data hold time	200	-	ns
t_{CSS}	$\overline{CS}$ setup time	240	-	ns
t_{CSH}	$\overline{CS}$ hold time time	120	-	ns
t_{SHW}	Serial clock H pulse width	200	-	ns
t_{SLW}	Serial clock L pulse width	200	-	ns
t_R	Rise time	-	30	ns
t_F	Fall time	-	30	ns

* (V_{DD1} = 2.2 – 5.5V, TA = +25°C)



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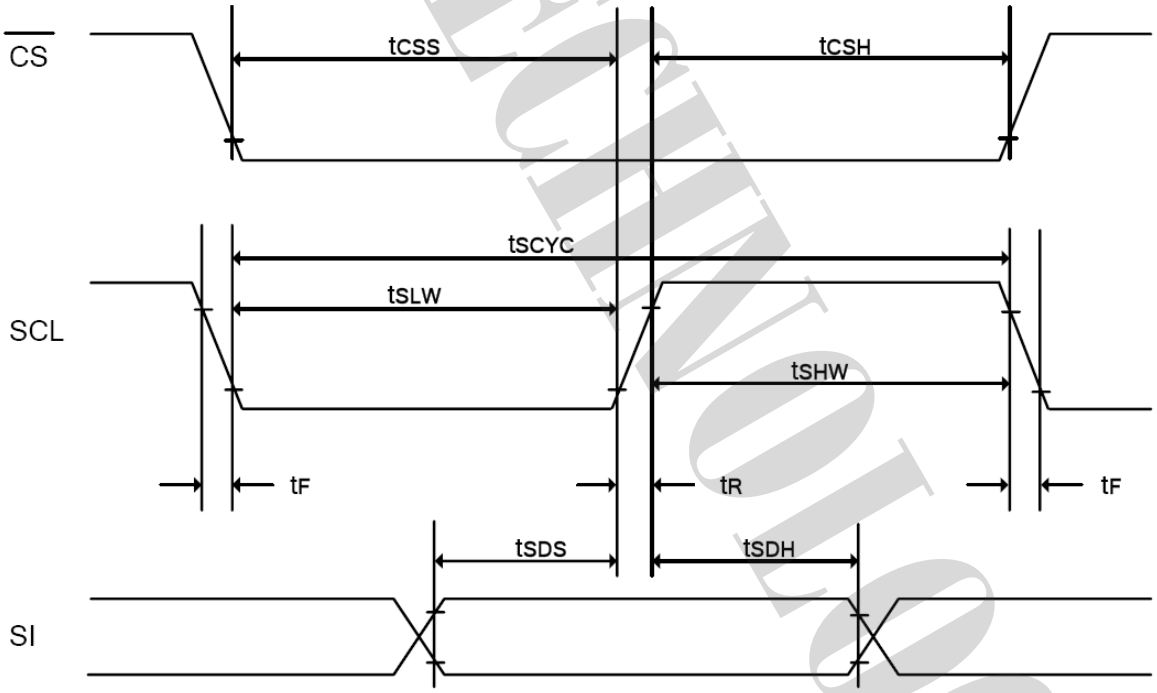
3.3.4 3- wire Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{SCYC}	Serial clock cycle	500	-	ns
t_{SDS}	Data setup time	200	-	ns
t_{SDH}	Data hold time	200	-	ns
t_{CSS}	$\overline{CS}$ setup time	240	-	ns
t_{CSH}	$\overline{CS}$ hold time time	120	-	ns
t_{SHW}	Serial clock H pulse width	200	-	ns
t_{SLW}	Serial clock L pulse width	200	-	ns
t_R	Rise time	-	30	ns
t_F	Fall time	-	30	ns

* (V_{DD1} = 2.2 – 5.5V, TA = +25°C)



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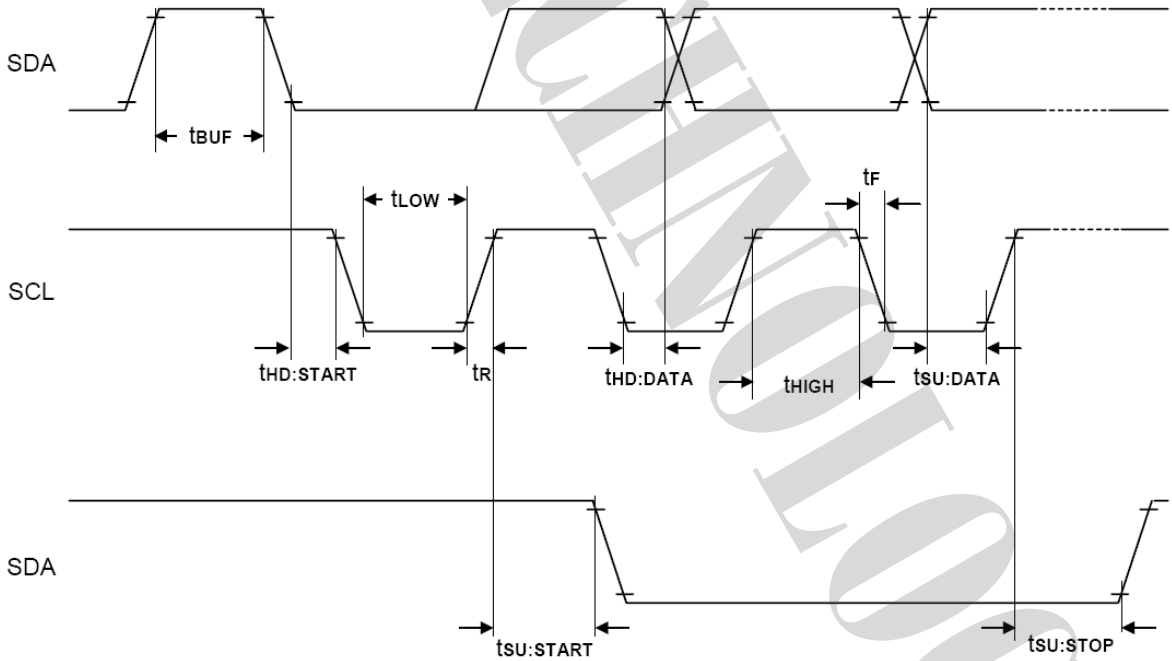
3.3.5 I²C Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
f_{SCL}	SCL clock frequency	DC	400	kHz
T_{LOW}	SCL clock Low pulse width	1.3	-	μs
T_{HIGH}	SCL clock H pulse width	0.6	-	μs
$T_{SU:DATA}$	data setup time	100	-	ns
$T_{HD:DATA}$	data hold time	0	0.9	μs
T_R	SCL，SDA rise time	20+0.1Cb	300	ns
T_F	SCL，SDA fall time	20+0.1Cb	300	ns
Cb	Capacity load on each bus line	-	400	pF
$T_{SU:START}$	Setup timefor re-START	0.6	-	μs
$T_{HD:START}$	START Hold time	0.6	-	μs
$T_{SU:STOP}$	Setup time for STOP	0.6	-	μs
T_{BUF}	Bus free times between STOP and START condition	1.3	-	μs

* (V_{DD1} = 2.2 – 5.5V, TA = +25°C)



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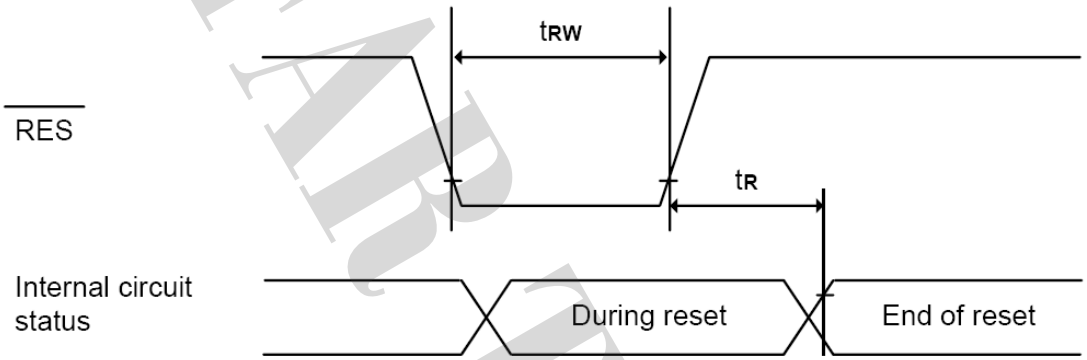
3.3.6 Reset Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_R	Reset time	-	2.0	μs
t_{RW}	Reset low pulse width	10.0	-	μs

* (V_{DD1} = 2.2 – 5.5V, TA = +25°C)



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4. Functional Specification

4.1. Commands

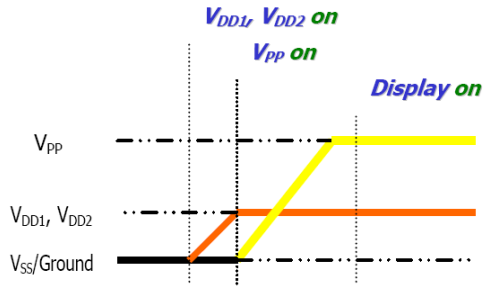
Refer to the Technical Manual for the US2011

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. It gives the OEL panel enough time to complete the action of charge and discharge before/after the operation.

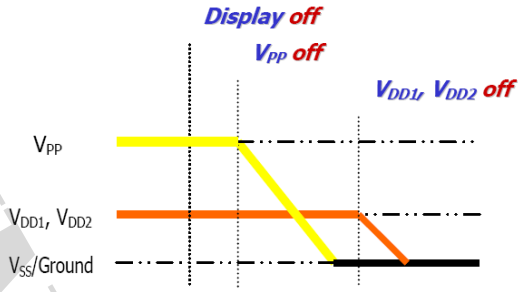
4.2.1 Power up Sequence:

1. Power up V_{DD1} & V_{DD2}
2. Send Display off command
3. Initialization
4. Clear Screen
5. Power up V_{PP}
6. Delay 100ms
   (When V_{PP} is stable)
7. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{PP}
3. Delay 100ms
   (When V_{PP} is reach 0 and panel is completely discharges)
4. Power down V_{DD1} & V_{DD2}



Note 9:

1) Since an ESD protection circuit is connected between VDD1, VDD2 and VPP inside the driver IC, VCC becomes lower than VDD1 & VDD2 whenever VDD1 & VDD2 is ON and V_{PP} is OFF.
2) VCC should be kept float (disable) when it is OFF.
3) Power Pins (VDD1, VDD2, VPP) can never be pulled to ground under any circumstance.
4) VDD1 & VDD2 should not be power down before VPP power down.

4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 5×8 Character Mode
3. Display start position is set at display RAM address 0
4. CGRAM address counter is set at 0
5. Cursor is OFF
6. Blink is OFF
7. Contrast control register is set at 7Fh
8. OLED command set is disabled
9. SEG direction set: SEG1 → SEG100
10. COM direction set: COM1 → COM32
11. Software set Font table disable
12. Font table select: Font table 1

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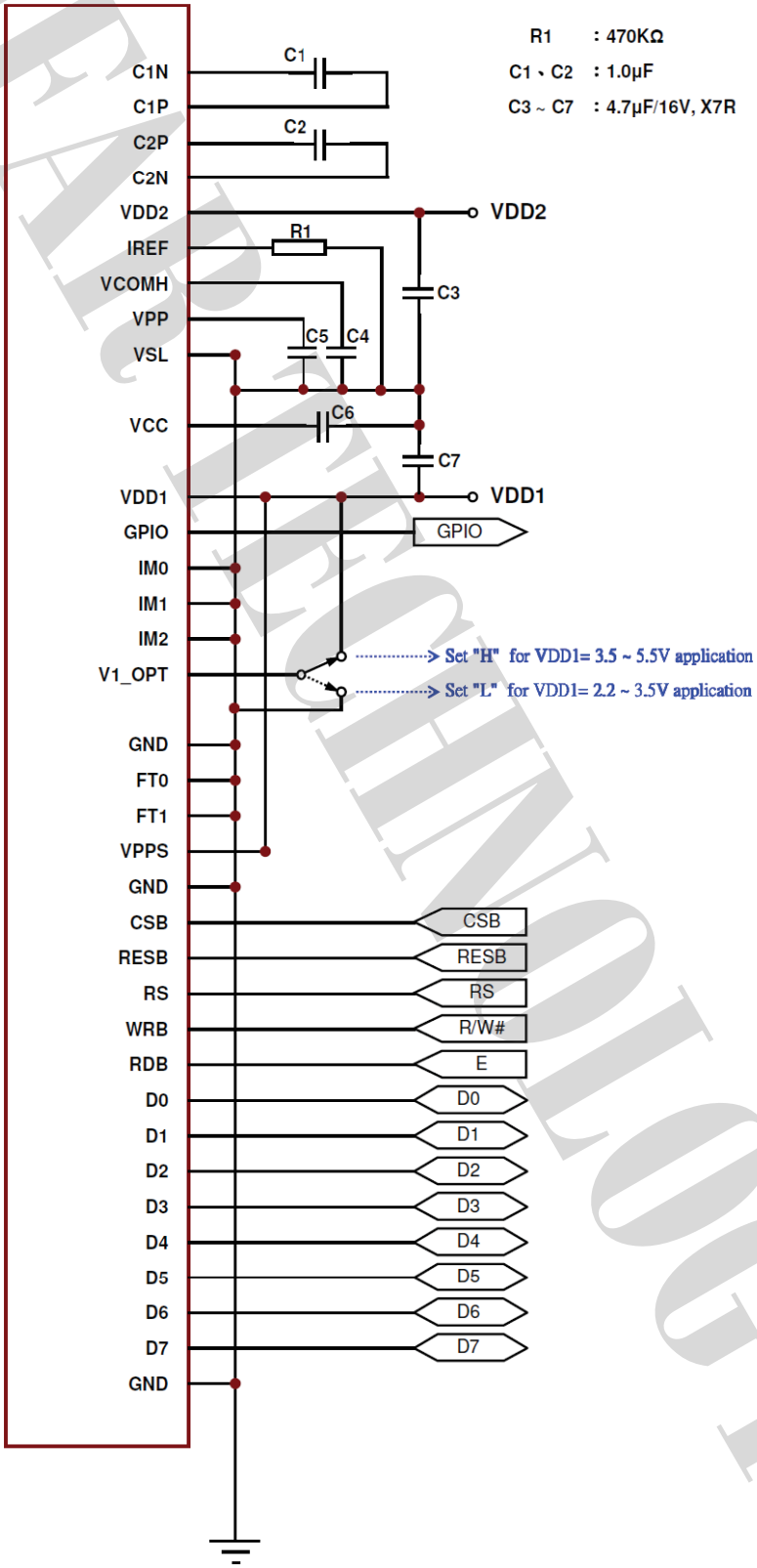
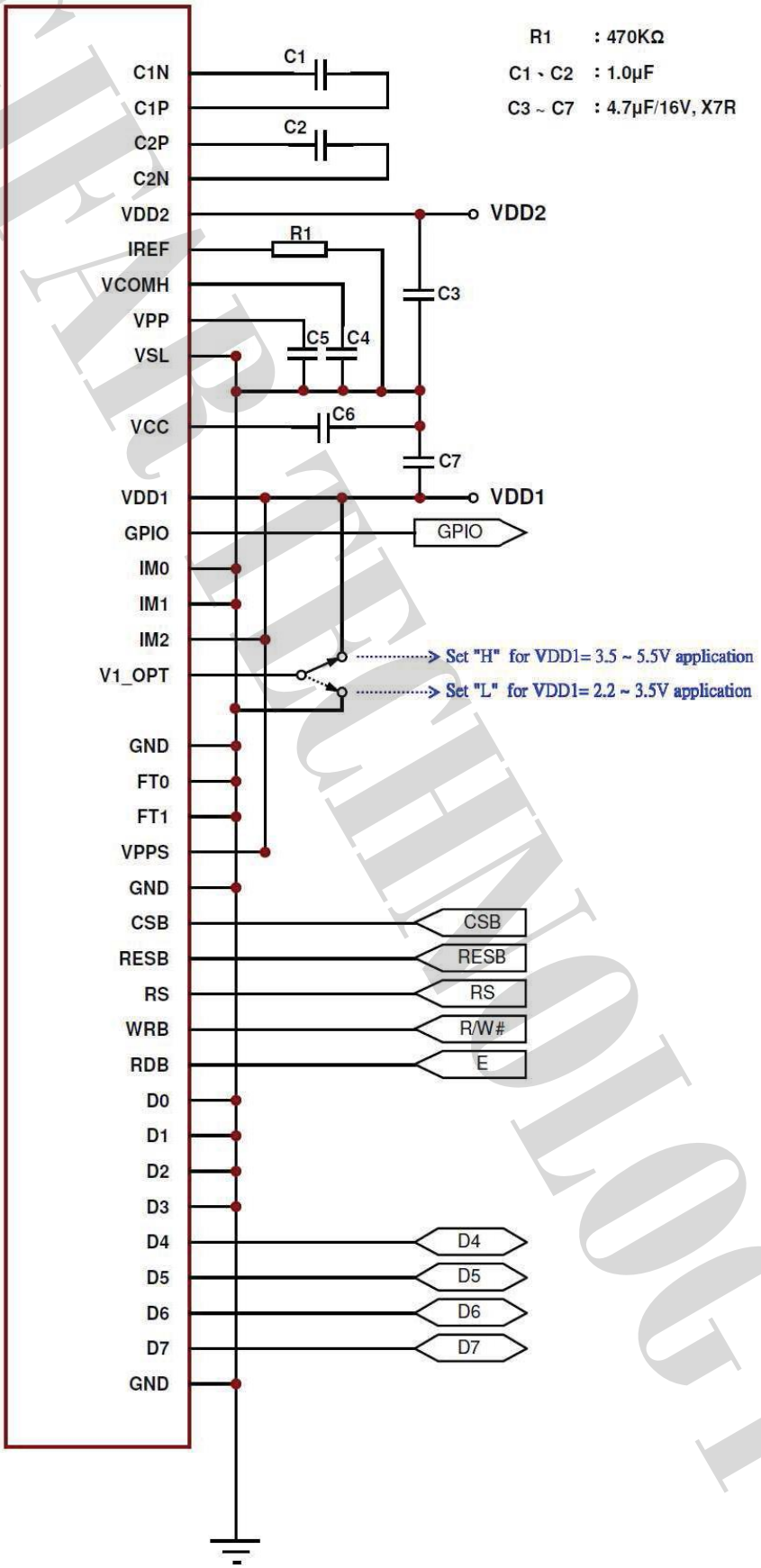
4.4 Application Circuit

4.4.1 68xx-Series MPU Parallel Interface

4.4.1.1 68xx 8bit Parallel Interface



4.4.1.2 68xx 4bit Parallel Interface



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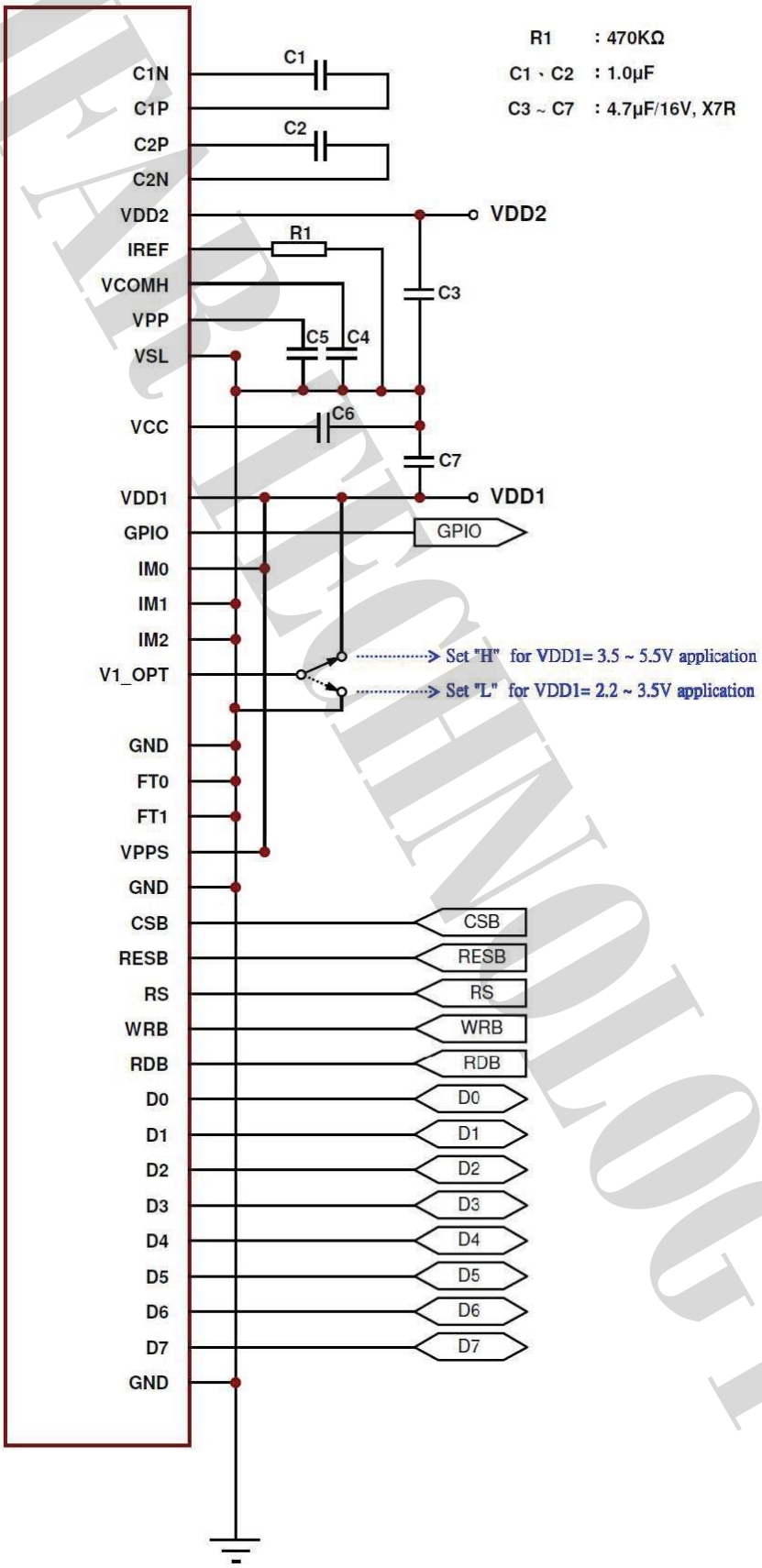
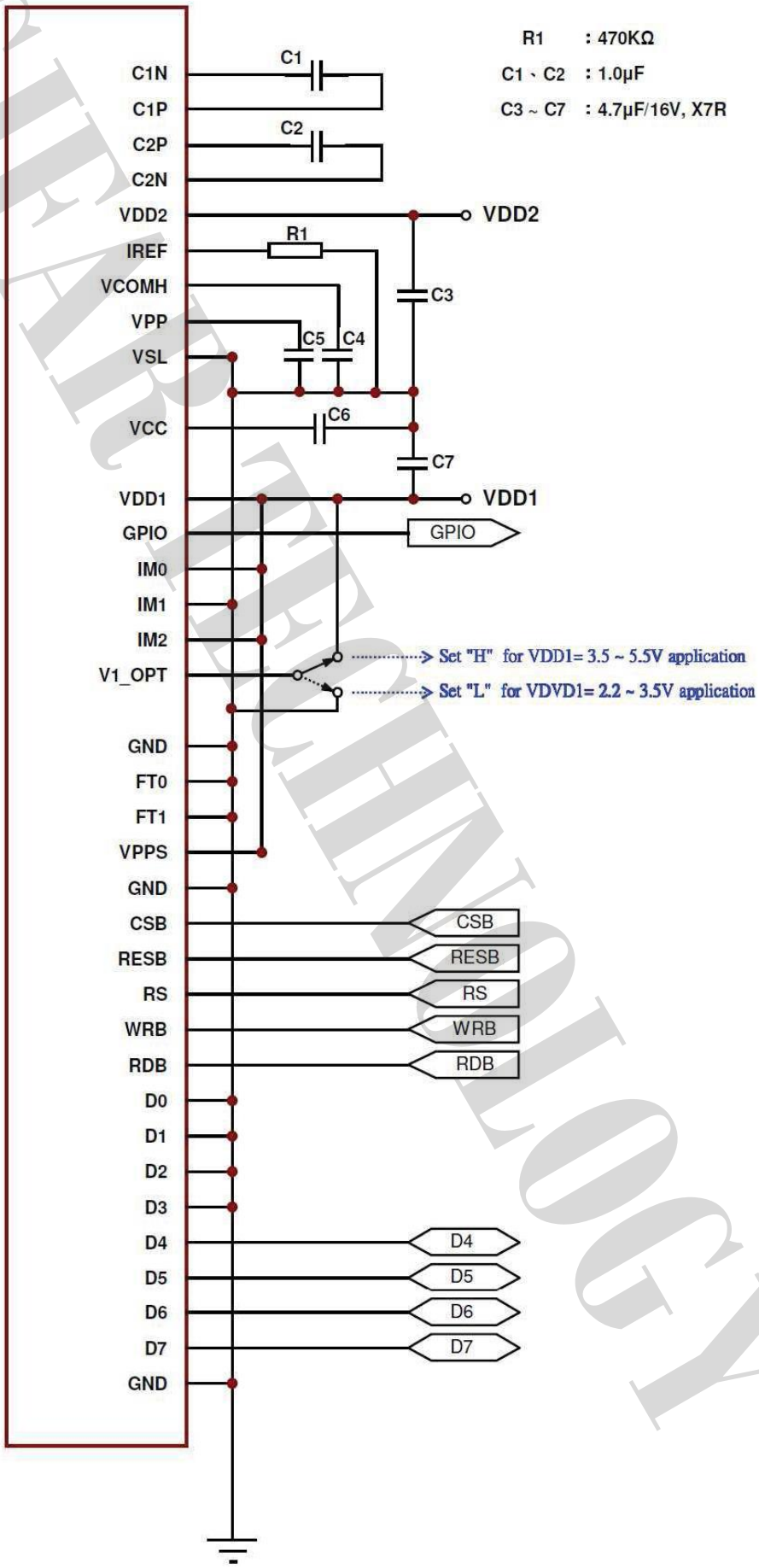
4.4.2 80XX-Series MPU Parallel Interface

4.4.2.1 80xx 8bit Parallel Interface



4.4.2.2 80xx 4bit Parallel Interface



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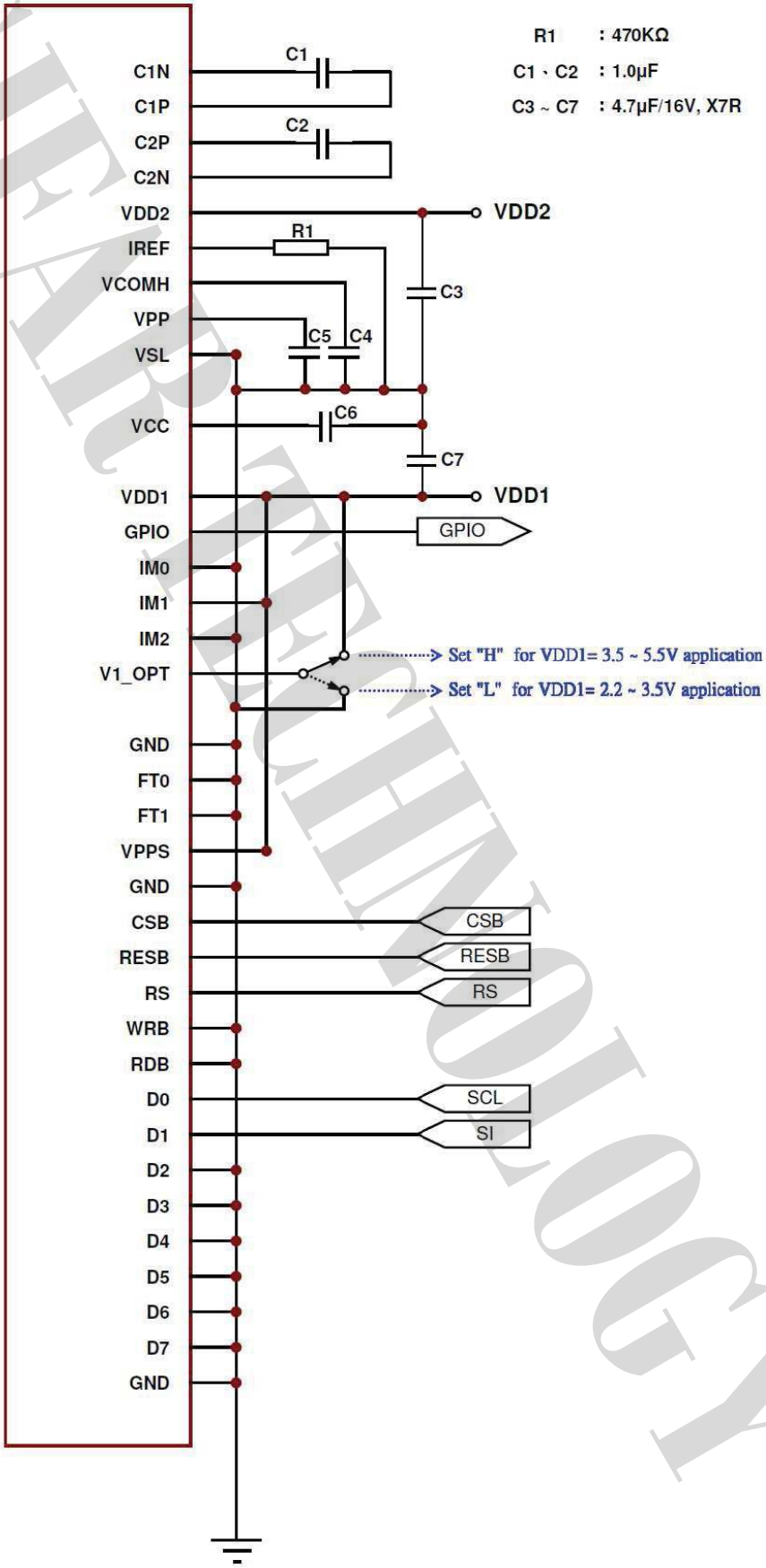
4.4.3 4-wire Serial Interface



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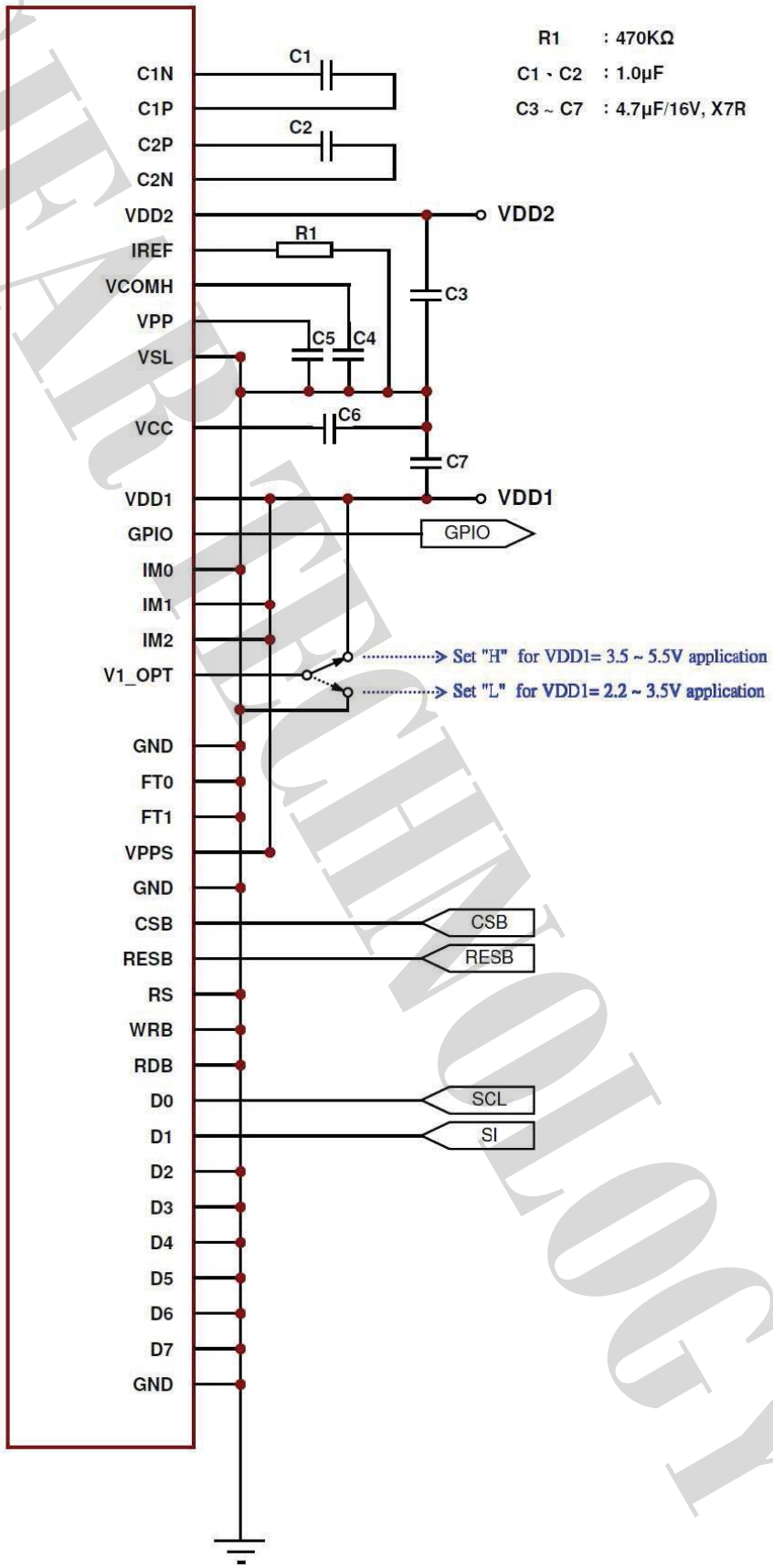
4.4.4 3-wire Serial Interface



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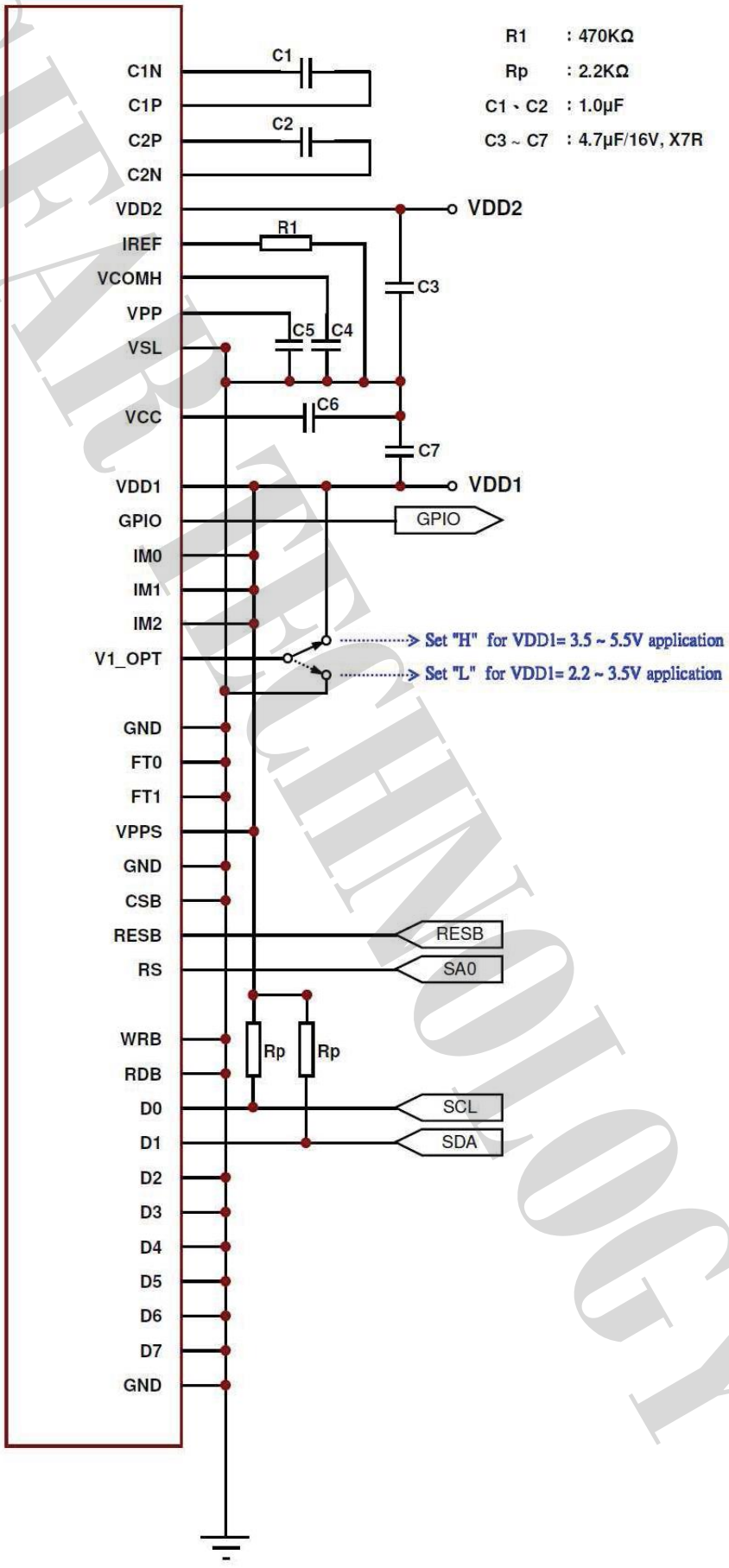
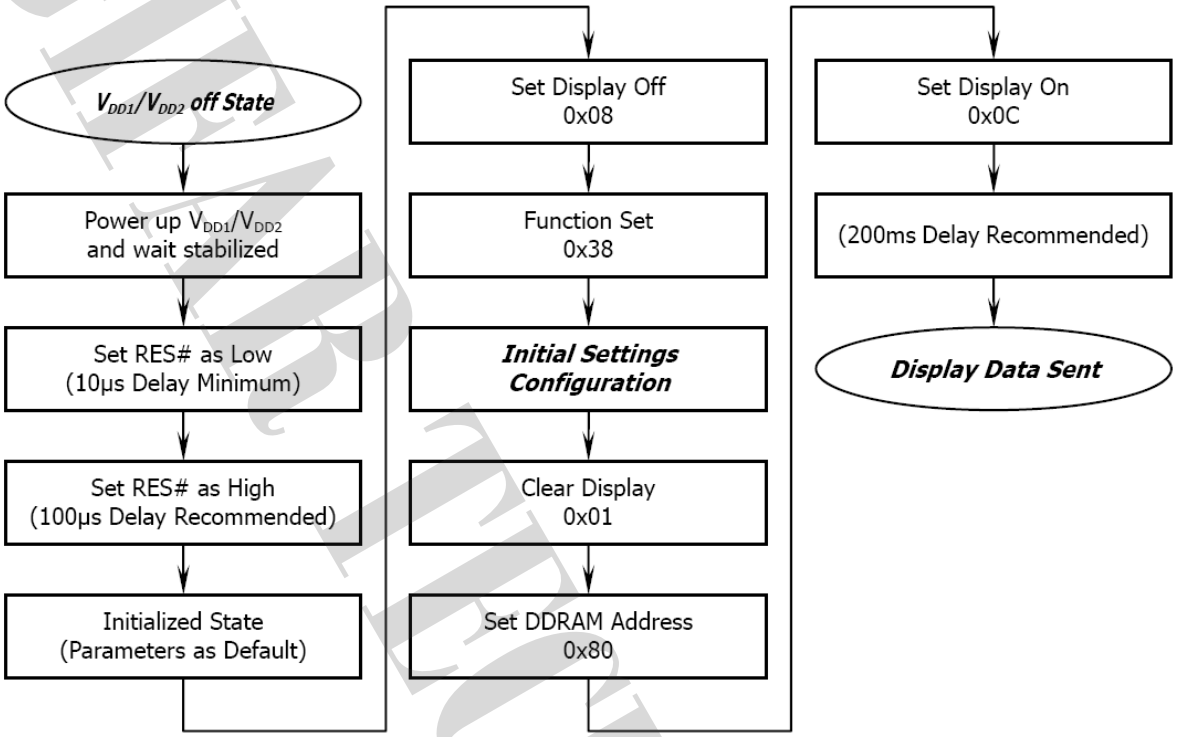
4.4.5 I²C Interface



4.5 Actual Application Example

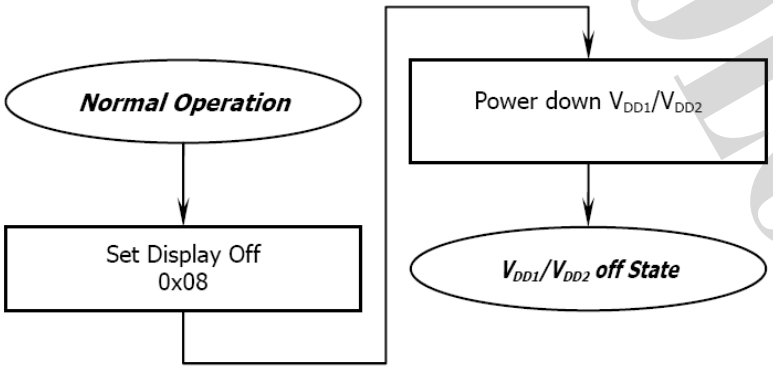
Command usage and explanation of an actual example

<Power up Sequence>



If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

<Power down Sequence>



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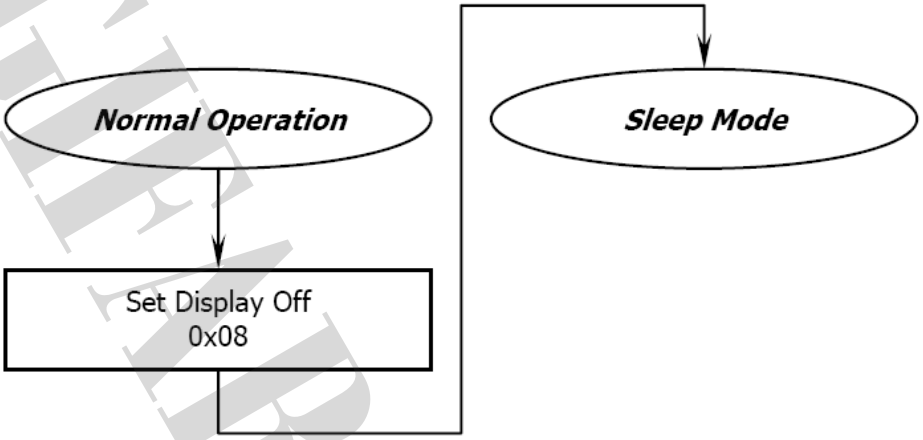
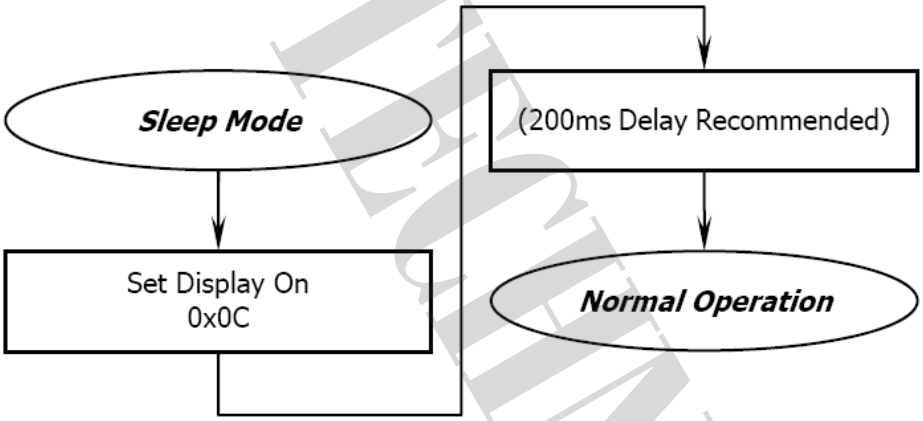
<Entering Sleep Mode>



<Exiting Sleep Mode>



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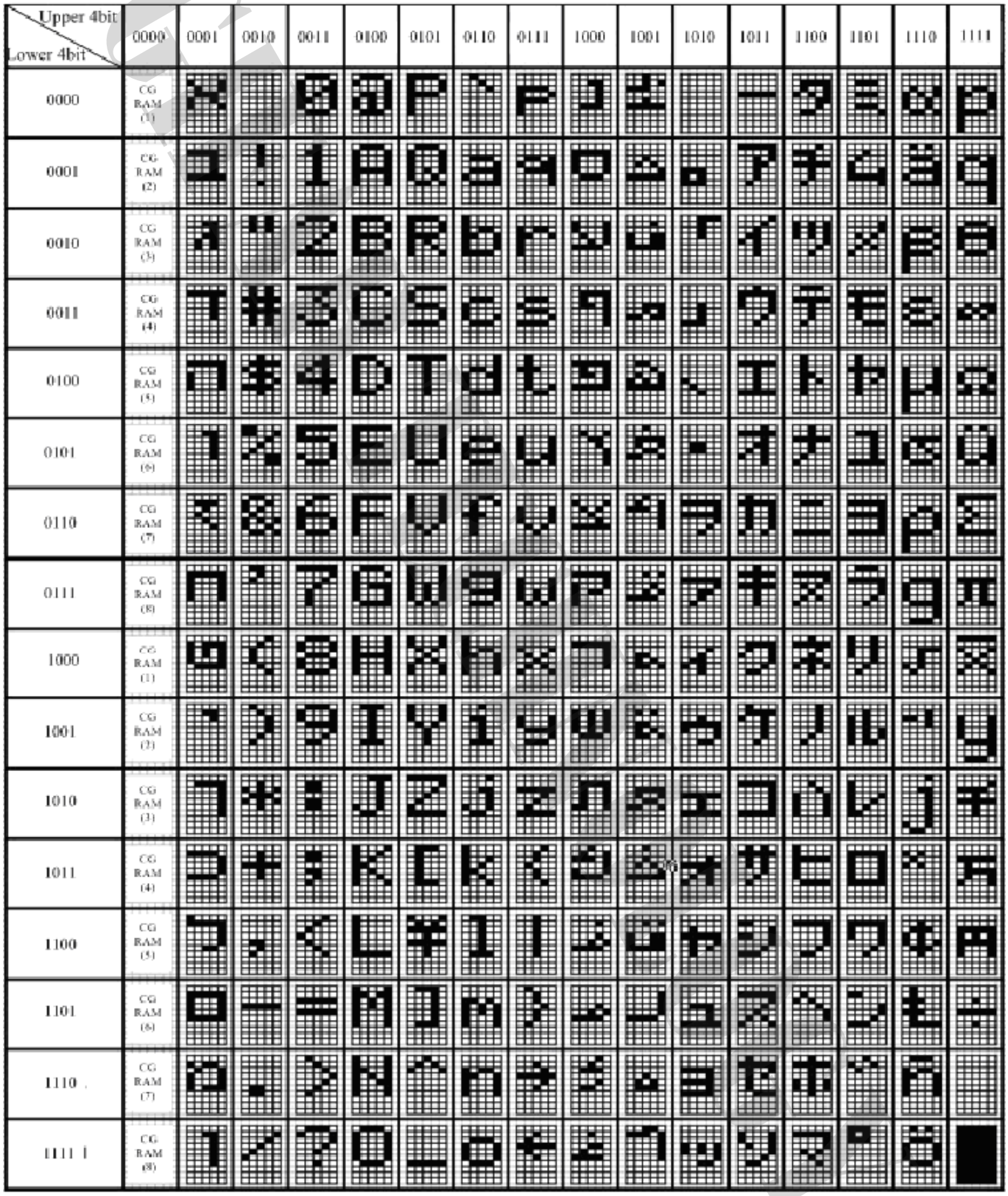
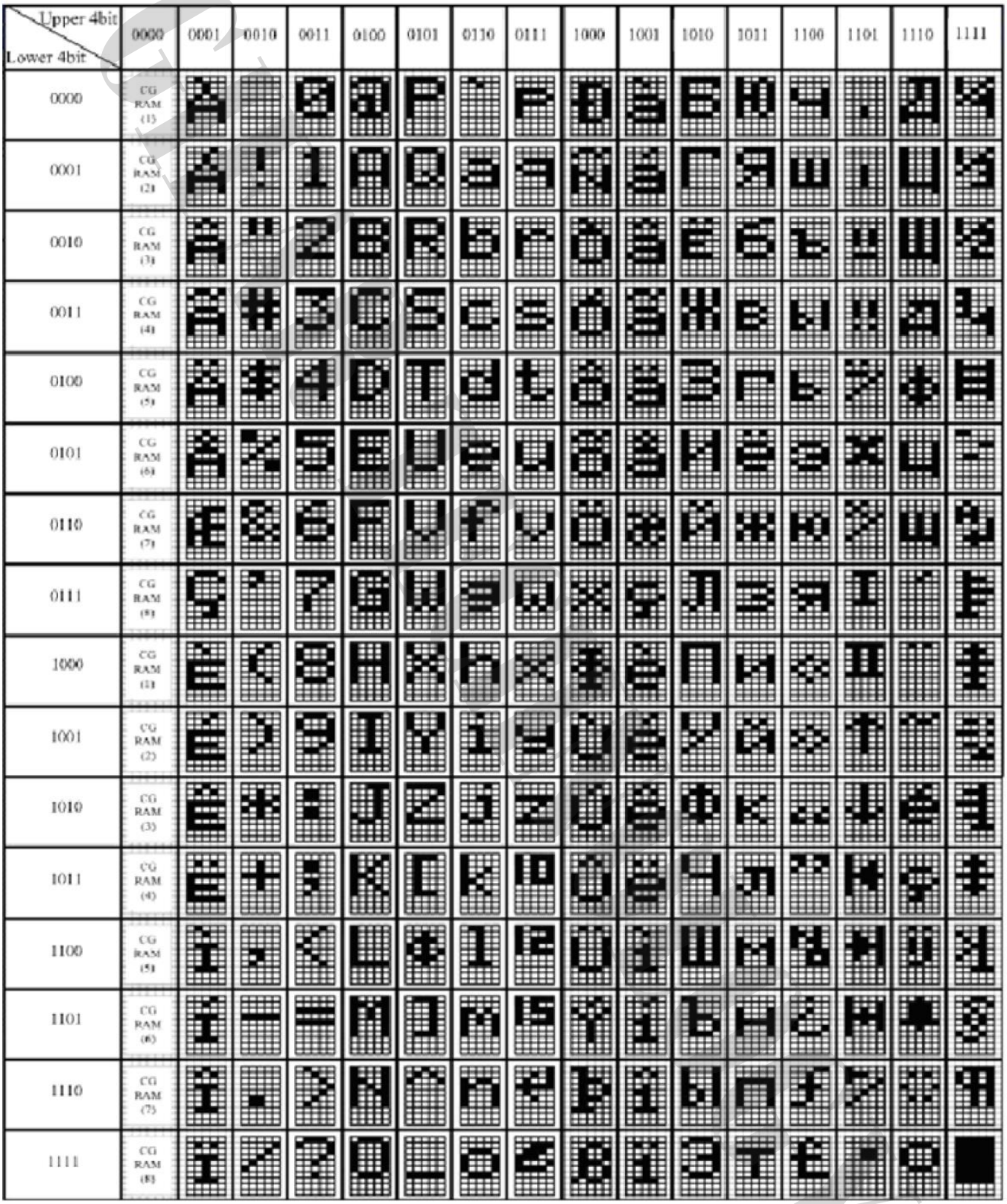
4.6 Built-in CGROM (Character Generator ROM)

ENGLISH_JAPANESE CHARACTER FONT TABLE (FT[1:0] = [0:0])

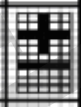
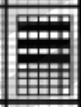
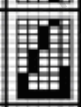
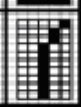
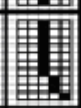
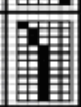
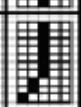
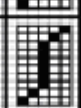
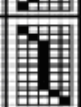
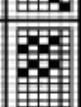
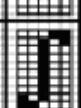
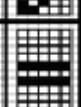
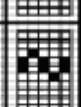
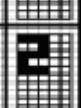
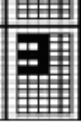


WESTERN EUROPEAN CHARACTER FONT TABLE I (FT[1:0]=01)

ENGLISH_RUSSIAN CHARACTER FONT TABLE(FT[1:0]=10)



WESTERN EUROPEAN CHARACTER FONT TABLE II (FT[1:0]=11)

Upper 4bit / Lower 4bit	0000	0001	0010	0011	0100	0101	0110	0111	1000	1001	1010	1011	1100	1101	1110	1111
0000	CG RAM (1)															
0001	CG RAM (2)															
0010	CG RAM (3)															
0011	CG RAM (4)															
0100	CG RAM (5)															
0101	CG RAM (6)															
0110	CG RAM (7)															
0111	CG RAM (8)															
1000	CG RAM (1)															
1001	CG RAM (2)															
1010	CG RAM (3)															
1011	CG RAM (4)															
1100	CG RAM (5)															
1101	CG RAM (6)															
1110	CG RAM (7)															
1111	CG RAM (8)															

5. Reliability

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	85°C, 240 hrs	The operational functions work.
Low Temperature Operation	-40°C,240 hrs	
High Temperature Storage	90°C, 240 hrs	
Low Temperature Storage	-40°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 240 hrs	
Thermal Shock	-40°C ⇔ 85°C, 100 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.

* No moisture condensation is observed during tests.

5.2 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

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6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15 %RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50 cm
Distance between the Panel & Eyes of the Inspector:	≥ 30 cm

Finger glove (or finger cover) must be worn by the inspector.

Inspection table or jig must be anti-electrostatic.

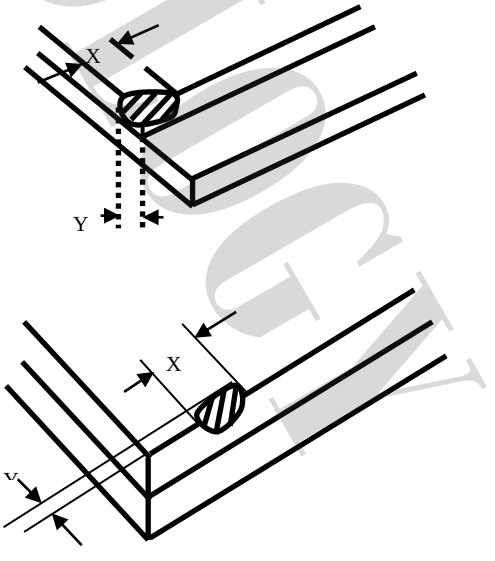
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

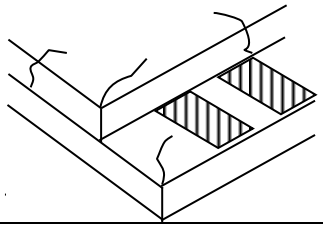
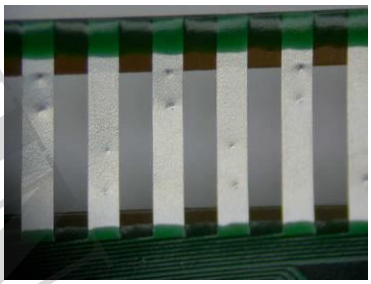
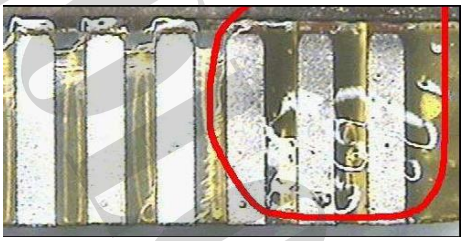
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

6.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) 

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Prober Mark	Acceptable	
Glue or Contamination on Pin (Couldn't Be Removed by Alcohol)	Minor	
Ink Marking on Back Side of panel(Exclude on Film)	Acceptable	Ignore for Any

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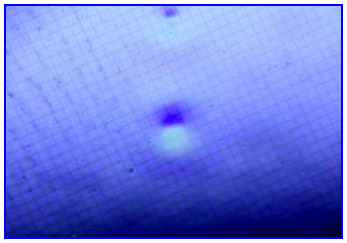
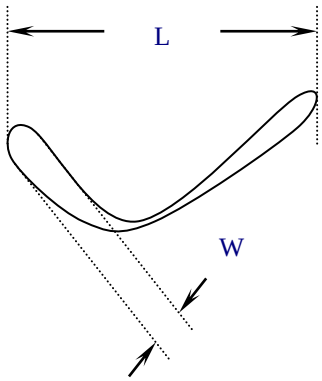
6.3.2 Cosmetic Check (Display Off) in Active Area

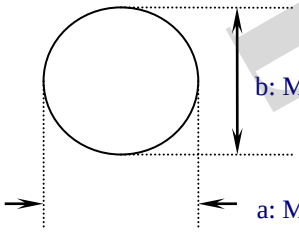
It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect (On Polarizer)	Minor	$W \le 0.1$ Ignore $W > 0.1$, $L \le 2$ $n \le 1$ $L > 2$ $n = 0$
Dirt, Black Spot, Foreign Material, (On Polarizer)	Minor	$\Phi \le 0.1$ Ignore $0.1 < \Phi \le 0.25$ $n \le 1$ $0.25 < \Phi$ $n = 0$
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	$\Phi \le 0.5$ ➔ Ignore if no Influence on Display $0.5 < \Phi$ $n = 0$ 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* Protective film should not be tear off when cosmetic check.

** Definition of W & L & Φ (Unit: mm): $\Phi = (a + b) / 2$





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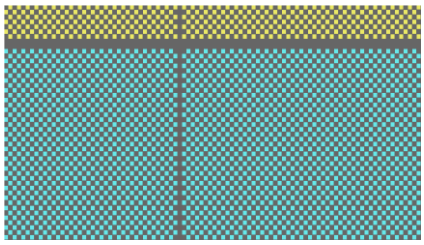
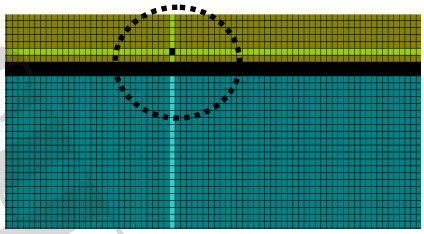
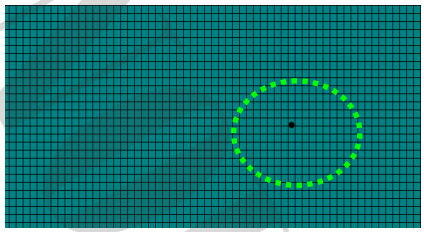
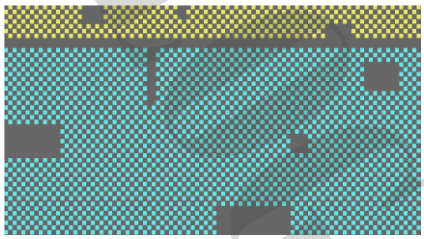
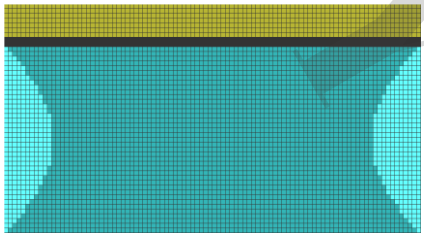
6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

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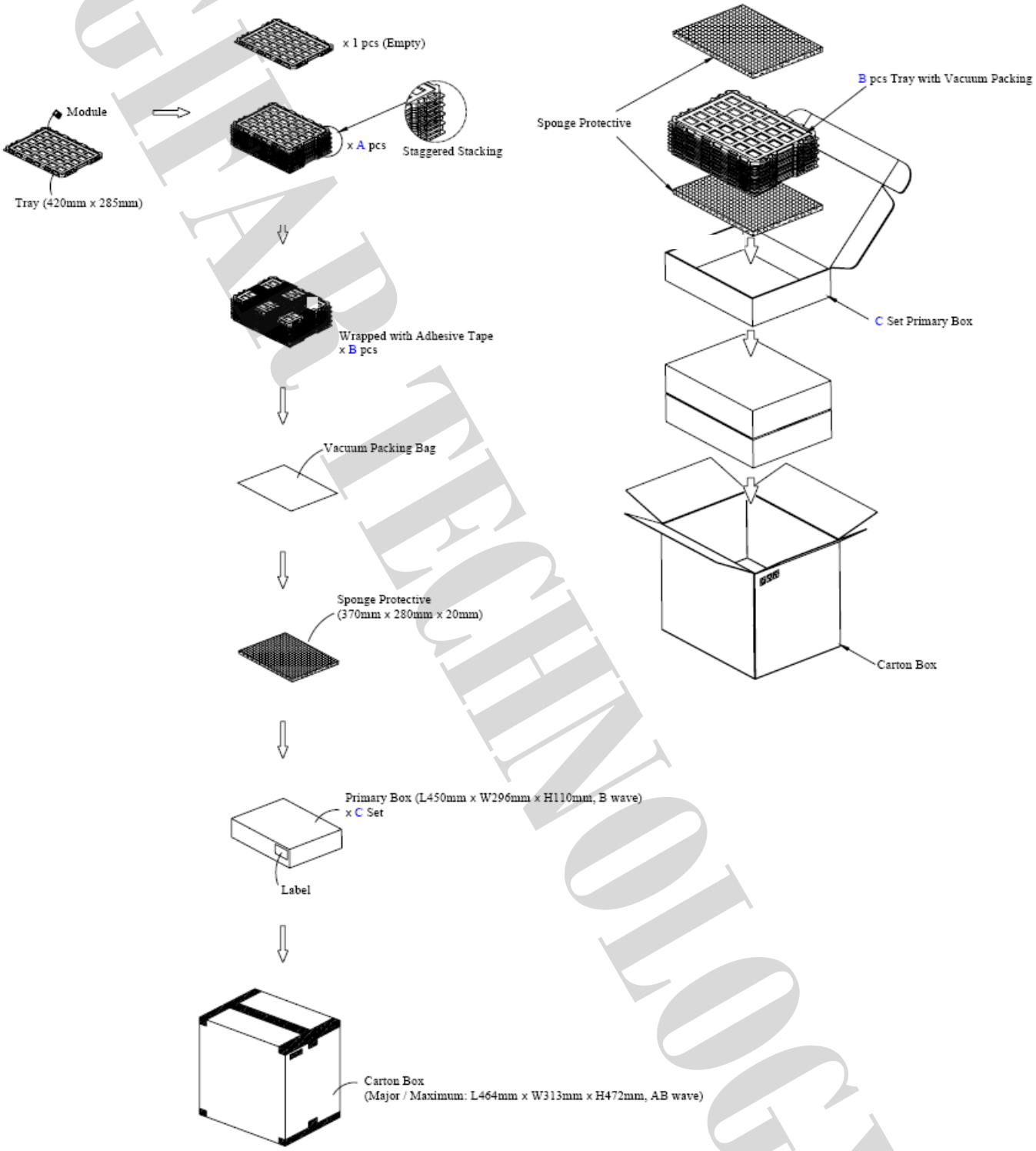
7. Package Specifications



Item	Quantity
Module	640 per Primary Box
Holding Trays (A)	20 per Primary Box
Total Trays (B)	21 per Primary Box (Including 1 Empty Tray)
Primary Box (C)	1~4 per Carton (4 as Major / Maximum)

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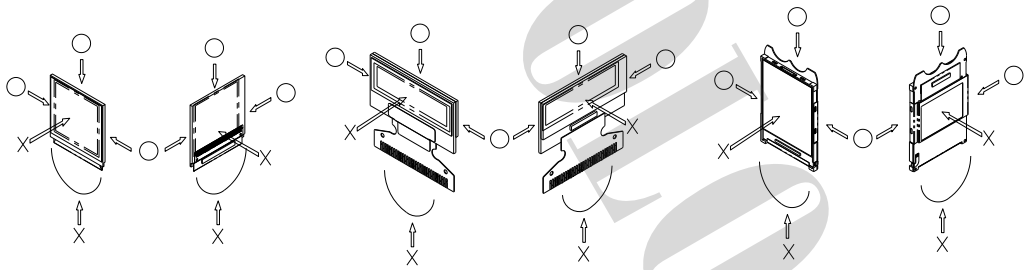
8. Precautions When Using These OEL Display Modules

8.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy. Also, pay attention that the following liquid and solvent may spoil the polarizer:

   * Water
   * Ketone
   * Aromatic Solvents
6) Hold OEL display module very carefully when placing OEL display module into the system housing. Do not apply excessive stress or pressure to OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display

module. Be careful since static electricity may be generated when exfoliating the protective film.

11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Univision Technology Inc.)

   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.

2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (V_{DD}). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: US2066

   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

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8.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

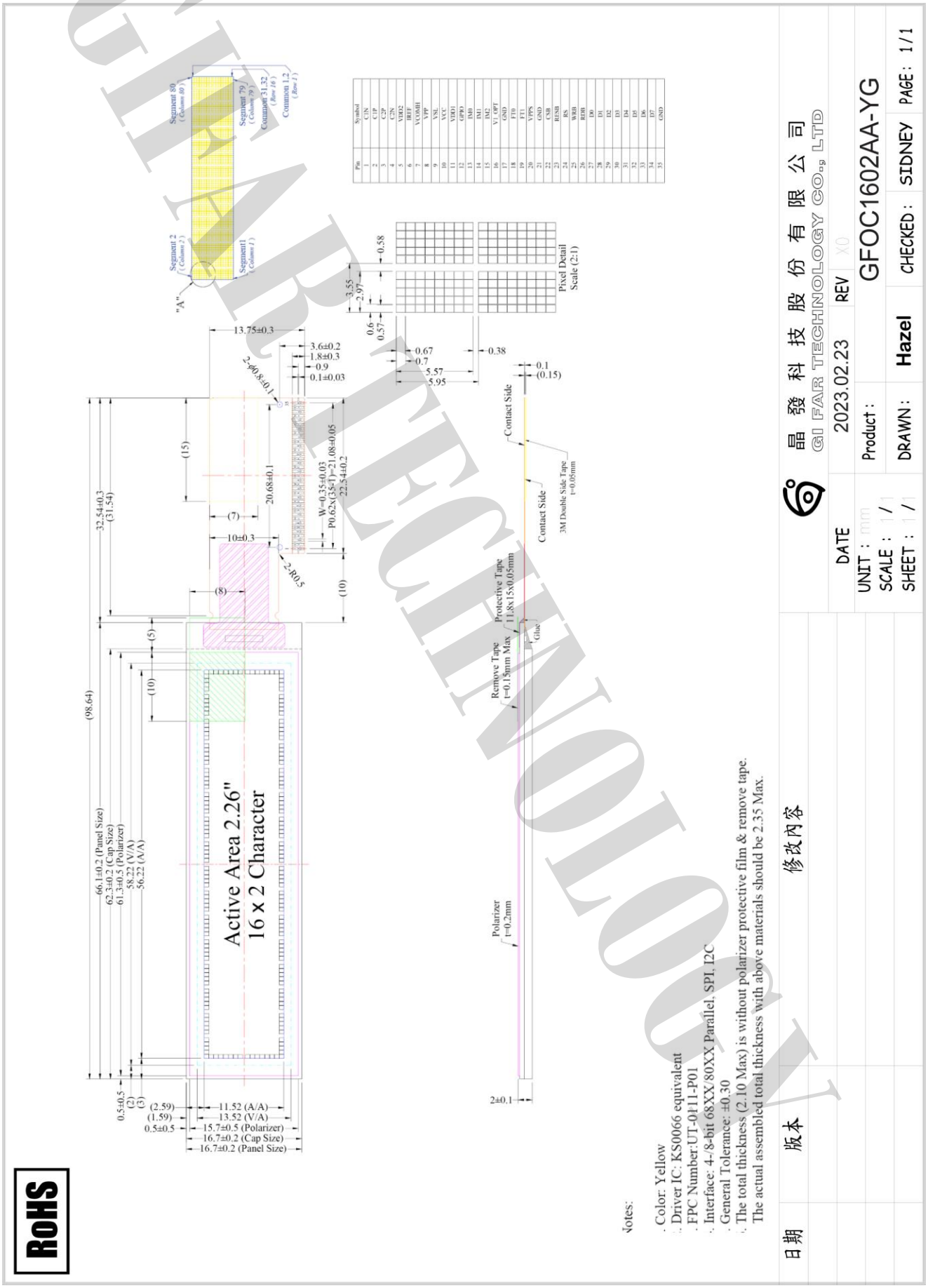
8.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the COF
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.

Warranty

The warranty period shall last twelve (12) months from the date of delivery. Buyer shall be completed to assemble all the processes within the effective twelve (12) months.

9. Mechanical Drawing



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