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LAPIS Technology Co., Ltd.
October 1, 2020

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FEUL620Q504H-02

ML620Q503H/Q504H
User's Manual

Issue Date: May.20, 2020

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Preface

This manual describes the operation of the hardware of the 16-bit microcontroller ML620Q503H/Q504H.

See the relevant manuals listed in supplementary volume; "MCU Relevant Documents list" as necessary.

Notation

Classification	Notation	Description
♦ Numeric value	xxh, xxH	Indicates a hexadecimal number. x: Any value in the range of 0 to F
	xxb	Indicates a binary number; "b" may be omitted. x: A value 0 or 1
♦ Unit	word, W	1 word = 16 bits
	byte, B	1 byte = 8 bits
	nibble, N	1 nibble = 4 bits
	mega-, M	10^6
	kilo-, K	$2^{10} = 1024$
	kilo-, k	$10^3 = 1000$
	milli-, m	10^{-3}
	micro-, μ	10^{-6}
	nano-, n	10^{-9}
	second, s (lower case)	second
♦ Terminology	"H" level, "1" level	Indicates high voltage signal levels V_{IH} and V_{OH} as specified by the electrical characteristics.
	"L" level, "0" level	Indicates low voltage signal levels V_{IL} and V_{OL} as specified by the electrical characteristics.

♦ Register description

R/W: Indicates that Read/Write attribute. "R" indicates that data can be read and "W" indicates that data can be written. "R/W" indicates that data can be read or written.

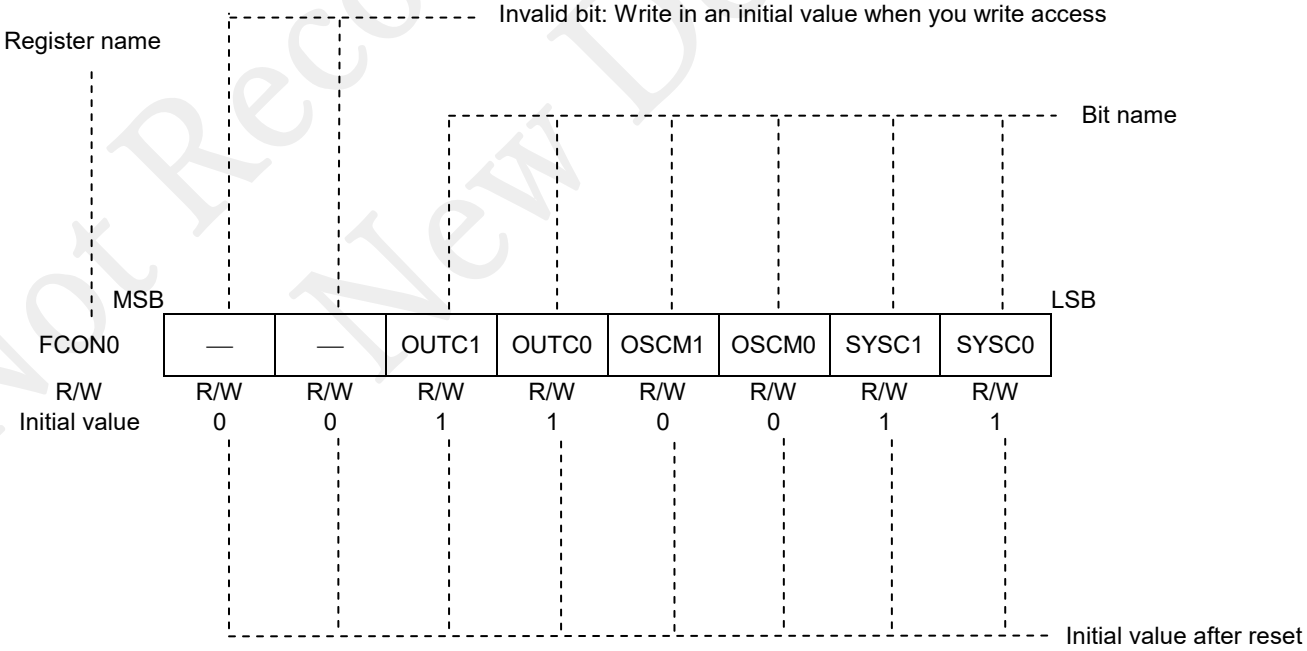


Table of Contents

Chapter 1

Chapter 2

Chapter 3

Chapter 4

Chapter 20

Chapter 21

Chapter 22

Chapter 23

Chapter 29

Chapter 30

Appendixes

Revision History

Chapter 1

Overview

1. Overview

1.1 Features

This LSI family is a high-performance 16-bit CMOS microcontroller into which rich peripheral circuits, such as synchronous serial port, UART, I^2C bus interface (master), supply voltage level detect circuit, RC oscillation type A/D converter, and successive approximation type A/D converter are incorporated around 16-bit CPU nX-U16/100.
The CPU nX-U16/100 is capable of efficient instruction execution in 1-instruction 1-clock mode by 3-stage pipe line architecture parallel processing. The Flash ROM* that is installed as program memory achieves low-voltage low-power consumption operation (read operation) is most suitable for battery-driven applications. And, this LSI has a data flash-memory* fill area by a software which can be written in.
The on-chip debug function that is installed enables program debugging and programming.

*: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc. SuperFlash® is a registered trademark of Silicon Storage Technology, Inc.

- CPU
  - 16-bit RISC CPU (CPU name: nX-U16/100)
  - Instruction system: 16-bit instructions
  - Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
  - Build-in On-Chip debug function
  - Minimum instruction execution time
    30.5 μs (@32.768 kHz system clock)
    62.5ns (@16 MHz system clock)

- Built-in coprocessor for multiplication, division, and multiply-accumulate operations
  - Signed or unsigned operation setting
  - Multiplication: 16bit × 16bit (operation time 4 cycles)
  - Division: 32bit / 16bit (operation time 8 cycles)
  - Division: 32bit / 32bit (operation time 16 cycles)
  - Multiply-accumulate (non-saturating): 16bit × 16bit + 32bit (operation time 4 cycles)
  - Multiply-accumulate (saturating): 16bit × 16bit + 32bit (operation time 4 cycles)

- Internal memory
  - Supports ISP function (re-writing the program memory area by software)
  - Number of segments

Product name	Flash memory		SRAM
	Program area**	Data area	
ML620Q503H	32KB (16K×16bit)	2KB(1K×16bit)	2KB(1K×16bit)
ML620Q504H	64KB (32K×16bit)	2KB(1K×16bit)	6KB(3K×16bit)

**: including 1KB of unusable test area

- Interrupt controller (INTC)
  - 1 non-maskable interrupt sources (Internal source: 1)
  - 37 maskable interrupt sources (Internal sources: 29, External sources: 8)
  - Software interrupt (SWI): maximum 64 sources
  - External interrupts and comparator allow edge selection and sampling selection
  - Priority level (4-level) can be set for each interrupt

- Time base counter (TBC)
  - Low-speed time base counter × 1 channel

- Timers (TMR)
  – 8 bits × 8 channels
    (Timer0-7: 16-bit × 4 configuration available by using Timer0-1 or Timer2-3, Timer4-5, Timer6-7)
  – Selection of one shot timer mode is possible
  – External clock can be selected as timer clock.

- Function Timers (FTM)
  – 16-bit × 4 channels
  – Equipped with the timer/capture/PWM functions using a 16-bit counter
  – Timer start/stop function by software/event trigger(external pin or other timer)
  – External pin can be selected as counter clock
  – Capture function (the measurement such as the pulse width is possible using external trigger input)
  – Two types of PWM with the same period and different duties and complementary PWM with the dead time set can be output.

- Watchdog timer (WDT)
  – Non-maskable interrupt and reset
  – Free running
  – Overflow period: 4 types selectable (125ms, 500ms, 2s, and 8s when LSCLK = 32.768 kHz)

- Synchronous serial port (SSIOF/ SSIO)
  – without FIFOs (SSIO) : 1 channel
  – with 4-byte transmits and receives FIFOs (SSIOF) : 1 channel
  – Master/slave are selectable
  – LSB first/MSB first are selectable
  – 8-bit length/16-bit length are selectable
  – Phase/Polarity of clock are selectable
  – supports slave-select signal (only SSIOF)

- UART (UARTF/ UART)
  – without FIFOs (UART) : 1ch
  – with 4-byte transmits and receives FIFOs (UARTF) : 1ch
  – Full duplex buffer system
  – Communication speed: Settable within the range of 2400bps to 115200bps.
  – Programmable interface (data length, parity, stop bits are selectable)

- I^2C bus interface (I^2C)
  – Master function × 2 channel
  – Fast mode (400 kbps), standard mode (100 kbps)

- General-purpose ports (PORT)
  – Input port x 2, Input/output port × 36 channels

- Melody driver (MELODY)
  – Tempo: 15 types
  – Scale: 29 types (Melody sound frequency: 508 Hz to 10.922 kHz)
  – Tone length: 63 types
  – Buzzer output mode (4 output modes, 8 buzzer frequencies, 7duty levels at 4.096kHz/15 duty levels at other buzzer frequencies)

- RC oscillation type A/D converter (RC-ADC)
  – Time division × 2 channels
  – 24-bit counter

- Successive approximation type A/D converter (SA-ADC)
  - Input × 12 channels
  - 12-bit A/D converter
  - Starting by trigger of Timer/FTM function.
  - Capacitive touch sense function

- Analog Comparator (CMP)
  - Input × 2 ch
  - Common mode input voltage: 0.2V to V_{DD} - 0.2V
  - Input offset voltage: 30mV(max)
  - Interrupt allow edge selection and sampling selection are selectable

- Voltage Level Supervisor (VLS)
  - Threshold voltages: selectable from 13 levels
  - interrupt or reset generate are selectable

- Low Level Detector(LLD)
  - Judgment Voltage: 1.8V±0.2V
  - Usable as low level detection reset

- Reset
  - Reset by the RESET_N pin
  - Reset by power-on detection
  - Reset by overflow of watchdog timer (WDT)
  - Reset by Voltage Level Supervisor(VLS)
  - Reset by Low Level Detector(LLD)

- Clock
  - Low-speed clock: (This LSI can not guarantee the operation without low-speed clock)
    - Crystal oscillation (32.768 kHz)
    - External clock input (30kHz to 36kHz)
    - Built-in RC oscillation (32.768kHz)
  - High-speed clock:
    - Crystal/Ceramic oscillation (16 MHz)
    - External clock input (2MHz to 16 MHz)
    - Built-in RC oscillation (16MHz)

- Power management
  - HALT mode: Instruction execution by CPU is suspended. All peripheral circuits can keep in operating states.
  - HALT-H mode: Instruction execution by CPU is suspended. Stop of high-speed oscillation automatically. All peripheral circuits can keep in operating states.
  - DEEP-HALT mode: Instruction execution by CPU is suspended. Some peripheral circuits(Timer, LTBC etc.) can keep in operating states.
  - STOP mode: Stop of low-speed oscillation and high-speed oscillation (Operations of CPU and peripheral circuits are stopped.)
  - Clock gear: The frequency of high-speed system clock can be changed by software (1/1, 1/2, 1/4, 1/8,1/16,1/32 of the oscillation clock)
  - Block Control Function: Power down (reset registers and stop clock supply) the circuits of unused peripherals.

- Shipment
  - Die *Please contact our responsible sales person for the pad layout information.
  - 48-pin plastic TQFP Tray/Tape and Reel
    ML620Q503H-xxxTB
    ML620Q504H-xxxTB

- Guaranteed operating range
  - Operating temperature (ambient) : –40°C to +85°C
  - Operating voltage: V_{DD} = 1.8V to 5.5V

1.2 Configuration of Functional Blocks

1.2.1 Block Diagram of ML620Q503H/Q504H

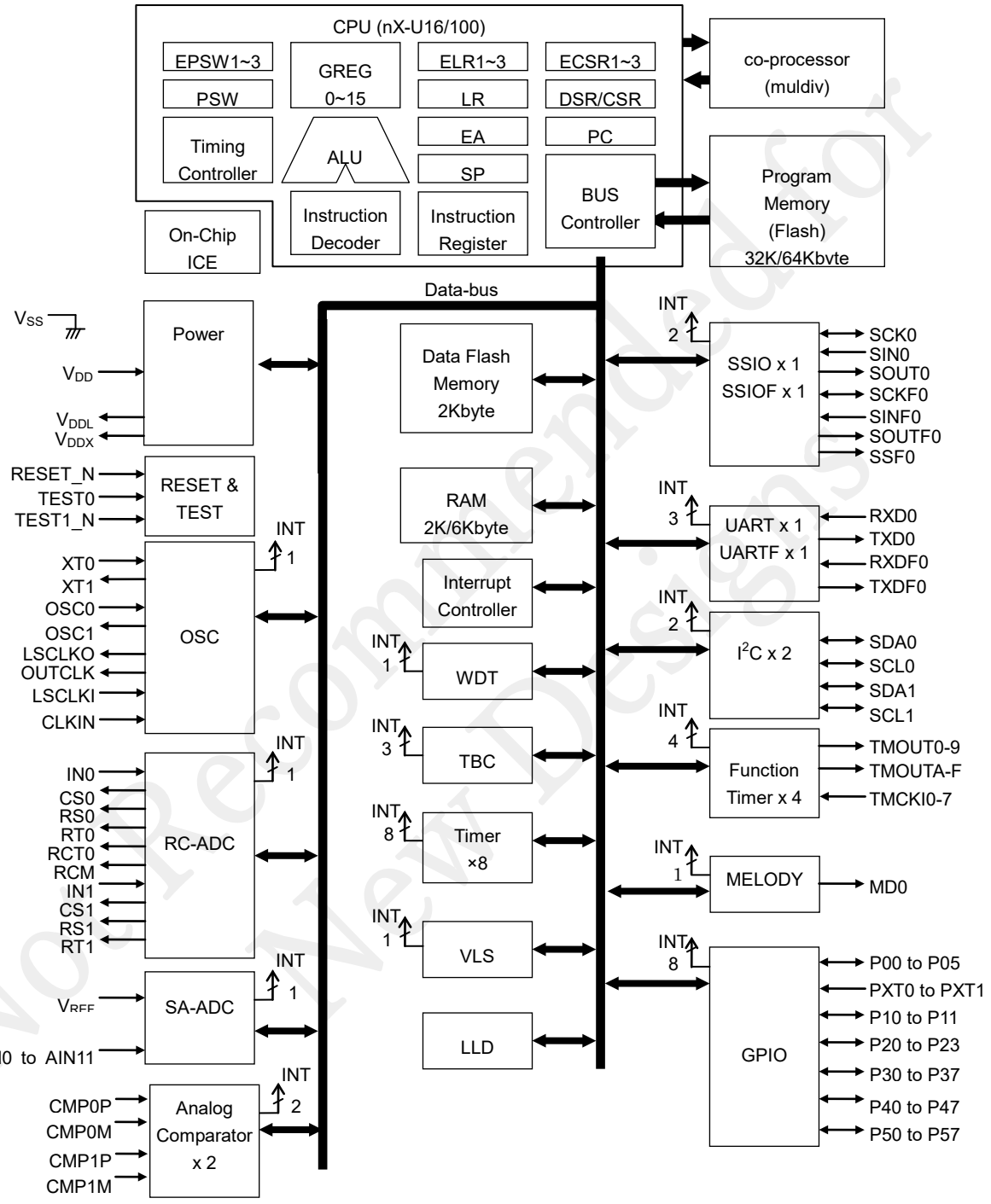
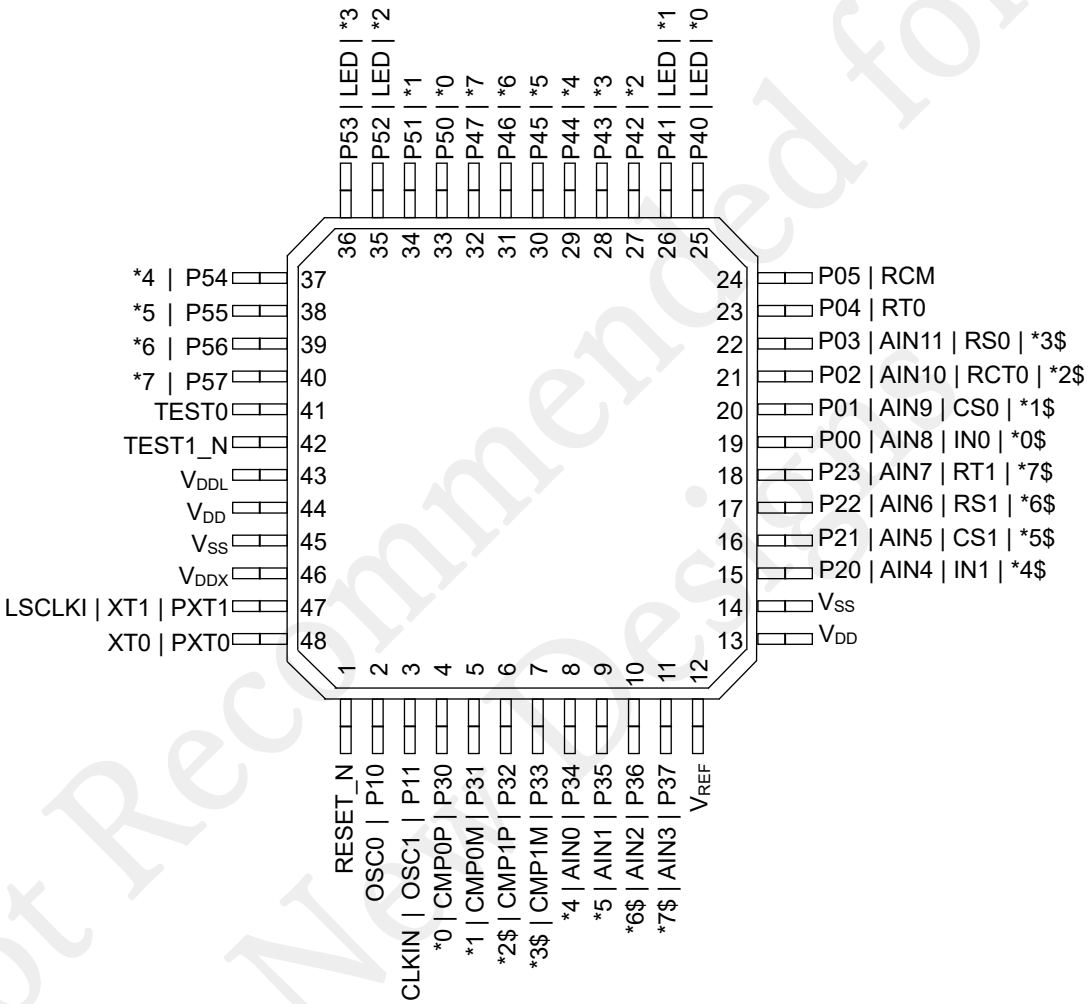


Figure 1-1 Block Diagram of ML620Q503H/Q504H

1.3 Pins

1.3.1 Pin Layout

1.3.1.1 Pin Layout of ML620Q503H/Q504H TQFP Package



External interrupt input pin(EXI) can be assigned to P00-P05, PXT0-1, P20-P57.
*0 to *7 and *0$ to *7$ has following functions. But 0-7 has limited function. Please refer to the pin list.

*0 : SDA0, SOUT0, RXD0	*4 : SDA1, SOUTF0, RXDF0
*1 : SCL0, SIN0 , TXD0	*5 : SCL1, SINF0, TXDF0
*2 : SCK0, TMOUT ,TMCKI	*6 : LSCLKO,SCKF0, TMOUT, TMCKI
*3 : MD0, TMOUT , TMCKI	*7 : OUTCLK,SSF0, TMOUT, TMCKI
*0$: SOUT0, RXD0	*4$: SOUTF0, RXDF0
*1$: SIN0, TXD0	*5$: SINF0, TXDF0
*2$: SCK0, TMOUT	*6$: SCKF0, TMOUT
*3$: MD0(P33 only), TMOUT	*7$: SSF0, TMOUT

Figure 1-2 Pin Layout of ML620Q503H/Q504H TQFP Package

1.3.2 List of Pins

1.3.2.1 List of Pins of ML620Q503H/Q504H TQFP Package

PKG Pin No.	1st Function				2nd/3rd/4th Function								
	Pin name	I/O	Reset State	Function	pin name	I/O	function	pin name	I/O	function	pin name	I/O	function
14, 45	V_{SS}	–	–	Negative power supply pin	–	–	–	–	–	–	–	–	–
13, 44	V_{DD}	–	–	Positive power supply pin	–	–	–	–	–	–	–	–	–
43	V_{DDL}	–	–	Power supply pin for internal circuit (internally generated)	–	–	–	–	–	–	–	–	–
46	V_{DDX}	–	–	Power supply pin for internal circuit (internally generated)	–	–	–	–	–	–	–	–	–
12	V_{REF}	–	–	Reference power supply pin of SA-ADC	–	–	–	–	–	–	–	–	–
1	RESET_N	I	Pull-up Input	Reset input pin	–	–	–	–	–	–	–	–	–
42	TEST1_N	I	Pull-up Input	Input pin for testing	–	–	–	–	–	–	–	–	–
41	TEST0	I/O	Pull-down Input	Input/output pin for testing	–	–	–	–	–	–	–	–	–
48	PXT0/ EXII0/ XT0	I	Input disable	Input port/ External interrupt/ Low-speed oscillation port	–	–	–	–	–	–	–	–	–
47	PXT1/ EXI1/ XT1/ LSCLKI	I/O	Hi-Z output	Input-Output port/ External interrupt/ Low-speed oscillation port Low-speed external clock input	–	–	–	–	–	–	–	–	–
19	P00/ EXI00/ AIN8	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	IN0	I	RC-ADC oscillation input	SOUT0	O	SSIO data output	RXD0	I	UART data input
20	P01/ EXI01/ AIN9	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	CS0	O	RC-ADC reference capacitance connection pin	SIN0	I	SSIO data input	TXD0	O	UART data output
21	P02/ EXI02/ AIN10	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	RCT0	O	RCADC resistor/capacitor sensor connection pin	SCK0	I/O	SSIO clock input/output	TMOUT0	O	FTM output
22	P03/ EXI03/ AIN11	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	RS0	O	RC-ADC reference resistor connection pin	–	–	–	TMOUT1	O	FTM output
23	P04/ EXI04	I/O	Hi-Z output	Input-Output port/ External interrupt	RT0	O	RC-ADC measurement resistor sensor connection pin	–	–	–	–	–	–
24	P05/ EXI05	I/O	Hi-Z output	Input-Output port/ External interrupt	RCM	O	RC-ADC oscillation monitor	–	–	–	–	–	–
2	P10/ OSC0	I/O	Hi-Z output	Input-Output port/ High-speed oscillation port	–	–	–	–	–	–	–	–	–
3	P11/ OSC1/ CLKIN	I/O	Hi-Z output	Input-Output port/ High-speed oscillation port High-speed external clock input	–	–	–	–	–	–	–	–	–
15	P20/ EXI20/ AIN4	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	IN1	I	RC-ADC oscillation input	SOUTF0	O	SSIOF data output	RXDF0	I	UARTF data input
16	P21/ EXI21/ AIN5	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	CS1	O	RC-ADC reference capacitance connection pin	SINF0	I	SSIOF data input	TXDF0	O	UARTF data output
17	P22/ EXI22/ AIN6	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	RS1	O	RC-ADC reference resistor connection pin	SCKF0	I/O	SSIOF clock input/output	TMOUT2	O	FTM output
18	P23/ EXI23/ AIN7	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	RT1	O	RC-ADC measurement resistor sensor connection pin	SSF0	I/O	SSIOF select input/output	TMOUT3	O	FTM output
4	P30/ EXI30/ CMP0P	I/O	Hi-Z output	Input-Output port/ External interrupt/ Comparator plus input	SDA0	I/O	I^2C data input/output	SOUT0	O	SSIO data output	RXD0	I	UART data input

PKG Pin No.	1st Function				2nd/3rd/4th Function								
	Pin name	I/O	Reset State	Function	pin name	I/O	function	pin name	I/O	function	pin name	I/O	function
5	P31/ EXI31/ CMP0 M	I/O	Hi-Z output	Input-Output port/ External interrupt/ Comparator minus input	SCL0	O	I^2C clock output	SIN0	I	SSIO data input	TXD0	O	UART data output
6	P32/ EXI32/ CMP1 P	I/O	Hi-Z output	Input-Output port/ External interrupt/ Comparator plus input	–	–	–	SCK0	I/O	SSIO clock input/output	TMOUT4	O	FTM output
7	P33/ EXI33/ CMP1 M	I/O	Hi-Z output	Input-Output port/ External interrupt/ Comparator minus input	MD0	O	Melody/Buzzer output	–	–	–	TMOUT5	O	FTM output
8	P34/ EXI34/ AIN0	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	SDA1	I/O	I^2C data input/output	SOUTF0	O	SSIOF data output	RXDF0	I	UARTF data input
9	P35/ EXI35/ AIN1	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	SCL1	O	I^2C clock output	SINF0	I	SSIOF data input	TXDF0	O	UARTF data output
10	P36/ EXI36/ AIN2	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	–	–	–	SCKF0	I/O	SSIOF clock input/output	TMOUT6	O	FTM output
11	P37/ EXI37/ AIN3	I/O	Hi-Z output	Input-Output port/ External interrupt/ SA-ADC input	–	–	–	SSF0	I/O	SSIOF select input/output	TMOUT7	O	FTM output
25	P40/ EXI40/ LED	I/O	Hi-Z output	Input-Output port/ External interrupt/ LED output	SDA0	I/O	I^2C data input/output	SOUT0	O	SSIO data output	RXD0	I	UART data input
26	P41/ EXI41/ LED	I/O	Hi-Z output	Input-Output port/ External interrupt/ LED output	SCL0	O	I^2C clock output	SIN0	I	SSIO data input	TXD0	O	UART data output
27	P42/ EXI42/ TMCKI 0	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input	–	–	–	SCK0	I/O	SSIO clock input/output	TMOUT8	O	FTM output
28	P43/ EXI43/ TMCKI 1	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input	MD0	O	Melody/Buzzer output	–	–	–	TMOUT9	O	FTM output
29	P44/ EXI44	I/O	Hi-Z output	Input-Output port/ External interrupt	SDA1	I/O	I^2C data input/output	SOUTF0	O	SSIOF data output	RXDF0	I	UARTF data input
30	P45/ EXI45	I/O	Hi-Z output	Input-Output port/ External interrupt	SCL1	O	I^2C clock output	SINF0	I	SSIOF data input	TXDF0	O	UARTF data output
31	P46/ EXI46/ TMCKI 2	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input	LSCLKO	O	Low-speed clock output	SCKF0	I/O	SSIOF clock input/output	TMOUTA	O	FTM output
32	P47/ EXI47/ TMCKI 3	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input	OUTCLK	O	High-speed clock output	SSF0	I/O	SSIOF select input/output	TMOUTB	O	FTM output
33	P50/ EXI50	I/O	Hi-Z output	Input-Output port/ External interrupt	SDA0	I/O	I^2C data input/output	SOUT0	O	SSIO data output	RXD0	I	UART data input
34	P51/ EXI51	I/O	Hi-Z output	Input-Output port/ External interrupt	SCL0	O	I^2C clock output	SIN0	I	SSIO data input	TXD0	O	UART data output
35	P52/ EXI52/ TMCKI 4/ LED	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input/ LED output	–	–	–	SCK0	I/O	SSIO clock input/output	TMOUTC	O	FTM output
36	P53/ EXI53/ TMCKI 5/ LED	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input/ LED output	MD0	O	Melody/Buzzer output	–	–	–	TMOUTD	O	FTM output
37	P54/ EXI54	I/O	Hi-Z output	Input-Output port/ External interrupt	SDA1	I/O	I^2C data input/output	SOUTF0	O	SSIOF data output	RXDF0	I	UARTF data input
38	P55/ EXI55	I/O	Hi-Z output	Input-Output port/ External interrupt	SCL1	O	I^2C clock output	SINF0	I	SSIOF data input	TXDF0	O	UARTF data output
39	P56/ EXI56/ TMCKI 6	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input	LSCLKO	O	Low-speed clock output	SCKF0	I/O	SSIOF clock input/output	TMOUTE	O	FTM output

PKG Pin No.	1st Function				2nd/3rd/4th Function								
	Pin name	I/O	Reset State	Function	pin name	I/O	function	pin name	I/O	function	pin name	I/O	function
40	P57/ EXI57/ TMCKI 7	I/O	Hi-Z output	Input-Output port/ External interrupt/ Timer clock input	OUTC LK	O	High-speed clock output	SSF0	I/O	SSIOF select input/output	TMOUTF	O	FTM output

1.3.3 Description of Pins

In the table below indicates the functional pin description.
The pin name represents the function pin name of the primary function of each terminal, The pin mode represents the set of mode register of Port Control.
(1st:primary function, 2nd:secondary function, 3rd: tertiary function, 4th: quartic function)

Pin name	I/O	Description	LSI pin name	Pin mode	Logic
System					
RESET_N	I	Reset input pin. When this pin is set to a "L" level, system reset mode is set and the internal section is initialized. When this pin is set to a "H" level subsequently, program execution starts. A pull-up resistor is internally connected.	RESET_N	–	L
XT0	I	Crystal connection pin for low-speed clock. Capacitors C_{DL} and C_{GL} are connected across this pin and V_{SS} as required.	PXT0	1st	–
XT1	O		PXT1	1st	–
LSCLKI	I	External clock input for Low-speed clock.	PXT1	1st	–
OSC0	I	Crystal/ceramic connection pin for high-speed clock (16 MHz max.). Capacitors C_{DH} and C_{GH} are connected across this pin and V_{ss}.	P10	1st	–
OSC1	O		P11	1st	–
CLKIN	I	External clock input for High-speed clock.	P11	1st	–
LSCLKO	O	Low-speed clock output pin.	P46,P56	2nd	–
OUTCLK	O	High-speed clock output pin.	P47,P57	2nd	–
General-purpose input/output port					
PXT0-PXT1	I	General-purpose input port(without pull-up/pull-down resister).	PXT0-PXT1	1st	–
P00-P05	I/O	General-purpose input/output port.	P00-P05	1st	–
P10-P11	I/O	General-purpose input/output port.	P10-P11	1st	–
P20-P23	I/O	General-purpose input/output port.	P20-P23	1st	–
P30-P37	I/O	General-purpose input/output port.	P30-P37	1st	–
P40-P47	I/O	General-purpose input/output port.	P40-P47	1st	–
P50-P57	I/O	General-purpose input/output port.	P50-P57	1st	–
External interrupt					
EXII0-EXII1 EXI00-05 EXI20-23 EXI30-37 EXI40-47 EXI50-57	I	External maskable interrupt input pins. It is possible, for each bit, to specify whether the interrupt is enabled and select the interrupt edge by software.	PXT0-PXT1 P00-P05 P20-P23 P30-P37 P40-P47 P50-P57	1st	H/L
LED					
LED	O	N-channel open drain output pins to drive LED.	P40,P41,P52,P53	1st	–
Melody/Buzzer					
MD0	O	Melody/buzzer signal output pin.	P33,P43,P53	2nd	H

Pin name	I/O	Description	LSI pin name	Pin mode	Logic
UART					
TXD0	O	UART0 data output pin.	P01,P31,P41,P51	4th	–
RXD0	I	UART0 data input pin.	P00,P30,P40,P50	4th	–
TXDF0	O	UART with FIFO data output pin.	P21,P35,P45,P55	4th	–
RXDF0	I	UART with FIFO data input pin.	P20,P34,P44,P54	4th	–
I^2C bus interface					
SDA0	I/O	I^2C0 data input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P30,P40,P50	2nd	–
SCL0	O	I^2C0 clock output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P31,P41,P51	2nd	–
SDA1	I/O	I^2C1 data input/output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P34,P44,P54	2nd	–
SCL1	O	I^2C1 clock output pin. This pin has an NMOS open drain output. When using this pin as a function of the I^2C, externally connect a pull-up resistor.	P35,P45,P55	2nd	–
Synchronous serial					
SCK0	I/O	Synchronous serial(SSIO) clock input/output pin.	P02,P32,P42,P52	3rd	–
SIN0	I	Synchronous serial(SSIO) data input pin.	P01,P31,P41,P51	3rd	–
SOUT0	O	Synchronous serial(SSIO) data output pin.	P00,P30,P40,P50	3rd	–
SCKF0	I/O	Synchronous serial with FIFO(SSIOF) clock input/output pin.	P22,P36,P46,P56	3rd	–
SINF0	I	Synchronous serial with FIFO(SSIOF) data input pin.	P21,P35,P45,P55	3rd	–
SOUTF0	O	Synchronous serial with FIFO(SSIOF) data output pin.	P20,P34,P44,P54	3rd	–
SSF0	I/O	Synchronous serial with FIFO(SSIOF) select input/output pin.	P23,P37,P47,P57	3rd	L
FTM					
TMOUT0-9 TMOUTA-F	O	FTM output pin.	P02,P03,P22,P23 P32,P33,P36,P37 P42,P43,P46,P47 P52,P53,P56,P57	4th	–
TMCKI0-7	I	External clock input pin for Timer	P42,P43,P46,P47 P52,P53,P56,P57	1st	–
RC oscillation type A/D converter					
IN0	I	Channel 0 oscillation input pin.	P00	2nd	–
CS0	O	Channel 0 reference capacitor connection pin.	P01	2nd	–
RS0	O	Reference resistor connection pin of Channel 0.	P03	2nd	–
RT0	O	Resistor sensor connection pin of Channel 0 for measurement.	P04	2nd	–
RCT0	O	Resistor/capacitor sensor connection pin of Channel 0 for measurement.	P02	2nd	–
RCM	O	RC oscillation monitor pin.	P05	2nd	–
IN1	I	Oscillation input pin of Channel 1.	P20	2nd	–
CS1	O	Reference capacitor connection pin of Channel 1.	P21	2nd	–
RS1	O	Reference resistor connection pin of Channel 1.	P22	2nd	–
RT1	O	Resistor sensor connection pin for measurement of Channel 1.	P23	2nd	–

Pin name	I/O	Description	LSI pin name	Pin mode	Logic
Successive approximation type A/D converter					
V_{REF}	I	Reference power supply pin for successive approximation type A/D converter.	V_{REF}	–	–
AIN0-11	I	Analog input for successive approximation type A/D converter.	(AIN0-3) P34-37, (AIN4-7) P20-23, (AIN8-11) P00-03	1st	–
Analog comparator					
CMP0P	I	Comparator0 Non-inverted input pin.	P30	1st	–
CMP0M	I	Comparator0 Inverted input pin.	P31	1st	–
CMP1P	I	Comparator1 Non-inverted input pin.	P32	1st	–
CMP1M	I	Comparator1 Inverted input pin.	P33	1st	–
For testing					
TEST0	I/O	Input/output pin for testing. A pull-down resistor is internally connected.	TEST0	–	–
TEST1_N	I	Input pin for testing. A pull-up resistor is internally connected.	TEST1_N	–	–
Power supply					
V_{SS}	–	Negative power supply pin.	V_{SS}	–	–
V_{DD}	–	Positive power supply pin.	V_{DD}	–	–
V_{DDL}	–	Positive power supply pin (internally generated) for internal logic. Capacitors C_{L0} and C_{L1} are connected between this pin and V_{SS}.	V_{DDL}	–	–
V_{DDX}	–	Positive power supply pin (internally generated) for internal oscillation. Capacitor C_{X1} is connected between this pin and V_{SS}.	V_{DDX}	–	–

1.3.4 Termination of Unused Pins

Table 1-1 shows methods of terminating the unused pins.

Table 1-1 Termination of Unused Pins

Pin	Recommended pin termination
RESET_N	Connect to V_{DD}
TEST0	open
TEST1_N	Connect to V_{DD}
V_{REF}	Connect to V_{DD}
P00 to P05	open
PXT0 to PXT1	open
P10 to P11	open
P20 to P23	open
P30 to P37	open
P40 to P47	open
P50 to P57	open

[Note]
For unused input ports or unused input/output ports, if the corresponding pins are configured as high-impedance inputs and left open, the supply current may become excessively large. Therefore, it is recommended to configure those pins as either inputs with a pull-down resistor/pull-up resistor or outputs.

Chapter 2

CPU and Memory Space

2. CPU and Memory Space

2.1 General Description

The CPU nX-U16/100 is capable of efficient instruction execution in 1-intruction 1-clock mode by 3-stage pipeline architecture parallel processing. It can also perform multiplication/division and multiply-accumulate operation by a coprocessor.

2.1.1 Features

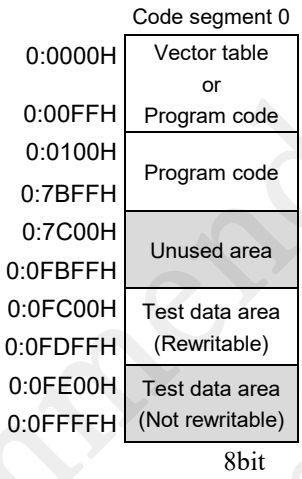
- 16-bit RISC CPU (CPU name: nX-U16/100)
- Instruction system: 16-bit length instruction
- Instruction set: Transfer, arithmetic operations, comparison, logic operations, multiplication/division, bit manipulations, bit logic operations, jump, conditional jump, call return stack manipulations, arithmetic shift, and so on
- Built in On-chip debug function
- Minimum instruction execution time
  30.5µs (@32.768kHz system clock)
  62.5ns (@16MHz system clock)
- Multiplication/division coprocessor mounted

2.1.2 Notes When Executing SB/RB Instruction

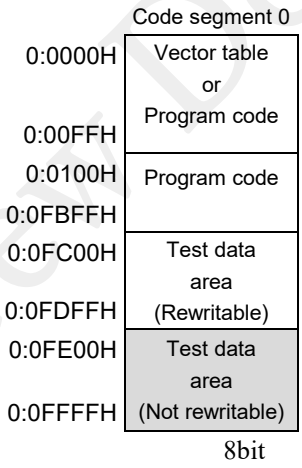
The bit manipulation SB/RB instruction reads in bytes from a register containing the target bits, generates the byte data while rewriting only the values of the target bits, then writes it in bytes.
If an SB/RB instruction is executed to a register where multiple bits are placed, bits not targeted for the SB/RB instruction are rewritten with the values read at that time.
Note that the SB/RB instruction may rewrite the state of bits not targeted for the SB/RB instruction if it is executed to a register where values of some bits change depending on the hardware state.

2.2 Program Memory Space

The program memory space stores program codes or vector tables.
The program codes have a length of 16 bits and are specified by a 16-bit program counter (PC).
The program memory space is configured by 32K words (64Kbytes) as one segment (code segment).
The vector table defines the entry address of the program executed at reset and interrupt and is placed in the segment 0's 0H to 0FEH.
The program memory space capacity determines the memory model. The ML620Q503H and ML620Q504H having a program memory space of 64Kbytes supports the small model. For details of memory model, see "nX-U16/100
Core Instruction Manual".
Figures 2-1 show the configuration of the program memory space.



(a) ML620Q503H Configuration of Program Memory Space



(b) ML620Q504H Configuration of Program Memory Space

Figure 2-1 Configuration of Program Memory Space

[Note]
- A program code cannot be placed in the test data area (1KB).
  When rewriting the content of program memory space, ensure to write "0FFH" in the test data area. If data in the area is uncertain or other data (i.e. not 0FFH), operating with the code cannot be guaranteed.
- It is recommended that the "0FFH" data (BRK instruction) is set in the unused area of the program memory space as a fail-safe.

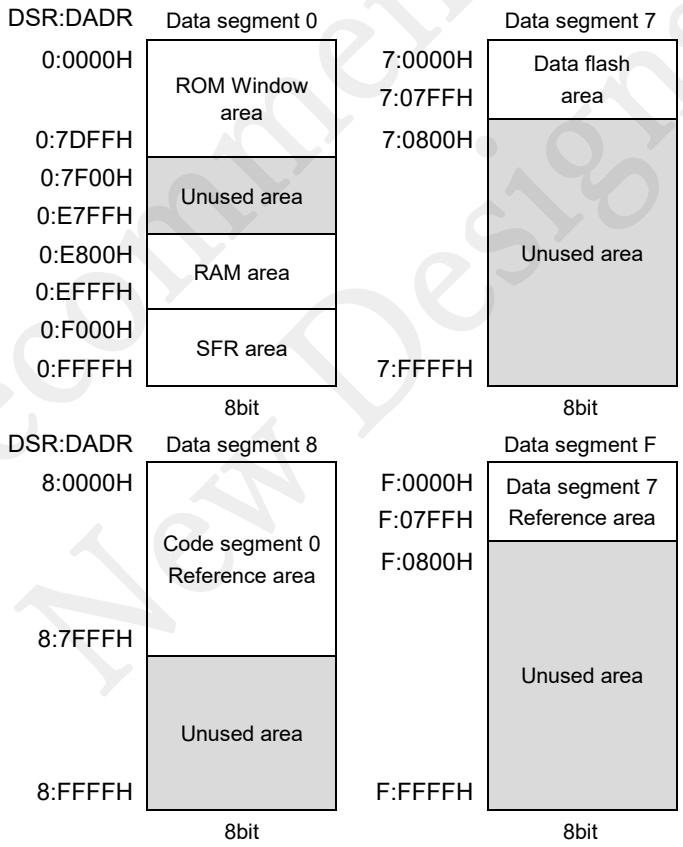
2.3 Data Memory Space

The data memory space consists of the segment 0 for the ROM window area, RAM area, and SFR area, the segments 7 and F for the flash data area, and the segments 1, 8, and 9 for the ROM reference area.
The data memory space is configured by 32K words (64Kbytes) as one segment (data segment).

The ROM window area is a window opened in the ROM area for the ROM area data to be accessed using the RAM addressing. The same address data in the program memory space can be read through this window.
In the SFR area, the special function registers (SFRs) that control the LSI function block operations are placed.
In the flash data area, the Flash memory is placed which is readable and writable as data area.
For writing to this area, see Chapter 27, "Flash Memory Control".
Note that the flash data area cannot be operated as program memory.

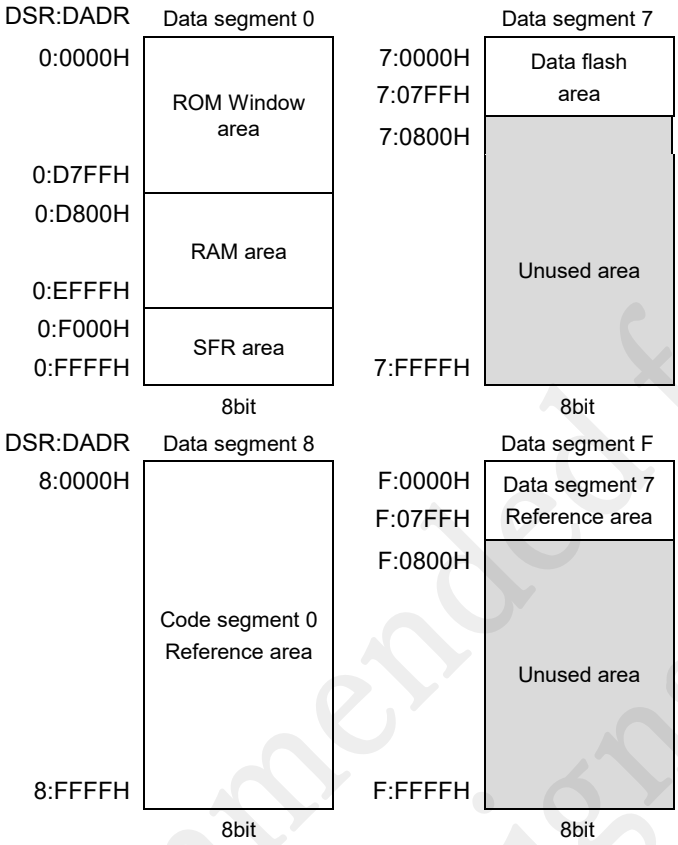
The data memory stores 8-bit data and is specified by 20 bits consisting of higher 4 bits as DSR and lower 16 bits as addressing specified by each instruction.
Figure 2-3 shows the configuration of the data memory space.

[Note]
The contents of the RAM area are undefined at power-on and system reset. Initialization of this area by software is required.



* Segments 1 to 6 and 9 to E are unused areas.

(a) ML620Q503H



* Segments 1 to 6 and 9 to E are unused areas.

(b) ML620Q504H

Figure 2-2 Configuration of the data memory space

2.4 Instruction Length

The length of an instruction is 16 bits.

2.5 Data Type

Data type of byte (8 bits) and word (16 bits) are supported.

2.6 Description of Registers

2.6.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F000	Data segment register	DSR	–	R/W	8	00

2.6.2 Data Segment Register (DSR)

Address: 0F000H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
DSR	–	–	–	–	DSR3	DSR2	DSR1	DSR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

DSR is a special function register (SFR) used to retain a data segment.
For details of DSR, see "nX-U16/100 Core Instruction Manual".

Description of Bits

- **DSR3-0** (bits 3 to 0)

DSR3	DSR2	DSR1	DSR0	Description
0	0	0	0	Data segment 0 (initial value)
0	0	0	1	Data segment 1
0	0	1	0	Data segment 2
0	0	1	1	Data segment 3
0	1	0	0	Data segment 4
0	1	0	1	Data segment 5
0	1	1	0	Data segment 6
0	1	1	1	Data segment 7
1	0	0	0	Data segment 8
1	0	0	1	Data segment 9
1	0	1	0	Data segment A
1	0	1	1	Data segment B
1	1	0	0	Data segment C
1	1	0	1	Data segment D
1	1	1	0	Data segment E
1	1	1	1	Data segment F

2.7 Multiplication/Division Coprocessor

2.7.1 General Description

This LSI has the built-in multiplication/division function as a coprocessor of the CPU nX-U16/100.
For the coprocessor instructions, see "nX-U16/100 Core Instruction Manual".
For the multiplication/division library including the routines that carry out operations using this function, see "MULDIVU8LIB User's Manual".

- Signed or unsigned operation setting
- Multiplication: 16bit x 16bit (operation time 4 cycles)
- Division: 32bit / 16bit (operation time 8 cycles)
- Division: 32bit / 32bit (operation time 16 cycles)
- Multiply-accumulate (non-saturating): 16bit x 16bit + 32bit (operation time 4 cycles)
- Multiply-accumulate (saturating): 16bit x 16bit + 32bit (operation time 4 cycles)
- In a saturating multiply-accumulate operation, the result is fixed to 7FFF_FFFFH for a positive number and 8000_0000H for a negative number when it is out of the expressible range.

2.7.2 List of Registers

These are byte type registers for carrying out operations.
Though the registers are in byte length, consecutive registers can be accessed as a word type register (ERn), double word type register (XRn), or quad type register (QRn) by combining them using different addressing modes.

Name	Symbol (Quad-Word)	Symbol (Double-Word)	Symbol (Word)	Symbol (Byte)	R/W	Size	Initial value [H]
A register L	CQR0	CXR0	CER0	CR0	R/W	8	00
A register H				CR1	R/W	8	00
B register L			CER2	CR2	R/W	8	00
B register H				CR3	R/W	8	00
C register L		CXR4	CER4	CR4	R/W	8	00
C register H				CR5	R/W	8	00
D register L			CER6	CR6	R/W	8	00
D register H				CR7	R/W	8	00
Operation mode register	CQR8	CXR8	CER8	CR8	R/W	8	00
Operation status register				CR9	R/W	8	00
–			CER10	CR10	-	-	00
–				CR11	-	-	00
–		CXR12	CER12	CR12	-	-	00
–				CR13	-	-	00
–			CER14	CR14	-	-	00
Coprocessor ID register				CR15	R	8	81

CR10 to CR14 have no function. Reading them gives "00H". Writing is ignored.

2.7.2.1 Registers A, B, C, and D (CR0 to CR7)

Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
CR0	AREG7	AREG6	AREG5	AREG4	AREG3	AREG2	AREG1	AREG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
CR1	AREG15	AREG14	AREG13	AREG12	AREG11	AREG10	AREG9	AREG8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
CR2	BREG7	BREG6	BREG5	BREG4	BREG3	BREG2	BREG1	BREG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
CR3	BREG15	BREG14	BREG13	BREG12	BREG11	BREG10	BREG9	BREG8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
CR4	CREG7	CREG6	CREG5	CREG4	CREG3	CREG2	CREG1	CREG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
CR5	CREG15	CREG14	CREG13	CREG12	CREG11	CREG10	CREG9	CREG8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	7	6	5	4	3	2	1	0
CR6	DREG7	DREG6	DREG5	DREG4	DREG3	DREG2	DREG1	DREG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0
	15	14	13	12	11	10	9	8
CR7	DREG15	DREG14	DREG13	DREG12	DREG11	DREG10	DREG9	DREG8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

Registers A to D (CR0 to CR7) store the operation input values and results.
The bit symbol cannot be used in the program.

2.7.2.2 Operation Mode Register (CR8)

Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CR8	CLEN	–	–	SIGN	–	CLMOD2	CLMOD1	CLMOD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The operation mode register sets the operation mode.
The bit symbol cannot be used in the program.

Description of Bits

- **CLMOD2-0** (bits 2 to 0)
  The CLMOD2-0 bits are used to select the operation mode. The mode can be selected from multiplication, division, multiply-accumulate (non-saturating) and multiply-accumulate (saturating).

CLMOD2	CLMOD1	CLMOD0	Description	
0	0	0	Multiplication (initial value)	16bit * 16bit
0	0	1	Division	32bit / 16bit
0	1	0	Multiply-accumulate (non-saturating)	16bit * 16bit + 32bit
0	1	1	Multiply-accumulate (saturating)	16bit * 16bit + 32bit
1	0	0	Reserved	
1	0	1	Division	32bit / 32bit
1	1	*	Reserved	

- **SIGN** (bit 4)
  SIGN is a bit to set the sign operation.

SIGN	Description
0	Unsigned operation (initial value)
1	Signed operation

- **CLEN** (bit 7)
  CLEN is a bit to set whether or not to enable the operation.

CLEN	Description
0	Operation prohibited (initial value)
1	Operation enabled

* Operation does not start unless CLEN is set to "1".
Also, if CLEN is cleared to "0" during an operation, the next operation does not start after that operation ends.

2.7.2.3 Operation Status Register (CR9)

Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CR9	C	Z	S	OV	Q	–	–	USE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Initial value	0	0	0	0	0	0	0	0

The operation status register stores the state of an operation execution result.
The bit symbol cannot be used in the program.

- **USE** (bit 0)
  USE is the status bit that indicates an ongoing operation.

USE	Description
0	Operation stopped (initial value)
1	Operating

- **Q** (bit 3)
  This becomes "1" for the saturated result of a saturating multiply-accumulate operation. The value is held in the next operation. To reset it to "0", "0" needs to be written.

- **OV** (bit 4)
  This becomes "1" if the operation result exceeds the range expressible by two's complement. This is set for each operation.
  Also, a value can be written.

- **S** (bit 5)
  This becomes "1" if the operation result is a negative number. For a multiply-accumulate (non-saturating/saturating) operation, this indicates the state of the most significant bit in the operation result. The value is set for each operation. Also, a value can be written.

- **Z** (bit 6)
  This becomes "1" if the operation result is 0. The value is set for each operation. Also, a value can be written.

- **C** (bit 7)
  This becomes "1" if the operation result is carried or the divisor is 0 in the division mode. The value is set for each operation. Also, a value can be written.

The flags changes during each operation as follows:

Operation mode	SIGN	C	Z	S	OV	Q
Multiplication	0	-	*	-	-	-
	1	-	*	*	-	-
Division	0	*	*	-	-	-
	1	*	*	*	*	-
Multiply-accumulate (non-saturating)	0	*	*	*	*	-
	1	*	*	*	*	-
Multiply-accumulate (saturating)	0	*	*	*	*	*
	1	*	*	*	*	*

*: Changes according to the result. -: No change.

2.7.2.4 Coprocessor ID Register (CR15)

Access: R
Access size: 8 bits
Initial value: 81H

	7	6	5	4	3	2	1	0
CR15	COPID7	COPID6	COPID5	COPID4	COPID3	COPID2	COPID1	COPID0
R/W	R	R	R	R	R	R	R	R
Initial value	1	0	0	0	0	0	0	1

The coprocessor ID register is the coprocessor register that indicates the coprocessor ID. The bit symbol cannot be used in the program.

2.7.3 Description of Operation

When using the multiplication/division function, see "MULDIVU8LIB User's Manual" for the available multiplication/division library.

The following example shows a program for multiplication without using the library.

; 0x1234H × 0x0AA55H multiplication example

```
MOV     R2    ,#55H     ; Set the multiplier
MOV     R3    ,#0AAH    ;
MOV     R0    ,#34H     ; Set the multiplicand
MOV     R1    ,#12H     ;
MOV     CR4   ,R0       ; Transfer the multiplier [7:0]
MOV     R0    ,#90H     ; Set the operation mode
MOV     CR8   ,R0       ; Set the signed operation mode
MOV     CR5   ,R1       ; Transfer the multiplier [15:8]
MOV     CR6   ,R2       ; Transfer the multiplicand [7:0]
MOV     CR7   ,R3       ; Transfer the multiplicand [15:8] and start the operation
NOP                     ; Operating. Waiting for end of operation (1 clock)
BAL   READ              ; Operating. Waiting for end of operation. Unconditionally branch to next
                                instruction (3 clocks)
;End of operation
READ:
MOV     R0    ,CR0      ; Transfer the product [7:0]
MOV     R1    ,CR1      ; Transfer the product [15:8]
MOV     R2    ,CR2      ; Transfer the product [23:16]
MOV     R3    ,CR3      ; Transfer the product [31:24]
```

Chapter 3

Reset Function

3 Reset Function

3.1 Overview

This LSI has the six reset functions shown below. If any of the six reset conditions is satisfied, this LSI enters system reset mode.

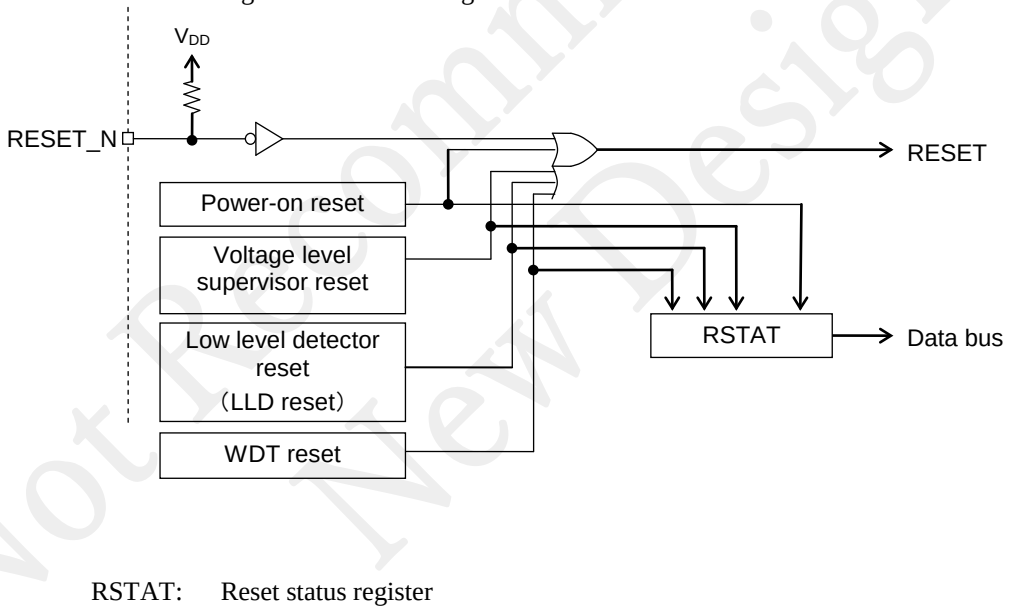
- Reset by the RESET_N pin
- Reset by power-on detection
- Reset by the 2nd overflow of watchdog timer (WDT)
- Reset by Voltage Level Supervisor(VLS)
- Reset by Low Level Detector(LLD)
- Software reset by execution of the BRK instruction

3.1.1 Features

- The RESER_N pin has an internal pull-up resistor
- 125 ms, 1 500ms, 2 sec, or 8 sec can be selected as the watchdog timer (WDT) overflow period when LSCLK=32.768 kHz)
- Built-in reset status register (RSTAT) indicating the reset generation causes
- Only the CPU is reset by the BRK instruction (neither the RAM area nor the SFR area are reset).

3.1.2 Configuration

Figure 3-1 shows the configuration of the reset generation circuit.



RSTAT: Reset status register

Figure 3-1 Configuration of Reset Generation Circuit

3.1.3 List of Pin

Pin name	I/O	Description
RESET_N	I	Reset input pin

3.2 Description of Registers

3.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F00C	Reset status register	RSTAT	–	R/W	8	–

3.2.2 Reset Status Register (RSTAT)

Address: 0F00CH
Access: R/W
Access size: 8 bits
Initial value: Undefined

	7	6	5	4	3	2	1	0
RSTAT	–	–	–	LLDR	VLSR	WDTR	–	POR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	x	x	x	0	x

*)The initial value depends on the reset factor

RSTAT is a special function register (SFR) that indicates the causes set to the system reset mode.
At the occurrence of reset, the contents of RSTAT are not initialized, while the bit indicating the cause of the reset is set to "1". When checking the reset cause using this function, perform write operation to RSTAT in advance and initialize the each reset cause flag of RSTAT to "0".

Description of Bits

- **POR** (bit 0)
  The POR bit is a flag that indicates that the power-on reset is generated. This bit is set to "1" when powered on.

POR	Description
0	Power-on reset not occurred
1	Power-on reset occurred

- **WDTR** (bit 2)
  The WDTR is a flag that indicates that the watchdog timer reset is generated. This bit is set to "1" when the reset by overflow of the watchdog timer is generated.

WDTR	Description
0	Watchdog timer reset not occurred
1	Watchdog timer reset occurred

- **VLSR** (bit 3)

The VLSR is a flag that indicates that the Voltage Level Supervisor reset is generated. This bit is set to "1" when the reset by overflow of the Voltage Level Supervisor generated. Also, the bit is undefined when the power is turned on.

VLSR	Description
0	Voltage Level Supervisor reset not occurred
1	Voltage Level Supervisor reset occurred

- **LLDR** (bit 4)
  The LLDR is a flag that indicates that the Low Level Detector reset is generated. This bit is set to "1" when the reset by overflow of the Lowe Level Detector is generated. Also, the bit is undefined when the power is turned on..

LLDR	Description
0	Low Level Detector reset not occurred
1	Low Level Detector reset occurred

[Note]
No flag is provided that indicates the occurrence of reset by the RESET_N pin.

3.3 Description of Operation

3.3.1 Cause of Reset

This LSI can be reset by hard reset from LSI pin, Software reset by BRK instruction, and LSI internal status.

- Reset by the RESET_N pin
  System Reset occur when "0" is input to RESET_N. The contents of reset status register(RSTAT) is not changed at system reset mode set.

- Software reset by execution of the BRK instruction
  System Reset by software. Only CPU is reset. RAM area and SFR area are not reset.
  The contents of reset status register(RSTAT) is not changed at system reset mode set by BRK instruction.

- Reset by power-on detection
  System reset occur when LSI is powered on. Reset status register(RSTAT) POR bit becomes "1" at system reset mode set by Power-on detection.

- Reset by the 2nd overflow of watchdog timer (WDT)
  System reset occur by WDT 2nd over flow.
  Please refer to the" Chapter 10 Watch dog timer" for detail of the functionality.
  Reset status register(RSTAT) WDTR bit becomes "1" at system reset occurred by WDT over flow,

- Reset by Voltage Level Supervisor(VLS)
  System reset occur when Power supply Voltage falls than threshold.
  VLS reset is disabled initially. Need to set Voltage Level Supervisor mode register VLSSEL0 bit "1" to enable VLS function.
  Please refer to the "Chapter 28 VLS circuit" for detail of the functionality.
  Reset status register(RSTAT) VLSR bit becomes "1" at system reset occurred by VLS.

- Reset by Low Level Detector(LLD)
  System reset occur when Power supply Voltage falls than threshold(1.8V Typ) LLD reset this LSI.
  LDD function is disabled initially. Need to set block control register 45 (BLKCON45) DLLD bit "0" to enable LLD function.
  Reset status register(RSTAT) LLDR bit becomes "1" at system reset occurred by LLD.

3.3.2 Operation of System Reset Mode

System reset has the highest priority among all the processing and any other processing being executed up to then is cancelled.
In system reset mode, the following processing is performed.

(1) The power circuit is initialized, however it is not initialized by the software reset by the BRK instruction execution.
(2) All the special function registers (SFRs) whose initial value is not undefined are initialized.
  however it is not initialized by the software reset by the BRK instruction execution. See Appendix A "Registers" for the initial values of the SFRs.
(3) CPU is initialized.
  - All the registers in CPU are initialized.
  - The contents of addresses 0000H and 0001H in the program memory are set to the stack pointer (SP).
  - The contents of addresses 0002H and 0003H in the program memory are set to the program counter (PC). However, when the interrupt level (ELEVEL) of the program status word (PSW) at reset by the BRK instruction is 1 or lower, the contents of addresses 0004H and 0005H of the program memory are set in the program counter (PC). For the BRK instruction, see "nX-U16/100 Core Instruction Manual".

[Note]
In system reset mode, the contents of data memory and those of any SFR whose initial value is undefined are not initialized and are undefined. Initialize them by software.
In system reset mode by the BRK instruction, no special function register (SFR) that has a fixed initial value is initialized either. Therefore initialize such an SFR by software.

The cause that shifted to System reset mode and the internal status of LSI are as below.

Initialize item／cause	RESET_N	POR	WDT	VLS	LLD	BRK instruction
SFR	O	O	O	O	O	X
CPU	O	O	O	O	O	O
Data memory	X	X	X	X	X	X
VLS enable *1	O	O	O	X	O	O
LLD enable *1	O	O	O	O	X	O

*1 VLS enable, LLD enable : enable/disable each function.
Initially, each items are set as disable. When reset occur by each causes, keep a status before reset occur.

Chapter 4

Power Management

4 Power Management

4.1 General Description

The LSI has four power management modes listed below to save the Power consumption.
It also has a block control function, which power downs the circuits of unused peripherals (reset registers and stop clock supplies) to make even more reducing the current consumption.

(1) HALT mode
(2) HALT-H mode
(3) DEEP-HALT mode
(4) STOP mode

4.1.1 Features

- HALT mode, where the CPU stops operating and only the peripheral circuit is operating
- HALT-H mode, where the high-speed clock is automatically stopped when the CPU stops operating.
- DEEP-HALT mode, where the CPU stops operating and only LTBC ,timer, VLS, LLD, and Analog Comparator can operate at lower power consumption
- STOP mode, where both low-speed oscillation and high-speed oscillation stop
- Stop code acceptor function, which controls transition to STOP mode
- Block control function, which power downs the circuits of unused function blocks (reset registers and stop clock supplies)

4.1.2 Configuration

Figure 4-1 shows an operating state transition diagram.

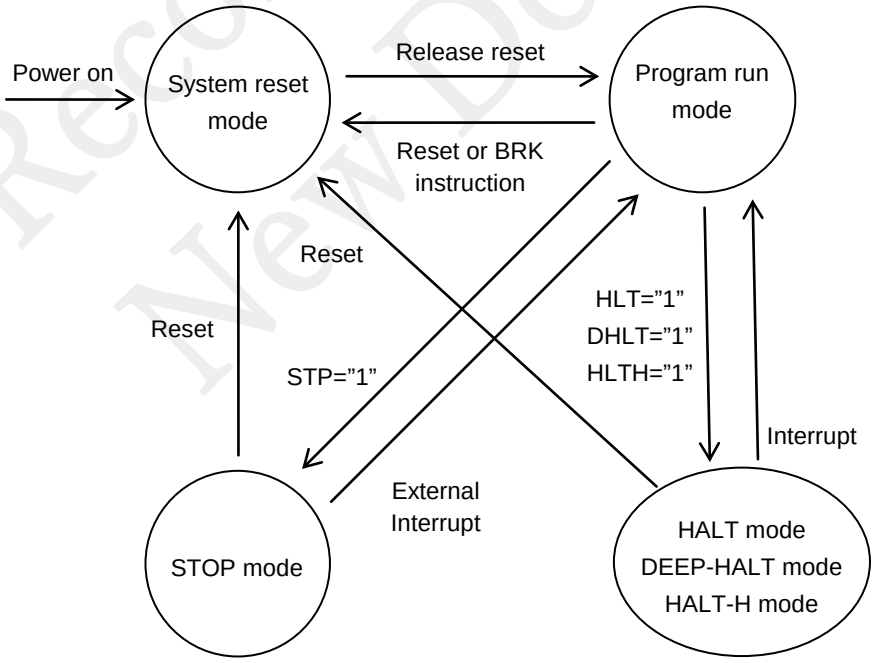


Figure 4-1 Operating State Transition Diagram

4.2 Description of Registers

4.2.1 Register Configuration List

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F008	Stop code acceptor	STPACP	–	W	8	–
0F009	Standby control register	SBYCON	–	W	8	00
0F068	Block control register 01	BLKCON0	BLKCON01	R/W	8/16	00
0F069		BLKCON1		R/W	8	00
0F06A	Block control register 23	BLKCON2	BLKCON23	R/W	8/16	00
0F06B		BLKCON3		R/W	8	00
0F06C	Block control register 45	BLKCON4	BLKCON45	R/W	8/16	00
0F06D		BLKCON5		R/W	8	04

4.2.2 Stop Code Acceptor (STPACP)

Address: 0F008H
Access: W
Access size: 8 bits
Initial value: -(Undefined)

	7	6	5	4	3	2	1	0
STPACP	–	–	–	–	–	–	–	–
R/W	W	W	W	W	W	W	W	W
Initial value	-	-	-	-	-	-	-	-

STPACP is a write-only special function register (SFR) that is used for setting a STOP mode.
When STPACP is read, “00H” is read.
When data is written to STPACP in the order of “5nH” and “0AnH” (where n is 0 to 0FH), the stop code acceptor is enabled. When the STP bit of the standby control register (SBYCON) is set to “1” in this state, the mode is changed to the STOP mode. When the STOP mode is set, the STOP code acceptor is disabled.
When another instruction is executed between the instruction that writes “5nH” to STPACP and the instruction that writes “0AnH”, the stop code acceptor is enabled after “0AnH” is written. Note that, if data other than “0AnH” is written to STPACP after “5nH” is written, the “5nH” writing process becomes invalid and “5nH” should be written again.
During a system reset, the stop code acceptor is disabled.

[Note]
•The stop code acceptor cannot be enabled on the condition that any interrupt enable flag and the corresponding interrupt request flag are both “1” (for example, an interrupt request occurs when the MIE flag is ”0”).
• The stop code acceptor is disabled on the condition that any interrupt enable flag and the corresponding interrupt request flag are both “1” after the stop code acceptor is enabled.

4.2.3 Standby Control Register (SBYCON)

Address: 0F009H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SBYCON	–	–	–	–	HLTH	DHLT	STP	HLT
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

SBYCON is a special function register (SFR) to control the operation mode of MCU.

Description of Bits

- **HLT** (bit 0)
  The HLT bit is used for setting the HALT mode. When the HLT bit is set to "1", the mode is changed to the HALT mode. Writing "0" to the HLT bit does not change the mode to the HALT mode.

- **STP** (bit 1)
  The STP bit is used for setting the STOP mode. When the STP bit is set to "1", the mode is changed to the STOP mode. Writing "0" to the STP bit does not change the mode to the STOP mode.
  Writing to the STP bit should be performed when the stop code acceptor is enabled by using STPACP. If writing to the STP bit is performed when the stop code acceptor is disabled, the writing becomes invalid.

- **DHLT** (bit 2)
  The DHLT bit is used for setting the DEEP-HALT mode. When the DHLT bit is set to "1", the mode is changed to the DEEP-HALT mode. Writing "0" to the DHLT bit does not change the mode to the DEEP-HALT mode.

- **HLTH** (bit 3)
  The HLTH bit is used for setting the HALT-H mode. When the HLTH bit is set to "1", the high-speed clock is stopped by the hardware and the mode is changed to the HALT-H mode. Writing "0" to the HLTH bit does not change the mode to the HALT-H mode.

  Plural these bits cannot be set to "1" at the same time.

[Note]
• When High speed oscillator is used and the mode switch to STOP, DEEP-HALT, or HALT-H mode , Frequency Status Register (FSTAT) HOSCS bit must be "0".
• When Low speed oscillator is used and the mode switch to DEEP-HALT mode, Frequency Status Register (FSTAT) LOSCS bit must be "0".
•The mode is not changed to the STOP mode, HALT mode, HALT-H mode , or DEEP-HALT mode on the condition that any interrupt enable flag and the corresponding interrupt request flag are both "1" (for example, an interrupt request occurs when the MIE flag is "0").
•When a maskable interrupt source (interrupt with enable bit) occurs while the MIE flag of the program status word (PSW) in the nX-U16/100 core is "0", the STOP mode, HALT mode, HALT-H mode , and DEEP-HALT mode are simply released and interrupt processing is not performed. For details of PSW, see "nX-U16/100 Core Instruction Manual".
•Since up to two instructions are executed during the period between each mode release and a transition to interrupt processing, place two NOP instructions next to the instruction that sets the each bit to "1".

4.2.4 Block Control Register 01 (BLKCON01)

Address: 0F068H
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
BLKCON0	DTM7	DTM6	DTM5	DTM4	DTM3	DTM2	DTM1	DTM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
BLKCON1	–	–	–	–	DFTM3	DFTM2	DFTM1	DFTM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON01 is a special function register (SFR) to control each block operation.

Description of Bits

- **DTM7-0** (bits 7 to 0)
  The DTM7-0 bits are used to control the 8-bit timer operation.

DTM0	Description
0	Enable operating the timer 0 (initial value)
1	Disable operating the timer 0

DTM1	Description
0	Enable operating the timer 1 (initial value)
1	Disable operating the timer 1

DTM2	Description
0	Enable operating the timer 2 (initial value)
1	Disable operating the timer 2

DTM3	Description
0	Enable operating the timer 3 (initial value)
1	Disable operating the timer 3

DTM4	Description
0	Enable operating the timer 4 (initial value)
1	Disable operating the timer 4

DTM5	Description
0	Enable operating the timer 5 (initial value)
1	Disable operating the timer 5

DTM6	Description
0	Enable operating the timer 6 (initial value)
1	Disable operating the timer 6

DTM7	Description
0	Enable operating the timer 7 (initial value)
1	Disable operating the timer 7

- **DFTM3-0** (bits 11 to 8)
  The DFTM3-0 bits are used to control the operation of multi-function timer(FTM).

DFTM0	Description
0	Enable operating the FTM 0 (initial value)
1	Disable operating the FTM 0

DFTM1	Description
0	Enable operating the FTM1 (initial value)
1	Disable operating the FTM 1

DFTM2	Description
0	Enable operating the FTM 2 (initial value)
1	Disable operating the FTM 2

DFTM3	Description
0	Enable operating the FTM 3 (initial value)
1	Disable operating the FTM 3

[Note]

•When any flag is set to "1" (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to that block stops. While the flag is set to "1", the writing to the registers of the block becomes invalid. To use the function of the block, reset the applicable flag of the block control register to "0" (enable operation).

4.2.5 Block Control Register 23 (BLKCON23)

Address: 0F06AH
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
BLKCON2	DI2C1	DI2C0	–	DUAF0	DUA1	DUA0	DSIOF0	DSIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
BLKCON3	DCMP1	DCMP0	–	–	–	–	–	DMD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

BLKCON23 is a special function register (SFR) to control each block operation.

Description of Bits

- **DSIO0** (bit 0)
  The DSIO0 bit is used to control the operation of the synchronous serial port operation.

DSIO0	Description
0	Enable operating the synchronous serial port 0 (initial value)
1	Disable operating the synchronous serial port 0

- **DSIOF0** (bit 1)
  The DSIOF0 bit is used to control the operation of the synchronous serial port operation with FIFO.

DSIOF0	Description
0	Enable operating the synchronous serial port 0 with FIFO (initial value)
1	Disable operating the synchronous serial port 0 with FIFO

- **DUA1-0** (bits 3 to 2)
  The DUA1-0 bits are used to control the UART0 operation.

DUA1	DUA0	Description
0	0	Enable operating UART0 (initial value)
0	1	Setting prohibited
1	0	Setting prohibited
1	1	Disable operating UART0

- **DUAF0**(bit 4)
  The DUAF0 bit is used to control the operation of UART with FIFO.

DUAF0	Description
0	Enable operating UART with FIFO (initial value)
1	Disable operating UART with FIFO

- **DI2C1-0** (bits 7 to 6)
  The DI2C1-0 bits are used to control the I^2C bus interface operation.

DI2C1	Description
0	Enable operating the I^2C bus interface 1 (initial value)
1	Disable operating the I^2C bus interface 1

DI2C0	Description
0	Enable operating the I^2C bus interface 0 (initial value)
1	Disable operating the I^2C bus interface 0

- **DMD0** (bit 8)
  The DMD0 bit is used to control the operation of the melody driver 0.

DMD0	Description
0	Enable operating the melody driver 0 (initial value)
1	Disable operating the melody driver 0

- **DCMP0** (bit 14)
  The DCMP0 bit is used to control the operation of the analog comparator 0.

DCMP0	Description
0	Enable operating the analog comparator 0 (initial value)
1	Disable operating the analog comparator 0

- **DCMP1** (bit 15)
  The DCMP1 bit is used to control the operation of the analog comparator 1.

DCMP1	Description
0	Enable operating the analog comparator 1 (initial value)
1	Disable operating the analog comparator 1

[Note]
•When any flag is set to "1" (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to that block stops. While the flag is set to "1", the writing to the registers of the block becomes invalid. To use the function of the block, reset the applicable flag of the block control register to "0" (enable operation).

4.2.6 Block Control Register 45 (BLKCON45)

Address: 0F06CH
Access: R/W
Access size: 8/16 bit
Initial value: 0400H

	7	6	5	4	3	2	1	0
BLKCON4	–	–	–	–	–	–	DRAD	DSAD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
BLKCON5	–	–	–	–	–	DLLD	DVLS	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	1	0	0

BLKCON45 is a special function register (SFR) to control each block operation.

Description of Bits

- **DSAD** (bit 0)
  The DSAD bit is used to control the successive approximation type (SA type) A/D converter operation.

DSAD	Description
0	Enable operating the SA type A/D converter (initial value)
1	Disable operating the SA type A/D converter

- **DRAD** (bit 1)
  The DRAD bit is used to control the RC oscillation type A/D converter operation.

DRAD	Description
0	Enable operating the RC oscillation type A/D converter (initial value)
1	Disable operating the RC oscillation type A/D converter

- **DVLS** (bit 9)
  The DVLS bit is used to control the operation of the power supply voltage detection circuit (VLS).

DVLS	Description
0	Enable operating VLS (initial value)
1	Disable operating VLS

- **DLLD** (bit 10)
  The DLLD bit is used to control the operation of the power supply voltage dropping detection circuit (LLD).

DLLD	Description
0	Enable operating LLD
1	Disable operating LLD (initial value)

[Note]

•When any flag is set to “1” (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to that block stops. While the flag is set to “1”, the writing to the registers of the block becomes invalid. To use the function of the block, reset the applicable flag of the block control register to “0” (enable operation).

4.3 Description of Operation

4.3.1 HALT Mode

4.3.1.1 HALT Mode

During the HALT mode, the CPU interrupts execution of instructions and only the peripheral circuits are running.
When the HLT bit of the standby control register (SBYCON) is set to "1", the mode changes to the HALT mode. When a WDT interrupt request, or an interrupt request enabled by an interrupt enable register (IE1 to IE7) is issued, the HLT bit is set to "0" on the falling edge of the next clock is selected as system clock (SYSCLK), the HALT mode is released, and the mode returns to the program run mode.
Figure 4-2 shows the operation waveforms in the HALT mode.

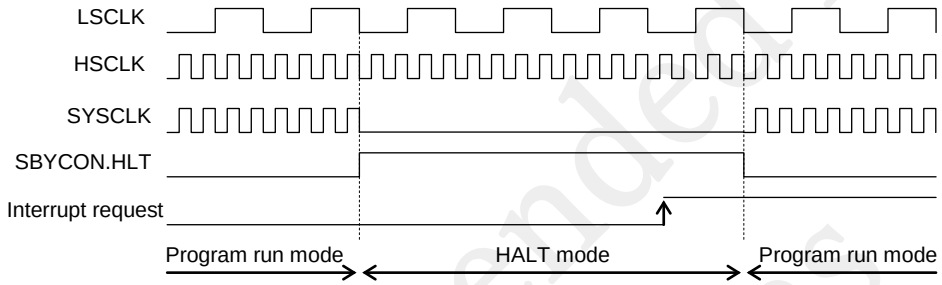


Figure 4-2(1) Operation Waveforms in HALT Mode (FCON1.SYSCLK=1, FCON1.ENOSC=1)

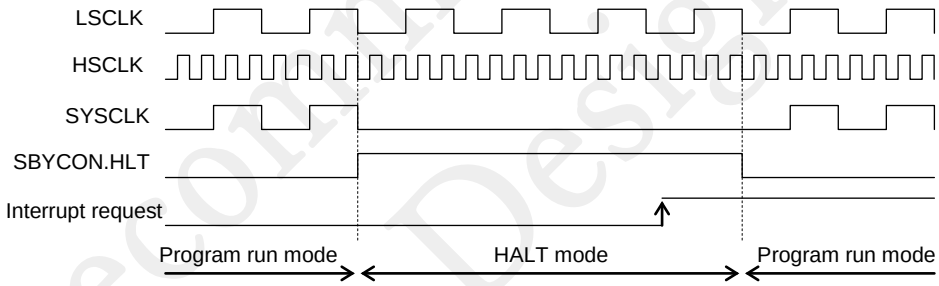


Figure 4-2(2) Operation Waveforms in HALT Mode (FCON1.SYSCLK=0, FCON1.ENOSC=1)

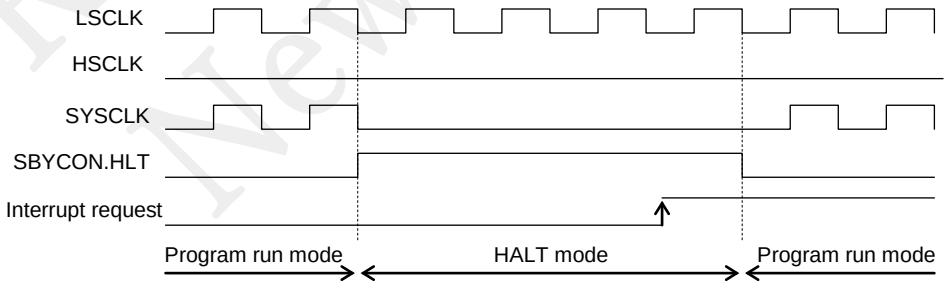


Figure 4-2(3) Operation Waveforms in HALT Mode (FCON1.SYSCLK=0, FCON1.ENOSC=0)

[Note]
•After release of the HALT mode, interrupts other than WDT interrupt start being processed if they are enabled ("1") by the MIE bit of PSW.
For details of PSW, refer to "nX-U16/100 Core Instruction Manual"
•Since up to two instructions are executed during the period between HALT mode release and a transition to interrupt processing, place two NOP instructions next to the instruction that sets the HLT bit to "1".

4.3.1.2 DEEP-HALT Mode

During the DEEP-HALT mode, the CPU interrupts execution of instructions, and the entire circuit stops operating except for some peripheral blocks such as watchdog timer and LTBC.
When the DHLT bit of the standby control register (SBYCON) is set to "1", the mode changes to the DEEP-HALT mode.
When a WDT interrupt request, or an enabled interrupt request (the interrupt enable flag is "1") is issued, the DHLT bit is set to "0" on the falling edge of the next system clock (SYSCLK), the DEEP-HALT mode is released, and the mode returns to the program run mode.
When the DHLT bit is set to "1" during operation with the high-speed clock, the clock switches to the low-speed clock and the mode changes to the DEEP-HALT mode. If a WDT interrupt request, or an enabled interrupt request (the interrupt enable flag is "1") is issued in this state, DHLT is set to "0", the mode returns to the program run mode, and the clock is switched to the high-speed clock again.

Restart of a high-speed clock is not related to the clock mode. When low-speed clock counts 29, after the interrupt request is generated, high-speed built-in RC oscillation starts oscillation. And the counts 512, as OSCLK clock supply. When a system clock is a high-speed clock, it returns to program operational mode simultaneously.
In the case of high-speed crystal oscillation mode, oscillation is started after high-speed oscillation start time (T_{XTH}) from LSCLK supply. And, OSCLK changes from RC oscillation into crystal oscillation by the automatically in case of the crystal oscillation counts 4096.
In the case of high-speed external clock mode, OSCLK changes from RC oscillation into external clock by the automatically in case of the external clock counts 128 from LSCLK supply.

Figure 4-3 shows the operation waveforms in the DEEP-HALT mode.

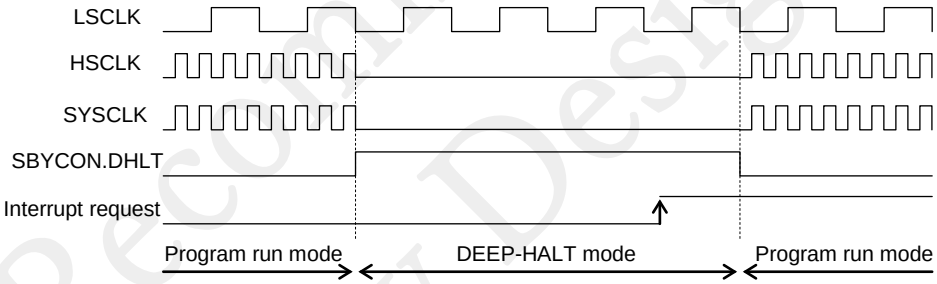


Figure 4-3 Operation Waveforms in DEEP-HALT Mode

[Note]
•When High speed crystal/ceramic oscillator is used and the mode switch to DEEP – HALT mode, Frequency Status Register (FSTAT) HOSCS bit must be "0".
•When Low speed crystal oscillator or external clock is used and the mode switch to DEEP – HALT mode, Frequency Status Register (FSTAT) LOSCS bit must be "0".
•After release of the DEEP-HALT mode, interrupts other than WDT interrupt start being processed if they are enabled ("1") by the MIE bit of PSW.
For details of PSW, refer to "nX-U16/100 Core Instruction Manual"
•Since up to two instructions are executed during the period between DEEP-HALT mode release and a transition to interrupt processing, place two NOP instructions next to the instruction that sets the DHLT bit to "1".

4.3.1.3 HALT-H Mode

During the HALT-H mode, the CPU interrupts execution of instructions, the high-speed clock is stopped, and only the peripheral circuits operate that can operate with the low-speed clock.
When the HLTH bit of the standby control register (SBYCON) is set to "1", the mode changes to the HALT-H mode.
When a WDT interrupt request, or an interrupt request enabled by an interrupt enable register (IE1 to IE7) is issued, the HLTH bit is set to "0" on the falling edge of the next system clock (SYSCLK), the HALT-H mode is released, and the mode returns to the program run mode.
When the HLTH bit is set to "1" during operation with the high-speed clock, the high-speed clock stops and the mode changes to the HALT-H mode. If a WDT interrupt request, or an enabled interrupt request (the interrupt enable flag is "1") is issued in this state, HLTH is set to "0", the high-speed clock restarts the operation, and the mode returns to the program run mode.

About restart of a high-speed clock, it is same as DEEP-HALT.

Figure 4-4 shows the operation waveforms when the mode is changed to the HALT-H mode during the high-speed clock operation.

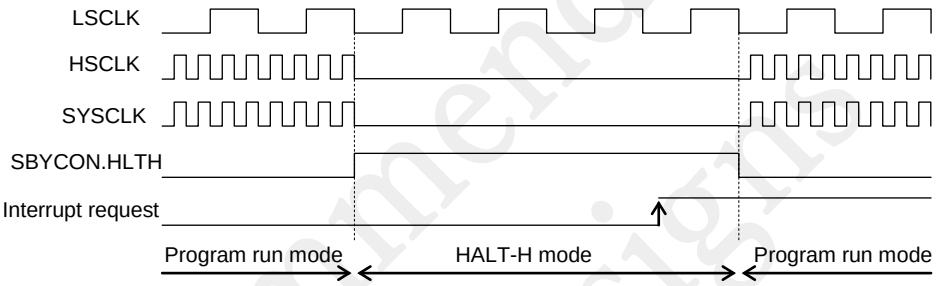


Figure 4-4 Operation Waveforms in HALT-H Mode

[Note]
•When the mode switch to HALT-H mode at High speed oscillator is used,
Frequency Status Register (FSTAT) HOSCS bit must be "0"..
•After release of the HALT-H mode, interrupts other than WDT interrupt start being processed if they are enabled ("1") by the MIE bit of PSW.
For details of PSW, refer to "nX-U16/100 Core Instruction Manual"
•Since up to two instructions are executed during the period between HALT-H mode release and a transition to interrupt processing, place two NOP instructions next to the instruction that sets the HLTH bit to "1".

4.3.2 STOP Mode

During the STOP mode, the low-speed oscillation and high-speed oscillation stop and the CPU and peripheral circuits stop the operation.
When the stop code acceptor is enabled by successively writing "5nH" and "0AnH" (where n is 0 to 0FH) to the stop code acceptor (STPACP) and the STP bit of the standby control register (SBYCON) is set to "1", the STOP mode is entered. When the STOP mode is set, the STOP code acceptor is disabled.
When an external pin interrupt request that is interrupt-enabled (the interrupt enable flag is "1") is issued, the STP bit is set to "0", the STOP mode is released, and the mode is returned to the program run mode.

[Note]
•When the mode switch to STOP mode at High speed oscillator is used,
Frequency Status Register (FSTAT) HOSCS bit must be "0".
•After release of the STOP mode, interrupts other than WDT interrupt start being processed if they are enabled ("1") by the MIE bit of PSW.
For details of PSW, refer to "nX-U16/100 Core Instruction Manual"
•Since up to two instructions are executed during the period between STOP mode release and a transition to interrupt processing, place two NOP instructions next to the instruction that sets the STP bit to "1".

4.3.2.1 Oscillation Stop and Restart Timing of Low-Speed Clock

When the stop code acceptor is in the enabled state and the STP bit of SBYCON is set to "1", the STOP mode is entered, stopping low-speed oscillation and high-speed oscillation.
When an external pin interrupt request that is interrupt-enabled (the interrupt enable flag is "1") is issued, the STP bit is set to "0", and the low-speed oscillation restarts. If the high-speed clock was oscillating before the STOP mode is entered, the high-speed oscillation restarts. When the high-speed clock was not oscillating before entering the Stopped state, high-speed oscillation does not start.
After generating interrupt request, low-speed built-in RC oscillation begins oscillating independently of the clock mode. And, the clock is supplied as LSCLK after counts 29. When a system clock is a low-speed clock, it returns to program operational mode simultaneously.
In the case of low-speed crystal oscillation mode, oscillation is started after low-speed oscillation start time (T_{XTL}) by interrupt request occurs. And, LSCLK changes from RC oscillation into crystal oscillation by the automatic operation in after counts 8192 by the crystal oscillation.
In the case of high-speed external clock mode, LSCLK changes from RC oscillation into external clock by the automatic operation after counts 16 by the external clock by interrupt request occurs.
For the low-speed oscillation start time (T_{XTL}), see Appendix C "Electrical Characteristics".
Figure 4-5 shows the operation waveforms in STOP mode when CPU operates with the low-speed clock.

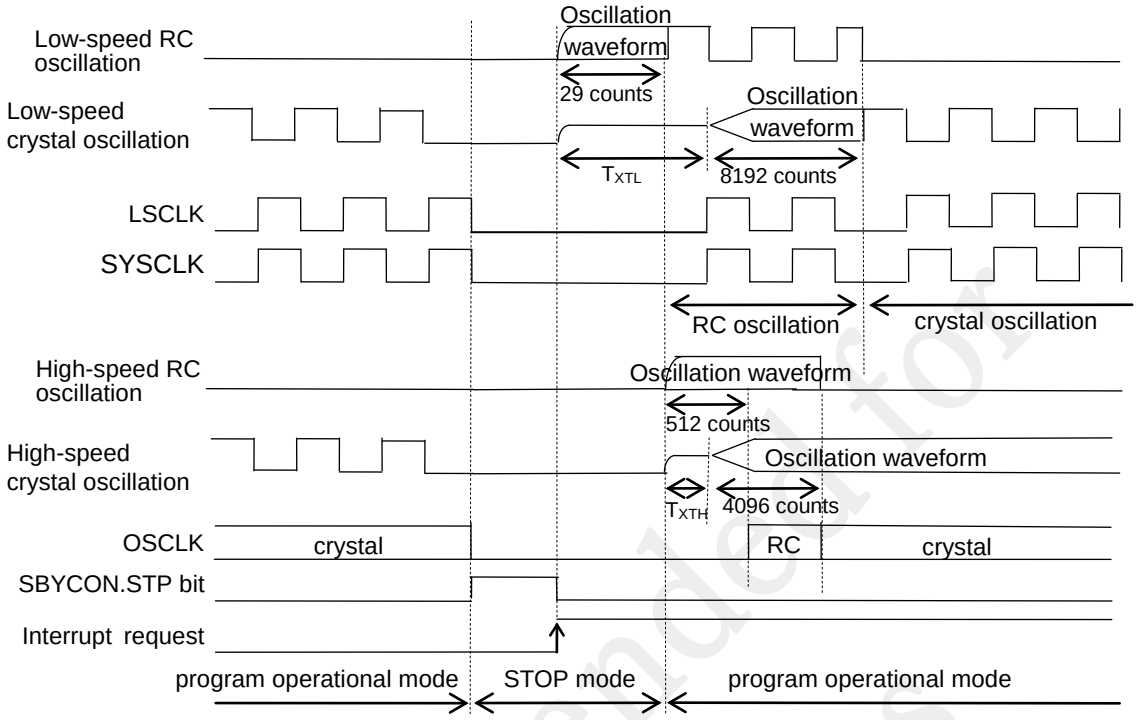


Figure 4-5 Operation Waveforms in STOP Mode When CPU Operates with Low-Speed Clock

4.3.2.2 Oscillation Stop and Restart Timing of High-Speed Clock

When the STP bit of SBYCON is set to "1" with the stop code acceptor enabled while the high-speed clock is operating, the mode changes to the STOP mode and the high-speed oscillation and low-speed oscillation stop. When an external pin interrupt request that is interrupt-enabled (the interrupt enable flag is "1") is issued, the STP bit is set to "0", and the high-speed oscillation and low-speed oscillation restart.

After generating interrupt request, low-speed built-in RC oscillation begins oscillating independently of the clock mode. And, the clock is supplied as LSCLK after counts 29. And the counts 512, as OSCLK clock supply after the high-speed built-in RC oscillation starts oscillation.
In the case of high-speed crystal/ceramic oscillation mode, oscillation is started after high-speed oscillation start time (T_{XTH}) from LSCLK supply. And, OSCLK changes from RC oscillation into crystal oscillation by the automatic operation after counts 4096 by the crystal oscillation.
In the case of high-speed external clock mode, OSCLK changes from RC oscillation into external clock by the automatic operation after counts 128 by the external clock from LSCLK supply.

For the high-speed oscillation start time (T_{XTH}) and low-speed oscillation start time (T_{XTL}), see the "Electrical Characteristics" Section in Appendix C.
Figure 4-6 shows the operation waveforms in STOP mode when CPU operates with the high-speed clock.

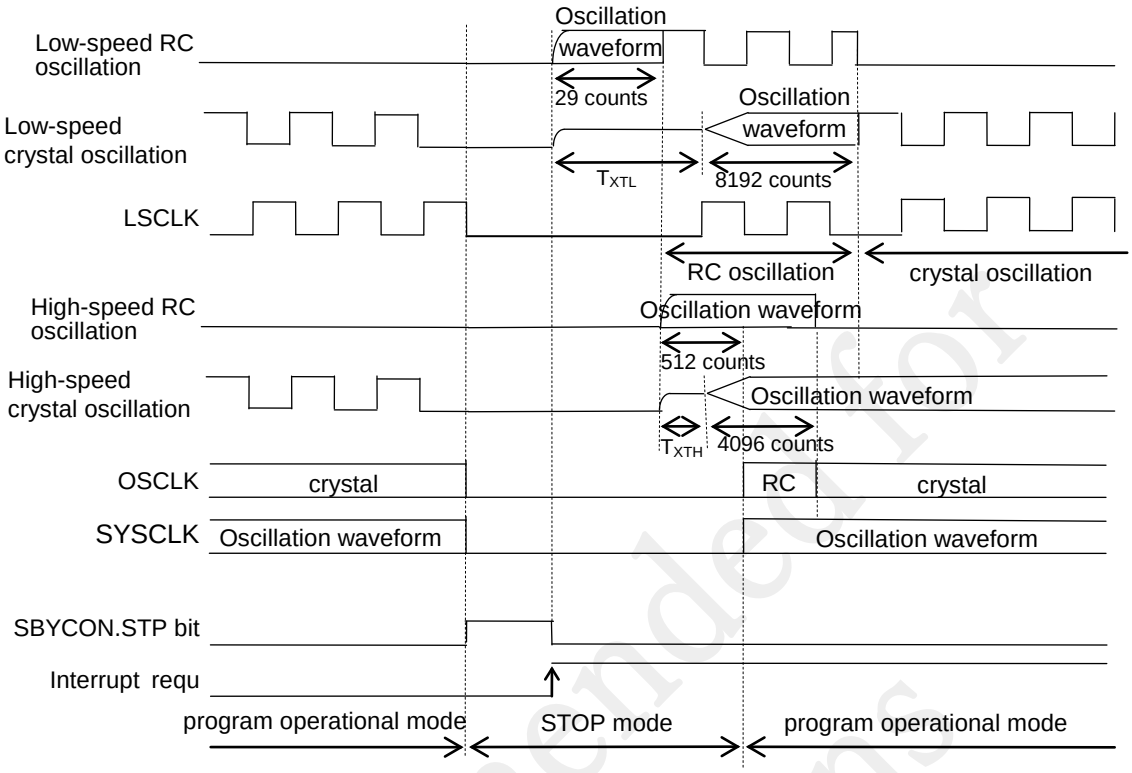


Figure 4-6 Operation Waveforms in STOP Mode When CPU Operates with High-Speed Clock

[Note]

•The STOP mode is entered two cycles after the instruction that sets the STP bit to “1” and up to two instructions are executed during the period between STOP mode release and a transition to interrupt processing. Therefore, place two NOP instructions next to the instruction that set the STP bit to “1”.

4.3.2.3 Note on Return Operation from STOP/HALT/DEEP-HALT/HALT-H Mode

The operation of returning from the STOP, HALT, DEEP-HALT, or HALT-H mode varies according to the interrupt level (ELEVEL) of the program status word (PSW), master interrupt enable flag (MIE), the contents of the interrupt enable register (IE0 to IE3), and whether the interrupt is a non-maskable interrupt or a maskable interrupt.
For details of PSW and the IE and IRQ registers, see "nX-U16/100 Core Instruction Manual" and Chapter 5, "Interrupt", respectively.

Table 4-1 and Table 4-2 show the return operations from the STOP/HALT/DEEP-HALT/HALT-H mode.

Table 4-1 Return Operation from STOP/HALT/DEEP-HALT/HALT-H Mode (Non-Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT/DEEP-HALT/HALT-H mode
*	*	-	0	Not returned from STOP/HALT/DEEP-HALT/HALT-H mode.
3	*	-	1	After the mode is returned from the STOP/HALT/DEEP-HALT/ HALT-H mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT/DEEP-HALT/HALT-H bit to "1". The program operation does not go to the interrupt routine.
0,1,2	*	-	1	After the mode is returned from the STOP/HALT/DEEP-HALT/ HALT-H mode, program operation restarts from the instruction following the instruction that sets the STP/HLT/DEEP-HALT/HALT-H bit to "1", then goes to the interrupt routine.

Table 4-2 Return Operation from STOP/HALT/DEEP-HALT/HALT-H Mode (Maskable Interrupt)

ELEVEL	MIE	IEn.m	IRQn.m	Return operation from STOP/HALT/DEEP-HALT/HALT-H mode
*	*	*	0	Not returned from STOP/HALT/DEEP-HALT/HALT-H mode.
*	*	0	1	
*	0	1	1	After the mode is returned from the STOP/HALT/DEEP-HALT/HALT-H mode, the program operation restarts from the instruction following the instruction that sets the STP/HLT/DHLT/HLTH bit to "1". The program operation does not go to the interrupt routine.
2,3	1	1	1	
0,1	1	1	1	After the mode is returned from the STOP/HALT/DEEP-HALT/HALT-H mode, program operation restarts from the instruction following the instruction that sets the STP/HLT/DHLT/HLTH bit to "1", then goes to the interrupt routine.

[Note]
- If the ELEVEL bit is 0H, it indicates that the CPU is performing neither non-maskable interrupt processing nor maskable interrupt processing nor software interrupt processing.
- If the ELEVEL bit is 1H, it indicates that the CPU is performing maskable interrupt processing or software interrupt processing. (ELEVEL is set during interrupt transition cycle.)
- If the ELEVEL bit is 2H, it indicates that the CPU is performing non-maskable interrupt processing. (ELEVEL is set during interrupt transition cycle.)
- If the ELEVEL bit is 3H, it indicates that the CPU is performing interrupt processing specific to the emulator. This setting is not allowed in normal applications.

4.3.3 Operation of Functions in STOP/HALT/DEEP-HALT/HALT-H Mode

Table 4-3 shows the states of the functions in each of the STOP, HALT, DEEP-HALT, and HALT-H modes.

Table 4-3 State of Functions in STOP/HALT/DEEP-HALT/HALT-H Mode

Function	HALT	HALT-H*2	DEEP-HALT*2	STOP
CPU	×	×	×	×
RAM	Retain	Retain	Retain	Retain
Watchdog timer	●	●	○	×
External Interrupt	Acceptable	Acceptable	Acceptable	Acceptable
LTBC	●	●	●	×
Timer	○	○	○	×
Function timer	○	○	○	×
UART	○	○	×	×
UART with FIFO	○*1	×	×	×
SSIO	○	○	×	×
SSIO with FIFO	○*1	×	×	×
I^2C	○*1	×	×	×
Melody driver	○	○	×	×
RC-ADC	○	○	×	×
SA-ADC	○	○	×	×
Comparator	○	○	○	○
VLS	○	○	○	○
LLD	○	○	○	○

*1 : Can operate only when the high-speed CLK is ON.
*2 : HALT-H/DEEP-HALT is only low-speed CLK operating.

●: Operate
○: Can operate
×: Cannot operate

4.3.4 Block Control Function

This LSI has a block control function, which resets and completely turns operating circuits of unused peripherals off to make even more reducing power consumption.
For each block control register without DLLD flag, the initial value of each flag is “0”, meaning the operation of each block is enabled. When any flag is set to “1” (disable operation), the function of the applicable block is reset (all registers are initialized) and the clock supply to such block stops. When this flag is set to “1”, the writing to all registers in the applicable block becomes invalid. When using the function of the applicable block, ensure to reset the applicable flag of this block control register to “0”, (enable operation).

BLKCON0 register: Controls (enables/disables) the circuit operation of timers 0 to 7.
BLKCON1 register: Controls (enables/disables) the circuit operation of multifunction timers 0 to 3.
BLKCON2 register: Controls (enables/disables) the circuit operation of I2C, UART and SSIO.
BLKCON3 register: Controls (enables/disables) the circuit operation of melody and analog comparator.
BLKCON4 register: Controls (enables/disables) the circuit operation of RC type A/D converter and successive approximation type A/D converter.
BLKCON5 register: Controls (enables/disables) the circuit operation of power supply voltage level detection (LLD, VLS).

[Note]
- •When certain flag of block control registers are set to ”1”, corresponding peripherals are reset (all registers are reset).
- •See each chapter for detail about the operation of each block and relevant notes.

Chapter 5

Interrupts

5 Interrupts

5.1 General Description

This LSI has 38 interrupt sources (External interrupts: 8 sources, Internal interrupts: 30 sources) and a software interrupt (SWI).
For details of each interrupt, see the following chapters:

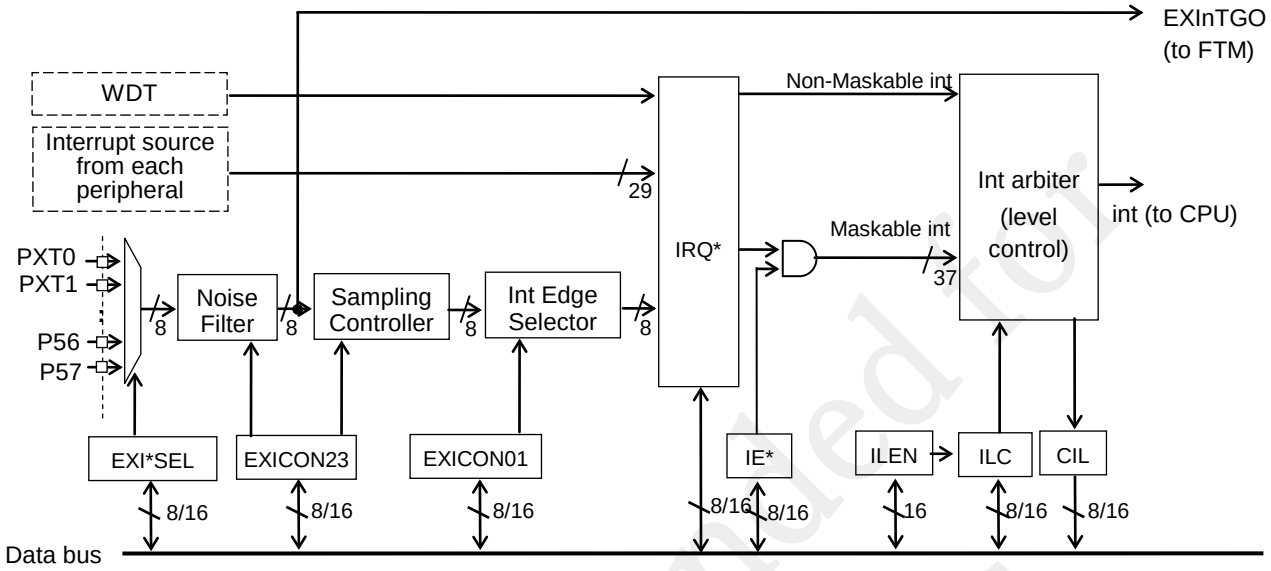
"Chapter 6 Clock Generation Circuit"
"Chapter 7 Time Base Counter "
"Chapter 8 Timer"
"Chapter 9 Function Timer(FTM)"
"Chapter 10 Watchdog Timer"
"Chapter 11 Synchronous Serial Port(SSIO)"
"Chapter 12 Synchronous Serial Port with FIFO(SSIOF)"
"Chapter 13 UART"
"Chapter 14 UART with FIFO (UARTF)"
"Chapter 15 I2C Bus Interface"
"Chapter 23 Melody Driver"
"Chapter 24 RC Oscillation type A/D Converter(RC-ADC)"
"Chapter 25 Successive Approximation Type A/D Converter(SA-ADC)"
"Chapter 26 Analog Comparator"
"Chapter 28 Voltage Level Supervisor(VLS)"

5.1.1 Features

- Non-maskable interrupt source: 1 (WDT)
- Maskable interrupt sources: 37 (Internal sources: 29, External sources: 8)
- Software interrupt (SWI): maximum 64 sources
- External interrupts and comparator allow edge selection and sampling selection
- Priority level (4-level) can be set for each interrupt

5.1.2 Configuration

Figure 5-1 shows the circuit of the interrupt controller.



IE* : Interrupt enable register 0 to 7
IRQ* : Interrupt source register 0 to 7
ILEN : Interrupt level control enable register
ILC : Interrupt level control register
CIL : Current interrupt level request register
EXICON01/23 : External interrupt control register
EXI*SEL : External interrupt mode register

Figure 5-1 Configuration of Circuit

5.2 Description of Registers

5.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F010	Interrupt enable register 01	IE0	IE01	R/W	8/16	00
0F011		IE1		R/W	8	00
0F012	Interrupt enable register 23	IE2	IE23	R/W	8/16	00
0F013		IE3		R/W	8	00
0F014	Interrupt enable register 45	IE4	IE45	R/W	8/16	00
0F015		IE5		R/W	8	00
0F016	Interrupt enable register 67	IE6	IE67	R/W	8/16	00
0F017		IE7		R/W	8	00
0F018	Interrupt request register 01	IRQ0	IRQ01	R/W	8/16	00
0F019		IRQ1		R/W	8	00
0F01A	Interrupt request register 23	IRQ2	IRQ23	R/W	8/16	00
0F01B		IRQ3		R/W	8	00
0F01C	Interrupt request register 45	IRQ4	IRQ45	R/W	8/16	00
0F01D		IRQ5		R/W	8	00
0F01E	Interrupt request register 67	IRQ6	IRQ67	R/W	8/16	00
0F01F		IRQ7		R/W	8	00
0F020	Interrupt level control enable register	ILENL	ILEN	R/W	8/16	00
0F021		ILENH		R/W	8	00
0F022	Current interrupt request level register	CILL	CIL	R/W	8/16	00
0F023		CILH		R/W	8	00
0F024	Interrupt level control register 1	ILC1L	ILC1	R/W	8/16	00
0F025		ILC1H		R/W	8	00
0F026	Interrupt level control register 2	ILC2L	ILC2	R/W	8/16	00
0F027		ILC2H		R/W	8	00
0F028	Interrupt level control register 3	ILC3L	ILC3	R/W	8/16	00
0F029		ILC3H		R/W	8	00
0F02A	Interrupt level control register 4	ILC4L	ILC4	R/W	8/16	00
0F02B		ILC4H		R/W	8	00
0F02C	Interrupt level control register 5	ILC5L	ILC5	R/W	8/16	00
0F02D		ILC5H		R/W	8	00
0F02E	Interrupt level control register 6	ILC6L	ILC6	R/W	8/16	00
0F02F		ILC6H		R/W	8	00
0F030	Interrupt level control register 7	ILC7L	ILC7	R/W	8/16	00
0F031		ILC7H		R/W	8	00
0F040	External interrupt control register 01	EXICON0	EXICON01	R/W	8/16	00
0F041		EXICON1		R/W	8	00
0F042	External interrupt control register 23	EXICON2	EXICON23	R/W	8/16	00
0F043		EXICON3		R/W	8	00
0F048	External interrupt 01 selection register	EXI0SEL	EXI01SEL	R/W	8/16	00
0F049		EXI1SEL		R/W	8	00

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F04A	External interrupt 23 selection register	EXI2SEL	EXI23SEL	R/W	8/16	00
0F04B		EXI3SEL		R/W	8	00
0F04C	External interrupt 45 selection register	EXI4SEL	EXI45SEL	R/W	8/16	00
0F04D		EXI5SEL		R/W	8	00
0F04E	External interrupt 67 selection register	EXI6SEL	EXI67SEL	R/W	8/16	00
0F04F		EXI7SEL		R/W	8	00

5.2.2 Interrupt Enable Register 01 (IE01)

Address: 0F010H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
IE0	–	–	–	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
IE1	EEXI7	EEXI6	EEXI5	EEXI4	EEXI3	EEXI2	EEXI1	EEXI0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE01 is a special function register (SFR) used to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE01 is not reset.

Description of Bits

- **EEXI0** (bit 8)
  EEXI0 is the enable flag for the external interrupt 0 (EXI0INT).

EEXI0	Description
0	Disabled (initial value)
1	Enabled

- **EEXI1** (bit 9)
  EEXI1 is the enable flag for the external interrupt 1 (EXI1INT).

EEXI1	Description
0	Disabled (initial value)
1	Enabled

- **EEXI2** (bit 10)
  EEXI2 is the enable flag for the external interrupt 2 (EXI2INT).

EEXI2	Description
0	Disabled (initial value)
1	Enabled

- **EEXI3** (bit 11)
  EEXI3 is the enable flag for the external interrupt 3 (EXI3INT).

EEXI3	Description
0	Disabled (initial value)
1	Enabled

- **EEXI4** (bit 12)
  EEXI4 is the enable flag for the external interrupt 4 (EXI4INT).

EEXI4	Description
0	Disabled (initial value)
1	Enabled

- **EEXI5** (bit 13)
  EEXI5 is the enable flag for the external interrupt 5 (EXI5INT).

EEXI5	Description
0	Disabled (initial value)
1	Enabled

- **EEXI6** (bit 14)
  EEXI6 is the enable flag for the external interrupt 6 (EXI6INT).

EEXI6	Description
0	Disabled (initial value)
1	Enabled

- **EEXI7** (bit 15)
  EEXI7 is the enable flag for the external interrupt 7 (EXI7INT).

EEXI7	Description
0	Disabled (initial value)
1	Enabled

5.2.3 Interrupt Enable Register 23 (IE23)

Address: 0F012H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
IE2	–	EUAF0	EUA1	EUA0	EI2C1	EI2C0	ESIOF0	ESIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
IE3	EMD0	EVLS	ELOSC	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE23 is a special function register (SFR) used to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE23 is not reset.

Description of Bits

- **ESIO0** (bit 0)
  ESIO0 is the enable flag for the synchronous serial port 0 interrupt (SIO0INT).

ESIO0	Description
0	Disabled (initial value)
1	Enabled

- **ESIOF0** (bit 1)
  ESIOF0 is the enable flag for the synchronous serial port 0 interrupt with FIFO (SIOF0INT).

ESIOF0	Description
0	Disabled (initial value)
1	Enabled

- **EI2C0** (bit 2)
  EI2C0 is the enable flag for the I2C bus 0 interrupt (I2C0INT).

EI2C0	Description
0	Disabled (initial value)
1	Enabled

- **EI2C1** (bit 3)
  EI2C1 is the enable flag for the I2C bus 1 interrupt (I2C1INT).

EI2C1	Description
0	Disabled (initial value)
1	Enabled

- **EUA0** (bit 4)
  EUA0 is the enable flag for the UART0 reception interrupt (UA0INT).

EUA0	Description
0	Disabled (initial value)
1	Enabled

- **EUA1** (bit 5)
  EUA1 is the enable flag for the UART0 transmission interrupt (UA1INT).

EUA1	Description
0	Disabled (initial value)
1	Enabled

- **EUAF0** (bit 6)
  EUAF0 is the enable flag for the UART0 transmission interrupt with FIFO (UAF0INT).

EUAF0	Description
0	Disabled (initial value)
1	Enabled

- **ELOSC** (bit 13)
  ELOSC is the enable flag for the low-speed oscillation clock switching interrupt (LOSCINT).

ELOSC	Description
0	Disabled (initial value)
1	Enabled

- **EVLS** (bit 14)
  EVLS is the enable flag for the VLS interrupt (VLSINT).

EVLS	Description
0	Disabled (initial value)
1	Enabled

- **EMD0** (bit 15)
  EMD0 is the enable flag for the melody 0 interrupt (MD0INT).

EMD0	Description
0	Disabled (initial value)
1	Enabled

5.2.4 Interrupt Enable Register 45 (IE45)

Address: 0F014H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
IE4	–	–	ECMP1	ECMP0	–	–	ERAD	ESAD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
IE5	ETM7	ETM6	ETM5	ETM4	ETM3	ETM2	ETM1	ETM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE45 is a special function register (SFR) used to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE45 is not reset.

Description of Bits

- **ESAD** (bit 0)
  ESAD is the enable flag for the successive approximation type A/D converter interrupt (SADINT).

ESAD	Description
0	Disabled (initial value)
1	Enabled

- **ERAD** (bit 1)
  ERAD is the enable flag for the RC oscillation type A/D converter interrupt (RADINT).

ERAD	Description
0	Disabled (initial value)
1	Enabled

- **ECMP0** (bit 4)
  ECMP0 is the enable flag for the comparator 0 interrupt (CMP0INT).

ECMP0	Description
0	Disabled (initial value)
1	Enabled

- **ECMP1** (bit 5)
  ECMP1 is the enable flag for the comparator 1 interrupt (CMP1INT).

ECMP1	Description
0	Disabled (initial value)
1	Enabled

- **ETM0** (bit 8)
  ETM0 is the enable flag for the 8-bit timer 0 interrupt (TM0INT).

ETM0	Description
0	Disabled (initial value)
1	Enabled

- **ETM1** (bit 9)
  ETM1 is the enable flag for the 8-bit timer 1 interrupt (TM1INT).

ETM1	Description
0	Disabled (initial value)
1	Enabled

- **ETM2** (bit 10)
  ETM2 is the enable flag for the 8-bit timer 2 interrupt (TM2INT).

ETM2	Description
0	Disabled (initial value)
1	Enabled

- **ETM3** (bit 11)
  ETM3 is the enable flag for the 8-bit timer 3 interrupt (TM3INT).

ETM3	Description
0	Disabled (initial value)
1	Enabled

- **ETM4** (bit 12)
  ETM4 is the enable flag for the 8-bit timer 4 interrupt (TM4INT).

ETM4	Description
0	Disabled (initial value)
1	Enabled

- **ETM5** (bit 13)
  ETM5 is the enable flag for the 8-bit timer 5 interrupt (TM5INT).

ETM5	Description
0	Disabled (initial value)
1	Enabled

- **ETM6** (bit 14)
  ETM6 is the enable flag for the 8-bit timer 6 interrupt (TM6INT).

ETM6	Description
0	Disabled (initial value)
1	Enabled

- **ETM7** (bit 15)
  ETM7 is the enable flag for the 8-bit timer 7 interrupt (TM7INT).

ETM7	Description
0	Disabled (initial value)
1	Enabled

5.2.5 Interrupt Enable Register 67 (IE67)

Address: 0F016H
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
IE6	–	–	–	–	EFTM3	EFTM2	EFTM1	EFTM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
IE7	–	–	–	–	–	ELTBC2	ELTBC1	ELTBC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IE67 is a special function register (SFR) used to control enable/disable for each interrupt request.
When an interrupt is accepted, the master interrupt enable flag (MIE) is set to "0", but the corresponding flag of IE67 is not reset.

Description of Bits

- **EFTM0** (bit 0)
  EFTM0 is the enable flag for the 16-bit timer 0 interrupt (FTM0INT).

EFTM0	Description
0	Disabled (initial value)
1	Enabled

- **EFTM1** (bit 1)
  EFTM1 is the enable flag for the 16-bit timer 1 interrupt (FTM1INT).

EFTM1	Description
0	Disabled (initial value)
1	Enabled

- **EFTM2** (bit 2)
  EFTM2 is the enable flag for the 16-bit timer 2 interrupt (FTM2INT).

EFTM1	Description
0	Disabled (initial value)
1	Enabled

- **EFTM3** (bit 3)
  EFTM3 is the enable flag for the 16-bit timer 3 interrupt (FTM3INT).

EFTM3	Description
0	Disabled (initial value)
1	Enabled

- **ELTBC0** (bit 8)
  ELTBC0 is the enable flag for the time base counter 0 interrupt (LTB0INT).

ELTBC0	Description
0	Disabled (initial value)
1	Enabled

- **ELTBC1** (bit 9)
  ELTBC1 is the enable flag for the time base counter 1 interrupt (LTB1INT).

ELTBC1	Description
0	Disabled (initial value)
1	Enabled

- **ELTBC2** (bit 10)
  ELTBC2 is the enable flag for the time base counter 2 interrupt (LTB2INT).

ELTBC2	Description
0	Disabled (initial value)
1	Enabled

5.2.6 Interrupt Request Register 01 (IRQ01)

Address: 0F018H
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
IRQ0	–	–	–	–	–	–	–	QWDT
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
IRQ1	QEXI7	QEXI6	QEXI5	QEXI4	QEXI3	QEXI2	QEXI1	QEXI0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ01 is a special function register (SFR) used to request an interrupt for each interrupt source.
The watchdog timer interrupt (WDTINT) is a non-maskable interrupt that does not depend on MIE. In this case, an interrupt is requested to the CPU regardless of the value of the Mask Interrupt Enable flag (MIE).
Each IRQ0 request flag is set to "1" regardless of the MIE value when an interrupt is generated.
Each IRQ1 request flag is set to "1" regardless of the IE1 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE1) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ01 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ01 is set to "0" by hardware when the interrupt request is accepted by the CPU.

Description of Bits

- **QWDT** (bit 0)
  QWDT is the request flag for the watchdog timer interrupt (WDTINT).

QWDT	Description
0	No request (initial value)
1	Request

[Note]
When an interrupt is generated by the write instruction to the interrupt request register (IRQ0), the interrupt shift cycle starts after the next 1 instruction is executed.

- **QEXI0** (bit 8)
  QEXI0 is the request flag for the external interrupt 0 (EXI0INT).

QEXI0	Description
0	No request (initial value)
1	Request

- **QEXI1** (bit 9)
  QEXI1 is the request flag for the external interrupt 1 (EXI1INT).

QEXI1	Description
0	No request (initial value)
1	Request

- **QEXI2** (bit 10)
  QEXI2 is the request flag for the external pin interrupt 2 (EXI2INT).

QEXI2	Description
0	No request (initial value)
1	Request

- **QEXI3** (bit 11)
  QEXI3 is the request flag for the external interrupt 3 (EXI3INT).

QEXI3	Description
0	No request (initial value)
1	Request

- **QEXI4** (bit 12)
  QEXI4 is the request flag for the external interrupt 4 (EXI4INT).

QEXI4	Description
0	No request (initial value)
1	Request

- **QEXI5** (bit 13)
  QEXI5 is the request flag for the external interrupt 5 (EXI5INT).

QEXI5	Description
0	No request (initial value)
1	Request

- **QEXI6** (bit 14)
  QEXI6 is the request flag for the external interrupt 6 (EXI6INT).

QEXI6	Description
0	No request (initial value)
1	Request

- **QEXI7** (bit 15)
  QEXI7 is the request flag for the external interrupt 7 (EXI7INT).

QEXI7	Description
0	No request (initial value)
1	Request

[Note]
When an interrupt is generated by the write instruction to the interrupt request register (IRQ1) or to the interrupt enable register (IE1), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.7 Interrupt Request Register 23 (IRQ23)

Address: 0F01AH
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
IRQ2	–	QUAF0	QUA1	QUA0	QI2C1	QI2C0	QSIOF0	QSIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
IRQ3	QMD0	QVLS	QLOSC	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ23 is a special function register (SFR) used to request an interrupt for each interrupt source.
Each IRQ23 request flag is set to "1" regardless of the IE23 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE23) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ23 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ2 is set to "0" by hardware when the interrupt request is accepted by the CPU.

Description of Bits

- **QSIO0** (bit 0)
  QSIO0 is the request flag for the synchronous serial port 0 interrupt (SIO0INT).

QSIO0	Description
0	No request (initial value)
1	Request

- **QSIOF0** (bit 1)
  QSIOF0 is the request flag for the synchronous serial port 0 interrupt with FIFO (SIOF0INT).

QSIOF0	Description
0	No request (initial value)
1	Request

- **QI2C0** (bit 2)
  QI2C0 is the request flag for the I2C bus 0 interrupt (I2C0INT).

QI2C0	Description
0	No request (initial value)
1	Request

- **QI2C1** (bit 3)
  QI2C1 is the request flag for the I2C bus 1 interrupt (I2C1INT).

QI2C1	Description
0	No request (initial value)
1	Request

- **QUA0** (bit 4)
  QUA0 is the request flag for the UART0 reception interrupt (UA0INT).

QUA0	Description
0	No request (initial value)
1	Request

- **QUA1** (bit 5)
  QUA1 is the request flag for the UART0 transmission interrupt (UA1INT).

QUA1	Description
0	No request (initial value)
1	Request

- **QUAF0** (bit 6)
  QUAF0 is the request flag for the UART0 interrupt with FIFO (UAF0INT).

QUAF0	Description
0	No request (initial value)
1	Request

- **QLOSC** (bit 13)
  QLOSC is the request flag for the low-speed oscillation clock switching interrupt (LOSCINT).

QLOSC	Description
0	No request (initial value)
1	Request

- **QVLS** (bit 14)
  QVLS is the request flag for the VLS interrupt (VLSINT).

QVLS	Description
0	No request (initial value)
1	Request

- **QMD0** (bit 15)
  QMD0 is the request flag for the melody 0 interrupt (MD0INT).

QMD0	Description
0	No request (initial value)
1	Request

[Note]
When an interrupt is generated by the write instruction to the interrupt request register (IRQ23) or to the interrupt enable register (IE23), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.8 Interrupt Request Register 45 (IRQ45)

Address: 0F01CH
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
IRQ4	–	–	QCMP1	QCMP0	–	–	QRAD	QSAD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
IRQ5	QTM7	QTM6	QTM5	QTM4	QTM3	QTM2	QTM1	QTM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ45 is a special function register (SFR) used to request an interrupt for each interrupt source.
Each IRQ45 request flag is set to "1" regardless of the IE45 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE45) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ45 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ45 is set to "0" by hardware when the interrupt request is accepted by the CPU.

Description of Bits

- **QSAD** (bit 0)
  QSAD is the request flag for the successive approximation type A/D converter interrupt (SADINT).

QSAD	Description
0	No request (initial value)
1	Request

- **QRAD** (bit 1)
  QRAD is the request flag for the RC oscillation type A/D converter interrupt (RADINT).

QRAD	Description
0	No request (initial value)
1	Request

- **QCMP0** (bit 4)
  QCMP0 is the request flag for the comparator 0 interrupt (CMP0INT).

QCMP0	Description
0	No request (initial value)
1	Request

- **QCMP1** (bit 5)
  QCMP1 is the request flag for the comparator 1 interrupt (CMP1INT).

QCMP1	Description
0	No request (initial value)
1	Request

- **QTM0** (bit 8)
  QTM0 is the request flag for the 8-bit timer 0 interrupt (TM0INT).

QTM0	Description
0	No request (initial value)
1	Request

- **QTM1** (bit 9)
  QTM1 is the request flag for the 8-bit timer 1 interrupt (TM1INT).

QTM1	Description
0	No request (initial value)
1	Request

- **QTM2** (bit 10)
  QTM2 is the request flag for the 8-bit timer 2 interrupt (TM2INT).

QTM2	Description
0	No request (initial value)
1	Request

- **QTM3** (bit 11)
  QTM3 is the request flag for the 8-bit timer 3 interrupt (TM3INT).

QTM3	Description
0	No request (initial value)
1	Request

- **QTM4** (bit 12)
  QTM4 is the request flag for the 8-bit timer 4 interrupt (TM4INT).

QTM4	Description
0	No request (initial value)
1	Request

- **QTM5** (bit 13)
  QTM5 is the request flag for the 8-bit timer 5 interrupt (TM5INT).

QTM5	Description
0	No request (initial value)
1	Request

- **QTM6** (bit 14)
  QTM6 is the request flag for the 8-bit timer 6 interrupt (TM6INT).

QTM6	Description
0	No request (initial value)
1	Request

- **QTM7** (bit 15)
  QTM7 is the request flag for the 8-bit timer 5 interrupt (TM7INT).

QTM7	Description
0	No request (initial value)
1	Request

[Note]
When an interrupt is generated by the write instruction to the interrupt request register (IRQ45) or to the interrupt enable register (IE45), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.9 Interrupt Request Register 67 (IRQ67)

Address: 0F01EH
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
IRQ6	–	–	–	–	QFTM3	QFTM2	QFTM1	QFTM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
IRQ7	–	–	–	–	–	QLTBC2	QLTBC1	QLTBC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

IRQ67 is a special function register (SFR) used to request an interrupt for each interrupt source.
Each IRQ67 request flag is set to "1" regardless of the IE67 and MIE values when an interrupt is generated. In this case, an interrupt is requested to the CPU when the related flag of the interrupt enable register (IE67) is set to "1" and the master interrupt enable flag (MIE) is set to "1".
By setting the IRQ67 request flag to "1" by software, an interrupt can be generated.
The corresponding flag of IRQ67 is set to "0" by hardware when the interrupt request is accepted by the CPU.

Description of Bits

- **QFTM0** (bit 0)
  QFTM0 is the request flag for the 16-bit timer 0 interrupt (FTM0INT).

QFTM0	Description
0	No request (initial value)
1	Request

- **QFTM1** (bit 1)
  QFTM1 is the request flag for the 16-bit timer 1 interrupt (FTM1INT).

QFTM1	Description
0	No request (initial value)
1	Request

- **QFTM2** (bit 2)
  QFTM2 is the request flag for the 16-bit timer 2 interrupt (FTM2INT).

QFTM2	Description
0	No request (initial value)
1	Request

- **QFTM3** (bit 3)
  QFTM3 is the request flag for the 16-bit timer 3 interrupt (FTM3INT).

QFTM3	Description
0	No request (initial value)
1	Request

- **QLTBC0** (bit 8)
  QLTBC0 is the request flag for the time base counter 0 interrupt (LTB0INT).

QLTBC0	Description
0	No request (initial value)
1	Request

- **QLTBC1** (bit 9)
  QLTBC1 is the request flag for the time base counter 1 interrupt (LTB1INT).

QLTBC1	Description
0	No request (initial value)
1	Request

- **QLTBC2** (bit 10)
  QLTBC2 is the request flag for the time base counter 2 interrupt (LTB2INT).

QLTBC2	Description
0	No request (initial value)
1	Request

[Note]
When an interrupt is generated by the write instruction to the interrupt request register (IRQ67) or to the interrupt enable register (IE67), the interrupt shift cycle starts after the next 1 instruction is executed.

5.2.10 Interrupt Level Control Enable Register (ILEN)

Address: 0F020H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
ILENL	–	–	–	–	–	–	–	ILE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
ILENH	–	–	–	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control enable register (ILEN) is a special function register (SFR) used to control enable/disable for the interrupt level control.

Description of Bits

- **ILE** (bit 0)
  The ILE bit controls enable/disable for the interrupt level control. Enable this bit setting to use the interrupt level control. If this bit setting is disabled, do not access the CIL and ILC registers.

ILE	Description
0	Disabled (initial value)
1	Enabled

[Note]
A write instruction to the interrupt level control enable register (ILEN) should be executed during the interrupts is disabled.
To disable the interrupt level control function, set both the values of ILC and CIL registers to 00H.

5.2.11 Current Interrupt Request Level Register (CIL)

Address: 0F022H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
CILL	CILN	–	–	–	CILM3	CILM2	CILM1	CILM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
CILH	–	–	–	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The current interrupt request level register (CIL) indicates the interrupt level of the interrupt currently being processed by the processor.
Access to this register is possible only when the interrupt level control is enabled by the ILEN register. If a write/read access is made while the interrupt level control is disabled, a write access is ignored and a read access reads either the value when the register was enabled or the initial value if the register has never been enabled.

When a "1" has been set in any bit position of CIL, the acceptance of interrupt requests is prohibited below the interrupt level indicated by the highest order bit position set to "1". It indicates that the processing is being done for an interrupt with the level corresponding to the bit position.
When "1"s have been set at several bit positions of CIL, it indicates that multiple interrupts are being processed.

<<Condition for setting>>
When the processor accepts an interrupt, "1" is set to the CILN bit if the interrupt request is non-maskable interrupt. If the interrupt request is maskable interrupt, "1" is set to the bit position of CILM corresponding to the level of the interrupt source.

<<Condition for clearing>>
When a write access is made, the highest order bit set to "1" is cleared. After the interrupt handler processing is completed, execute a write access once.

Description of Bits

- **CILM3-0** (bits 3 to 0)
  Indicates the level of the maskable interrupt request being processed by CPU.

CILM0	Description
0	Interrupt level 1 is not in processing (initial value)
1	Interrupt level 1 is in processing

CILM1	Description
0	Interrupt level 2 is not in processing (initial value)
1	Interrupt level 2 is in processing

CILM2	Description
0	Interrupt level 3 is not in processing (initial value)
1	Interrupt level 3 is in processing

CILM3	Description
0	Interrupt level 4 is not in processing (initial value)
1	Interrupt level 4 is in processing

- **CILN** (bit 7)
  Indicates whether CPU is processing a non-maskable interrupt request or not.

CILN	Description
0	Non-maskable interrupt is not in processing (initial value)
1	Non-maskable interrupt is in processing

5.2.12 Interrupt Level Control Register 1 (ILC1)

Address: 0F024H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
ILC1L	L1EXI3	L0EXI3	L1EXI2	L0EXI2	L1EXI1	L0EXI1	L1EXI0	L0EXI0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
ILC1H	L1EXI7	L0EXI7	L1EXI6	L0EXI6	L1EXI5	L0EXI5	L1EXI4	L0EXI4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 1 is a special function register (SFR) used to set the level of the interrupt source enabled by IE1.
Write access to this register is possible only when the interrupt level control is enabled by the ILEN register.
Level 1 to 4 can be set for each interrupt source. The register which has the higher level is given the higher priority.

Description of Bits

- **L1-0EXI0** (bits 1 to 0)
  L1-0EXI0 set the level of the external interrupt 0 (EXI0INT).

L1EXI0	L0EXI0	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0EXI1** (bits 3 to 2)
  L1-0EXI1 set the level of the external interrupt 1 (EXI1INT).

L1EXI1	L0EXI1	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0EXI2** (bits 5 to 4)
  L1-0EXI2 set the level of the external interrupt 2 (EXI2INT).

L1EXI2	L0EXI2	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0EXI3** (bits 7 to 6)
  L1-0EXI3 set the level of the external interrupt 3 (EXI3INT).

L1EXI3	L0EXI3	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0EXI4** (bits 9 to 8)
  L1-0EXI4 set the level of the external interrupt 4 (EXI4INT).

L1EXI4	L0EXI4	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0EXI5** (bits 11 to 10)
  L1-0EXI5 set the level of the external interrupt 5 (EXI5INT).

L1EXI5	L0EXI5	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0EXI6** (bits 13 to 12)
  L1-0EXI6 set the level of the external interrupt 6 (EXI6INT).

L1EXI6	L0EXI6	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0EXI7** (bits 15 to 14)
  L1-0EXI7 set the level of the external interrupt 7 (EXI7INT).

L1EXI7	L0EXI7	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

[Note]
A write instruction to the interrupt level control register 1 (ILC1) should be executed after disabling the interrupt.
Except this way, the write instruction to the interrupt level control register 1(ILC1) is not guaranteed.

5.2.13 Interrupt Level Control Register 2 (ILC2)

Address: 0F026H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
ILC2L	L1I2C1	L0I2C1	L1I2C0	L0I2C0	L1SIOF0	L0SIOF0	L1SIO0	L0SIO0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
ILC2H	–	–	L1UAF0	L0UAF0	L1UA1	L0UA1	L1UA0	L0UA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 2 is a special function register (SFR) used to set the level of the interrupt source enabled by IE2.
Write access to this register is possible only when the interrupt level control is enabled by the ILEN register.
Level 1 to 4 can be set for each interrupt source. The register which has the higher level is given the higher priority..

Description of Bits

- **L1-0SIO0** (bits 1 to 0)
  L1-0SIO0 set the level of the synchronous serial port 0 interrupt (SIO0INT).

L1SIO0	L0SIO0	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0SIOF0** (bits 3 to 2)
  L1-0SIOF0 set the level of the synchronous serial port 0 with FIFO (SIOF0INT).

L1SIOF0	L0SIOF0	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0I2C0** (bits 5 to 4)
  L1-0I2C0 set the level of the I2C bus 0 interrupt (I2C0INT).

L1I2C0	L0I2C0	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0I2C1** (bits 7 to 6)
  L1-0I2C1 set the level of the I2C bus 1 interrupt (I2C1INT).

L1I2C1	L0I2C1	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0UA0** (bits 9 to 8)
  L1-0UA0 set the level of the UART0 reception interrupt (UA0INT).

L1UA0	L0UA0	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0UA1** (bits 11 to 10)
  L1-0UA1 set the level of the UART0 transmission interrupt (UA1INT).

L1UA1	L0UA1	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0UAF0** (bits 13 to 12)
  L1-0UAF0 set the level of the UART0 interrupt with FIFO (UAF0INT).

L1UAF0	L0UAF0	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

[Note]
A write instruction to the interrupt level control enable register (ILC2) should be executed during the interrupts is disabled.
Except this way, the write instruction to the interrupt level control register 2(ILC2) is not guaranteed.

5.2.14 Interrupt Level Control Register 3 (ILC3)

Address: 0F028H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
ILC3L	–	–	–	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
ILC3H	L1MD0	L0MD0	L1VLS	L0VLS	L1LOSC	L0LOSC	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 3 is a special function register (SFR) used to set the level of the interrupt source enabled by IE3.
Write access to this register is possible only when the interrupt level control is enabled by the ILEN register.
Level 1 to 4 can be set for each interrupt source. The register which has the higher level is given the higher priority.

Description of Bits

- **L1-0LOSC** (bits 11 to 10)
  L1-0LOSC set the level of the OSC interrupt (LOSCINT).

L1LOSC	L0LOSC	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0VLS** (bits 13 to 12)
  L1-0VLS set the level of the VLS interrupt (VLSINT).

L1VLS	L0VLS	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0MD0** (bits 15 to 14)
  L1-0MD0 set the level of the melody 0 interrupt (MD0INT).

L1MD0	L0MD0	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

[Note]
A write instruction to the interrupt level control register 3 (ILC3) should be executed after disabling the interrupt.
Except this way, the write instruction to the interrupt level control register 3(ILC3) is not guaranteed..

5.2.15 Interrupt Level Control Register 4 (ILC4)

Address: 0F02AH
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
ILC4L	–	–	–	–	L1RAD	L0RAD	L1SAD	L0SAD
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
ILC4H	–	–	–	–	L1CMP1	L0CMP1	L1CMP0	L0CMP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 4 is a special function register (SFR) used to set the level of the interrupt source enabled by IE4.
Write access to this register is possible only when the interrupt level control is enabled by the ILEN register.
Level 1 to 4 can be set for each interrupt source. The register which has the higher level is given the higher priority.

Description of Bits

- **L1-0SAD** (bits 1 to 0)
  L1-0SAD set the level of the successive approximation type A/D converter interrupt (SADINT).

L1SAD	L0SAD	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0RAD** (bits 3 to 2)
  L1-0RAD set the level of the RC oscillation type A/D converter interrupt (RADINT).

L1RAD	L0RAD	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0CMP0** (bits 9 to 8)
  L1-0CMP0 set the level of the comparator 0 interrupt (CMP0INT).

L1CMP0	L0CMP0	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0CMP1** (bits 11 to 10)
  L1-0CMP1 set the level of the comparator 1 interrupt (CMP1INT).

L1CMP1	L0CMP1	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

[Note]
A write instruction to the interrupt level control register 4 (ILC4) should be executed after disabling the interrupt.
Except this way, the write instruction to the interrupt level control register 4(ILC4) is not guaranteed..

5.2.16 Interrupt Level Control Register 5 (ILC5)

Address: 0F02CH
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
ILC5L	L1TM3	L0TM3	L1TM2	L0TM2	L1TM1	L0TM1	L1TM0	L0TM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
ILC5H	L1TM7	L0TM7	L1TM6	L0TM6	L1TM5	L0TM5	L1TM4	L0TM4
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 5 is a special function register (SFR) used to set the level of the interrupt source enabled by IE5.
Write access to this register is possible only when the interrupt level control is enabled by the ILEN register.
Level 1 to 4 can be set for each interrupt source. The register which has the higher level is given the higher priority.

Description of Bits

- **L1-0TM0** (bits 1 to 0)
  L1-0TM0 set the level of the 8-bit timer 0 interrupt (TM0INT).

L1TM0	L0TM0	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0TM1** (bits 3 to 2)
  L1-0TM1 set the level of the 8-bit timer 1 interrupt (TM1INT).

L1TM1	L0TM1	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0TM2** (bits 5 to 4)
  L1-0TM2 set the level of the 8-bit timer 2 interrupt (TM2INT).

L1TM2	L0TM2	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0TM3** (bits 7 to 6)
  L1-0TM3 set the level of the 8-bit timer 3 interrupt (TM3INT).

L1TM3	L0TM3	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0TM4** (bits 9 to 8)
  L1-0TM4 set the level of the 8-bit timer 4 interrupt (TM4INT).

L1TM4	L0TM4	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0TM5** (bits 11 to 10)
  L1-0TM5 set the level of the 8-bit timer 5 interrupt (TM5INT).

L1TM5	L0TM5	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0TM6** (bits 13 to 12)
  L1-0TM6 set the level of the 8-bit timer 6 interrupt (TM6INT).

L1TM6	L0TM6	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0TM7** (bits 15 to 14)
  L1-0TM7 set the level of the 8-bit timer 7 interrupt (TM7INT).

L1TM7	L0TM7	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

[Note]
A write instruction to the interrupt level control register 5 (ILC5) should be executed after disabling the interrupt.
Except this way, the write instruction to the interrupt level control register 5(ILC5) is not guaranteed.

5.2.17 Interrupt Level Control Register 6 (ILC6)

Address: 0F02EH
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
ILC6L	L1FTM3	L0FTM3	L1FTM2	L0FTM2	L1FTM1	L0FTM1	L1FTM0	L0FTM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
ILC6H	–	–	–	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 6 is a special function register (SFR) used to set the level of the interrupt source enabled by IE6.
Write access to this register is possible only when the interrupt level control is enabled by the ILEN register.
Level 1 to 4 can be set for each interrupt source. The register which has the higher level is given the higher priority.

Description of Bits

- **L1-0FTM0** (bits 1 to 0)
  L1-0FTM0 set the level of the 16-bit timer 0 interrupt (FTM0INT).

L1FTM0	L0FTM0	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0FTM1** (bits 3 to 2)
  L1-0FTM1 set the level of the 16-bit timer 1 interrupt (FTM1INT).

L1FTM1	L0FTM1	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0FTM2** (bits 5 to 4)
  L1-0FTM2 set the level of the 16-bit timer 2 interrupt (FTM2INT).

L1FTM2	L0FTM2	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0FTM3** (bits 7 to 6)
  L1-0FTM3 set the level of the 16-bit timer 3 interrupt (FTM3INT).

L1FTM3	L0FTM3	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

[Note]
A write instruction to the interrupt level control register 6 (ILC6) should be executed after disabling the interrupt.
Except this way, the write instruction to the interrupt level control register 6(ILC6) is not guaranteed.

5.2.18 Interrupt Level Control Register 7 (ILC7)

Address: 0F030H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
ILC7L	–	–	L1LTBC2	L0LTBC2	L1LTBC1	L0LTBC1	L1LTBC0	L0LTBC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
ILC7H	–	–	–	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

The interrupt level control register 6 is a special function register (SFR) used to set the level of the interrupt source enabled by IE6.
Write access to this register is possible only when the interrupt level control is enabled by the ILEN register.
Level 1 to 4 can be set for each interrupt source. The register which has the higher level is given the higher priority.

Description of Bits

- **L1-0LTBC0** (bits 1 to 0)
  L1-0LTBC0 set the level of the time base counter 0 interrupt (LTB0INT).

L1LTBC0	L0LTBC0	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0LTBC1** (bits 3 to 2)
  L1-0LTBC1 set the level of the time base counter 1 interrupt (LTB1INT).

L1LTBC1	L0LTBC1	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

- **L1-0TLBC2** (bits 5 to 4)
  L1-0LTBC2 set the level of the time base counter 2 interrupt (LTB2INT).

L1LTBC2	L0LTBC2	Description
0	0	Level 1 (initial value)
0	1	Level 2
1	0	Level 3
1	1	Level 4

[Note]
A write instruction to the interrupt level control register 7 (ILC7) should be executed after disabling the interrupt.
Except this way, the write instruction to the interrupt level control register 7(ILC7) is not guaranteed.

5.2.19 External Interrupt Control Registers 01 (EXICON01)

Address: 0F040H
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
EXICON0	EXI7E0	EXI6E0	EXI5E0	EXI4E0	EXI3E0	EXI2E0	EXI1E0	EXI0E0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
EXICON1	EXI7E1	EXI6E1	EXI5E1	EXI4E1	EXI3E1	EXI2E1	EXI1E1	EXI0E1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

EXICON01 is a special function register (SFR) used to select the interrupt edge of external interrupt.

Description of Bits

- **EXI7-0E0**(bits 7 to 0)**, EXI7-0E1** (bits 15 to 8)
  The EXI7-0E0 and EXI7-0E1 bits are used to select the interrupt disabled mode, falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode for EXI0 to 7, respectively.
  For the EXIn setting, the EXInE0 and EXInE1 bits determine the interrupt mode of the external interrupt (Example: When EXI0E0 = "0" and EXI0E1 = "1", the external interrupt is in the rising-edge interrupt mode).

EXI7-0E1	**EXI7-0E0**	Description
0	0	Interrupt disabled (initial value)
0	1	Falling-edge interrupt
1	0	Rising-edge interrupt
1	1	Both-edge interrupt

5.2.20 External Interrupt Control Registers 23 (EXICON23)

Address: 0F042H
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
EXICON2	EXI7SM	EXI6SM	EXI5SM	EXI4SM	EXI3SM	EXI2SM	EXI1SM	EXI0SM
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
EXICON3	EXI7FL	EXI6FL	EXI5FL	EXI4FL	EXI3FL	EXI2FL	EXI1FL	EXI0FL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

EXICON23 is a special function register (SFR) used to select the interrupt edge of external interrupt.

Description of Bits

- **EXI7-0SM** (bits 7 to 0)
  The EXI7-0SM bits are used to select detection of signal edge for an external interrupt with or without sampling. The sampling clock is T16KHz of the low-speed time base counter (LTBC).

EXI7SM to EXI0SM	Description
0	Detects the input signal edge for an external interrupt without sampling (initial value).
1	Detects with sampling

[Note]
In STOP mode, since the sampling clock (T16KHZ) stops, no sampling is performed regardless of the values set in EXI7SM to EXI0SM.

- **EXI7-0FL** (bits 15 to 8)
  The EXI7-0FL bits are used to select detection of signal edge for an external interrupt with or without noise filter.

EXI7FL to EXI0FL	Description
0	Detects without noise filter (initial value)
1	Detects with noise filter

5.2.21 External Interrupt 01 Selection Register (EXI01SEL)

Address: 0F048H
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
EXI0SEL	EXI0S7	EXI0S6	EXI0S5	EXI0S4	EXI0S3	EXI0S2	EXI0S1	EXI0S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
EXI1SEL	EXI1S7	EXI1S6	EXI1S5	EXI1S4	EXI1S3	EXI1S2	EXI1S1	EXI1S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

EXI01SEL is a special function register (SFR) used to select the port used as EXI0/1.

Description of Bits

- **EXI0S3-0** (bits 3 to 0), **EXI0S7-4** (bits 7 to 4)
  The EXI0S3-0 registers are used to select the bit of the port used as EXI0.
  The EXI0S7-4 registers are used to select the group of the port used as EXI0 (Example: When EXI0S7-4 = "5" and EXI0S3-0 = "1", Port 51 is used as EXI0).

EXI0S7-4	EXI0S3-0							
	0	1	2	3	4	5	6	7
0	P00	P01	P02	P03	P04	P05	-	-
1	PXT0	PXT1	-	-	-	-	-	-
2	P20	P21	P22	P23	-	-	-	-
3	P30	P31	P32	P33	P34	P35	P36	P37
4	P40	P41	P42	P43	P44	P45	P46	P47
5	P50	P51	P52	P53	P54	P55	P56	P57

Setting other than above is prohibited.

- **EXI1S3-0** (bits 11 to 8), **EXI1S7-4** (bits 15 to 12)
  The EXI1S3-0 registers are used to select the bit of the port used as EXI1.
  The EXI1S7-4 registers are used to select the group of the port used as EXI1 (Example: When EXI1S7:4 = "5" and EXI1S3-0 = "1", Port 51 is used as EXI1).

EXI1S7-4	EXI1S3-0							
	0	1	2	3	4	5	6	7
0	P00	P01	P02	P03	P04	P05	-	-
1	PXT0	PXT1	-	-	-	-	-	-
2	P20	P21	P22	P23	-	-	-	-
3	P30	P31	P32	P33	P34	P35	P36	P37
4	P40	P41	P42	P43	P44	P45	P46	P47
5	P50	P51	P52	P53	P54	P55	P56	P57

Setting other than above is prohibited.

[Note]
A write instruction to the External Interrupt Selection Register(EXI01SEL) should be executed after disabling the interrupt to be changed. And the request bit which correspond to the request register need to be cleared after the change.

5.2.22 External Interrupt 23 Selection Register (EXI23SEL)

Address: 0F04AH
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
EXI2SEL	EXI2S7	EXI2S6	EXI2S5	EXI2S4	EXI2S3	EXI2S2	EXI2S1	EXI2S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
EXI3SEL	EXI3S7	EXI3S6	EXI3S5	EXI3S4	EXI3S3	EXI3S2	EXI3S1	EXI3S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

EXI23SEL is a special function register (SFR) used to select the port used as EXI2/3.

Description of Bits

- **EXI2S3-0** (bits 3 to 0), **EXI2S7-4** (bits 7 to 4)
  The EXI2S3-0 registers are used to select the bit of the port used as EXI2.
  The EXI2S7-4 registers are used to select the group of the port used as EXI2 (Example: When EXI2S7-4 = "5" and EXI2S3-0 = "1", Port 51 is used as EXI2).

EXI2S7-4	EXI2S3-0							
	0	1	2	3	4	5	6	7
0	P00	P01	P02	P03	P04	P05	-	-
1	PXT0	PXT1	-	-	-	-	-	-
2	P20	P21	P22	P23	-	-	-	-
3	P30	P31	P32	P33	P34	P35	P36	P37
4	P40	P41	P42	P43	P44	P45	P46	P47
5	P50	P51	P52	P53	P54	P55	P56	P57

Setting other than above is prohibited.

- **EXI3S3-0** (bits 11 to 8), **EXI3S7-4** (bits 15 to 12)
  The EXI3S3-0 registers are used to select the bit of the port used as EXI3.
  The EXI3S7-4 registers are used to select the group of the port used as EXI3 (Example: When EXI3S7-4 = "5" and EXI3S3-0 = "1", Port 51 is used as EXI3).

EXI3S7-4	EXI3S3-0							
	0	1	2	3	4	5	6	7
0	P00	P01	P02	P03	P04	P05	-	-
1	PXT0	PXT1	-	-	-	-	-	-
2	P20	P21	P22	P23	-	-	-	-
3	P30	P31	P32	P33	P34	P35	P36	P37
4	P40	P41	P42	P43	P44	P45	P46	P47
5	P50	P51	P52	P53	P54	P55	P56	P57

Setting other than above is prohibited.

[Note]
A write instruction to the External Interrupt Selection Register(EXI23SEL) should be executed after disabling the interrupt to be changed. And the request bit which correspond to the request register need to be cleared after the change.

5.2.23 External Interrupt 45 Selection Register (EXI45SEL)

Address: 0F04CH
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
EXI4SEL	EXI4S7	EXI4S6	EXI4S5	EXI4S4	EXI4S3	EXI4S2	EXI4S1	EXI4S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
EXI5SEL	EXI5S7	EXI5S6	EXI5S5	EXI5S4	EXI5S3	EXI5S2	EXI5S1	EXI5S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

EXI45SEL is a special function register (SFR) used to select the port used as EXI4/5.

Description of Bits

- **EXI4S3-0** (bits 3 to 0), **EXI4S7-4** (bits 7 to 4)
  The EXI4S3-0 registers are used to select the bit of the port used as EXI4.
  The EXI4S7-4 registers are used to select the group of the port used as EXI4 (Example: When EXI4S7-4 = "5" and EXI4S3-0 = "1", Port 51 is used as EXI4).

EXI4S7-4	EXI4S3-0							
	0	1	2	3	4	5	6	7
0	P00	P01	P02	P03	P04	P05	-	-
1	PXT0	PXT1	-	-	-	-	-	-
2	P20	P21	P22	P23	-	-	-	-
3	P30	P31	P32	P33	P34	P35	P36	P37
4	P40	P41	P42	P43	P44	P45	P46	P47
5	P50	P51	P52	P53	P54	P55	P56	P57

Setting other than above is prohibited.

- **EXI5S3-0** (bits 11 to 8), **EXI5S7-4** (bits 15 to 12)
  The EXI5S3-0 registers are used to select the bit of the port used as EXI5.
  The EXI5S7-4 registers are used to select the group of the port used as EXI5 (Example: When EXI5S7-4 = "5" and EXI5S3-0 = "1", Port 51 is used as EXI5).

EXI5S7-4	EXI5S3-0							
	0	1	2	3	4	5	6	7
0	P00	P01	P02	P03	P04	P05	-	-
1	PXT0	PXT1	-	-	-	-	-	-
2	P20	P21	P22	P23	-	-	-	-
3	P30	P31	P32	P33	P34	P35	P36	P37
4	P40	P41	P42	P43	P44	P45	P46	P47
5	P50	P51	P52	P53	P54	P55	P56	P57

Setting other than above is prohibited.

[Note]
A write instruction to the External Interrupt Selection Register(EXI45SEL) should be executed after disabling the interrupt to be changed. And the request bit which correspond to the request register need to be cleared after the change.

5.2.24 External Interrupt 67 Selection Register (EXI67SEL)

Address: 0F04EH
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
EXI6SEL	EXI6S7	EXI6S6	EXI6S5	EXI6S4	EXI6S3	EXI6S2	EXI6S1	EXI6S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
EXI7SEL	EXI7S7	EXI7S6	EXI7S5	EXI7S4	EXI7S3	EXI7S2	EXI7S1	EXI7S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

EXI67SEL is a special function register (SFR) used to select the port used as EXI6/7.

Description of Bits

- **EXI6S3-0** (bits 3 to 0), **EXI6S7-4** (bits 7 to 4)
  The EXI6S3-0 registers are used to select the bit of the port used as EXI6.
  The EXI6S7-4 registers are used to select the group of the port used as EXI6 (Example: When EXI6S7-4 = "5" and EXI6S3-0 = "1", Port 51 is used as EXI6).

EXI6S7-4	EXI6S3-0							
	0	1	2	3	4	5	6	7
0	P00	P01	P02	P03	P04	P05	-	-
1	PXT0	PXT1	-	-	-	-	-	-
2	P20	P21	P22	P23	-	-	-	-
3	P30	P31	P32	P33	P34	P35	P36	P37
4	P40	P41	P42	P43	P44	P45	P46	P47
5	P50	P51	P52	P53	P54	P55	P56	P57

Setting other than above is prohibited.

- **EXI7S3-0** (bits 11-8), **EXI7S7-4** (bits 15-12)
  The EXI7S3-0 registers are used to select the bit of the port used as EXI7.
  The EXI7S7-4 registers are used to select the group of the port used as EXI7 (Example: When EXI7S7-4 = "5" and EXI7S3-0 = "1", Port 51 is used as EXI7).

EXI7S7-4	EXI7S3-0							
	0	1	2	3	4	5	6	7
0	P00	P01	P02	P03	P04	P05	-	-
1	PXT0	PXT1	-	-	-	-	-	-
2	P20	P21	P22	P23	-	-	-	-
3	P30	P31	P32	P33	P34	P35	P36	P37
4	P40	P41	P42	P43	P44	P45	P46	P47
5	P50	P51	P52	P53	P54	P55	P56	P57

Setting other than above is prohibited.

[Note]
A write instruction to the External Interrupt Selection Register(EXI67SEL) should be executed after disabling the interrupt to be changed. And the request bit which correspond to the request register need to be cleared after the change.

5.3 Description of Operation

5.3.1 Interrupt Source

With the exception of the watchdog timer interrupt (WDTINT), interrupt enable/disable for 37 sources is controlled by the master interrupt enable flag (MIE) and the individual interrupt enable registers (IE0 to 7). WDTINT is a non-maskable interrupt.
When the interrupt conditions are satisfied, the program calls a branching destination address from the vector table determined for each interrupt source and the interrupt shift cycle starts to branch to the interrupt processing routine.
Table 5-1 lists the interrupt sources.

Table 5-1 Interrupt Sources

Interrupt priority level	Interrupt source	Symbol	Vector table address
1	Watchdog timer interrupt	WDTINT	0008H
5	EXI0 interrupt	EXI0INT	0010H
6	EXI1 interrupt	EXI1INT	0012H
7	EXI2 interrupt	EXI2INT	0014H
8	EXI3 interrupt	EXI3INT	0016H
9	EXI4 interrupt	EXI4INT	0018H
10	EXI5 interrupt	EXI5INT	001AH
11	EXI6 interrupt	EXI6INT	001CH
12	EXI7 interrupt	EXI7INT	001EH
13	Synchronous serial port 0 interrupt	SIO0INT	0020H
14	Synchronous serial port 0 interrupt with FIFO	SIOF0INT	0022H
15	I2C bus 0 interrupt	I2C0INT	0024H
16	I2C bus 1 interrupt	I2C1INT	0026H
17	UART0 reception interrupt	UA0INT	0028H
18	UART0 transmission interrupt	UA1INT	002AH
19	UART0 interrupt with FIFO	UAF0INT	002CH
26	low-speed oscillation clock switching interrupt	LOSCINT	003AH
27	VLS interrupt	VLSINT	003CH
28	Melody 0 interrupt	MD0INT	003EH
29	Successive approximation type A/D converter interrupt	SADINT	0040H
30	RC oscillation type A/D converter interrupt	RADINT	0042H
33	Comparator 0 interrupt	CMP0INT	0048H
34	Comparator 1 interrupt	CMP1INT	004AH
37	Timer 0 interrupt	TM0INT	0050H
38	Timer 1 interrupt	TM1INT	0052H
39	Timer 2 interrupt	TM2INT	0054H
40	Timer 3 interrupt	TM3INT	0056H
41	Timer 4 interrupt	TM4INT	0058H
42	Timer 5 interrupt	TM5INT	005AH
43	Timer 6 interrupt	TM6INT	005CH

44	Timer 7 interrupt	TM7INT	005EH
45	Function timer 0 interrupt	FTM0INT	0060H
46	Function timer 1 interrupt	FTM1INT	0062H
47	Function timer 2 interrupt	FTM2INT	0064H
48	Function timer 3 interrupt	FTM3INT	0066H
53	Time base counter 0 interrupt	LTB0INT	0070H
54	Time base counter 1 interrupt	LTB1INT	0072H
55	Time base counter 2 interrupt	LTB2INT	0074H

[Note]

•When multiple interrupts are generated concurrently, they are processed starting from the highest interrupt setting level and, among the same interrupt setting level, from the highest priority level. Interrupts with lower interrupt setting level or lower priority level will be pending.

•Please define vector tables for all unused interrupts for fail safe.

5.3.2 Maskable Interrupt Processing

When an interrupt is generated with the MIE flag set to "1", the following processing is executed by hardware and the processing of program shifts to the interrupt destination.

(1) Transfer the program counter (PC) to ELR1
(2) Transfer CSR to ECSR1
(3) Transfer PSW to EPSW1
(4) Set the MIE flag to "0"
(5) Set the ELEVEL field to"1"
(6) Load the interrupt start address into PC

5.3.3 Non-Maskable Interrupt Processing

When an interrupt is generated regardless of the state of MIE flag, the following processing is performed by hardware and the processing of program shifts to the interrupt destination.

(1) Transfer PC to ELR2
(2) Transfer CSR to ECSR2
(3) Transfer PSW to EPSW2
(4) Set the ELEVEL field to"2"
(5) Load the interrupt start address into PC

5.3.4 Software Interrupt Processing

A software interrupt is generated as required within an application program. When the SWI instruction is performed within the program, a software interrupt is generated, the following processing is performed by hardware, and the processing program shifts to the interrupt destination. The vector table is specified by the SWI instruction.

(1) Transfer PC to ELR1
(2) Transfer CSR to ECSR1
(3) Transfer PSW to EPSW1
(4) Set the MIE flag to "0"
(5) Set the ELEVEL field to"1"
(6) Load the interrupt start address into PC

[Reference]
For the MIE flag, Program Counter (PC), CSR, PSW, and ELEVEL, see "nX-U16/100 Core Instruction Manual".

5.3.5 Notes on Interrupt Routine

Notes are different in programming depending on whether a subroutine is called or not by the program in executing an interrupt routine, whether multiple interrupts are enabled or disabled, and whether such interrupts are maskable or non-maskable.

Status A: Maskable interrupt is being processed

A-1: When a subroutine is not called by the program in executing an interrupt routine

A-1-1: When multiple interrupts are disabled

•Processing immediately after the start of interrupt routine execution

No specific notes.

•Processing at the end of interrupt routine execution

Specify the RTI instruction to return the contents of the ELR register to the PC and those of the EPSW register to PSW.

A-1-2: When multiple interrupts are enabled

•Processing immediately after the start of interrupt routine execution

Specify "PUSH ELR, EPSW" to save the interrupt return address and the PSW status in the stack.

•Processing at the end of interrupt routine execution

Specify "POP PC, PSW" instead of the RTI instruction to return the contents of the stack to PC and PSW.

Example of description: Status A-1-1

```
Intrpt_A-1-1:          ; A-1-1 state
    DI                 ; Disable interrupt
    :
    :
    :
    RTI                ; Return PC from ELR
                       ; Return PSW form EPSW
                       ; End
```

Example of description: Status A-1-2

```
Intrpt_A-1-2:          ; Start
  PUSH  ELR,           ; Save ELR and EPSW at the
EPSW                   beginning
  EI                   ; Enable interrupt
  :
  :
  :
  :
  :
  POP   PC, PSW        ; Return PC from the stack
                       ; Return PSW from the stack
                       ; End
```

A-2: When a subroutine is called by the program in executing an interrupt routine

A-2-1: When multiple interrupts are disabled

•Processing immediately after the start of interrupt routine execution

Specify the "PUSH LR" instruction to save the subroutine return address in the stack.

•Processing at the end of interrupt routine execution

Specify "POP LR" immediately before the RTI instruction to return from the interrupt processing after returning the subroutine return address to LR.

A-2-2: When multiple interrupts are enabled

•Processing immediately after the start of interrupt routine execution

Specify "PUSH LR, ELR, EPSW" to save the interrupt return address, the subroutine return address, and the EPSW status in the stack.

•Processing at the end of interrupt routine execution

Specify "POP PC, PSW, LR" instead of the RTI instruction to return the saved data of the interrupt return address to PC, the saved data of EPSW to PSW, and the saved data of LR to LR.

Example of description: Status A-2-2

```
Intrpt_A-2-2:           ; Start
  PUSH                  ; Save ELR, EPSW, LR
ELR,EPSW,LR             at the beginning

  EI                    ; Enable interrupt
  :
  :
  :

  BL Sub_1              ; Call subroutine Sub_1
  :
  POP   PC, PSW, LR     ; Return PC from the stack
                        ; Return PSW from the stack
                        ; Return LR from the stack
                        ; End
```

```
Sub_1:          ;
DI              ; Disable interrupt
                :
                :
                :
RT              ; Return PC from LR
                ; End of subroutine
```

Status B: Non-maskable interrupt is being processed

B-1: When no instruction is executed in an interrupt routine
- •Processing immediately after the start of interrupt routine execution
  Specify the RTI instruction to return the contents of the ELR register to the PC and those of the EPSW register to PSW.

B-2: When one or more instructions are executed in an interrupt routine

B-2-1: When a subroutine is not called by the program in executing an interrupt routine
- •Processing immediately after the start of interrupt routine execution
  Specify "PUSH ELR, EPSW" to save the interrupt return address and the PSW status in the stack.
- •Processing at the end of interrupt routine execution
  Specify "POP PC, PSW" instead of the RTI instruction to return the saved data of the interrupt return address to PC and the saved data of EPSW to PSW.

B-2-2: When a subroutine is called by the program in executing an interrupt routine
- •Processing immediately after the start of interrupt routine execution
  Specify "PUSH LR, ELR, EPSW" to save the interrupt return address, the subroutine return address, and the EPSW status in the stack.
- •Processing at the end of interrupt routine execution
  Specify "POP PC, PSW, LR" instead of the RTI instruction to return the saved data of the interrupt return address to PC, the saved data of EPSW to PSW, and the saved data of LR to LR.

Example of description: Status B-1

```
Intrpt_B-1:          ; B-1 state
    RTI              ; Return PC from ELR
                     ; Return PSW form EPSW
                     ; End
```

Example of description: B-2-1

```
Intrpt_B-2-1:        ; Start
  PUSH  ELR,         ; Save ELR and EPSW at the
EPSW                 beginning
  :
  :
  :
  POP   PC, PSW      ; Return PC from the stack
                     ; Return PSW from the stack
                     ; End
```

Example of description: B-2-2

```
Intrpt_B-2-2:              ; Start
  PUSH                     ; Save ELR, EPSW, LR
ELR,EPSW,LR                at the beginning
  :
  :
  :

  BL Sub_1                 ; Call subroutine Sub_1
  :
  POP   PC, PSW, LR        ; Return PC from the stack
                           ; Return PSW from the stack
                           ; Return LR from the stack
                           ; End
```

```
Sub_1:          ;
                :
                :
                :
                :
RT              ; Return PC from LR
                ; End of subroutine
```

5.3.6 Interrupt Processing When Interrupt Level Control Enabled

(1) Interrupt processing

The interrupt handler carries out the following processing.

i. The following processing is made when multiple interrupts are enabled.
When a higher level interrupt request occurs, that request should be processed with priority. For this reason, the general-purpose registers are saved to memory and the EPW and EPSW registers are pushed in order to retain the processor state at return.

ii. When multiple interrupts are ready to be processed, the EI instruction is executed to enable the processor interrupt.

(2) Return from interrupt

The interrupt handler carries out the following processing.

i. After the desired processing is completed by the interrupt, the processor interrupt is disabled.

ii. A write access is made to the current interrupt request level register (CIL) to clear the highest current interrupt request level.

iii. If the interrupt is in the highest level, the general-purpose registers are restored from memory, and the RTI instruction is executed to return from the interrupt. Otherwise, the general-purpose registers are restored from memory, and the PC and PSW registers are popped.

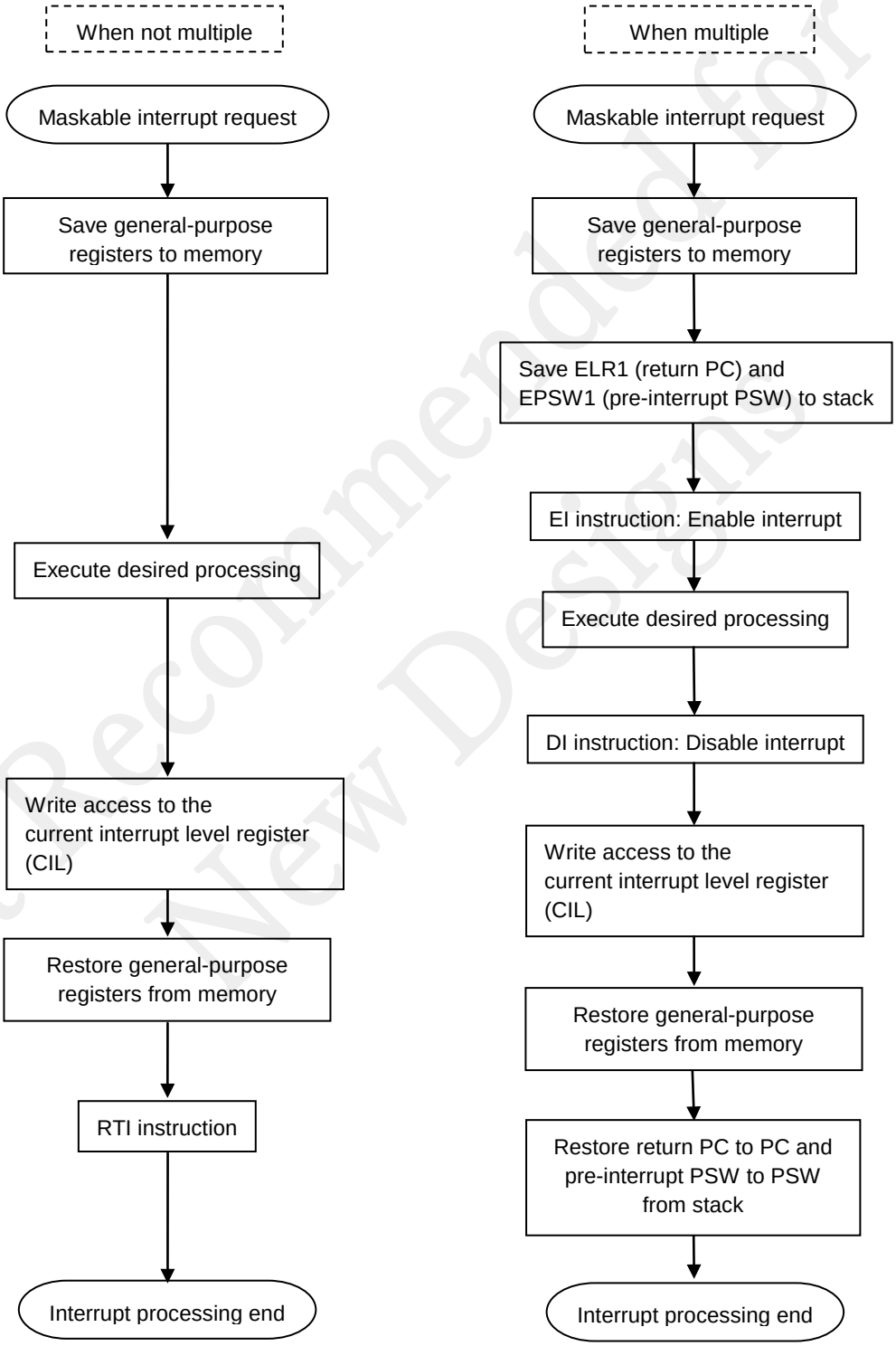
The following processing is made on the hardware.

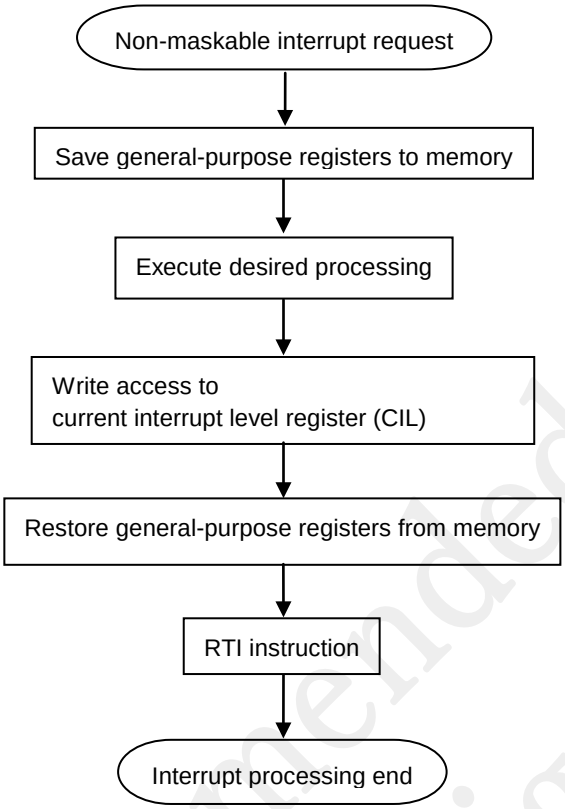
i. When a write access is made to the current interrupt request level register (CIL), the highest order set bit of the CIL register is cleared.

ii. If there is an interrupt request flag with a higher interrupt level than the current interrupt request level of the CIL register among the interrupt request flags which are pending in the interrupt request register (IRQ), an interrupt request is made to the U16 processor. In this case, if there are multiple interrupt request flags with higher interrupt levels than the current interrupt request level of the CIL register, the interrupt with the highest priority is requested to the U16 processor.

5.3.7 Flow Chart (When Interrupt Level Control Enabled)

The figure below shows the flow chart of the software processing of a maskable interrupt when the interrupt level control is enabled. The EI and DI instructions allow the execution of multiple interrupts by a higher-level maskable interrupt request during the "execution of the desired processing". Note that a non-maskable interrupt can be made for a maskable interrupt regardless of the execution of EI and DI instructions due to the specification of U16 processor.





5.3.8 Interrupt Disable State

Even if the interrupt conditions are satisfied, an interrupt may not be accepted depending on the operating state. This is called an interrupt disabled state. See below for the interrupt disabled state and the handling of interrupts in this state.

Interrupt disabled state 1: Between the interrupt shift cycle and the instruction at the beginning of the interrupt routine

When the interrupt conditions are satisfied in this interval, an interrupt is generated immediately following the execution of the instruction at the beginning of the interrupt routine corresponding to the interrupt that has already been enabled.

Interrupt disabled state 2: Between the DSR prefix instruction and the next instruction

When the interrupt conditions are satisfied in this interval, an interrupt is generated immediately after execution of the instruction following the DSR prefix instruction.

For the DSR prefix instruction, see "nX-U16/100 Core Instruction Manual".

5.3.9 External Interrupt

When an interrupt edge selected with the external interrupt control register 0/1 (EXICON01) occurs at one of external interrupts EXI0 to 7, any of the maskable EXI0 to EXI7 interrupts (EXI0INT to EXI7INT) occurs. It is possible to set the external interrupt control register 2/3 (EXICON23) to perform the filtering with noise filtering and/or sampling (2ϕ sampling with T16KHZ that is 2 dividing of LSCLK) for an external pin input. But the signal for the trigger of FTM is filtered by noise filter/not sampling without relation for control of EXICON23.

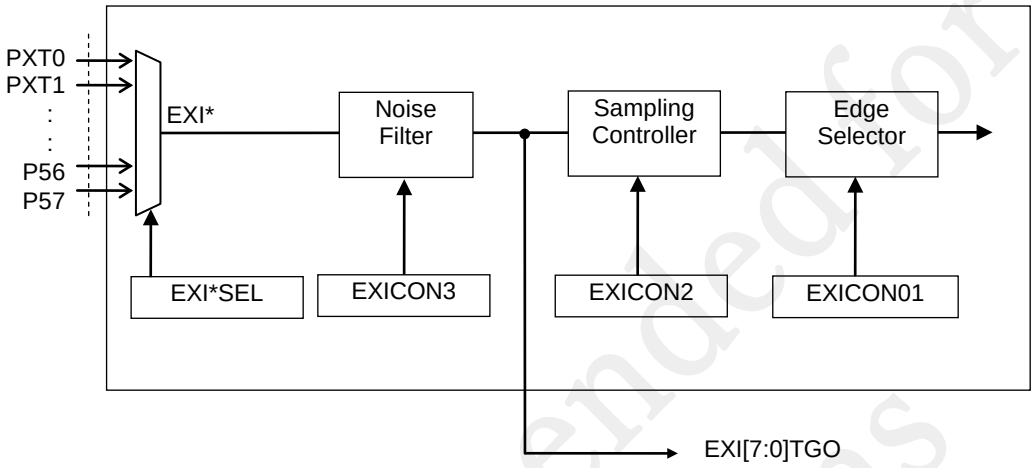
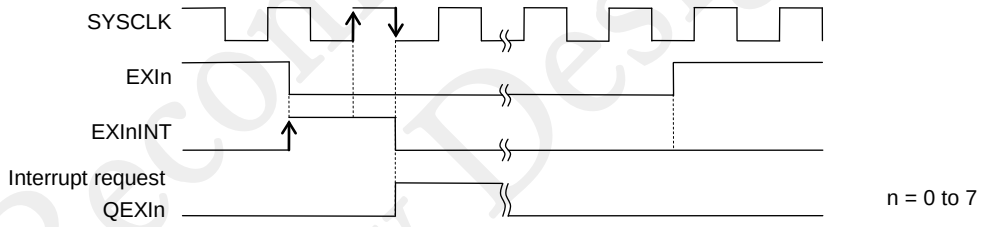
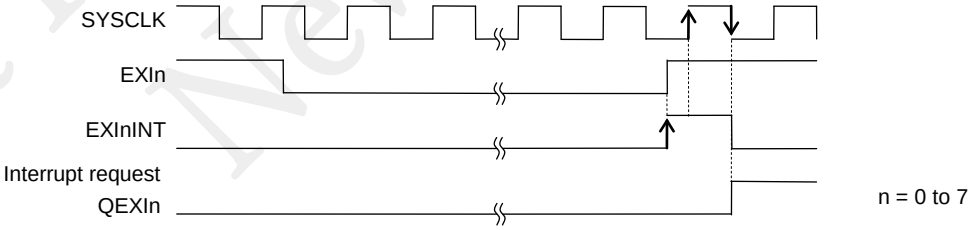


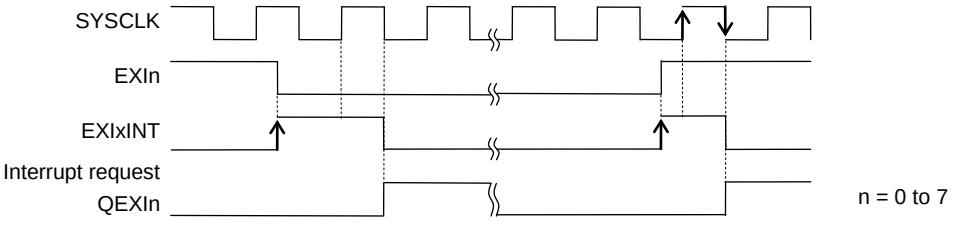
Figure 5-2 shows the interrupt generation timing in rising-edge interrupt mode, in falling-edge interrupt mode, and in both-edge interrupt mode without sampling, and in rising-edge interrupt mode with sampling.



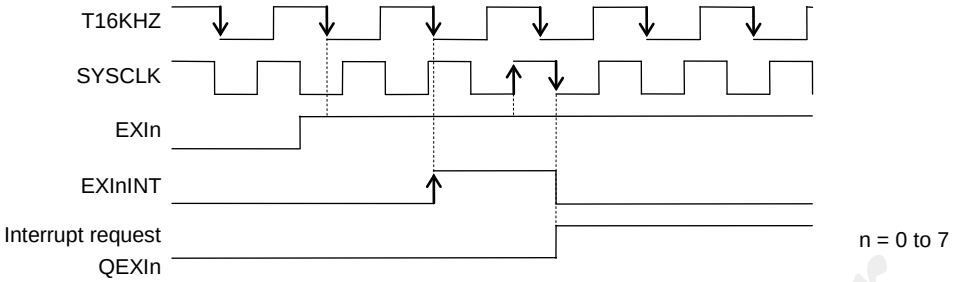
(a) When Falling-Edge Interrupt Mode without Sampling is Selected



(b) When Rising-Edge Interrupt Mode without Sampling is Selected



(c) When Both-Edge Interrupt Mode without Sampling is Selected



(d) When Rising-Edge Interrupt Mode with Sampling is Selected

Figure 5-2 External Interrupt Generation Timing

Chapter 6

Clock Generation Circuit

6 Clock Generation Circuit

6.1 General Description

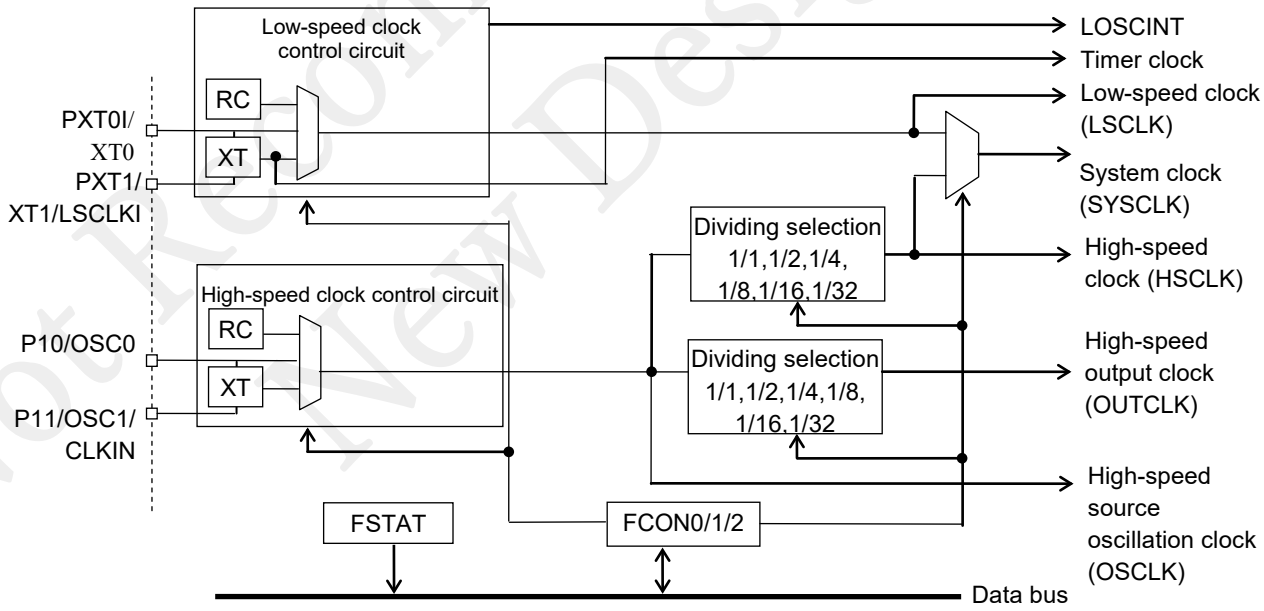
The clock generation circuit generates and provides the low-speed clock (LSCLK), the high-speed clock (HSCLK), the system clock (SYSCLK), and the high-speed output clock (OUTCLK). LSCLK and HSCLK are time base clocks for the peripheral circuits, SYSCLK is a basic operation clock of CPU, and OUTCLK is a clock that is output from a port.
For the OUTCLK output port, see Chapter 21, "Port 4", Chapter 22, "Port 5".
For the STOP mode described in this chapter, see Chapter 4, "Power Management".

6.1.1 Features

- Low-speed clock generation circuit:
  - Crystal oscillation mode
  - Built-in RC oscillation mode
  - External clock input mode
  - Interrupt generation at low-speed clock mode shift
- High-speed clock generation circuit:
  - Crystal/ceramic oscillation mode
  - Built-in RC oscillation mode
  - External clock input mode

6.1.2 Configuration

Figure 6-1 shows the configuration of the clock generation circuit.



FCON0 : Frequency control register 0
FCON1 : Frequency control register 1
FCON2 : Frequency control register 2
FSTAT : Frequency status register

Figure 6-1 Configuration of Clock Generation Circuit

[Note]
After power-on or system reset, the operation starts by the clock supplied from the built-in high-speed RC clock generation circuit. At initialization by software, set the FCON0, FCON1 and FCON2 register to switch to the required clock.

6.1.3 List of Pins

Pin Name	I/O	Function
XT0	I	Pin for connecting a crystal for low-speed clock.
XT1/ LSCLKI	I/O	Pin for connecting a crystal for low-speed clock. Used for low-speed external clock input
OSC0	I	Pin for connecting a crystal/ceramic oscillator for high-speed clock.
OSC1/ CLKIN	I/O	Pin for connecting a crystal/ceramic oscillator for high-speed clock. Used for high-speed external clock input.

6.1.4 Clock Configuration Diagram

Figure 6-2 shows the clock system diagram.

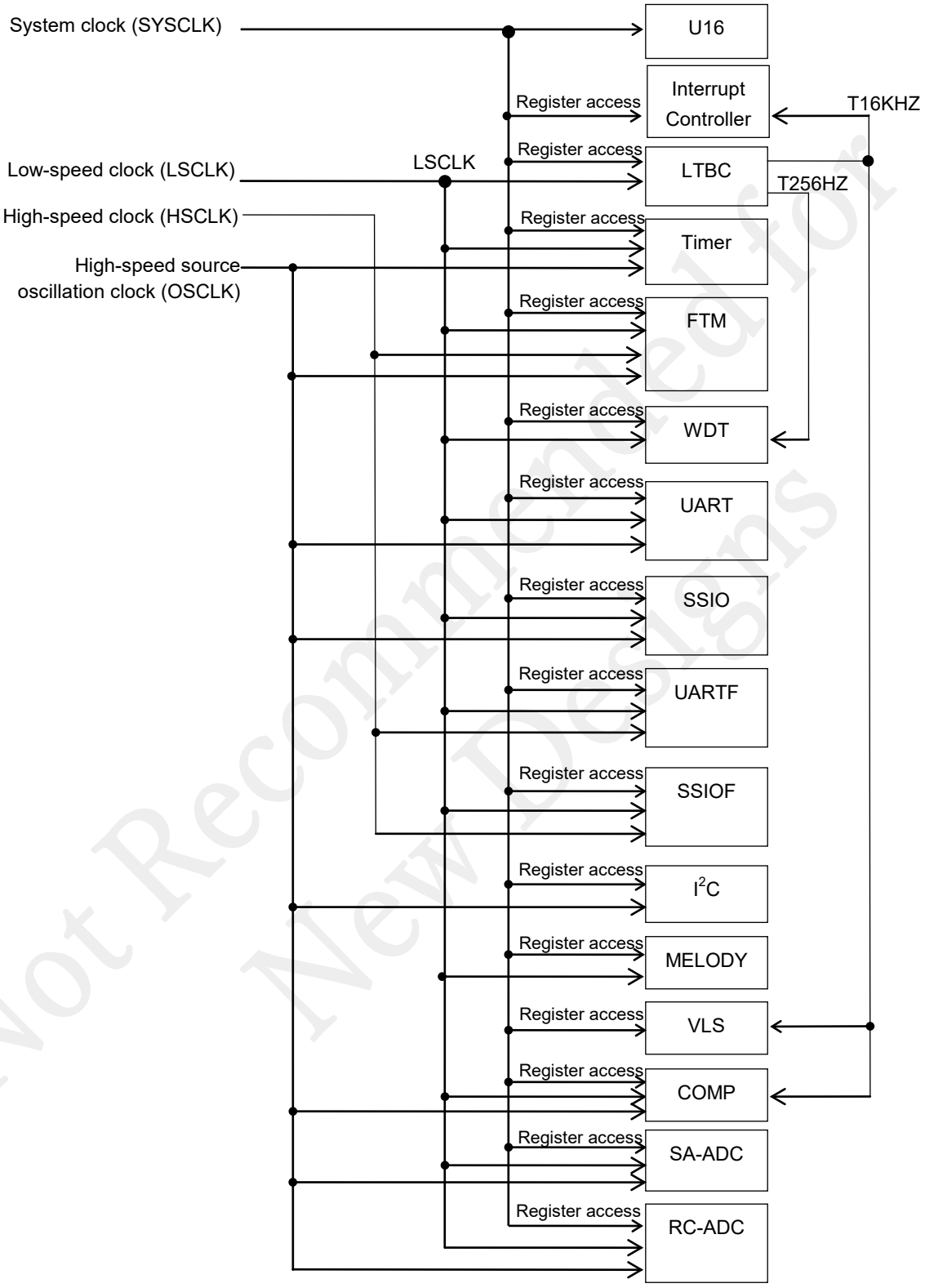


Figure 6-2 Clock System Diagram

6.2 Description of Registers

6.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F002	Frequency control register 01	FCON0	FCON01	R/W	8/16	73
0F003		FCON1		R/W	8	03
0F004	Frequency control register 23	FCON2	FCON23	R/W	8/16	02
0F005		FCON3		R/W	8	00
0F00A	Frequency status register	FSTAT	–	R	8	06

6.2.2 Frequency Control Register 01 (FCON01)

Address: 0F002H
Access: R/W
Access size: 8/16 bit
Initial value: 0373H

	7	6	5	4	3	2	1	0
FCON0	OUTC2	OUTC1	OUTC0	OSCM1	OSCM0	SYSC2	SYSC1	SYSC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	1	1	1	0	0	1	1

	15	14	13	12	11	10	9	8
FCON1	HOSST	LOSST	–	–	LOSCON	–	ENOSC	SYSCLK
R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	1	1

FCON01 is a special function register (SFR) used to control the high-speed clock generation circuit and to select system clock.

Description of Bits

- **SYSC2-0** (bits 2 to 0)
  The SYSC2-0 bits are used to select the frequency of the high-speed clock (HSCLK) used for system clock and peripheral circuits. OSCLK, 1/2OSCLK, 1/4OSCLK, 1/8OSCLK, 1/16OSCLK, or 1/32OSCLK can be selected.
  At system reset, 1/8OSCLK is selected.

SYSC2	SYSC1	SYSC0	Description
0	0	0	OSCLK
0	0	1	1/2OSCLK
0	1	0	1/4OSCLK
0	1	1	1/8OSCLK (initial value)
1	0	0	1/16OSCLK
1	0	1	1/32OSCLK
1	1	0	Setting prohibited (1/32OSCLK)
1	1	1	Setting prohibited (1/32OSCLK)

- **OSCM1-0** (bits 4 to 3)
  The OSCM1-0 bits are used to select the high-speed clock mode. Crystal/ceramic oscillation mode, built-in RC oscillation mode, or external clock input mode can be selected.
  OSCM1 and OSCM0 can be rewritten only when high-speed oscillation is being stopped (ENOSC bit of FCON1 is "0").
  At system reset, the built-in RC oscillation mode is selected.
  When switching the high-speed clock mode, please first stop high-speed oscillation(set the ENOSC bit of FCON1 register to "0") and then switch the system clock back to the low-speed clock (set SYSCLK bits of the FCON1 register to "0").

OSCM1	OSCM0	Description
0	0	Setting prohibited (the setting is ignored and the previous value is held)
0	1	High-speed Crystal/ceramic oscillation mode
1	0	High-speed Built-in RC oscillation mode (initial value)
1	1	External high-speed clock input mode

- **OUTC2-0** (bits 7 to 5)
  The OUTC2, OUTC1, and OUTC0 bits select the frequency of the high-speed output clock (OUTCLK) output when the secondary function of the port is used. 1/1OSCLK, 1/2OSCLK, 1/4OSCLK, 1/8OSCLK, 1/16OSCLK, or 1/32OSCLK can be selected.
  At system reset, 1/8OSCLK is selected.

OUTC2	OUTC1	OUTC0	Description
0	0	0	1/1OSCLK
0	0	1	1/2OSCLK
0	1	0	1/4OSCLK
0	1	1	1/8OSCLK (initial value)
1	0	0	1/16OSCLK
1	0	1	1/32OSCLK
1	1	0	Setting prohibited (1/32OSCLK)
1	1	1	Setting prohibited (1/32OSCLK)

- **SYSCLK** (bit 8)
  The SYSCLK bit is used to select system clock. The low-speed clock (LSCLK) or the HSCLK (1/n OSCLK: n = 1,2, 4, 8, 16, 32) selected by the FCON0 high-speed clock frequency selection bit (SYSC2,1,0) can be selected.
  When the oscillation of high-speed clock is stopped (ENOSC bit = "0"), the SYSCLK bit is fixed to "0" and the low-speed clock (LSCLK) is selected for system clock.

SYSCLK	Description
0	LSCLK
1	HSCLK (initial value)

- **ENOSC** (bit 9)
  The ENOSC bit is used to select enable/disable of the oscillation of the high-speed clock oscillator circuit.

ENOSC	Description
0	Disables high-speed oscillation
1	Enables high-speed oscillation (initial value)

- **LOSCON** (bit 11)
  The LOSCON bit also permits the low-speed crystal oscillator circuit to oscillate when the low-speed built-in RC oscillation mode is selected. When LOSCON is turned to "1", the low-speed crystal oscillator circuit is enabled to oscillate at the same time even though the built-in RC oscillation mode is selected by the XTM1 or XTM0 bit.
  Note that the low-speed crystal oscillation clock at this time is supplied only to the timer block. Clocks selected by the XTM1 and XTM0 bits are supplied to peripherals other than the timer block. If the low-speed crystal oscillation is selected as the clock for timer block, set the LOSCON bit to "1".

LOSCON	Description
0	Prohibit low-speed crystal oscillation when the low-speed built-in RC oscillation mode is selected (initial value)
1	Permit low-speed crystal oscillation when the low-speed built-in RC oscillation mode is selected

- **LOSST** (bit 14)
  LOSST is the flag used to indicate the oscillation state of the low-speed crystal oscillator circuit.

LOSST	Description
0	The low-speed crystal oscillation has stopped, or the low-speed crystal oscillation stabilization time is being counted (initial value)
1	The low-speed crystal oscillation is in the stable state

- **HOSST** (bit 15)
  HOSST is the flag used to indicate the oscillation state of the high-speed crystal/ceramic oscillator circuit.

HOSST	Description
0	The high-speed crystal/ceramic oscillation has stopped, or the stabilization time is being counted (initial value)
1	The high-speed crystal/ceramic oscillation is in the stable state

[Note]
•When switching the high-speed clock mode using the OSCM1 and OSCM0 bits, please first stop the high-speed oscillation(set the ENOSC bit of FCON1 register to “0”) and then set the system clock to the low-speed clock (set the SYSCLK bits of the FCON1 register to "0").
• In the high-speed external clock input mode, input a clock that does not exceed 16MHz.

6.2.3 Frequency Control Register 23(FCON23)

Address: 0F004H
Access: R/W
Access size: 8/16 bits
Initial Value: 0002H

	7	6	5	4	3	2	1	0
FCON2	HFLTSEL	HFLTSEL	–	LFLTSEL	–	–	XTM1	XTM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	1	0
	15	14	13	12	11	10	9	8
FCON3	–	–	–	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FCON23 is a special function register (SFR) used to select the clock for the low-speed clock generation circuit.

Description of Bits

- **XTM1-0** (bits 1 to 0)
  The XTM1-0 bits are used to select the low-speed clock mode. Low-speed Crystal/ceramic oscillation mode, low-speed built-in RC oscillation mode, or low-speed external clock input mode can be selected. At system reset, the built-in low-speed RC oscillation mode is selected.

XTM1	XTM0	Description
0	0	Setting prohibited (the setting is ignored and the previous value is held)
0	1	Low-speed Crystal oscillation mode
1	0	Low-speed Built-in RC oscillation mode (initial value)
1	1	External low-speed clock input mode

[Note]
When switching the clock mode from the external low-speed clock input mode to a the low-speed crystal oscillation mode, set the clock mode to the low-speed crystal oscillation mode after setting the clock mode in low-speed built-in RC oscillation mode.
Also when switching the clock mode from the low-speed crystal oscillation mode to the low-speed external clock input mode, set the clock mode to the external low-speed clock input mode after setting the clock mode in low-speed build in RC oscillation mode.
If low-speed built-in RC oscillation mode is not set before setting low-speed crystal oscillation mode or external low-speed clock input mode, these functions cannot be guaranteed.

- LFLTSEL（bit 4）
  LFLTSEL bit is used to select noise filter on/off at low-speed crystal/ceramic oscillation or external low-speed clock input mode.

LFLTSEL	Description
0	Low speed clock noise filter is off (initial value)
1	Low speed clock noise filter is on

- **HFLTSEL1-0**（bit 7 to 6）
  HFLTSEL1-0 bits are used to select noise filter on/off at high-speed crystal/ceramic oscillation or external high-speed clock input mode.
  Two different elimination width are selectable. When noise filter is on at 16MHz high speed clock operation, select “High-speed clock noise filter1”.

HFLTSEL1	HFLTSEL0	Description
0	0	High speed clock noise filter is off (initial value)
0	1	High speed clock noise filter1 is on（use this setting at 16MHz operation）
1	0	High speed clock noise filter2 is on
1	1	High speed clock noise filter is off

6.2.4 Frequency Status Register (FSTAT)

Address: 0F00AH
Access: R
Access size: 8 bits
Initial value: 06H

	7	6	5	4	3	2	1	0
FSTAT	–	–	–	–	–	LOSCS	HOSCS	–
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	1	1	0

FSTAT is a special function register (SFR) used to show the clock generation circuit state.

Description of Bits

- **HOSCS** (bit 1)
  HOSCS indicates the oscillation mode of the high-speed oscillator circuit. HOSCS changes when the high-speed oscillation mode switches.
  HOSCS is always "1" if the high-speed built-in RC oscillation mode is selected by the OSCM1 or OSCM0 bit of the FCON0 register. Regardless of the high-speed oscillation mode, this becomes "1" when the mode enters the STOP mode, DEEP-HALT mode, HALT-H mode.

HOSCS	Description
0	Operating in the high-speed crystal/ceramic oscillation mode or the external clock input mode
1	•Operating with the high-speed built-in RC oscillator circuit (initial value) •For the high-speed crystal/ceramic oscillation mode, the high-speed crystal/ceramic oscillation has stopped or the stabilization time is being counted

- **LOSCS** (bit 2)
  LOSCS indicates the oscillation mode of the low-speed oscillator circuit. LOSCS changes when the low-speed oscillation mode switches. LOSCS is always "1" if the low-speed built-in RC oscillation mode is selected by the XTM1 or XTM0 bit of the FCON2 register. Regardless of the low-speed oscillation mode, this becomes "1" when the mode enters the STOP mode.

LOSCS	Description
0	Operating in the low-speed crystal oscillation mode or the external clock input mode
1	•Operating with the low-speed built-in RC oscillator circuit (initial value) •For the low-speed crystal oscillation mode, the low-speed crystal oscillation has stopped or the stabilization time is being counted

6.3 Description of Operation

6.3.1 Low-Speed Clock

6.3.1.1 Low-Speed Built-In RC Oscillation Mode

Figure 6-3 shows the low-speed clock generation circuit configuration in the built-in RC oscillation mode.
When the RC oscillation clock is counted to 128, the low-speed oscillation clock (LSCLK) starts to be supplied.

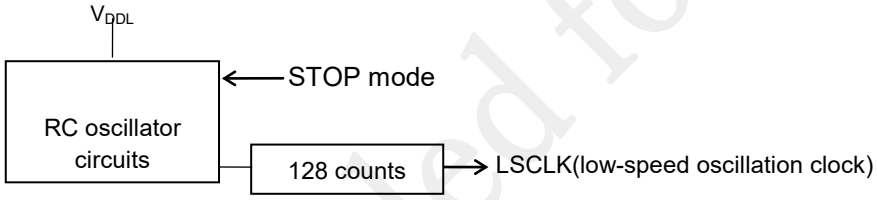


Figure 6-3 Circuit Configuration in the low-speed Built-in RC Oscillation Mode

6.3.1.2 Low-Speed Crystal Oscillation Mode

Figure 6-4 shows the low-speed clock generation circuit configuration in the crystal oscillation mode.
The low-speed clock generation circuit is provided with an external 32.768 kHz crystal. To match the oscillation frequency by using a trimmer capacitor, connect external capacitors (C_{GL} and C_{DL}) as required.

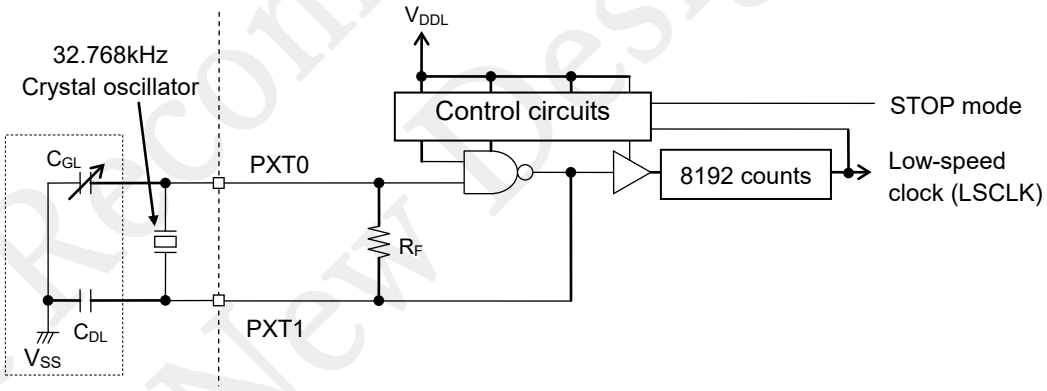


Figure 6-4 Circuit Configuration of the Crystal Oscillation Mode

[Note]
•Carefully design a board so that the crystal oscillator does not stop.
-Install the crystal oscillator near LSI as much as possible, and do not place a signal and power supply wiring that it becomes a noise source near the crystal oscillator and the wiring.
-The impedance between XT1 and XT0 might decrease by moisture uptake of circuit board in high moisture environment and condensation on the circuit board, and then the oscillation trouble may occur. Please make moisture measures such as coating the circuit board when used in such environments. The oscillation stop might be caused due to condensation.
Refer to the application note; “Precautions for MCU board design” for details.

6.3.1.3 Low-Speed External Clock Input Mode

In external low-speed clock input mode, external clock is input from the PXT1 pin. Figure 6-5 shows the circuit configuration in the external low-speed clock input mode.

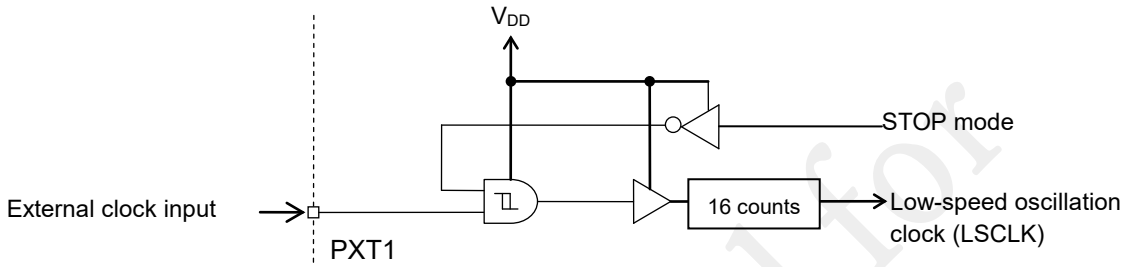


Figure 6-5 Circuit Configuration in the External Clock Input Mode

[Note]

- Since the PXT1 pin has a built-in diode to V_{DD} and V_{SS}, avoid applying voltages higher than the V_{DD} and lower than the V_{SS}.
- If the PXT1 pin is left open in low-speed external clock input mode, excessive current can flow. Therefore, make sure that the "H" level (V_{DD}) or the "L" level (V_{SS}) is input.
- For the PXT1 pin, an input clock should not exceed 36kHz.

6.3.1.4 Low-Speed Built-In RC Oscillation Mode Operation

The low-speed built-in RC oscillation mode starts by the occurrence of power ON reset.
After power-on, the built-in RC oscillation clock is counted to 128 as the low-speed clock, then the built-in RC oscillation clock (LSCLK) is supplied to the peripheral circuits.
The RC low-speed clock generation circuit stops oscillation when it shifts to the STOP mode by software. It restart oscillation when the stop mode is released by an external interrupt. The built-in RC oscillation clock is counted to 29 as the low-speed clock, then the built-in RC oscillation clock (LSCLK) is supplied to the peripheral circuits. For STOP mode, see Chapter 4, "Power Management".
Figure 6-6 shows the operation waveforms of the low-speed clock generation circuit in the built-in RC oscillation mode.

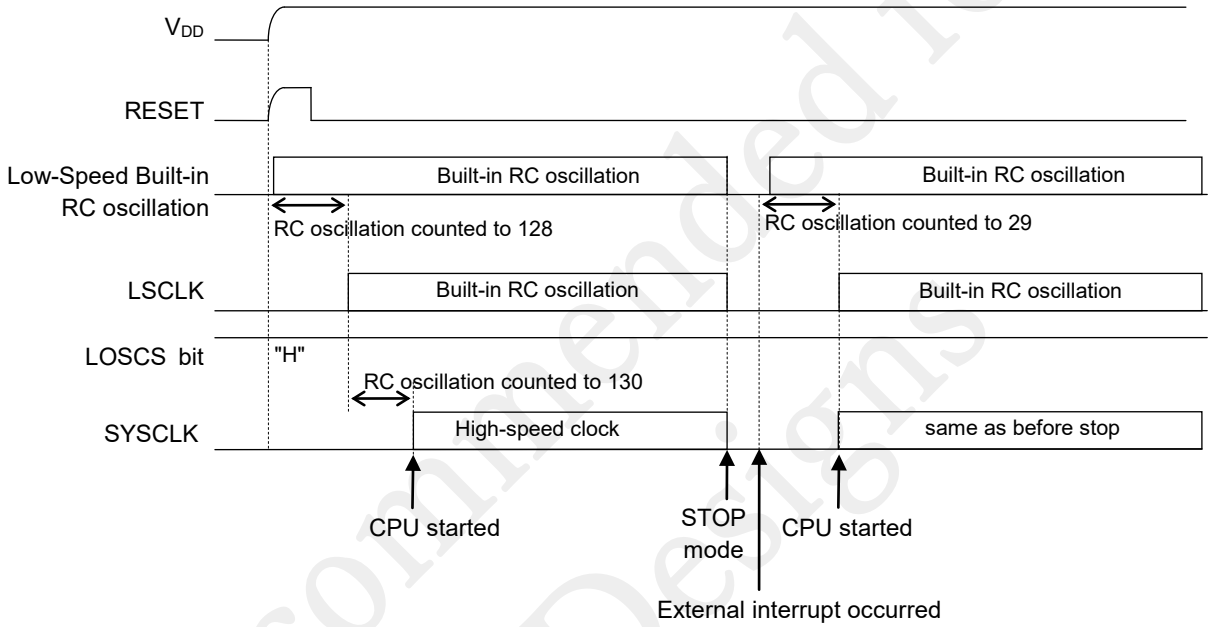


Figure 6-6 Low-Speed Clock Generation Circuit Operation (Built-In RC Oscillation Mode)

6.3.1.5 Low-Speed Crystal Oscillation Mode Operation

For the low-speed crystal oscillation, the oscillation start/stop can be controlled by the frequency control register 1 (FCON1) or 2 (FCON2).
If it sets the XTM1 and XTM0 bits of FCON2 to "01" or the LOSCON bit of FCON1 to "1", Crystal oscillator circuit starts oscillation. After waiting for the low-speed crystal oscillation start time (T_{XTL}) and the low-speed crystal oscillation stabilization time (8192 counts), the low-speed clock (LSCLK) switches from the build-in RC oscillation clock to the low-speed crystal oscillation clock. In this time, the low-speed oscillation clock switch interrupt(LOSCINT) is generated.
Refer to Chapter 4 “Power Management” for the operation at each power down mode.

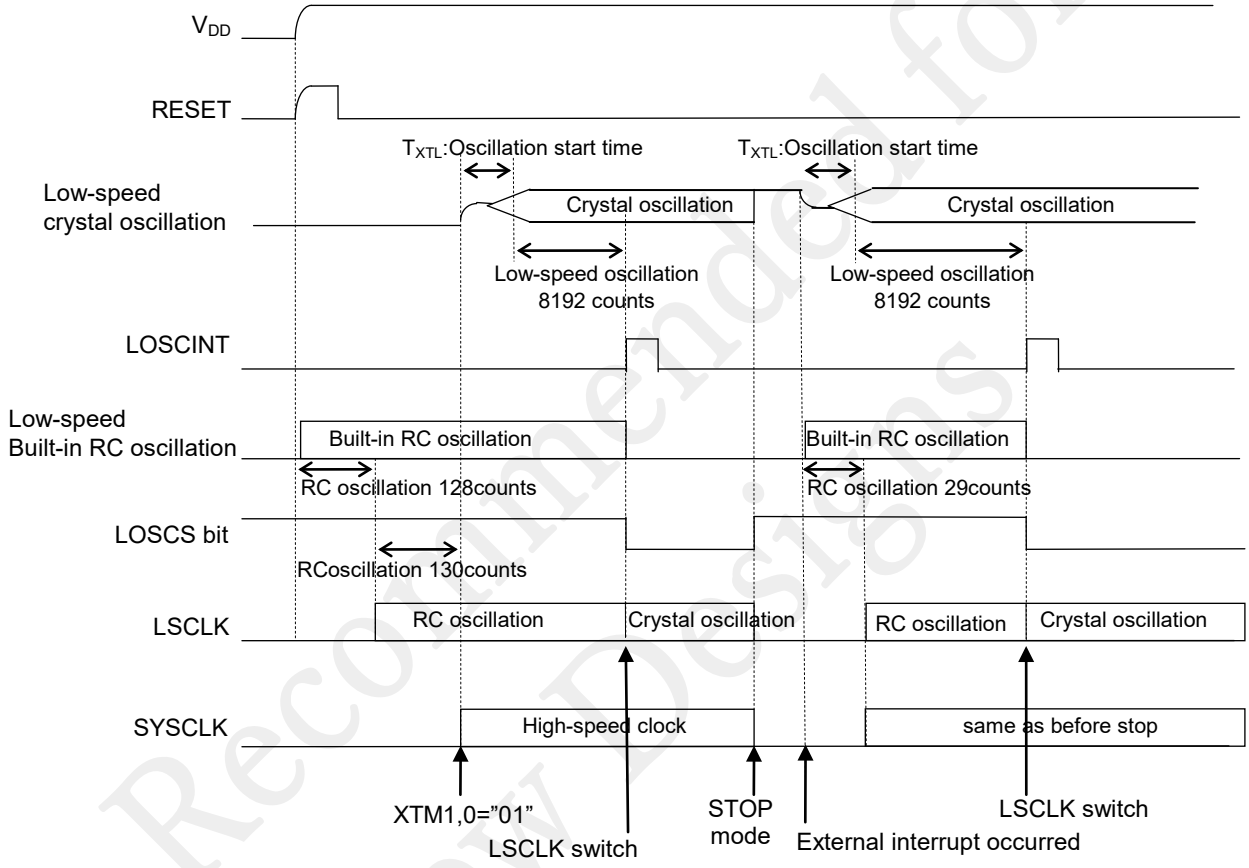


Figure 6-7 Low-Speed Clock Generation Circuit Operation (Crystal Oscillation Mode)

6.3.1.6 Low-Speed External Clock Input Mode Operation

For the low-speed external clock, the oscillation start/stop can be controlled by the frequency control register 2 (FCON2).
If it sets the XTM0 and XTM1 bits of FCON2 to "11", external clock input becomes accepted and then the external clock input is counted to 16, then the low-speed clock (LSCLK) switches to the external clock.
In this time, the low-speed oscillation clock switch interrupt(LOSCINT) is generated.
Refer to Chapter 4 “Power Management” for the operation at each power down mode.

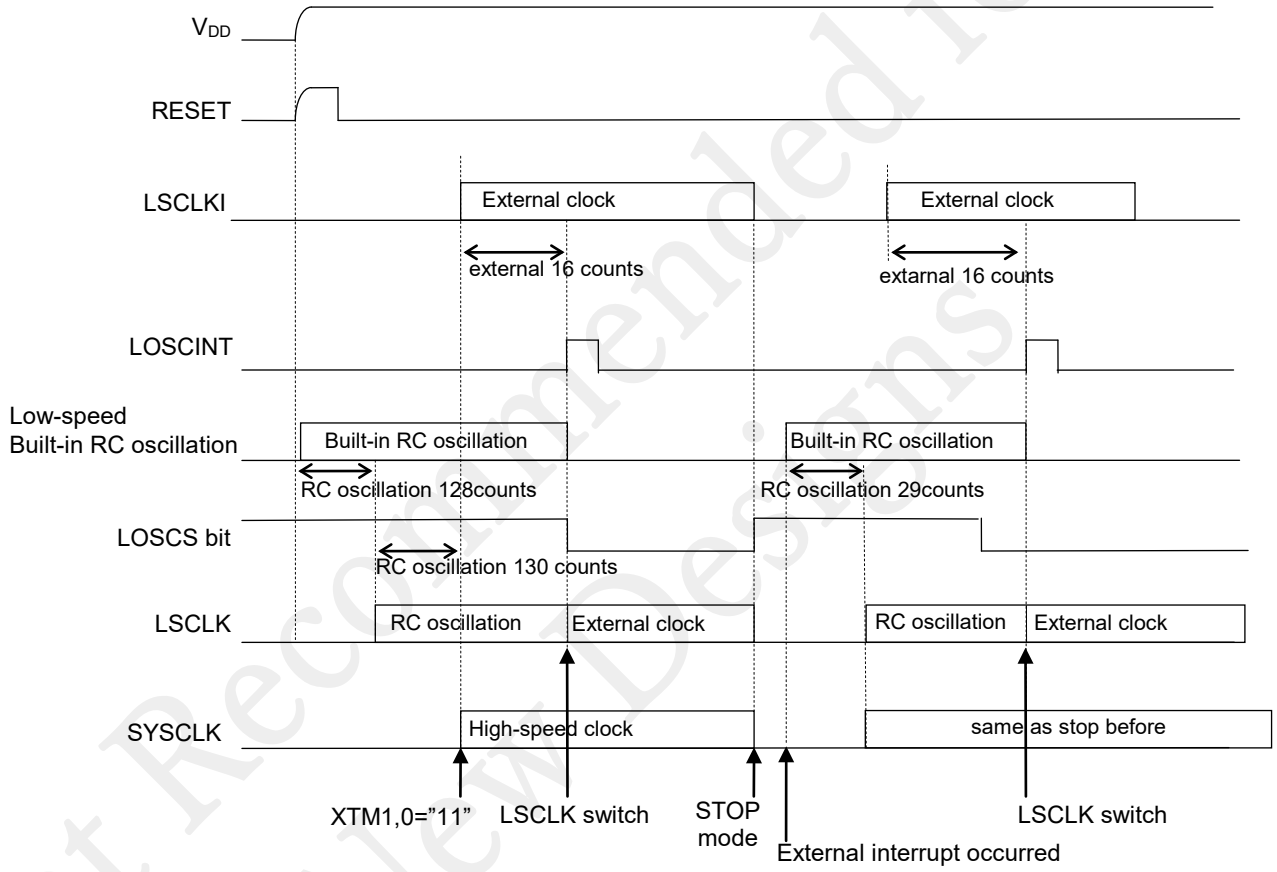


Figure 6-8 Low-Speed Clock Generation Circuit Operation (External Clock Mode)

6.3.2 High-Speed Clock

For the high-speed clock generation circuit, the built-in RC oscillation mode, the crystal/ceramic oscillation mode, or the external clock input mode can be selected.

6.3.2.1 High-Speed Built-in RC Oscillation Mode

Figure 6-9 shows the high-speed clock generation circuit configuration in the built-in RC oscillation mode.
When the RC oscillation clock is counted to 512, the high-speed oscillation clock (OSCLK) starts to be supplied.

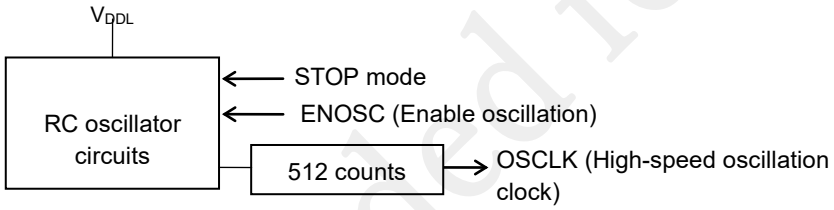


Figure 6-9 Circuit Configuration in the Built-In RC Oscillation Mode

6.3.2.2 High-Speed Crystal/Ceramic Oscillation Mode

In crystal/ceramic oscillation mode, both the P10/OSC0 pin and the P11/OSC1 pin are used for crystal/ceramic oscillation.
In crystal/ceramic oscillation mode, a crystal or a ceramic oscillator is externally connected to the P10/OSC0 and P11/OSC1 pins. If the high-speed oscillation clock pulse count reaches 4096 after oscillation enable, the clock is output to OSCLK (high-speed oscillation clock).
Figure 6-10 shows the circuit configuration in the crystal/ceramic oscillation mode.

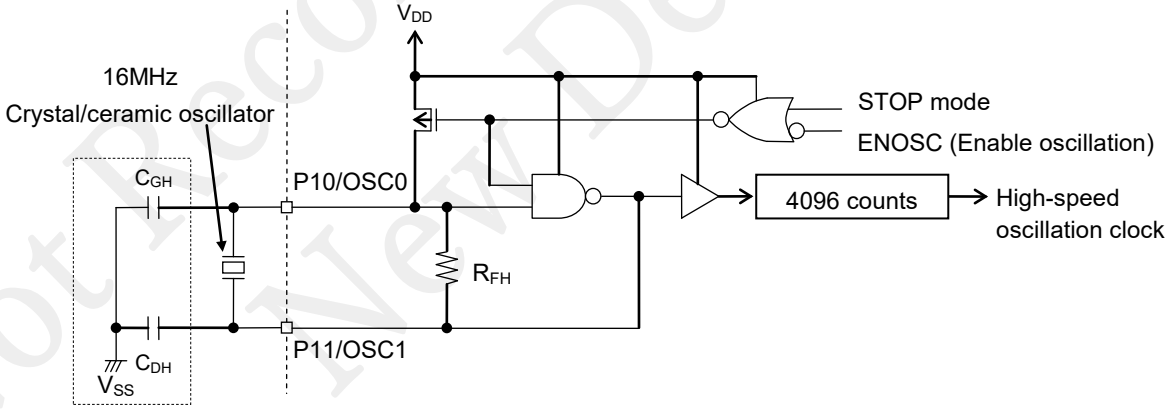


Figure 6-10 Circuit Configuration in the Crystal/Ceramic Oscillation Mode

[Note]
- Install a crystal or a ceramic oscillator as close to the LSI as possible and make sure that signals causing noise and power supply wiring are not near the crystal or the ceramic oscillator and their wiring.
- Note that oscillation may stop due to condensation.

6.3.2.3 High-Speed External Clock Input Mode

In external high-speed clock input mode, external clock is input from the P11/OSC1 pin.
Figure 6-11 shows the circuit configuration in the external clock input mode.

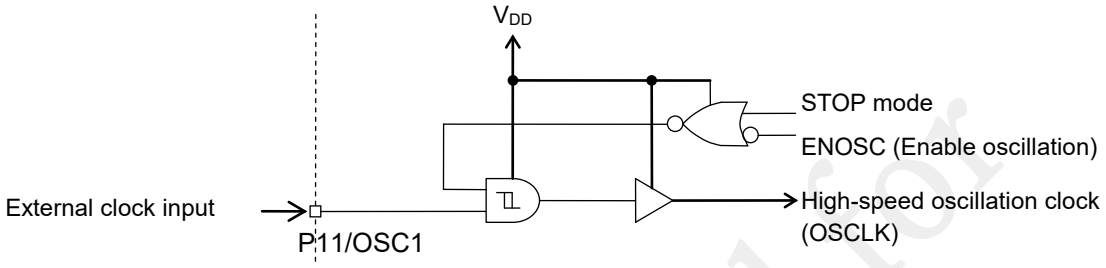


Figure 6-11 Circuit Configuration in the External Clock Input Mode

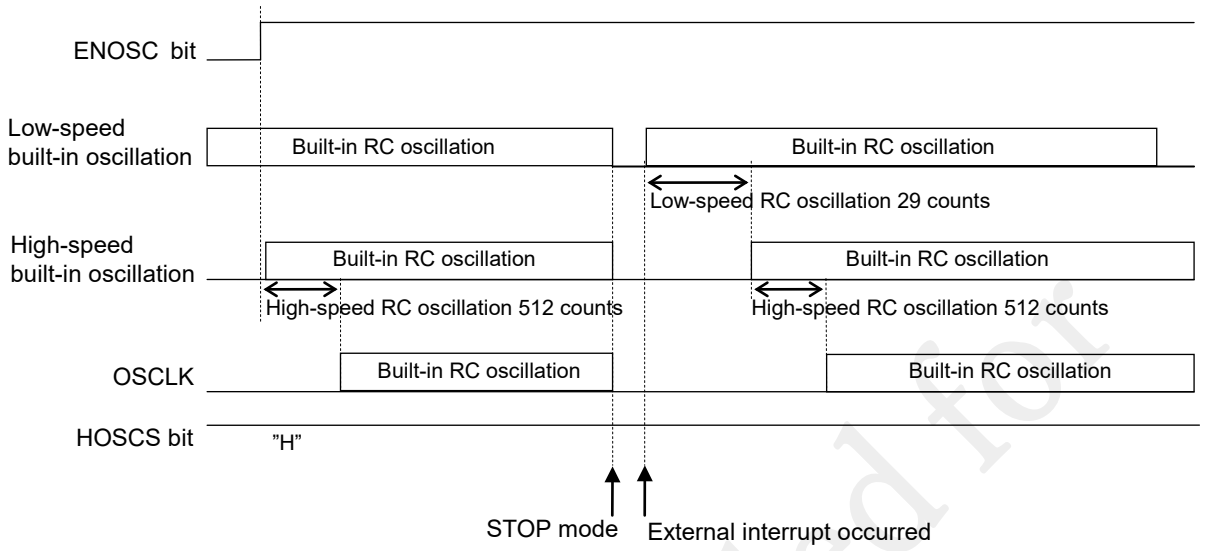
[Note]
•Since the P11/OSC1 pin has a built-in diode to V_{DD} and V_{SS}, avoid applying voltages higher than the V_{DD} and lower than the V_{SS}.
•If the P11/OSC1 pin is left open in high-speed external clock input mode, excessive current can flow. Therefore, make sure that the "H" level (V_{DD}) or the "L" level (V_{SS}) is input.
•For the P11/OSC1 pin, an input clock should not exceed 16MHz.

6.3.2.4 High-Speed Built-In RC Oscillation Mode Operation

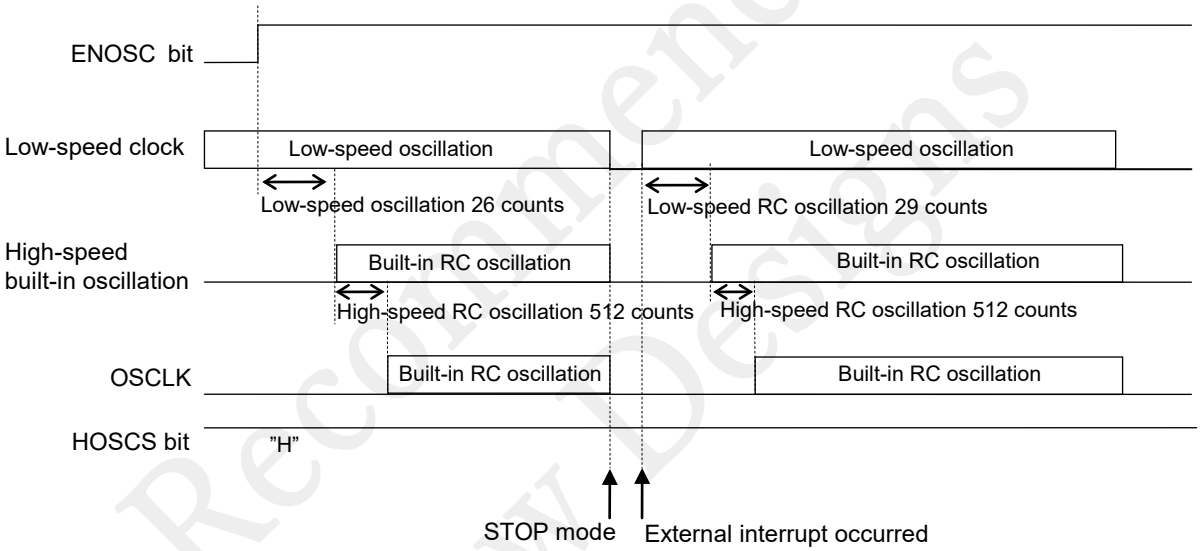
For the high-speed built-in RC oscillation, the oscillation start/stop can be controlled by the frequency control register 1 (FCON1).
Oscillation can be started by setting the ENOSC bit of FCON1 to "1". OSCLK starts to be supplied after the built-in RC oscillation clock is counted to 512 after the oscillation starts. In the low-speed crystal oscillation mode or external clock input mode, high-speed built-in oscillation starts after the low-speed clock is counted to 26.

The high-speed clock generation circuit stops oscillation when it shifts to the STOP mode by software. By releasing the stop mode by an external interrupt, the low-speed built-in RC oscillation clock is counted to 29 and then the high-speed built-in RC oscillation clock is counted to 512, then the built-in RC oscillation clock is supplied as OSCLK.
Refer to Chapter 4 “Power Management” for the operation at each power down mode.

Figure 6-12 shows the operation waveforms of the high-speed clock generation circuit in the built-in RC oscillation mode.



(a) In the low-speed built-in RC oscillation mode



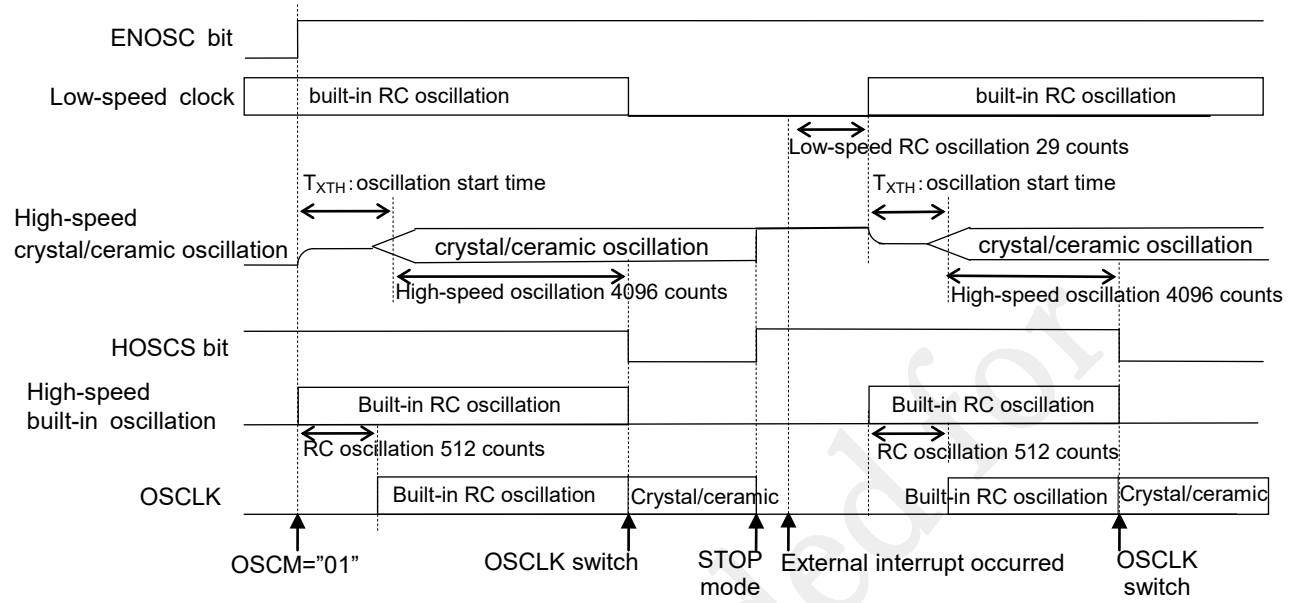
(b) In the low-speed crystal oscillation or external clock input mode

Figure 6-12 High-Speed Clock Generation Circuit Operation (Built-In RC Oscillation Mode)

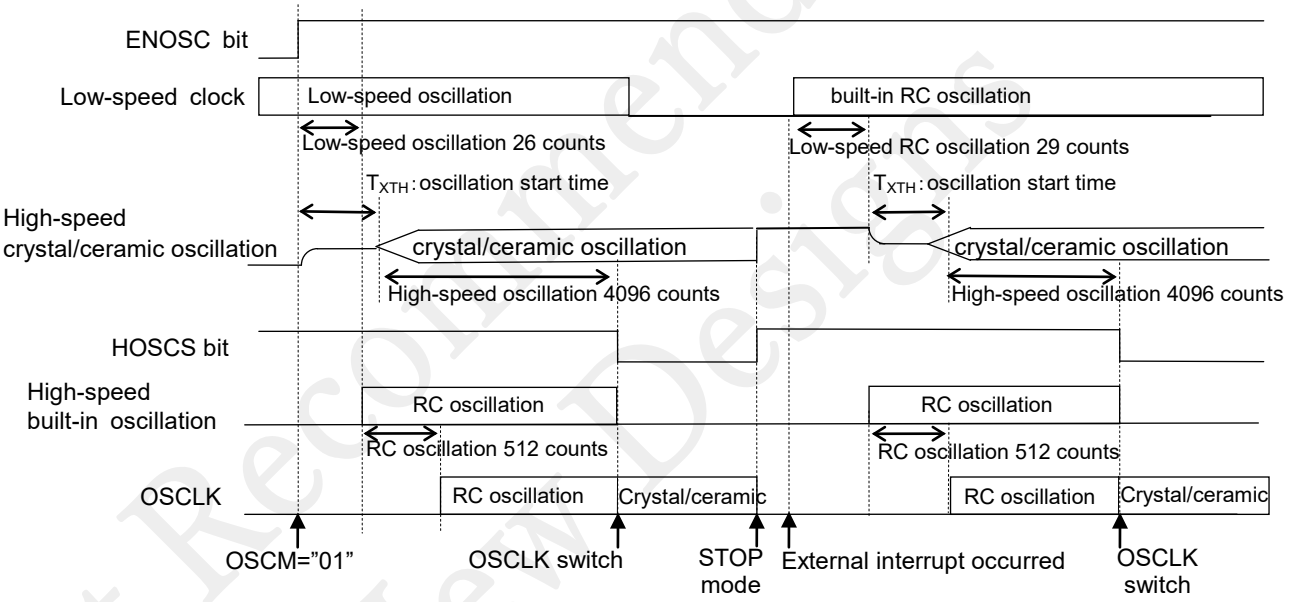
6.3.2.5 High-Speed Crystal/Ceramic Oscillation Mode Operation

High speed clock is switch to crystal/ceramic oscillation mode by setting FCON0 bit of OSCM1,0 to “01”.
If the ENOSC bit of FCON1 is set to "1", the built-in RC oscillation clock is counted to 512 as the high-speed clock, then the built-in RC oscillation clock is supplied as OSCLK. If the OSC1,0 bits of FCON0 are set to "01", After waiting for the crystal/ceramic oscillation start time (T_{XTH}) and the crystal/ceramic oscillation stabilization time (4096 counts), the high-speed clock (OSCLK) switches from the built-in RC oscillation clock to the crystal/ceramic oscillation clock.
In the case of low-speed crystal oscillation mode or external clock input mode, high-speed built-in oscillation starts after the low-speed clock is counted to 26.
The high-speed clock generation circuit stops oscillation when it shifts to the STOP mode by software.
When the mode switch to STOP mode, FSTAT bit of HOSCS must be “0” and clock input from crystal/ceramic oscillator must be stable.
By releasing the stop mode by an external interrupt, the low-speed built-in RC oscillation clock is counted to 29 and then the high-speed built-in RC oscillation clock is counted to 512, then the built-in RC oscillation clock is supplied as OSCLK. After waiting for the crystal/ceramic oscillation start time (T_{XTH}) and the crystal/ceramic oscillation stabilization time (4096 counts), the high-speed clock (OSCLK) switches from the built-in RC oscillation clock to the crystal/ceramic oscillation clock. Refer to Chapter 4 “Power Management” for the operation at each power down mode.

Figure 6-13 shows the waveforms of the high-speed clock generation circuit in crystal/ceramic oscillation mode.



(a) In the low-speed built-in RC oscillation mode



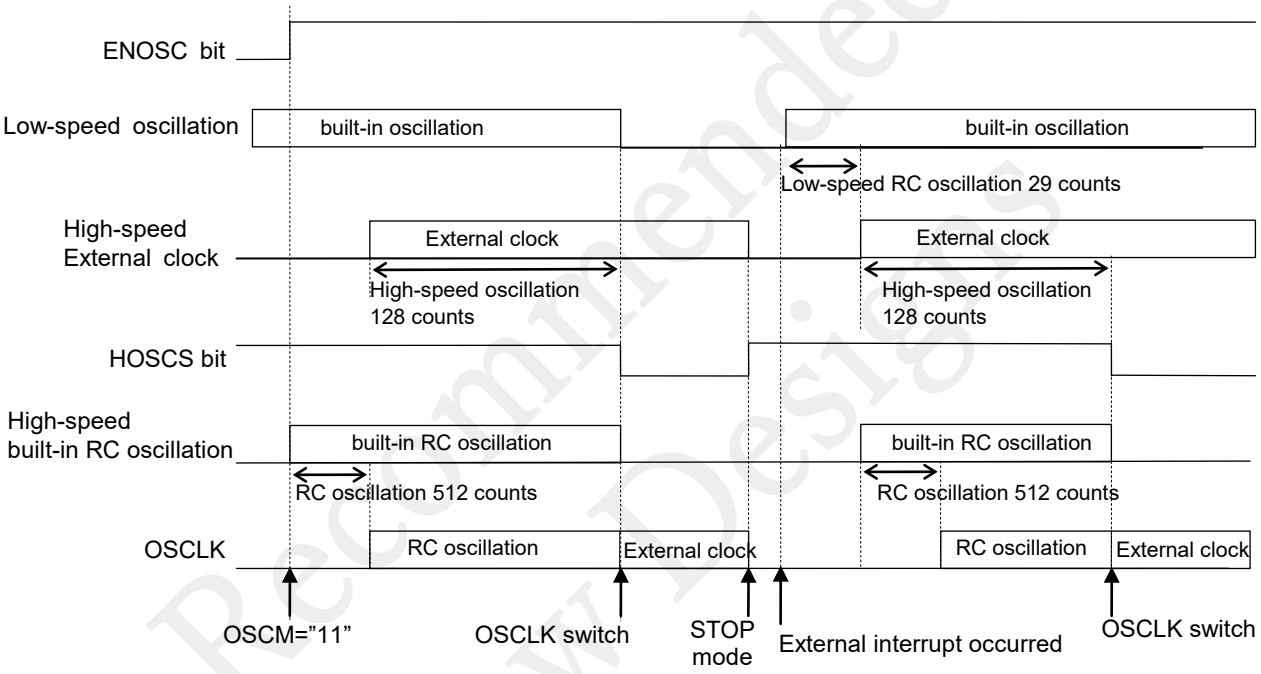
(b) In the low-speed crystal oscillation or external clock input mode

Figure 6-13 High-Speed Clock Generation Circuit Operation (Crystal/Ceramic Oscillation Mode)

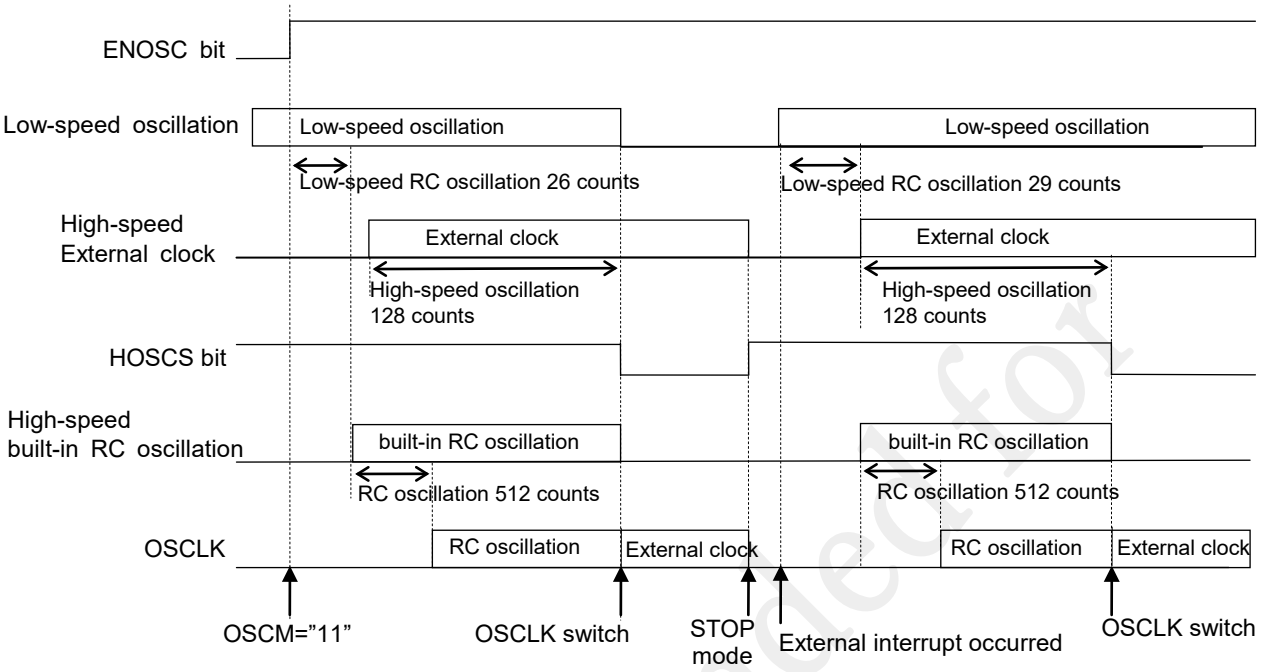
6.3.2.6 High-Speed External Clock Mode Operation

For the high-speed external clock, the oscillation start/stop can be controlled by the frequency control register1 (FCON1).
Oscillation can be started by setting the ENOSC bit of FCON1 to "1". The external clock starts to be supplied as OSCLK after the built-in RC oscillation clock is counted to 512 after the oscillation starts and then the external clock is counted to 128. The high-speed clock generation circuit stops oscillation when it shifts to the STOP mode by software. By releasing the stop mode by an external interrupt, the low-speed built-in RC oscillation clock is counted to 29 and then the high-speed built-in RC oscillation clock is counted to 512, then the built-in RC oscillation clock is supplied as OSCLK. And OSCLK changes from RC oscillation into external clock by the automatic operation in case of 128 counts by the external clock.
Refer to Chapter 4 “Power Management” for the operation at each power down mode.

Figure 6-14 shows the operation waveforms of the high-speed clock generation circuit in the external clock input mode.



(a) In the low-speed built-in RC oscillation mode

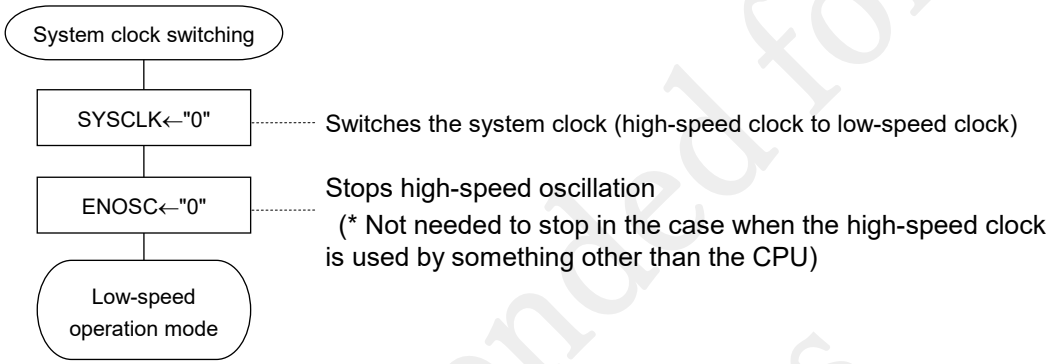


(b) In the low-speed crystal oscillation or external clock input mode

Figure 6-14 High-Speed Clock Generation Circuit Operation (External Clock Input Mode)

6.3.3 Switching of System Clock

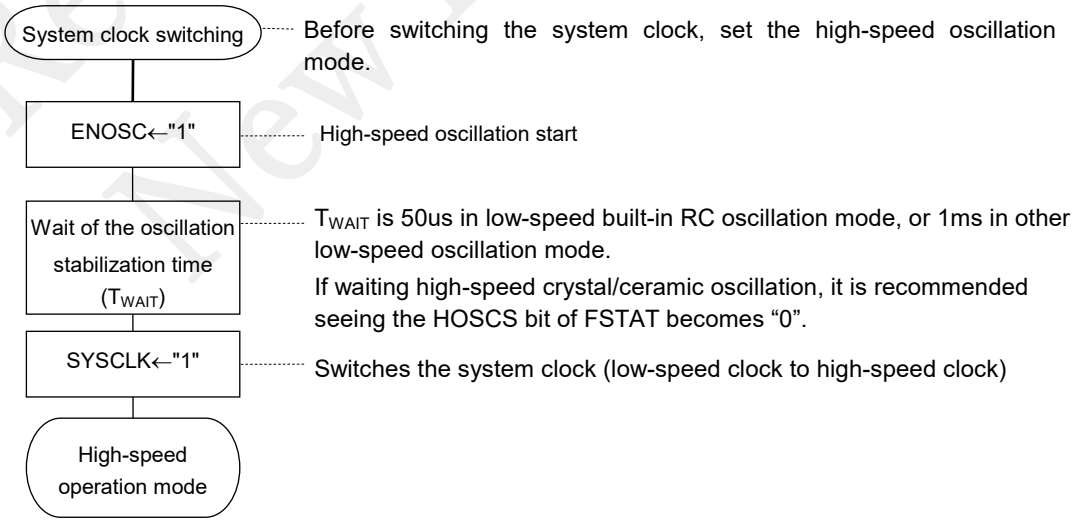
The system clock can be switched between high-speed clock (HSCLK) and low-speed clock (LSCLK) by using the frequency control registers (FCON0, FCON1).
Figure 6-15 shows the flow chart of the system clock switching processing (HSCLK→LSCLK), and Figure 6-16 shows the flow chart of the system clock switching processing (LSCLK→HSCLK).



▼

Figure 6-15 Flow Chart of System Clock Switching Processing (HSCLK→LSCLK)

[Note]
If the system clock is switched from the high-speed clock to the low-speed clock before the low-speed clock (LSCLK) starts oscillation, the CPU becomes the stopped state until LSCLK starts to be supplied to the peripheral circuits.



▼

Figure 6-16 Flow Chart of System Clock Switching Processing (LSCLK→HSCLK)

6.3.4 Low-speed oscillation clock switch interrupt

The low-speed oscillation clock change interrupt occurs only when switching the mode from low-speed built-in RC oscillation mode to low-speed crystal oscillation mode or external low-speed clock input mode. The interrupt does not occurs when switching the mode from low-speed crystal oscillation mode or external low-speed clock input mode to low-speed build-in RC oscillation mode.

Chapter 7

Time Base Counter

7. Time Base Counter

7.1 Overview

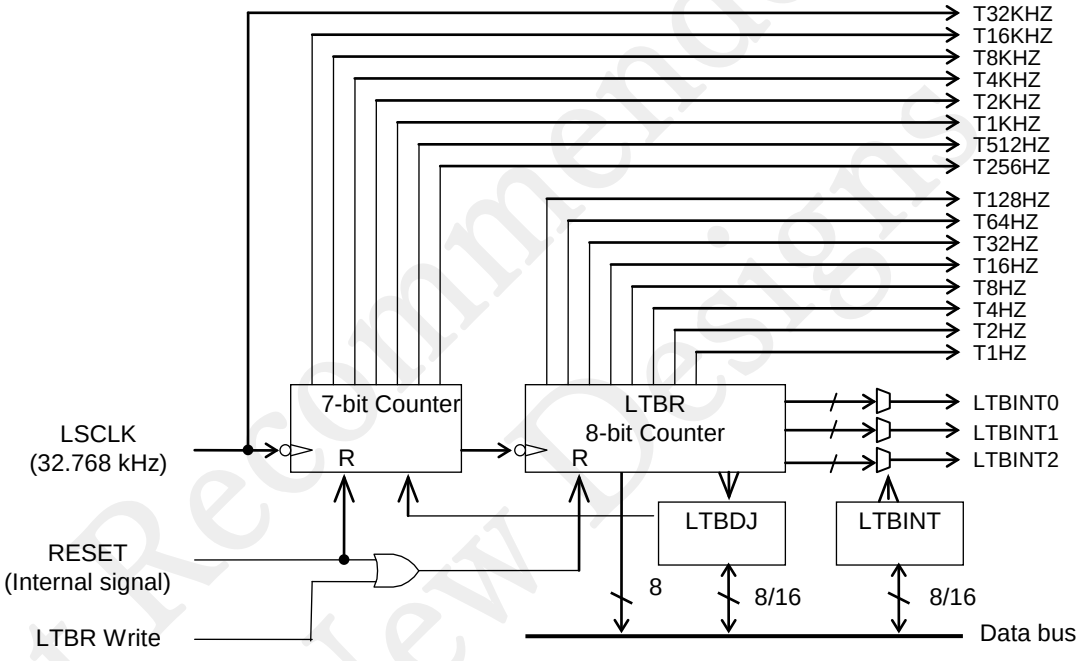
The time base counter generates base clocks for peripheral circuits, and generates interrupt periodically.

7.1.1 Features

- LTBC generates T32KHZ to T1HZ signals by dividing the low-speed clock (LSCLK).
- LTBC allows frequency adjustment (Adjustment range: Approx. −488ppm to +488ppm. Adjustment accuracy: Approx. 0.48ppm) by using the low-speed time base counter frequency adjustment registers (LTBADJH and LTBADJL).
- 3clocks between 128Hz and 1Hz can be used as interrupt signal.

7.1.2 Configuration

Figure 7-1 show the configuration of a low-speed time base counter respectively.



LTBR : Low-speed time base counter register
LTBADJ : Low-speed time base counter frequency adjust register
LTBINT : Low-speed time base counter interrupt select

Figure 7-1 Configuration of Low-Speed Time Base Counter (LTBC)

7.2 Description of Registers

7.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F060	Low-speed time base counter register	LTBR	–	R/W	8	00
0F062	Low-speed time base counter frequency adjustment register	LTBADJL	LTBADJ	R/W	8/16	00
0F063		LTBADJH		R/W	8	00
0F064	Low-speed time base counter interrupt select resister	LTBINTL	LTBINT	R/W	8/16	30
0F065		LTBINTH		R/W	8	06

7.2.2 Low-Speed Time Base Counter (LTBR)

Address: 0F060H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
LTBR	T1HZ	T2HZ	T4HZ	T8HZ	T16HZ	T32HZ	T64HZ	T128HZ
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LTBR is a special function register (SFR) to read the T128HZ-T1HZ outputs of the low-speed time base counter. When write to LTBR, the content of LTBR becomes "0" regardless of the write data.

[Note]
LTBC interrupts may occur depending on the LTBR write timing (see 7.3.1 "Low-Speed Time Base Counter"). Therefore, take care in software programming.

7.2.3 Low-Speed Time Base Counter Frequency Adjustment Registers (LTBADJ)

Address: 0F062H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
LTBADJL	LADJ7	LADJ6	LADJ5	LADJ4	LADJ3	LADJ2	LADJ1	LADJ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
LTBADJH	–	–	–	–	–	LADJ10	LADJ9	LADJ8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

LTBADJL and LTBADJH are special function registers (SFRs) to set the frequency adjustment values of the low-speed time base clock.

Description of Bits

- **LADJ10-0** (bits 10 to 0)
  The LADJ10-0 bits are used to adjust frequency.
  Adjustment range: Approx. –488ppm to +488ppm.
  Adjustment accuracy: Approx. 0.48ppm

  Frequency adjustment (Adjustment range: Approx. –488ppm to +488ppm. Adjustment accuracy: Approx. 0.48ppm) is possible for outputs of T8KHZ to T1HZ of LTBC by using the low-speed time base counter frequency adjust registers (LTBADJH and LTBADJL).
  Table7-1 shows correspondence between the frequency adjustment values (LTBADJH, LTBADJL) and adjustment ratio.

Table 7-1 Correspondence between Frequency Adjustment Values (LTBADJH, LTBADJL) and Adjustment Ratio

LADJ10 to 0											Hexadecimal	Frequency adjustment ratio (ppm)
0	1	1	1	1	1	1	1	1	1	1	3FFH	+487.80
0	1	1	1	1	1	1	1	1	1	0	3FEH	+487.33
:	:	:	:	:	:	:	:	:	:	:	:	:
0	0	0	0	0	0	0	0	0	1	1	003H	+1.43
0	0	0	0	0	0	0	0	0	1	0	002H	+0.95
0	0	0	0	0	0	0	0	0	0	1	001H	+0.48
0	0	0	0	0	0	0	0	0	0	0	000H	0
1	1	1	1	1	1	1	1	1	1	1	7FFH	–0.48
1	1	1	1	1	1	1	1	1	1	0	7FEH	–0.95
:	:	:	:	:	:	:	:	:	:	:	:	:
1	0	0	0	0	0	0	0	0	0	1	401H	–487.80
1	0	0	0	0	0	0	0	0	0	0	400H	–488.28

The adjustment values (LADJ10-0) to be set in LTBADJH and LTBADJL can be obtained by using the following equations:

Adjustment value = Frequency adjustment ratio × 2097152 (decimal)
= Frequency adjustment ratio × 200000h (hexadecimal)

Example 1: When adjusting +15.0ppm (gaining time)
Adjustment value = +15.0ppm × 2097152 (decimal)
= $+15.0 \times 10^{-6} \times 2097152$
= +31.45728 (decimal)
≅ 01Fh (hexadecimal)

Example 2: When adjusting −25.5ppm (losing time)
Adjustment value = −25.5ppm × 2097152 (decimal)
= $-25.5 \times 10^{-6} \times 2097152$
= −53.477376 (decimal)
≅ 7CCh (hexadecimal)

[Note]
The low-speed clock (LSCLK) and the outputs of T32KHZ and T16KHZ of LTBC are not adjusted by the frequency adjust function.
The frequency adjustment accuracy does not guarantee the accuracy including the frequency variation of the crystal oscillation (32.768kHz) due to temperature variations.

7.2.4 Low-Speed Time Base Counter Interrupt select Registers (LTBINT)

Address: 0F064H
Access: R/W
Access size: 8/16 bits
Initial value: 0630H

	7	6	5	4	3	2	1	0
LTBINTL	–	LTI1S2	LTI1S1	LTI1S0	–	LTI0S2	LTI0S1	LTI0S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	1	1	0	0	0	0

	15	14	13	12	11	10	9	8
LTBINTH	–	–	–	–	–	LTI2S2	LTI2S1	LT2S0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	1	1	0

LTBINT is a special function register(SFR) which specify low speed time base clock which is used as an interrupt signal.

Description of Bits

- **LTI0S2-0** (bit 2 to 0)
  The bits specify an assignable clock to LTBINT0. Initial value is T128HZ.。

- **LTI1S2-0** (bit 6 to 4)
  The bits specify an assignable clock to LTBINY1. Initial value is T16HZ.

- **LTI2S2-0** (bit 10 to 8)
  The bits specify an assignable clock to LTBINT2. Initical value is T2HZ.

LTInS2	**LTInS1**	**LTInS0**	Assignable clock
0	0	0	T128HZ
0	0	1	T64HZ
0	1	0	T32HZ
0	1	1	T16HZ
1	0	0	T8HZ
1	0	1	T4HZ
1	1	0	T2HZ
1	1	1	T1HZ

* an interrupt may occur at setting.

7.3 Description of Operation

7.3.1 Low-Speed Time Base Counter

The low-speed time base counter (LTBC) starts counting from 0000H on the LSCLK falling edge after system reset.
Three of LBC interrupt request interrupt by falling edge of clock output which was assigned by the low-speed time base counter interrupt select register.
The output data of T128HZ to T1HZ of LTBC can be read from the low-speed time base counter register (LTBR). When reading the data, read LTBR twice and check that the two values coincide to prevent reading of undefined data during counting.
Figure 7-2 shows an example of program to read LTBR.

```
        LEA     offset LTBR     ; EA←LTBR address
MARK:
        L       R0,     [EA]        ; 1st read
        L       R1,     [EA]        ; 2nd read
;
        CMP     R0,     R1          ; Comparison for LTBR
        BNE     MARK            ; To MARK when the values do not coincide
;
           :
```

Figure 7-2 Programming Example for Reading LTBR

LTBR is reset when write operation is performed and the T128HZ to T1HZ outputs are set to "0". At this time, Interrupt occurs when clock is assigned to LTBC interrupt changing from "1" to "0". Therefore, when LTBR is reset, After prohibits each TBC interrupts of interrupt controller, LTBR is reset and the processing which clears LTBR interrupt request which occurred by reset is needed. Figure 7-3 shows the sequence to clear the LTBC interrupt request.

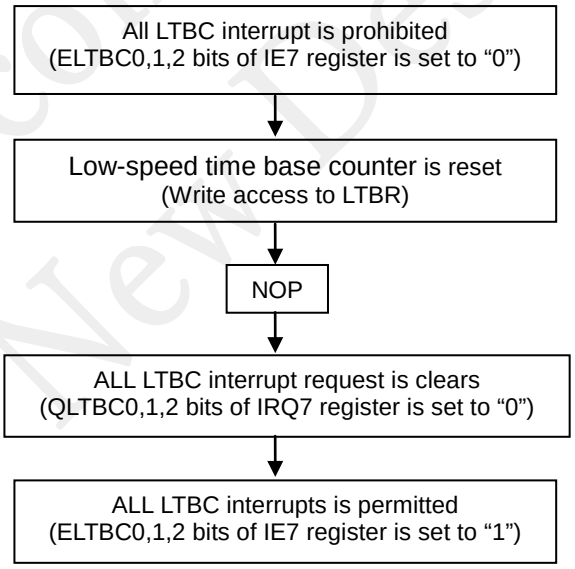


Figure 7-3 Sequence to Clear the LTBC Interrupt Request which Occurred by LTBR Reset

1CPU cycle is needed after LTBR interrupt occurs until LTBC interrupt request flag of interrupt controller is set. When LTBC interrupt request is cleared after the writing LTBR, Please do not put the order to clear request flag just after an order to write in LTBR at. Please clear request flag after placing NOP, and putting time.

Figure 7-4 shows interrupt generation timing of the time base counter output by writing to LTBR.

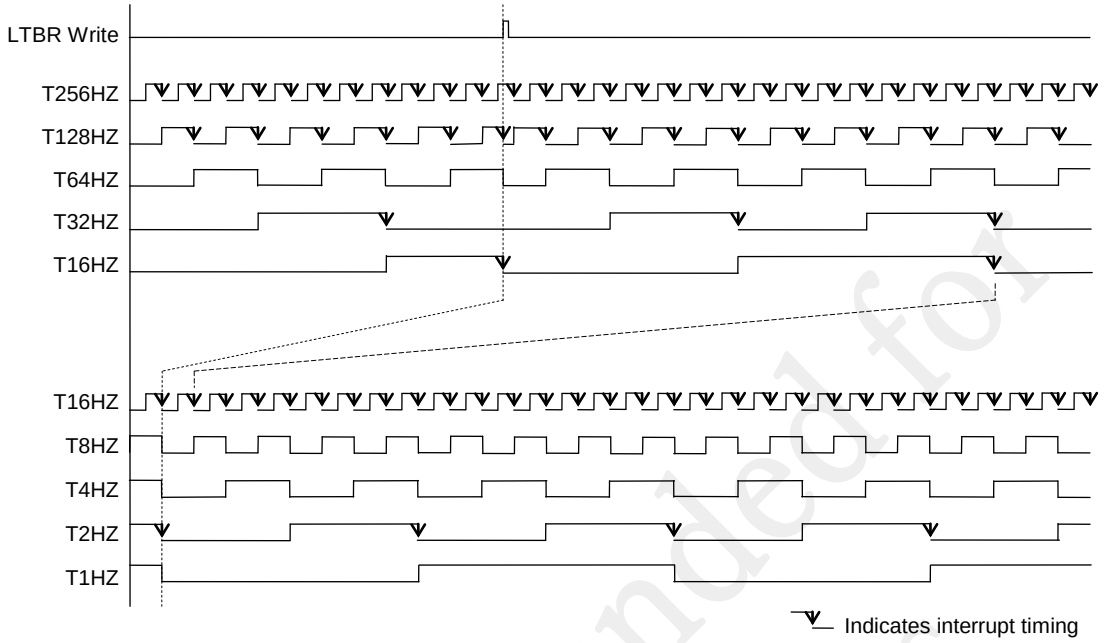


Figure 7-4 Interrupt Timing by Writing to LTBR

Chapter 8

Timers

8. Timers

8.1 Overview

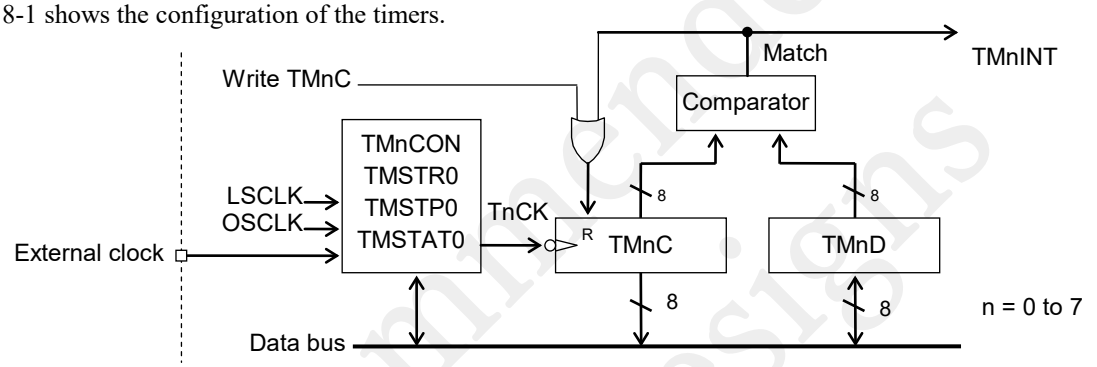
This LSI includes 8 channels of 8-bit timers. A pair of 2 timers functions as 16-bit timer.

8.1.1 Features

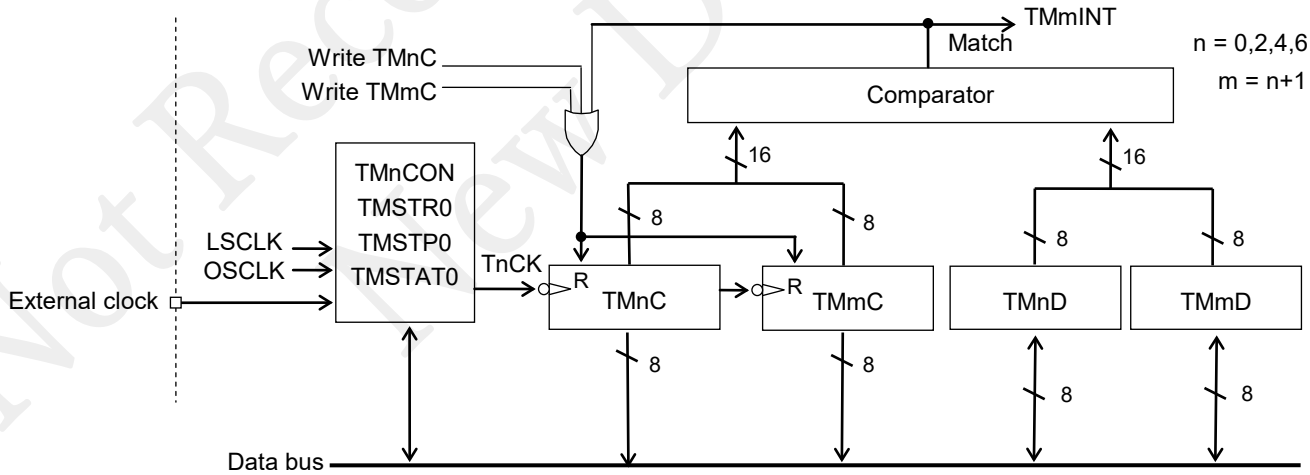
- The timer interrupt (TMnINT, n=0 to 7) is generated when the values of timer counter register (TMnC, n=0 to7) and timer data register (TMnD, n=0 to 7) coincide.
- A timer configured by combining timer 0 and timer 1 or timer 2 and timer 3 or timer 4 and timer 5 or timer 6 and timer 7 can be used as a 16-bit timer.
- low-speed clock(LSCLK), high-speed clock(OSCLK), and external input(P42/P43/P52/P53) are selectable as timer clock(selectable clock is different every channel).
- Timer clock can be divided by 1, 2, 4, 8, 16, 32, and 64 by divider function.

8.1.2 Configuration

Figure 8-1 shows the configuration of the timers.



(a) In 8-bit Timer Mode (Timers 0 to 7)



(b) 16-bit Timer Mode (Timers 0 to 7)

TMnCON:	Timer control register	TMSTR0:	Timer start register 0
TMmD, TMnD:	Timer data registers	TMSTP0:	Timer stop register 0
TMmC, TMnC:	Timer counter registers	TMSTAT0:	Timer status register 0

Figure 8-1 Configuration of Timers

Alternative counter clock of each channels are as below
8bit mode case

channel	Selectable clock
0	LSCLK/OSCLK
1	
2	LSCLK/OSCLK/external pin(P42)
3	LSCLK/OSCLK/external pin(P43)
4	LSCLK/OSCLK/external pin(P52)
5	LSCLK/OSCLK/external pin(P53)
6	LSCLK/OSCLK/low-speed crystal oscillation(*1)
7	

16 bit mode case

channel	Selectable clock
0,1	LSCLK/OSCLK
2,3	LSCLK/OSCLK/external pin(P42)
4,5	LSCLK/OSCLK/external pin(P52)
6,7	LSCLK/OSCLK/low-speed crystal oscillation(*1)

(*1) When low-speed built-in RC oscillation is assigned to LSCLK, only timer can be functioned by using low-speed crystal oscillation. In this case, it is necessary to permit low-speed crystal oscillation by frequency control resister 01(FCON01) LOSCON bit.

8.2 Description of Registers

8.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F300	Timer 01 data register	TM0D	TM01D	R/W	8/16	FF
0F301		TM1D		R/W	8	FF
0F302	Timer 23 data register	TM2D	TM23D	R/W	8/16	FF
0F303		TM3D		R/W	8	FF
0F304	Timer 45 data register	TM4D	TM45D	R/W	8/16	FF
0F305		TM5D		R/W	8	FF
0F306	Timer 67 data register	TM6D	TM67D	R/W	8/16	FF
0F307		TM7D		R/W	8	FF
0F310	Timer 01 counter register	TM0C	TM01C	R/W	8/16	00
0F311		TM1C		R/W	8	00
0F312	Timer 23 counter register	TM2C	TM23C	R/W	8/16	00
0F313		TM3C		R/W	8	00
0F314	Timer 45 counter register	TM4C	TM45C	R/W	8/16	00
0F315		TM5C		R/W	8	00
0F316	Timer 67 counter register	TM6C	TM67C	R/W	8/16	00
0F317		TM7C		R/W	8	00
0F320	Timer 01 control register	TM0CON	TM01CON	R/W	8/16	00
0F321		TM1CON		R/W	8	00
0F322	Timer 23 control register	TM2CON	TM23CON	R/W	8/16	00
0F323		TM3CON		R/W	8	00
0F324	Timer 45 control register	TM4CON	TM45CON	R/W	8/16	00
0F325		TM5CON		R/W	8	00
0F326	Timer 67 control register	TM6CON	TM67CON	R/W	8/16	00
0F327		TM7CON		R/W	8	00
0F330	Timer start register 0	TMSTR0	–	W	8	00
0F332	Timer stop register 0	TMSTP0	–	W	8	00
0F334	Timer status register 0	TMSTAT0	–	R	8	00

8.2.2 Timer n Data Register (TMnmD : {n,m}={0,1} , {2,3} , {4,5} , {6,7})

Address: 0F300H(TM0D/TM01D), 0F301H(TM1D), 0F302H(TM2D/TM23D), 0F303H(TM3D),
0F304H(TM4D/TM45D), 0F305H(TM5D), 0F306H(TM6D/TM67D), 0F307H(TM7D)
Access: R/W
Access size: 8/16 bits
Initial value: FFFFH

	7	6	5	4	3	2	1	0
TMnD	TnD7	TnD6	TnD5	TnD4	TnD3	TnD2	TnD1	TnD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8
TMmD	TmD7	TmD6	TmD5	TmD4	TmD3	TmD2	TmD1	TmD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

TMnD is a special function register (SFR) to set the value to be compared with the timer n counter register (TMnC) value.

[Note]
Set TMnD when the timer stops.
When "00H" is written in TMnD, TMnD is set to "01H" (8bit mode case).
When "0000H" is written in TMnD, TMnD is set to "0001H" (16bit mode case).

8.2.3 Timer n Counter Register (TMnmC : {n,m}={0,1} , {2,3} , {4,5} , {6,7})

Address: 0F310H(TM0C/TM01C), 0F311H(TM1C), 0F312H(TM2C/TM23C), 0F313H(TM3C),
0F314H(TM4C/TM45C), 0F315H(TM5C), 0F316H(TM6C/TM67C), 0F317H(TM7C)
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
TMnC	TnC7	TnC6	TnC5	TnC4	TnC3	TnC2	TnC1	TnC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
TMmC	TmC7	TmC6	TmC5	TmC4	TmC3	TmC2	TmC1	TmC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

TMnC is a special function register (SFR) that functions as an 8-bit binary counter.
When write random data to TMnC (TMmC), TMnC is cleared to "00H".
In 16-bit timer mode, the combination becomes "TM0C and TM1C", "TM2C and TM3C", "TM4C and TM5C" and "TM6C and TM7C".
Even if write to either Low-order(TM0C,TM2C,TM4C,TM6C) timer counter or high-order (TM1C,TM3C,TM5C,TM7C) timer counter, both timer counters are cleared to "00H".

Case of a combination of Timer clock and System clock shown in Table 8-1, able to read the TMnC even during operation.

Table 8-1 TMnC Read Enable condition during Timer Operation

System clock SYSCLK	Timer clock TnCK
LSCLK	LSCLK and divided LSCLK However, except for Timer6,7 low-speed crystal oscillator selection.
HSCLK	OSCLK and divided OSCLK However, when frequency of SYSCLK is more than TnCK

8.2.4 Timer nm Control Register (TMnmCON : {n,m}={0,1}, {2,3}, {4,5}, {6,7})

Address: 0F320H(TM0CON/TM01CON), 0F321H(TM1CON), 0F322H(TM2CON/TM23CON), 0F323H(TM3CON), 0F324H(TM4CON/TM45CON), 0F325H(TM5CON), 0F326H(TM6CON/TM67CON), 0F327H(TM7CON)
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
TMnCON	TnOST	TnmM16	TnDIV2	TnDIV1	TnDIV0	–	TnCS1*	TnCS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
TMmCON	TmOST	–	TmDIV2	TmDIV1	TmDIV0	–	TmCS1*	TmCS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

n=0 to 7, m= 01, 23, 45, 67
* T0CS1 bit of TM0CON and T1CS1 bit of TM1CON is fixed as "0".

TMnCON is a special function (SFR) register to control a timer.
Timer control register(TMnCON) is a special function register(SFR) which control timer.
Timer control register setting need to be done while target timer is stop(TMSTAT0 register TnSTAT state is "0")
TM0CON and TM1CON are accessable as 16bit TM01CON.
TM2CON and TM3CON are accessable as 16bit TM23CON.
TM4CON and TM5CON are accessable as 16bit TM45CON.
TM6CON and TM7CON are accessable as 16bit TM67CON.

Description of Bits

- **TnCS1-0** (bit 1 to 0), **TmCS1-0** (bit 9 to 8)
  The TnCS1-0(TmCS1-0) bits are used for selecting the operation clock of timer n(timer m). The clock assigned by TM0CON, TM2CON, TM4CON, and TM6CON is used as the operation clock at 16bit timer mode.

TnCS1 TmCS1	**TnCS0 TmCS0**	Description					
		Timer 7,6	Timer 5	Timer 4	Timer 3	Timer 2	Timer 1,0
0	0	LSCLK (initial value)					
0	1	OSCLK					
1	0	Low-speed oscillation clock	LSCLK				Prohibited
1	1	LSCLK	External clock (P53)	External clock(P52)	External clock (P43)	External clock (P42)	Prohibited

- **TnDIV2-0** (bit 5 to 3), **TmDIV2-0** (bit 13 to 11)
  TnDIV2-0(TmDIV2-0) bits are used for selecting dividing rate of operation clock .
  The dividing rate is assigned by TM0CON, TM2CON, TM4CON, TM6CON at 16bit timer mode.

TnDIV2 TmDIV2	TnDIV1 TmDIV1	TnDIV0 TmDIV0	Description
0	0	0	Clock assigned by TnCS1 ~ TnCS0 (initial value)
0	0	1	Clock assigned by TnCS1 ~ TnCS0 divide by 2
0	1	0	Clock assigned by TnCS1 ~ TnCS0 divide by 4
0	1	1	Clock assigned by TnCS1 ~ TnCS0 divide by 8
1	0	0	Clock assigned by TnCS1 ~ TnCS0 divide by 16
1	0	1	Clock assigned by TnCS1 ~ TnCS0 divide by 32
1	1	0	Clock assigned by TnCS1 ~ TnCS0 divide by 64
1	1	1	No use（Assigned clock by TnCS1 ~ TnCS0）

- **TnmM16** (bit 6)
  The TnmM16 bit is used for selecting a 16-bit timer mode. TM0CON, TM2CON, TM4CON, and TM6CON has the TnmM16 bit. When the TnmM16 is set to 1, two timers are connected and function as a 16bit timer. When the TnmM16 bit is set to "0", two each timers function 8bit timer.

TnmM16	Description
0	8-bit timer mode (initial value)
1	16-bit timer mode

The below table shows the TnmM16 bit of each timer control register, connect timer, interrupts which is used.

Timer control register	TnmM16 bit	Connect timer (H-L)	interrupt
TM0CON	T01M16	Timer1 – Timer0	Timer1
TM2CON	T23M16	Timer3 – Timer2	Timer3
TM4CON	T45M16	Timer5 – Timer4	Timer5
TM6CON	T67M16	Timer7 – Timer6	Timer7

- **TnOST** (bit 7), TmOST(bit 15)
  The TnOST(TmOST) is used for selecting a normal timer mode or a one-shot timer mode. When the TnOST bit is set to "1", timer n is selected a one-shot timer mode.
  In 16bit timer mode, Timer function mode is selected by TMnCON.

TnOST TmOST	Description
0	normal timer mode (initial value)
1	one-shot timer mode

8.2.5 Timer Start Register 0 (TMSTR0)

Address: 0F330H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMSTR0	T7RUN	T6RUN	T5RUN	T4RUN	T3RUN	T2RUN	T1RUN	T0RUN
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

TMSTR0 is a special function (SFR) to control timer 0 to timer 7.

Description of Bits

- **TnRUN** (bits n : n= 0 to 7)
  TnRUN is the control bit of Timer n count start.
  In initial state after power on, the counter is stopped.
  Timer n Count up is started by writing TnRUN bit to "1".
  Timer n and (n+1) count up is started at 16bit timer mode. (n = 0, 2, 4, 6)

TnRUN	Description
0	Keep current status (initial)
1	Start count

	8-bit timer mode	16-bit timer mode
T0RUN	For timer0	For timer0 and 1
T1RUN	For timer1	Setting prohibited
T2RUN	For timer2	For timer2 and 3
T3RUN	For timer3	Setting prohibited
T4RUN	For timer4	For timer4 and 5
T5RUN	For timer5	Setting prohibited
T6RUN	For timer6	For timer6 and 7
T7RUN	For timer7	Setting prohibited

8.2.6 Timer Stop Register 0 (TMSTP0)

Address: 0F332H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMSTP0	T7STP	T6STP	T5STP	T4STP	T3STP	T2STP	T1STP	T0STP
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

TMSTP0 is a special function (SFR) to control a timer 0 to timer 7.

Description of Bits

- **TnSTP** (bits n : n = 0 to 7)
  TnSTP is Timer n count stop control bit.
  Counter is stop at initial state after power on. "1" setting while count stop is invalid.
  Timer n Count up is stopped by setting TnSTP bit to "1".
  Timer n and (n+1) count up is stopped at 16bit timer mode. (n = 0, 2, 4, 6)

TnSTP	Description
0	Keep current status (initial)
1	Stop count

	8-bit timer mode	16-bit timer mode
T0STP	For timer0	For timer0 and 1
T1STP	For timer1	Setting prohibited
T2STP	For timer2	For timer2 and 3
T3STP	For timer3	Setting prohibited
T4STP	For timer4	For timer4 and 5
T5STP	For timer5	Setting prohibited
T6STP	For timer6	For timer6 and 7
T7STP	For timer7	Setting prohibited

8.2.7 Timer Status Register 0 (TMSTAT0)

Address: 0F334H
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
TMSTAT0	T7STAT	T6STAT	T5STAT	T4STAT	T3STAT	T2STAT	T1STAT	T0STAT
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

TMSTAT0 is a special function (SFR) to control timer 0 to timer 7.

Description of Bits

- **TnSTAT** (bits n : n = 0 to 7)
  TnSTAT bit indicate timer n status(counting/stopping) .

TnSTAT	Description
0	Stopping(initial value)
1	counting

	8-bit timer mode	16-bit timer mode
T0STAT	For timer0	For timer0 and 1
T1STAT	For timer1	Not used (kept value "0".)
T2STAT	For timer2	For timer2 and 3
T3STAT	For timer3	Not used (kept value "0".)
T4STAT	For timer4	For timer4 and 5
T5STAT	For timer5	Not used (kept value "0".)
T6STAT	For timer6	For timer6 and 7
T7STAT	For timer7	Not used (kept value "0".)

8.3 Description of operation

8.3.1 Normal timer mode operation

When the TnRUN bit of timer n register0(TMSTR0) are set to 1, The timer counters(TMnC) is in operation state(TnSTAT ="1") by the first falling edge of the timer clock(TnCK) that are selected by the Timer control register(TMnCON), and start count up by the second falling edge.
When the count value of TMnC coincide with the timer data register (TMnD), timer interrupt (TMnINT) occurs on the next falling edge of timer clock, at same time TMnC are reset to "00H" and continues incremental count.

When the TnSTP bits are set to "1", TMnC stop a count after one fall count of the timer clock (TnCK) , and TnSTAT bit of timer status register 0(TMSTAT0) becomes "0".

When the TnRUN bits are set to "1" again, TMn restart an incremental count from the previous values. To initialize TMnC to "00H", perform write operation in TMnC.

The timer interrupt period (T_{TMI}) is expressed by the following equation.

$$T_{TMI} = \frac{TMnD + 1}{TnCK\ (Hz)} \quad (n=0 \sim 7)$$

TMnD: Timer 0 to 7 data register (TMnD) setting value (01H to 0FFH)
TnCK: Clock frequency selected by the Timer 0 to 7 control register 0 (TMnCON)

After TnRUN bit are set to "1", timer counter are synchronized by the timer clock and counting starts so that an error of a maximum of 1 clock period occurs until the first timer interrupt. The timer interrupt periods from the second time are constant.
Figure 8-2 shows the normal timer mode operation timing diagram of Timer 0 to 7

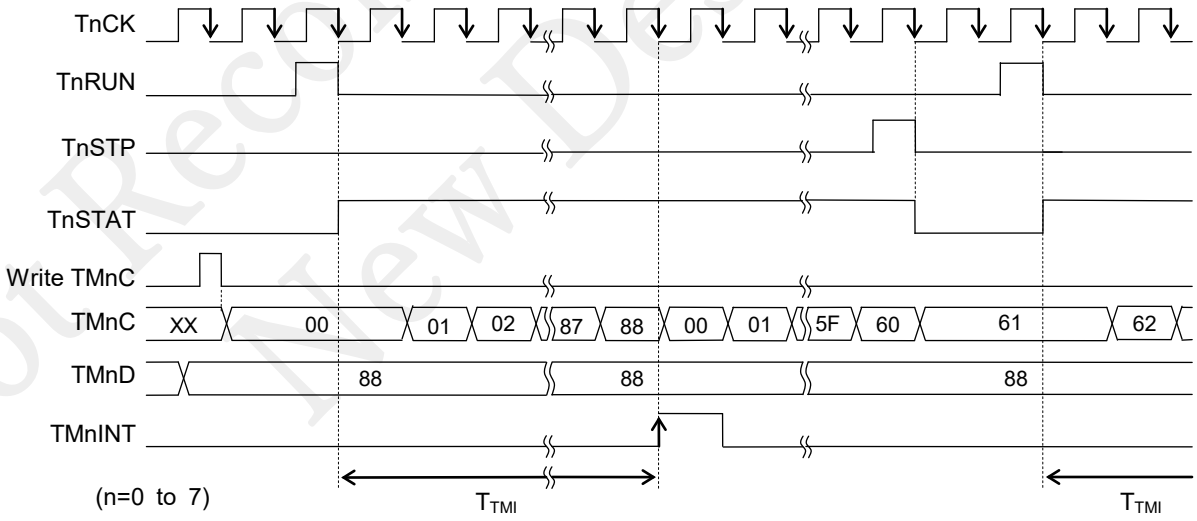


Figure 8-2 Normal Timer Mode Operation Timing Diagram of Timer 0 to 7

[Note]
Count stop and Timer interrupt may occur at same time because Counter stop operation is performed synchronizing with count operation.

8.3.2 One shot timer mode operation

When TMnCON register TnOST bit set to "1", Timer operate one-shot timer mode.
In one-shot timer mode, When the count value (TMnC) and the timer 0 to 7 data register (TMnD) coincide, TnRUN bits are cleared automatically .

Figure 8-3 shows the one-shot timer mode operation timing diagram

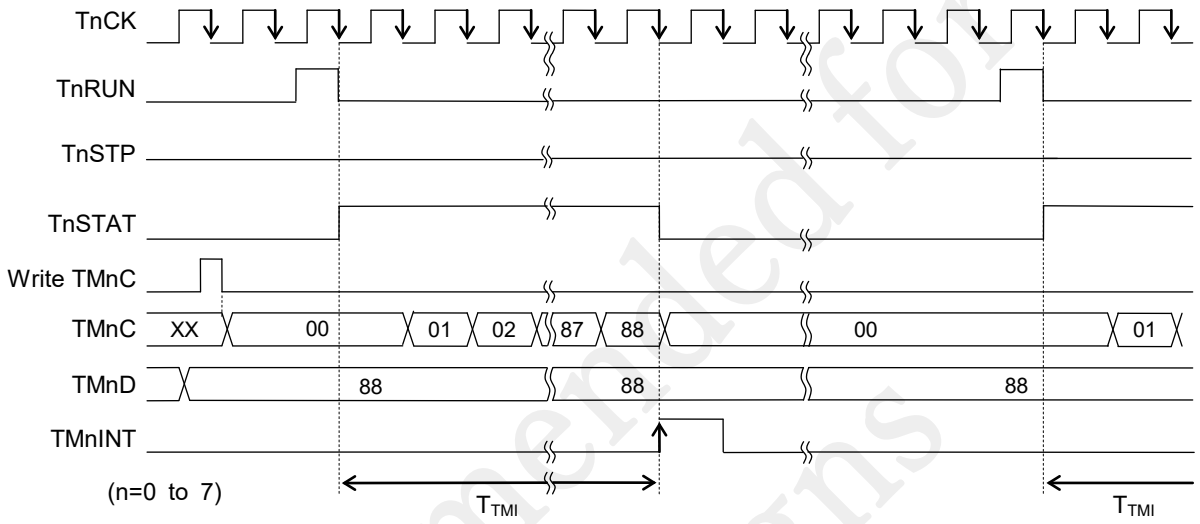


Figure 8-3 One-Shot Timer Mode Operation Timing Diagram

8.3.3 16bit timer mode

Two of 8bit timer can be used as 16bit timer by TMnCON(N=0,2,4,6) register TnM16 bit.
At 16bit timer mode, channel n(n=0.2.4.6) is lower bit, channel m(m=1,3,5,7) is higher bit.
The following shows a corresponding list of timer-channels and related registers.

channel / Control	0,1	2,3	4,5	6,7
Data register	Higher : TM1D Lower : TM0D	Higher : TM3D Lower : TM2D	Higher : TM5D Lower : TM4D	Higher : TM7D Lower : TM6D
Counter register	Higher : TM1C Lower : TM0C	Higher : TM3C Lower : TM2C	Higher : TM5C Lower : TM4C	Higher : TM7C Lower : TM6C
Control register	TM0CON	TM2CON	TM4CON	TM6CON
RUN bit	T0RUN	T2RUN	T4RUN	T6RUN
STOP bit	T0STP	T2STP	T4STP	T6STP
START bit	T0STAT	T2STAT	T4STAT	T6STAT
Interrupt	TM1INT	TM3INT	TM5INT	TM7INT

8.3.4 Restriction

When using a 16bit timer configured by two 8bit timers, there are following two restrictions.

<Restriction 1>
When using the 16bit timer configured by two 8bit timers, do not set "0FEh" to the lower byte of timer data register(TMnD). Set data except for "0FEh"("00h to 0FDh" or "0FFh"). There is no restriction for the higher byte of timer data register(TMmD).
If the "0FEh" is set to the lower byte of timer data register, it works normally for the first interrupt cycle but shortens the cycle by 256 clocks for the second or later interrupt because the timer counter is not reset to "0000h" and restart counting up from "0100h".
<Restriction 2>
When using the 16bit timer configured by two 8bit timers and also if you restart the timer after the timer is stopped by the software or automatically stopped in one shot timer mode, always reset the timer counter register(TMmC, TMnC) to "0000h" by making a write operaton to the register even the data is "0000h". The write operation to one of the higher byte register(TMmC) or lower byte register(TMnC) resets both registers. If not reset the timer counter registers, the first interrupt cycle after restarting the timer may be incorrect.

Example for programming code when using 16bit timer mode with Timer0 and Timer1 in order to avoid the aforementioned restriction 1 and restriction 2 :

```
if ( TM0D == 0xfe ) TM0D = 0xfd;    //  Check the data of timer register (for restriction 1)
TM0C = 0x00;                        //  Initialize the timer counter register (for restriction 2)
T0RUN = 1;                          // Start timer
```

The example shows that it checks the lower byte of timer data register(TM0D) and changes it to 0FDh if it is 0FEh, and starts the timer after initializing the timer counter register (TM1C, TM0C).

Chapter 9

Function Timer(FTM)

9 Function Timer (FTM)

9.1 General Description

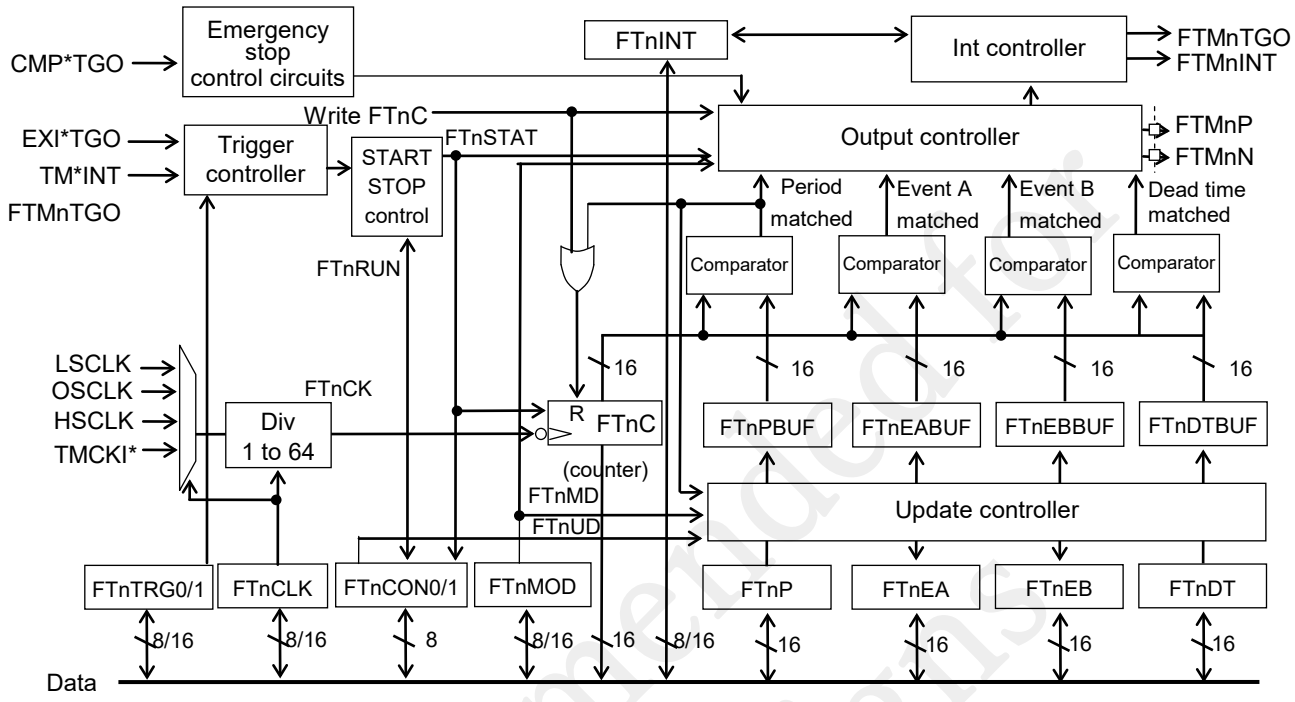
FTM is a 16-bit multifunction timer with the capture and PWM functions in addition to the timer function. It can be started/stopped using an external input signal and a signal from another timer as a trigger.
The LSI includes four channels of the multifunction timer.

9.1.1 Features

- Equipped with the timer/capture/PWM functions using a 16-bit counter
- 1 to 64 dividing of LSCLK/OSCLK/HSCLK/external input selectable as timer clock
- The timer output signal can be switched between the positive and negative logics
- Duty interrupt and coincident interrupt with the setting value as well as the cyclic interrupt generated
- Equipped with one-shot mode
- An event trigger (external pin input interrupt or timer interrupt request) can control start/stop/clear of the timer (however, the minimum pulse width of pin input is timer clock 3ϕ)
- An external input can generate an emergency stop and emergency stop interrupt.
- Two types of PWM with the same period and different duties and complementary PWM with the dead time set can be output
- The capture function can measure the duty/cycle of the input signal (41.6kHz at 128 resolution @ 16MHz timer clock)
- Interrupt source to be notified can be set

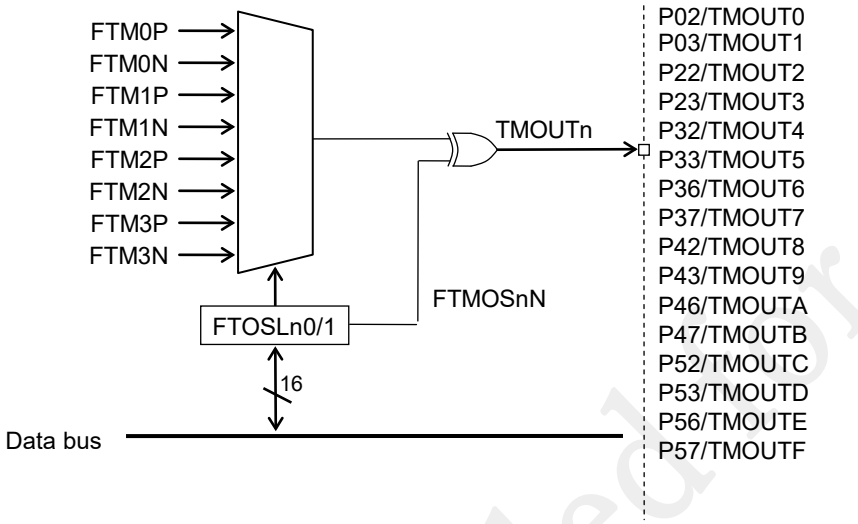
9.1.2 Configuration

Figure 9-1 shows the configuration of the FTM circuit.



FTnP	: FTMn period register	FTnPBUF	: FTMn period buffer
FTnEA/B	: FTMn event A/B register	FTnEA/BBUF	: FTMn event A/B buffer
FTnDT	: FTMn dead time register	FTnDTBUF	: FTMn dead time buffer
FTnC	: FTMn counter register	FTnMOD	: FTMn mode register
FTnCON0/1	: FTMn control register 0,1	FTnCLK	: FTMn clock register
FTnTRG0/1	: FTMn trigger register 0,1		
FTnINTE/S/C	: FTMn interrupt enable/status/clear register		

Figure 9-1 (a) Configuration of Circuit



FTOSLn0/1 : FTM output selection register n0/1 (n = 0 to F)

Figure 9-1 (b) Configuration of FTM Output Selection Circuit

9.1.3 List of Pins

Pin Name	I/O	Function
TMCLKI0-7	I	External clock input
TMOUT0-9 TMOUTA-F	O	Timer output (selectable from FTM 0 to 3)

9.2 Description of Registers

9.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F400	FTM0 period register	–	FT0P	R/W	16	FFFF
0F402	FTM0 event register A	–	FT0EA	R/W	16	0000
0F404	FTM0 event register B	–	FT0EB	R/W	16	0000
0F406	FTM0 dead time register	–	FT0DT	R/W	16	0000
0F408	FTM0 counter register	–	FT0C	R/W	16	0000
0F40A	FTM0 control register 0	FT0CON0	–	R/W	8	00
0F40B	FTM0 control register 1	FT0CON1		R/W	8	00
0F40C	FTM0 mode register	FT0MODL	FT0MOD	R/W	8/16	00
0F40D		FT0MODH		R/W	8	00
0F40E	FTM0 clock register	FT0CLKL	FT0CLK	R/W	8/16	00
0F40F		FT0CLKH		R/W	8	00
0F410	FTM0 trigger register 0	FT0TRG0L	FT0TRG0	R/W	8/16	00
0F411		FT0TRG0H		R/W	8	00
0F412	FTM0 trigger register 1	FT0TRG1L	FT0TRG1	R/W	8/16	00
0F413		FT0TRG1H		R/W	8	00
0F418	FTM0 interrupt enable register	FT0INTEL	FT0INTE	R/W	8/16	00
0F419		FT0INTEH		R/W	8	00
0F41A	FTM0 interrupt status register	FT0INTSL	FT0INTS	R	8/16	00
0F41B		FT0INTSH		R	8	00
0F41C	FTM0 interrupt clear register	FT0INTCL	FT0INTC	W	8/16	00
0F41D		FT0INTCH		W	8	00
0F420	FTM1 period register	–	FT1P	R/W	16	FFFF
0F422	FTM1 event register A	–	FT1EA	R/W	16	0000
0F424	FTM1 event register B	–	FT1EB	R/W	16	0000
0F426	FTM1 dead time register	–	FT1DT	R/W	16	0000
0F428	FTM1 counter register	–	FT1C	R/W	16	0000
0F42A	FTM1 control register 0	FT1CON0	–	R/W	8	00
0F42B	FTM1 control register 1	FT1CON1		R/W	8	00
0F42C	FTM1 mode register	FT1MODL	FT1MOD	R/W	8/16	00
0F42D		FT1MODH		R/W	8	00
0F42E	FTM1 clock register	FT1CLKL	FT1CLK	R/W	8/16	00
0F42F		FT1CLKH		R/W	8	00
0F430	FTM1 trigger register 0	FT1TRG0L	FT1TRG0	R/W	8/16	00
0F431		FT1TRG0H		R/W	8	00
0F432	FTM1 trigger register 1	FT1TRG1L	FT1TRG1	R/W	8/16	00
0F433		FT1TRG1H		R/W	8	00
0F438	FTM1 interrupt enable register	FT1INTEL	FT1INTE	R/W	8/16	00
0F439		FT1INTEH		R/W	8	00

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F43A	FTM1 interrupt status register	FT1INTSL	FT1INTS	R	8/16	00
0F43B		FT1INTSH		R	8	00
0F43C	FTM1 interrupt clear register	FT1INTCL	FT1INTC	W	8/16	00
0F43D		FT1INTCH		W	8	00
0F440	FTM2 period register	–	FT2P	R/W	16	FFFF
0F442	FTM2 event register A	–	FT2EA	R/W	16	0000
0F444	FTM2 event register B	–	FT2EB	R/W	16	0000
0F446	FTM2 dead time register	–	FT2DT	R/W	16	0000
0F448	FTM2 counter register	–	FT2C	R/W	16	0000
0F44A	FTM2 control register 0	FT2CON0	–	R/W	8	00
0F44B	FTM2 control register 1	FT2CON1		R/W	8	00
0F44C	FTM2 mode register	FT2MODL	FT2MOD	R/W	8/16	00
0F44D		FT2MODH		R/W	8	00
0F44E	FTM2 clock register	FT2CLKL	FT2CLK	R/W	8/16	00
0F44F		FT2CLKH		R/W	8	00
0F450	FTM2 trigger register 0	FT2TRG0L	FT2TRG0	R/W	8/16	00
0F451		FT2TRG0H		R/W	8	00
0F452	FTM2 trigger register 1	FT2TRG1L	FT2TRG1	R/W	8/16	00
0F453		FT2TRG1H		R/W	8	00
0F458	FTM2 interrupt enable register	FT2INTEL	FT2INTE	R/W	8/16	00
0F459		FT2INTEH		R/W	8	00
0F45A	FTM2 interrupt status register	FT2INTSL	FT2INTS	R	8/16	00
0F45B		FT2INTSH		R	8	00
0F45C	FTM2 interrupt clear register	FT2INTCL	FT2INTC	W	8/16	00
0F45D		FT2INTCH		W	8	00
0F460	FTM3 period register	–	FT3P	R/W	16	FFFF
0F462	FTM3 event register A	–	FT3EA	R/W	16	0000
0F464	FTM3 event register B	–	FT3EB	R/W	16	0000
0F466	FTM3 dead time register	–	FT3DT	R/W	16	0000
0F468	FTM3 counter register	–	FT3C	R/W	16	0000
0F46A	FTM3 control register 0	FT3CON0	–	R/W	8	00
0F46B	FTM3 control register 1	FT3CON1		R/W	8	00
0F46C	FTM3 mode register	FT3MODL	FT3MOD	R/W	8/16	00
0F46D		FT3MODH		R/W	8	00
0F46E	FTM3 clock register	FT3CLKL	FT3CLK	R/W	8/16	00
0F46F		FT3CLKH		R/W	8	00
0F470	FTM3 trigger register 0	FT3TRG0L	FT3TRG0	R/W	8/16	00
0F471		FT3TRG0H		R/W	8	00
0F472	FTM3 trigger register 1	FT3TRG1L	FT3TRG1	R/W	8/16	00
0F473		FT3TRG1H		R/W	8	00
0F478	FTM3 interrupt enable register	FT3INTEL	FT3INTE	R/W	8/16	00
0F479		FT3INTEH		R/W	8	00

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F47A	FTM3 interrupt status register	FT3INTSL	FT3INTS	R	8/16	00
0F47B		FT3INTSH		R	8	00
0F47C	FTM3 interrupt clear register	FT3INTCL	FT3INTC	W	8/16	00
0F47D		FT3INTCH		W	8	00
0F480	FTM output 01 select register	FTO0SL	FTO01SL	R/W	8/16	00
0F481		FTO1SL		R/W	8	00
0F482	FTM output 23 select register	FTO2SL	FTO23SL	R/W	8/16	00
0F483		FTO3SL		R/W	8	00
0F484	FTM output 45 select register	FTO4SL	FTO45SL	R/W	8/16	00
0F485		FTO5SL		R/W	8	00
0F486	FTM output 67 select register	FTO6SL	FTO67SL	R/W	8/16	00
0F487		FTO7SL		R/W	8	00
0F488	FTM output 89 select register	FTO8SL	FTO89SL	R/W	8/16	00
0F489		FTO9SL		R/W	8	00
0F48A	FTM output AB select register	FTOASL	FTOABSL	R/W	8/16	00
0F48B		FTOBSL		R/W	8	00
0F48C	FTM output CD select register	FTOCSL	FTOCDSL	R/W	8/16	00
0F48D		FTODSL		R/W	8	00
0F48E	FTM output EF select register	FTOESL	FTOEFSL	R/W	8/16	00
0F48F		FTOFSL		R/W	8	00

9.2.2 FTMn Period Register (FTnP : n=0,1,2,3)

Address: 0F400H(FT0P), 0F420H(FT1P), 0F440H(FT2P), 0F460H(FT3P)
Access: R/W
Access size: 16 bits
Initial value: FFFFH

	7	6	5	4	3	2	1	0
-	FTnP7	FTnP6	FTnP5	FTnP4	FTnP3	FTnP2	FTnP1	FTnP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8
-	FTnP15	FTnP14	FTnP13	FTnP12	FTnP11	FTnP10	FTnP9	FTnP8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

FTnP is a special function register (SFR) used to set the cycle (clock count of one cycle) of FTMn.
The valid range is 0001H to FFFFH (clock count: 2 to 65536).
Set this register after setting the operation mode using FTnMD.

Description of Bits

- **FTnP15-0** (bits 15 to 0)

FTnMD	FTnP15-0	Description
TIMER CAPTURE PWM1 PWM2	0001H-FFFFH	Set one period to FTnP setting value + 1 clock.

[Note]
When 0000H is written to this register, one period is set to 2 clocks. The read value is 0000H.

9.2.3 FTMn Event Register A (FTnEA : n=0,1,2,3)

Address: 0F402H(FT0EA), 0F422H(FT1EA), 0F442H(FT2EA), 0F462H(FT3EA)
Access: R/W
Access size: 16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
-	FTnEA7	FTnEA6	FTnEA5	FTnEA4	FTnEA3	FTnEA2	FTnEA1	FTnEA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
-	FTnEA15	FTnEA14	FTnEA13	FTnEA12	FTnEA11	FTnEA10	FTnEA9	FTnEA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FTnEA is a special function register (SFR) used to set the event timing of FTMn or indicate the captured data. Set this register after setting the operation mode using FTnMD. In the CAPTURE mode, this is a read-only register. It cannot be written.

Description of Bits

- **FTnEA15-0** (bits 15 to 0)

FTnMD	FTnEA15-0	Description
TIMER	0000H-FFFFH	Set the count value to generate an interrupt. (interrupt timing is FTnEA setting value + 1) This value must be less than the period register FTnP.
CAPTURE	0000H-FFFFH	The captured count value is stored. When it is read, FTnFLGA/FTnISA is cleared. In the CAPTURE mode, writing to FTnEA is disabled.
PWM1	0000H-FFFFH	Set the duty of PWM output FTMnP of FTMn.
PWM2	0000H-FFFFH	Set the duty of PWM output FTMnP and FTMnN of FTMn.

9.2.4 FTMn Event Register B (FTnEB : n=0,1,2,3)

Address: 0F404H(FT0EB), 0F424H(FT1EB), 0F444H(FT2EB), 0F464H(FT3EB)
Access: R/W
Access size: 16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
-	FTnEB7	FTnEB6	FTnEB5	FTnEB4	FTnEB3	FTnEB2	FTnEB1	FTnEB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
-	FTnEB15	FTnEB14	FTnEB13	FTnEB12	FTnEB11	FTnEB10	FTnEB9	FTnEB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FTnEB is a special function register (SFR) used to set the event timing of FTMn or indicate the captured data.
Set this register after setting the operation mode using FTnMD.
In the CAPTURE mode, this is a read-only register. It cannot be written.

Description of Bits

- **FTnEB15-0** (bits 15 to 0)

FTnMD	FTnEB15-0	Description
TIMER	0000H-FFFFH	Set the count value to generate an interrupt. (interrupt timing is FTnEB setting value + 1) This value must be less than the period register FTnP.
CAPTURE	0000H-FFFFH	The captured count value is stored. When it is read, FTnFLGB/FTnISB is cleared. In the CAPTURE mode, writing to FTnEB is disabled.
PWM1	0000H-FFFFH	Set the duty of PWM output FTMnN of FTMn.
PWM2	*	Set FTnIEB/FTnIOB to 0 in this mode.

9.2.5 FTMn Dead Time Register (FTnDT : n=0,1,2,3)

Address: 0F406H(FT0DT), 0F426H(FT1DT), 0F446H(FT2DT), 0F466H(FT3DT)
Access: R/W
Access size: 16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
-	FTnDT7	FTnDT6	FTnDT5	FTnDT4	FTnDT3	FTnDT2	FTnDT1	FTnDT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
-	FTnDT15	FTnDT14	FTnDT13	FTnDT12	FTnDT11	FTnDT10	FTnDT9	FTnDT8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FTnDT is a special function register (SFR) used to set the DeadTime of the timer output.
Set this register after setting the operation mode using FTnMD.

Description of Bits

- **FTnDT15-0** (bits 15 to 0)

FTnMD	FTnDT15-0	Description
TIMER PWM1/2	0000H-FFFFH	Set deadTime of timer output (the dead-time width is FTnDT setting value + 1) This bit is enable when FTnDTEN bit of FTnMOD register is set to "1".
CAPTURE	*	This register is disabled

9.2.6 FTMn Counter Register (FTnC : n=0,1,2,3)

Address: 0F408H(FT0C), 0F428H(FT1C), 0F448H(FT2C), 0F468H(FT3C)
Access: R/W
Access size: 16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
-	FTnC7	FTnC6	FTnC5	FTnC4	FTnC3	FTnC2	FTnC1	FTnC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
-	FTnC15	FTnC14	FTnC13	FTnC12	FTnC11	FTnC10	FTnC9	FTnC8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FTnC is a special function register (SFR) used to indicate the counter value of FTMn.
When writing to this register, the counter is cleared to "0000H".
This register should be accessed when the counter is stopped.

9.2.7 FTMn Control Register 0 (FTnCON0 : n=0,1,2,3)

Address: 0F40AH(FT0CON0), 0F42AH(FT1CON0), 0F44AH(FT2CON0), 0F46AH(FT3CON0)
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FTnCON0	–	–	FTnSDN	–	FTnEMGEN	–	FTnTGEN	FTnRUN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FTnCON0 is a special function register (SFR) used to set the function of FTMn.

Description of Bits

- **FTnRUN** (bit 0)
  Stop/start counting of FTMn by the software.

FTnMD	FTnRUN	Description
TIMER CAPTURE PWM1/2	0	Stop counting (initial value)
	1	Start counting/during counting

- **FTnTGEN** (bit 1)
  Allow stopping/starting counting by a trigger event.

FTnMD	FTnGTEN	Description
TIMER CAPTURE PWM1/2	0	Trigger operation disabled (initial value)
	1	Trigger operation enabled

- **FTnEMGEN** (bit 3)
  Allow emergency stop of FTMn.

FTnMD	FTnEMGEN	Description
TIMER	0	Emergency stop disabled (initial value)
PWM1/2	1	Emergency stop enabled
CAPTURE	*	This bit is disabled.

- **FTnSDN** (bit 5)
  Mask the output of FTMn to L.

FTnMD	FTnSDN	Description
TIMER PWM1/2	0	Release the output mask (initial value)
	1	Set the output mask (fix output to L).
CAPTURE	*	This bit is disabled.

9.2.8 FTMn Control Register 1 (FTnCON1 : n=0,1,2,3)

Address: 0F40BH(FT0CON1), 0F42BH(FT1CON1), 0F44BH(FT2CON1), 0F46BH(FT3CON1)
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FTnCON1	FTnSTAT	FTnFLGC	FTnFLGB	FTnFLGA	–	–	–	FTnUD
R/W	R	R	R	R	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FTnCON1 is a special function register (SFR) used to set the function of FTMn.

Description of Bits

- **FTnUD** (bit 0)
  This bit is used to update FTnP, FTnEA, FtnEB and FTnDT of FTMn during operation. To update FTnP, FTnEA, FtnEB and FTnDT, write "1" to this bit after setting these registers. Writing "1" transfers the setting values to the internal buffer of FTnP, FTnEA, FtnEB and FTnDT at the same time. When the transfer completes, this bit is cleared automatically.

FTnMD	FTnUD	Description
TIMER CAPTURE PWM1/2	0	Update completed (initial value)
	1	Requesting update

[Note]
To write "1" to this bit (to update register value), do so after reading this bit and confirm that the value is "0" (update is completed).

- **FTnFLGA** (bit 4)
  Indicates the state of event timing A of FTMn.

FTnMD	FTnFLGA	Description
TIMER PWM1/2	0	Counter value < Value of event register A (initial value)
	1	Counter value ≥ Value of event register A
CAPTURE	0	Capture data not available
	1	Capture data available. When FTnEA is read, it is cleared

- **FTnFLGB** (bit 5)
  Indicates the state of event timing B of FTMn.

FTnMD	FTnFLGB	Description
TIMER PWM1/2	0	Counter value < Value of event register B (initial value)
	1	Counter value ≥ Value of event register B
CAPTURE	0	Capture data not available
	1	Capture data available. When FTnEB is read, it is cleared

- **FTnFLGC** (bit 6)
  Indicates the control state by the CST bit of FTMn.
  When FTnC is read, it is cleared.

FTnMD	FTnFLGC	Description
TIMER PWM1/2 CAPTURE	0	Start enable state by event trigger (initial value)
	1	Start disable state by event trigger

- **FTnSTAT** (bit 7)
  Indicates the operation status of FTMn.

FTnMD	FTnSTAT	Description
TIMER CAPTURE PWM1/2	0	Counter stopped (initial value)
	1	Counter running

9.2.9 FTMn Mode Register (FTnMOD : n=0,1,2,3)

Address: 0F40CH(FT0MODL/FT0MOD), 0F40DH(FT0MODH),
0F42CH(FT1MODL/FT1MOD), 0F42DH(FT1MODH),
0F44CH(FT2MODL/FT2MOD), 0F44DH(FT2MODH),
0F46CH(FT3MODL/FT3MOD), 0F46DH(FT3MODH)
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
FTnMODL	FTnOST	FTnDTEN	–	–	–	–	FTnMD1	FTnMD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
FTnMODH	–	–	–	–	–	–	–	FTnSTPO
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FTnMOD is a special function register (SFR) used to set the function of FTMn.

Description of Bits

- **FTnMD1-0** (bits 1 to 0)
  Sets the mode of FTMn.

FTnMD	FTnMD1-0	Description
-	0	TIMER mode (initial value)
	1	CAPTURE mode
	2	PWM1 mode
	3	PWM2 mode

- **FTnDTEN** (bit 6)
  Enables the dead time of FTMn.

FTnMD	FTnDTEN	Description
TIMER PWM1/2	0	Dead time disabled (initial value)
	1	Dead time enabled
CAPTURE	*	This bit is disabled.

- **FTnOST** (bit 7)
  Sets auto-reload/one-shot mode of FTMn.

FTnMD	FTnOST	Description
TIMER PWM1/2	0	Auto-reload mode (initial value)
	1	One-shot mode
CAPTURE	0	Auto mode Even if the capture is performed once, the data of EA and EB is overwritten (updated) when the next capture is performed. When the counter goes round, it restarts from 0.
	1	Single mode Once captured into EA or EB, the next capture is not performed before read. When the counter goes round, it stops.

[Note]
When using the One-shot mode / Single mode, set to "1" FTnIEP of FTnINTE register and confirm that FTnISP of FTnINTS register is "0" always.

- **FTnSTPO** (bit 8)
  Sets the output state when FTMn stops.

FTnMD	FTnSTPO	Description
TIMER PWM1/2	0	Set the output to L at stop. If restarted without clearing the counter, it is L until the next period. (initial value)
	1	The current output state is kept after stop. When restarted without clearing the counter, the output depends on the counter value.
CAPTURE	*	Setting disabled.

9.2.10 FTMn Clock Register (FTnCLK : n=0,1,2,3)

Address: 0F40EH(FT0CLKL/FT0CLK), 0F40FH(FT0CLKH),
0F42EH(FT1CLKL/FT1CLK), 0F42FH(FT1CLKH),
0F44EH(FT2CLKL/FT2CLK), 0F44FH(FT2CLKH),
0F46EH(FT3CLKL/FT3CLK), 0F46FH(FT3CLKH)
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
FTnCLKL	–	FTnCKD2	FTnCKD1	FTnCKD0	–	–	FTnCK1	FTnCK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
FTnCLKH	–	–	–	–	–	FTnXCK2	FTnXCK1	FTnXCK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FTnCLK is a special function register (SFR) used to set the function of FTMn.

Description of Bits

- **FTnCK1-0** (bits 1 to 0)
  Selects the timer clock source of FTMn.

FTnMD	FTnCK	Description
TIMER CAPTURE PWM1/2	0	LSCLK (initial value)
	1	OSCLK
	2	HSCLK
	3	EXTCLK(Clock selected by FTnXCK2-0)

- **FTnCKD2-0** (bits 6 to 4)
  Selects the dividing ratio of the timer clock source of FTMn.

FTnMD	FTnCKD	Description
TIMER CAPTURE PWM1/2	0	divide by 1 (initial value)
	1	divide by 2
	2	divide by 4
	3	divide by 8
	4	divide by 16
	5	divide by 32
	6	divide by 64
	7	Reserved

- **FTnXCK2-0** (bits 10 to 8)
  Selects the source when selecting EXTCLK as a timer clock source of FTMn.

FTnMD	FTnXCK	Description
TIMER CAPTURE PWM1/2	0	TMCKI0 (initial value)
	1	TMCKI1
	2	TMCKI2
	3	TMCKI3
	4	TMCKI4
	5	TMCKI5
	6	TMCKI6
	7	TMCKI7

9.2.11 FTMn Trigger Register 0 (FTnTRG0 : n=0,1,2,3)

Address: 0F410H(FT0TRG0L/FT0TRG0), 0F411H(FT0TRG0H),
0F430H(FT1TRG0L/FT1TRG0), 0F431H(FT1TRG0H),
0F450H(FT2TRG0L/FT2TRG0), 0F451H(FT2TRG0H),
0F470H(FT3TRG0L/FT3TRG0), 0F471H(FT3TRG0H)
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
FTnTRG0L	–	–	–	–	FTnCST	FTnEXCL	FTnST1	FTnST0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
FTnTRG0H	FTnSTSS	–	–	–	FTnSTS3	FTnSTS2	FTnSTS1	FTnSTS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FTnTRG0 is a special function register (SFR) used to set the function of FTMn.

Description of Bits

- **FTnST0** (bit 0)
  Selects whether a trigger event starts the counter.

FTnMD	FTnST0	Description
TIMER CAPTURE PWM1/2	0	Starting counter enabled (initial value)
	1	Starting counter disabled

- **FTnST1** (bit 1)
  Selects whether a trigger event stops the counter.

FTnMD	FTnST1	Description
TIMER CAPTURE PWM1/2	0	Stopping counter disabled (initial value)
	1	Stopping counter enabled

- **FTnEXCL** (bit 2)
  Selects whether the counter is cleared when a trigger event stops it. It is not cleared at emergency stop regardless of the this bit setting.

FTnMD	FTnEXCL	Description
TIMER CAPTURE PWM1/2	0	Clearing the counter disabled (initial value)
	1	Clearing the counter enabled

- **FTnCST** (bit 3)
  Selects the operation mode of starting the counter by trigger event.

FTnMD	FTnCST	Description
TIMER CAPTURE PWM1/2	0	A trigger event always starts the counter when it is stopped (except for emergency stop) (initial value)
	1	A trigger event does not start the counter before FTnC is read when it is stopped (except for emergency stop)

- **FTnSTSS, FTnSTS3-0** (bits 15, 11 to 8)
  Selects the source of the trigger event for FTMn. Do not select itself, for example, FTM0 for the FTM0 setting.

FTnMD	FTnSTS*					Description
	S	3	2	1	0	
TIMER CAPTURE PWM1/2	0	0	0	0	0	EXI0TGO (initial value)
	0	0	0	0	1	EXI1TGO
	0	0	0	1	0	EXI2TGO
	0	0	0	1	1	EXI3TGO
	0	0	1	0	0	EXI4TGO
	0	0	1	0	1	EXI5TGO
	0	0	1	1	0	EXI6TGO
	0	0	1	1	1	EXI7TGO
	1	0	0	0	0	TM0INT
	1	0	0	0	1	TM1INT
	1	0	0	1	0	TM2INT
	1	0	0	1	1	TM3INT
	1	0	1	0	0	TM4INT
	1	0	1	0	1	TM5INT
	1	0	1	1	0	TM6INT
	1	0	1	1	1	TM7INT
	1	1	0	0	0	FTM0TGO
	1	1	0	0	1	FTM1TGO
	1	1	0	1	0	FTM2TGO
	1	1	0	1	1	FTM3TGO
	others					Reserved

[Note]
EXInTGO is the trigger signal from external terminals.
The timer interrupt request (TMnINT) is an interrupt request signal independent of the interrupt enabled/disabled setting of the interrupt enable register.
FTM trigger output(FTMnTGO) is used only for event trigger.

9.2.12 FTMn Trigger Register 1 (FTnTRG1 : n=0,1,2,3)

Address: 0F412H(FT0TRG1L/FT0TRG1), 0F413H(FT0TRG1H),
0F432H(FT1TRG1L/FT1TRG1), 0F433H(FT1TRG1H),
0F452H(FT2TRG1L/FT2TRG1), 0F453H(FT2TRG1H),
0F472H(FT3TRG1L/FT3TRG1), 0F473H(FT3TRG1H)
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
FTnTRG1L	–	–	FTnEST1	FTnEST0	–	–	FTnTRM1	FTnTRM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
FTnTRG1H	–	–	–	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FTnTRG1 is a special function register (SFR) used to set the function of FTMn.

Description of Bits

- **FTnTRM1-0** (bits 1 to 0)
  Selects the edge of the trigger event for FTMn.
  It is enabled only when EXI0-7 is selected as the event trigger source. Otherwise, it is fixed to the rising edge.

FTnMD	FTnTRM1-0		Description	
			Counter start	Counter stop/clear
TIMER CAPTURE PWM1/2	0	0	Rising edge	Rising edge (initial value)
	0	1	Falling edge	Rising edge
	1	0	Rising edge	Falling edge
	1	1	Falling edge	Falling edge

- **FTnEST1-0** (bits 5 to 4)
  Selects the emergency stop trigger source of FTMn. This bit is effective only when FTnEMGEN is 1.

FTnMD	FTnEST	Description
TIMER CAPTURE PWM1/2	0	Rising edge of EXI0TGO (initial value)
	1	Rising edge of EXI4TGO
	2	Rising edge of CMP0TGO
	3	Rising edge of CMP1TGO

[Note]
EXInTGO is the trigger signal from external terminals.
CMP0TGO,CMP1TGO is signal for trigger of the comparator.

9.2.13 FTMn Interrupt Enable Register (FTnINTE: n = 0,1,2,3)

Address: 0F418H(FT0INTEL/FT0INTE), 0F419H(FT0INTEH),
0F438H(FT1INTEL/FT1INTE), 0F439H(FT1INTEH),
0F458H(FT2INTEL/FT2INTE), 0F459H(FT2INTEH),
0F478H(FT3INTEL/FT3INTE), 0F479H(FT3INTEH)
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
FTnINTEL	–	–	–	FTnIETR	FTnIETS	FTnIEB	FTnIEA	FTnIEP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
FTnINTEH	–	–	–	–	–	FTnIOB	FTnIOA	FTnIOP
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FTnINTE is a special function register (SFR) used to control the interrupt of FTMn.
Setting a bit of FTnINTE to "1" makes the interrupt enabled and notifies the interrupt controller.

Description of Bits

- **FTnIEP** (bit 0)
  Sets the period interrupt enable of FTMn.

FTnMD	FTnIEP	Description
TIMER CAPTURE PWM1/2	0	Period interrupt disabled (initial value)
	1	Period interrupt enabled

- **FTnIEA** (bit 1)
  Sets the event timing A interrupt enable of FTMn.

FTnMD	FTnIEA	Description
TIMER PWM1/2	0	Event timing A interrupt disabled (initial value)
	1	Event timing A interrupt enabled
CAPTURE	0	Capture A interrupt disabled
	1	Capture A interrupt enabled

- **FTnIEB** (bit 2)
  Sets the event timing B interrupt enable of FTMn.

FTnMD	FTnIEB	Description
TIMER PWM1/2	0	Event timing B interrupt disabled (initial value)
	1	Event timing B interrupt enabled
PMW2	0	Set FTnIEB to 0 in this mode.
	1	Prohibited in this mode.
CAPTURE	0	Capture B interrupt disabled
	1	Capture B interrupt enabled

- **FTnIETS** (bit 3)
  Sets the trigger counter stop interrupt enable of FTMn.

FTnMD	FTnIETS	Description
TIMER CAPTURE PWM1/2	0	Trigger counter stop interrupt disabled (initial value)
	1	Trigger counter stop interrupt enabled

- **FTnIETR** (bit 4)
  Sets the trigger counter start interrupt enable of FTMn.

FTnMD	FTnIETR	Description
TIMER CAPTURE PWM1/2	0	Trigger counter start interrupt disabled (initial value)
	1	Trigger counter start interrupt enabled

- **FTnIOP** (bit 8)
  Outputs a period interrupt request of FTMn as the trigger for another peripheral.

FTnMD	FTnIOP	Description
TIMER CAPTURE PWM1/2	0	Period interrupt trigger disabled (initial value)
	1	Period interrupt trigger enabled

- **FTnIOA** (bit 9)
  Outputs an event timing A interrupt request of FTMn as the trigger for another peripheral.

FTnMD	FTnIOA	Description
TIMER CAPTURE PWM1/2	0	Event timing A interrupt trigger disabled (initial value)
	1	Event timing A interrupt trigger enabled

- **FTnIOB** (bit 10)
  Outputs an event timing B interrupt request of FTMn as the trigger for another peripheral.

FTnMD	FTnIOB	Description
TIMER CAPTURE PWM1/2	0	Event timing B interrupt trigger disabled (initial value)
	1	Event timing B interrupt trigger enabled
PWM2	0	Set FTnIOB to 0 in this mode.
	1	Prohibited in this mode.

9.2.14 FTMn Interrupt Status Register (FTnINTS : n=0,1,2,3)

Address: 0F41AH(FT0INTSL/FT0INTS), 0F41BH(FT0INTSH),
0F43AH(FT1INTSL/FT1INTS), 0F43BH(FT1INTSH),
0F45AH(FT2INTSL/FT2INTS), 0F45BH(FT2INTSH),
0F47AH(FT3INTSL/FT3INTS), 0F47BH(FT3INTSH)
Access: R
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
FTnINTSL	–	–	FTnISES	FTnISTR	FTnISTS	FTnISB	FTnISA	FTnISP
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
FTnINTSH	–	–	–	–	–	–	–	–
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

FTnINTS is a special function register (SFR) used to indicate the interrupt status of FTMn.
FTnINTS is a read-only register. Writing to it has no effect.

Description of Bits

- **FTnISP** (bit 0)
  Indicates the period interrupt state of FTMn.

FTnMD	FTnISP	Description
TIMER CAPTURE PWM1/2	0	Period interrupt has not occurred (initial value)
	1	Period interrupt has occurred This bit is cleared when writing 1 to FTnICP

- **FTnISA** (bit 1)
  Indicates the state of event timing A interrupt of FTMn.
  Indicates that the captured data is stored to FTnEA in the CAPTURE mode.

FTnMD	FTnISA	Description
TIMER PWM1/2	0	Event timing A interrupt has not occurred (initial value)
	1	Event timing A interrupt has occurred This bit is cleared when writing 1 to FTnICA
CAPTURE	0	Capture A interrupt has not occurred
	1	Capture A interrupt has occurred This bit is cleared when writing 1 to FTnICA or reading FTnEA

- **FTnISB** (bit 2)
  Indicates the state of event timing B interrupt of FTMn.

FTnMD	FTnISB	Description
TIMER PWM1/2	0	Event timing B interrupt has not occurred (initial value)
	1	Event timing B interrupt has occurred This bit is cleared when writing 1 to FTnIB
CAPTURE	0	Capture B interrupt has not occurred
	1	Capture B interrupt has occurred Indicates that the captured data is stored to FTnEB. This bit is cleared when writing 1 to FTnICB or reading FTnEB

- **FTnISTS** (bit 3)
  Indicates the trigger counter stop interrupt state of FTMn.

FTnMD	FTnISTS	Description
TIMER CAPTURE PWM1/2	0	Trigger counter stop interrupt has not occurred (initial value)
	1	Trigger counter stop interrupt has occurred This bit is cleared when writing 1 to FTnICTS

- **FTnISTR** (bit 4)
  Indicates trigger counter start interrupt state of FTMn.

FTnMD	FTnISTR	Description
TIMER CAPTURE PWM1/2	0	Trigger counter start interrupt has not occurred (initial value)
	1	Trigger counter start interrupt has occurred This bit is cleared when writing 1 to FTnICTR

- **FTnISES** (bit 5)
  Indicates the emergency stop interrupt state of FTMn.

FTnMD	FTnISES	Description
TIMER CAPTURE PWM1/2	0	Emergency stop interrupt has not occurred (initial value)
	1	Emergency stop interrupt has occurred This bit is cleared when writing 1 to FTnICES

9.2.15 FTMn Interrupt Clear Register (FTnINTC : n=0,1,2,3)

Address: 0F41CH(FT0INTCL/FT0INTC), 0F41DH(FT0INTCH),
0F43CH(FT1INTCL/FT1INTC), 0F43DH(FT1INTCH),
0F45CH(FT2INTCL/FT2INTC), 0F45DH(FT2INTCH),
0F47CH(FT3INTCL/FT3INTC), 0F47DH(FT3INTCH)
Access: W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
FTnINTCL	–	–	FTnICES	FTnICTR	FTnICTS	FTnICB	FTnICA	FTnICP
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
FTnINTCH	FTnIR	–	–	–	–	–	–	–
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

FTnINTC is a special function register (SFR) used to clear the interrupt status of FTMn.
When writing 1 to this bit, the target interrupt status is cleared.
When reading it, 0000H is always read.

Description of Bits

- **FTnICP** (bit 0)
  Clears the period interrupt of FTMn.

- **FTnICA** (bit 1)
  Clears the event timing A interrupt of FTMn.

- **FTnICB** (bit 2)
  Clears the event timing B interrupt of FTMn.

- **FTnICTS** (bit 3)
  Clears trigger counter stop interrupt of FTMn.

- **FTnICTR** (bit 4)
  Clears trigger counter start interrupt of FTMn.

- **FTnICES** (bit 5)
  Clears the emergency stop interrupt of FTMn.

- **FTnIR** (bit 15)
  Interrupt request bit of FTMn.
  Write "1" before exiting the interrupt vector. When there is any unprocessed interrupt source, the interrupt request is issued again.

9.2.16 FTM Output nm Select Register (FTOnmSL : n = 0,2,4,6,8,A,C,E, m=n+1)

Address: 0F480H(FTO0SL/FTO01SL), 0F481H(FTO1SL), 0F482H(FTO2SL/FTO23SL), 0F483H(FTO3SL), 0F484H(FTO4SL/FTO45SL), 0F485H(FTO5SL), 0F486H(FTO6SL/FTO67SL), 0F487H(FTO7SL), 0F488H(FTO8SL/FTO89SL), 0F489H(FTO9SL), 0F48AH(FTOASL/FTOABSL), 0F48BH(FTOBSL), 0F48CH(FTOCSL/FTOCDSL), 0F48DH(FTODSL), 0F48EH(FTOESL/FTOEFSL), 0F48FH(FTOFSL)
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
FTOnSL	FTOnSN	–	–	–	–	FTOnS2	FTOnS1	FTOnS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
FTOmSL	FTOmSN	–	–	–	–	FTOmS2	FTOmS1	FTOmS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FTOnmSL is a special function register (SFR) used to control assignment and output polarity of output FTMnP/FTMnN of FTM to TMOUT0 - F.

The word symbol FTOnmSL (nm=01,23,45,67,89,AB,CD,EF) corresponds to TMOUT0 - F as follows:

Pin name	Output signal name	Word symbol	Byte symbol
P02	TMOUT0	FTO01SL	FTO0SL
P03	TMOUT1		FTO1SL
P22	TMOUT2	FTO23SL	FTO2SL
P23	TMOUT3		FTO3SL
P32	TMOUT4	FTO45SL	FTO4SL
P33	TMOUT5		FTO5SL
P36	TMOUT6	FTO67SL	FTO6SL
P37	TMOUT7		FTO7SL
P42	TMOUT8	FTO89SL	FTO8SL
P43	TMOUT9		FTO9SL
P46	TMOUTA	FTOABSL	FTOASL
P47	TMOUTB		FTOBSL
P52	TMOUTC	FTOCDSL	FTOCSL
P53	TMOUTD		FTODSL
P56	TMOUTE	FTOEFSL	FTOESL
P57	TMOUTF		FTOFSL

Description of Bits

- **FTOnS2-0** (bits 2 to 0)/**FTOmS2-0** (bits 10 to 8)
  These bits used to select the FTM output that is assigned TMOUTx(X=0-F) output signal.

FTOnS2/ FTOmS2	FTOnS1/ FTOmS1	FTOnS0/ FTOmS0	Description
0	0	0	FTM0P (Initial value)
0	0	1	FTM0N
0	1	0	FTM1P
0	1	1	FTM1N
1	0	0	FTM2P
1	0	1	FTM2N
1	1	0	FTM3P
1	1	1	FTM3N

- **FTOnSN** (bit 7) / **FTOmSN** (bit 15)
  These bits reverse the FTM output.

FTOnSN/ FTOmSN	Description
0	Does not reverse the output. (Initial value)
1	Reverses the output.

9.3 Description of Operation

This operates as timer, capture, or PWM according to the mode set in FTnMD1-0.
This section describes start/stop by software/event trigger, emergency stop, interrupt processing, and output control for each mode.
FTMn has four types of operation mode: TIMER, CAPTURE, PWM1, and PWM2.

TIMER mode:
It controls the interrupt generation and output signal using the counter overflow.

CAPTURE mode:
It stores the count value when the selected trigger event is generated to the FTMn event register A (FTnEA) and FTMn event register B (FTnEB).

PWM1 mode:
It can generate two types of PWM waveform with the same period and aligned start edges, using the FTMn event register A (FTnEA) as the DUTY value of the output signal FTMnP and the FTMn event register B (FTnEB) as the DUTY value of the output signal FTMnN.

PWM2 mode:
It can generate a complementary PWM waveform where the output signal FTMnN operates exclusively, using the FTMn event register A (FTnEA) as the DUTY value of the output signal FTMnP. Also, the dead time can be set using the FTMn DeadTimer register (FTMnDT).

9.3.1 Common Sequence

FTM starts control by FTnCON0 after setting 1-6 described below as needed.
Then it processes interrupts and updates cycle/event settings and so on.

1: Mode setting (FTnMOD)
Select the mode using the mode register (FTnMOD). Also, set the dead time to output waveform, and so on.

2: Clock setting (FTnCLK)
Select the counter clock. This sets the source clock and the dividing ratio.

3: Trigger setting (FTnTRG0/1)
Use this setting when starting/stopping the counter by event trigger. Select the event trigger source and action for FTnTRG0, and the edge of the event trigger/emergency stop/capture for FTnTRG1.

4: Interrupt setting (FTnINTE)
Set the interrupt source. Select from period/event (counter coincide, duty, capture) and trigger start/stop interrupt.
When using the One-shot mode / Single mode, set to “1” FTnIEP of FTnINTE register and confirm that FTnISP of FTnINTS register is “0” always.

5: Period/event setting (FTnP, FTnEA, FTnEB, FTnDT)
Set the period, data for counter coincide, duty and dead time.

	TIMER	CAPTURE	PWM1	PWM2
FTnP	Auto-reload period or timeout of one-shot			
FTnEA	Coincident interrupt setting value	(Capture data.)	FTMnP duty	Duty
FTnEB	Coincident interrupt setting value		FTMnN duty	(Unused)
FTnDT	Dead time for output	(Unused)	Dead time for output	Dead time for output

The period is calculated as follows:

$$T_{priod} = \frac{FTnP + 1}{FTnCK\ [Hz]} \quad (FTnP : 0001H \text{ to } FFFFH)$$

6: Output setting (FTOSL*, Each Port Setting)
Set which output to which port, and reverse.

7: Control start/stop (FTnCON0)
Allow the software start or event trigger reception. Also, set the emergency stop enable.
The counter operates at a falling edge of FTnCK. The software start/stop are synchronized by FTnCK. FTnSTAT is set to H after FTnCK1 cycle at start, and the counter starts operating after two cycles. At stop, the counter is stopped in FTnCK1 cycle, and FTnSTAT is set to L. The counter value is kept at this time. If started again, it restarts after one cycle. To clear the counter, use write access to FTnC.

8: Processing during operation (FTnCON0/1, FTnINTS/C)
The state during operation can be seen in FTnCON1 or FTnINTS. To change the waveform of PWM, etc., set the period/event and set FTnUD of FTnCON1. Then, it is updated in the next period. Also, setting FTnSDN of FTnCON0 forces the output to be masked to L.

9.3.2 Counter Operation

The internal counter of FTM operates in the same way in all the modes.
It counts up until the setting value of the FTMn period register (FTnP).
At overflow in auto-reload mode (FTnOST bit of the FTMn mode register (FTnMOD) is "0"), the counter is cleared and continues counting again. At overflow in one-shot mode (FTnOST bit of FTnMOD is "1" and FTnIPE bit of FTnINTE is “1”), the counter is cleared and stops counting.
The software or trigger event can start/stop counting.

9.3.2.1 Starting/Stopping Counting by Software

When FTnRUN bit of the FTMn control register 0 (FTnCON0) is set to "1", the counter starts.
In one-shot mode (FTnOST bit of the FTMn mode register (FTnMOD) is "1"), FTnRUN bit is automatically set to "0" when the counter stops due to overflow.

If the counter is operating (FTnSTAT bit of the FTMn control register 1 (FTnCON1) is "1"), the counter stops when FTnRUN is set to "0". At this time, the counter keeps the value when it stops. When FTnRUN bit is set to "1" again, the counter continues from the stopped value.
To clear the counter, write to the FTMn counter register (FTnC) when it is not operating. (This written data is meaningless.)

9.3.2.2 Starting/Stopping Counting by Trigger Event

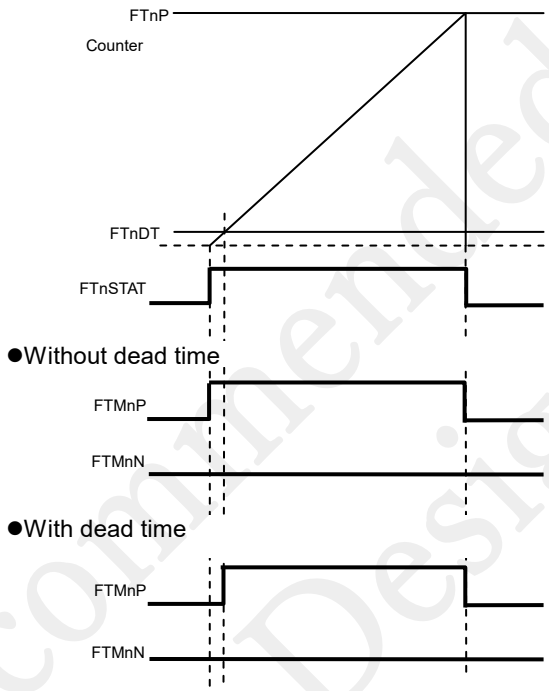
When FTnGTEN bit of the FIMTERn control register 0 (FTnCON0) is set to "1", the counter is made controllable by triggers.
Set the FTMn trigger setting register 0 and 1 (FTnTRG0, FTnTRG1) to select a trigger and so on.
The trigger event source can be selected from the external interrupts, the timer interrupts, and another FTM triggers.
The counter start, counter stop, or counter start/ stop can be selected by selecting a trigger event.

9.3.3 TIMER Mode Operation

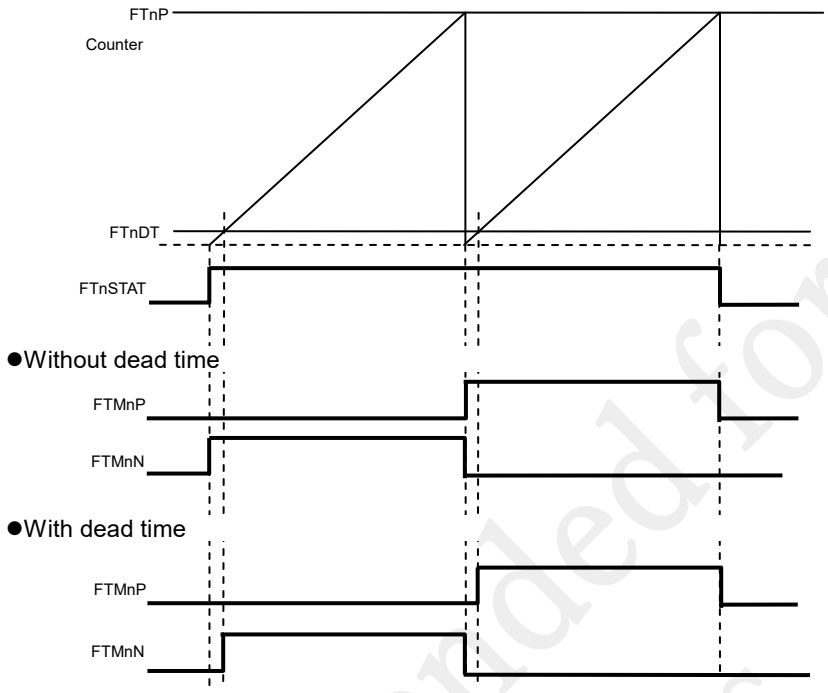
The TIMER mode controls the interrupt generation and output signal using the counter overflow.

9.3.3.1 Output Waveform in TIMER Mode

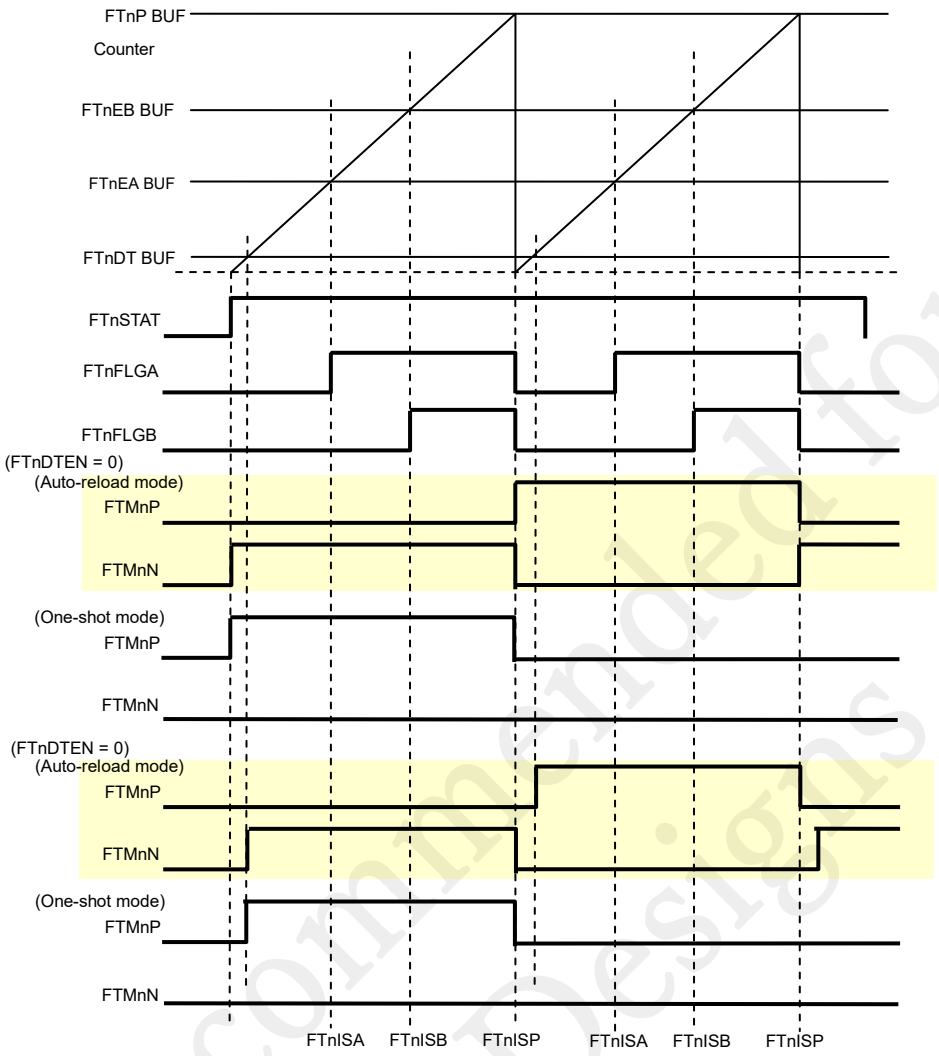
In the timer output auto-reload modem, the output is toggled for each period.
If the counter value is "0000H", FTMnP starts with L and FTMnN starts with H when FTnRUN bit of the FTMn control register 0 (FTnCON0) is set to "1".
In the one-shot mode, it stops after outputting H pulse of one period from FTMnP. FTMnN is fixed to L.
When the dead time is set using the FTMn DeadTime register (FTnDT), the output is L after starting the counter before passing the count set in FTnDT.



(a) TIMER mode output waveform (one-shot mode)



(b) TIMER mode output waveform (auto-reload mode)



(c) waveform and interrupt timing

$$T_{priod} = \frac{FTnP + 1}{FTnCK\ [Hz]} \quad (FTnP : 0001H \text{ to } FFFFH)$$

$$T_{eventA/B} = \frac{FTnEA(or\ FTnEB) + 1}{FTnCK\ [Hz]} \quad (FTnA/FTnB : 0000H \text{ to } FFFEH)$$

$$T_{deadtime} = \frac{FTnDT + 1}{FTnCK\ [Hz]} \quad (FTnDT : 0000H \text{ to } FFFEH)$$

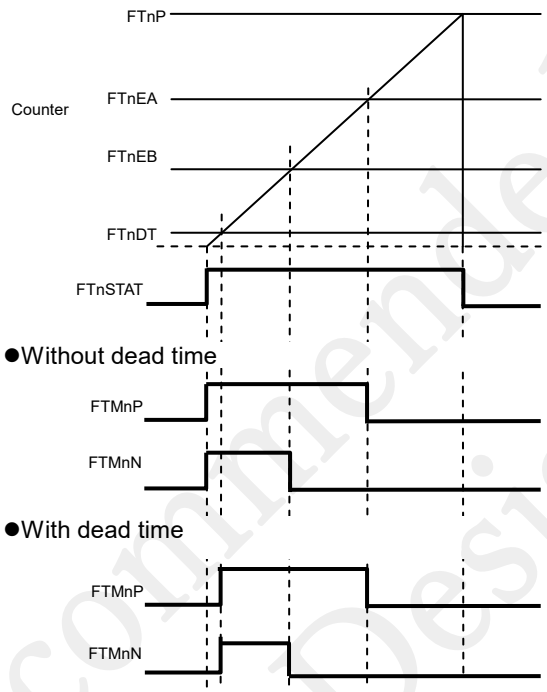
Figure 9-2 waveform in TIMER mode

9.3.4 PWM1 Mode Operation

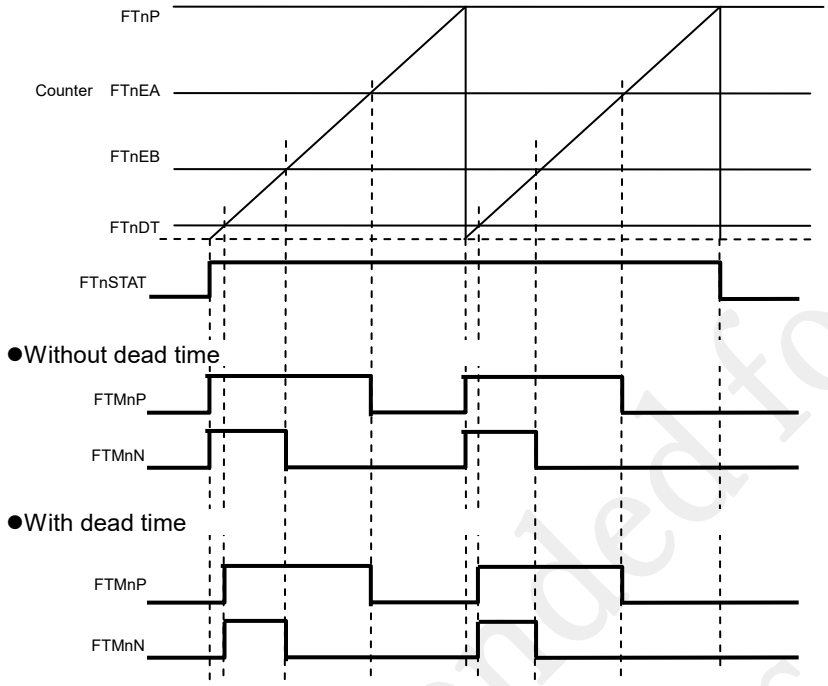
The PWM1 mode generates synchronization output pulses with the period set in FTnP. The duties of the output FTMnP and FTMnN are set in FTnEA and FTnEB respectively.

9.3.4.1 Output Waveform in PWM1 Mode

In the Auto-reload mode, the initial values of FTMnP and FTMnN are L, and they change to H at start. Each of them changes to L at the duty value. It changes to H in the next period. This is repeated until they stop. In the one-shot mode, they automatically stop and change to L after one period.
If the dead time is enabled, the FTMnP and FTMnN are L during the dead time from start of the counter.



(a) PWM1 mode output waveform (one-shot mode)



(b) PWM1 mode output waveform (auto-reload mode)

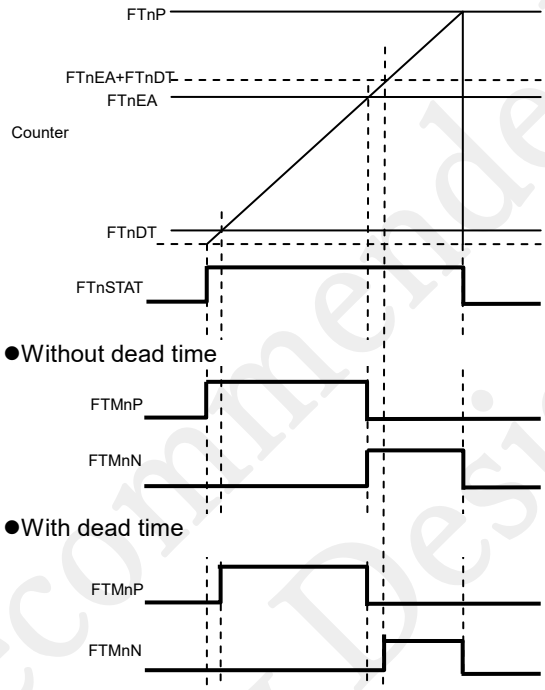
Figure 9-3 waveform in PWM1 mode

9.3.5 PWM2 Mode Operation

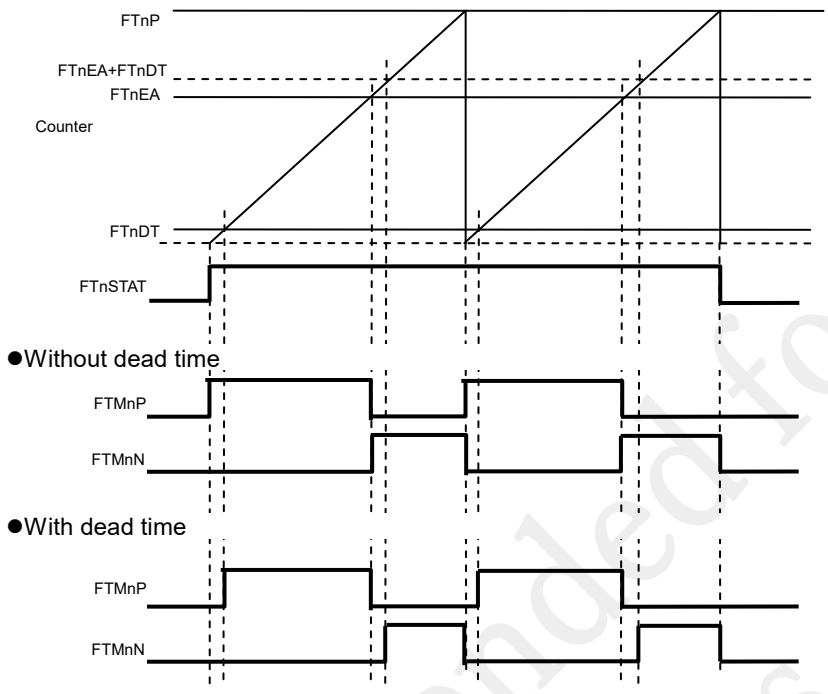
The PWM2 mode generates a complementary output pulse with the cycle set in FTnP. Set the duties of the output FTMnP/N in FTnEA. FTnEB is not used.

9.3.5.1 Output Waveform in PWM2 Mode

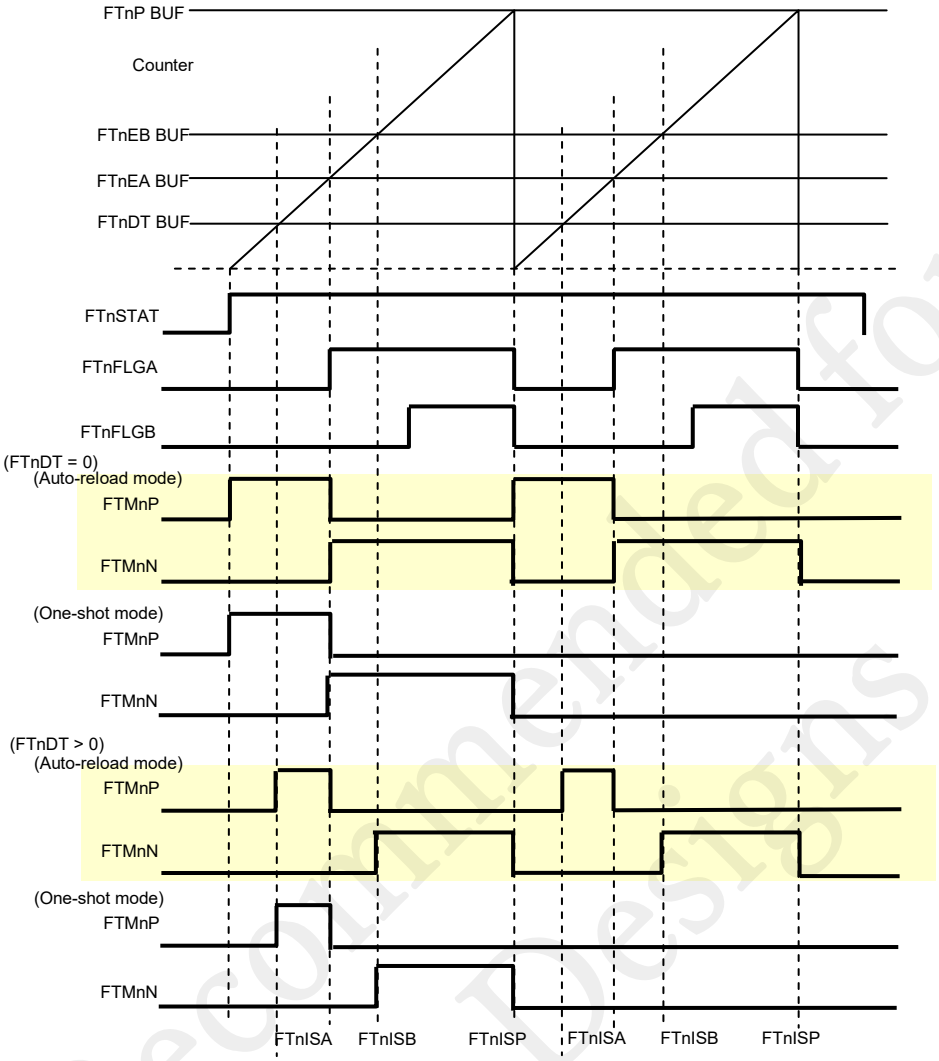
In the Auto-reload mode, the initial values of FTMnP and FTMnN are L, and FTMnP changes to H at start. FTMnP changes to L and FTMnN changes to H at the duty value. FTMnP changes to H and FTMnN changes to L in the next period. This is repeated until they stop. In the one-shot mode, they automatically stop and change to L after one period.
If the dead time is enabled, L is output during the dead time from start of the counter for FTMnP and from coincidence of duty for FTMnN.



(a) PWM2 mode output waveform (one-shot mode)



(b) PWM2 mode output waveform (auto-reload mode)



(c) waveform and interrupt timing

$$T_{priod} = \frac{FTnP + 1}{FTnCK\ [Hz]} \quad (FTnP : 0001H \text{ to } FFFFH)$$

$$T_{duty} = \frac{FTnEA + 1}{FTnCK\ [Hz]} \quad (FTnA/FTnB : 0000H \text{ to } FFFEH)$$

$$T_{deadtime1} = \frac{FTnDT + 1}{FTnCK\ [Hz]} \quad (FTnDT : 0000H \text{ to } FFFEH)$$

Figure 9-4 waveform in PWM2 mode

9.3.6 CAPTURE Mode Operation

The CAPTURE mode stores the count value at the time when an event trigger source is generated, to the FTnEA/FTnEB register. The event trigger source to be captured is common to that used at counter start/stop.

Stored data in FTnEA	Counter value at the time when an event trigger rising edge is generated
Stored data in FTnEB	Counter value at the time when an event trigger falling edge is generated

9.3.6.1 Measurement Example in the CAPTURE Mode

The following example shows the measurement of the period and duty of PWM input from EXI0 using CAPTURE mode and counter start/stop by trigger events.

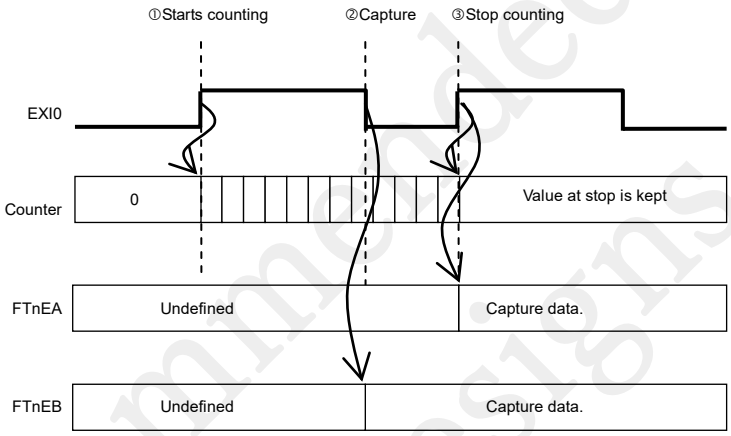


Figure 9-5 Measurement example in the CAPTURE mode

Set the FTnMOD register to the capture mode (FTnMD=01b).
Use the FTnINTE register (FTnIETS=1) to enable the trigger counter stop interrupt.
Use the FTnTRG0 register to set the trigger event source to EXI0 (FTnSTSS=0, FTnSTS=00H), enable counter start (FTnST0=1), and enable counter stop (FTnST1=1).
Use the FTnTRG1 register to set counter start and stop to rising edge (FTnTRM=00b).
Use the FTnCON0 register to enable the trigger operation (FTnTGEN=1).

The counter starts at rising of EXI0. (①)
Then the counter value is stored to the FTnEB register at falling of EXI0. (②)
When the rising of EXI0 is detected again, the counter stops, and an interrupt occurs. (③)
And the counter value is stored to the FTnEA register at rising of EXI0.

At this time, the values of FTnEA and FTnEB correspond to the period and the duty of EXI0 respectively.

The operation after capture depends on the FTnOST bit of the FTnMOD register.

●When FTnOST=0 (auto mode)

After the counter restarts at the next rising of EXI0, the value of FTnEA is updated at falling of EXI0.

●When FTnOST=1 (single mode)

After the counter restarts at the next rising of EXI0, the value of FTnEA is not updated at falling of EXI0.

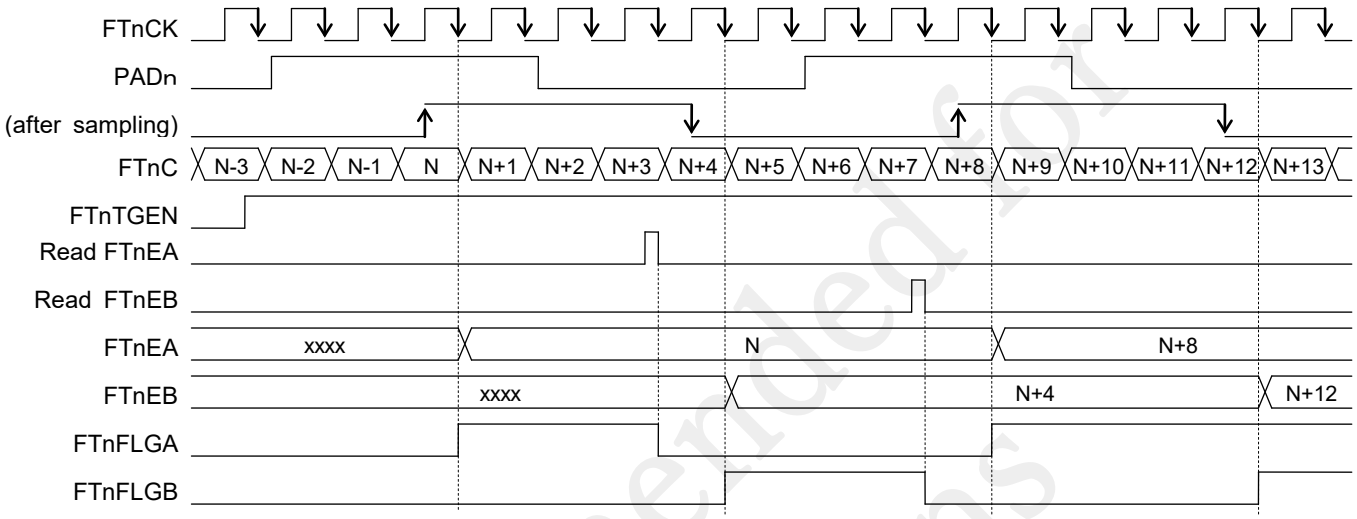


Figure 9-6 (a) FTnEA, FTnEB register read before next trigger (FTnOST=0,1)

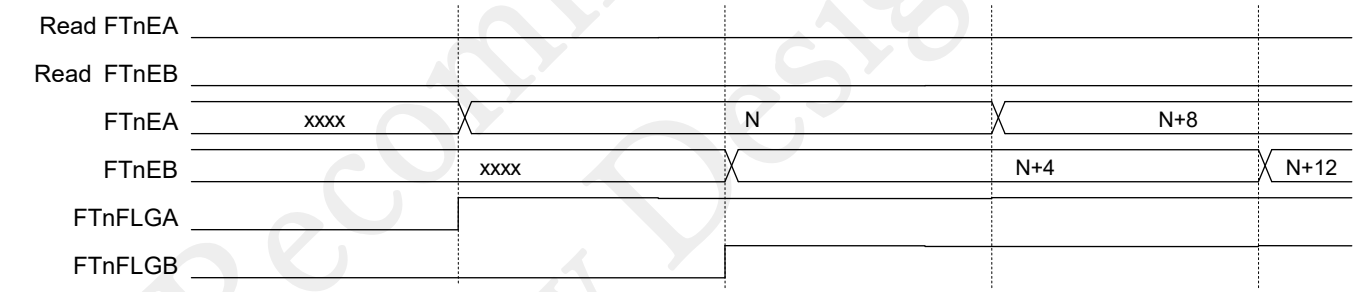


Figure 9-6 (b) Next trigger occurred without register read (FTnOST=0)

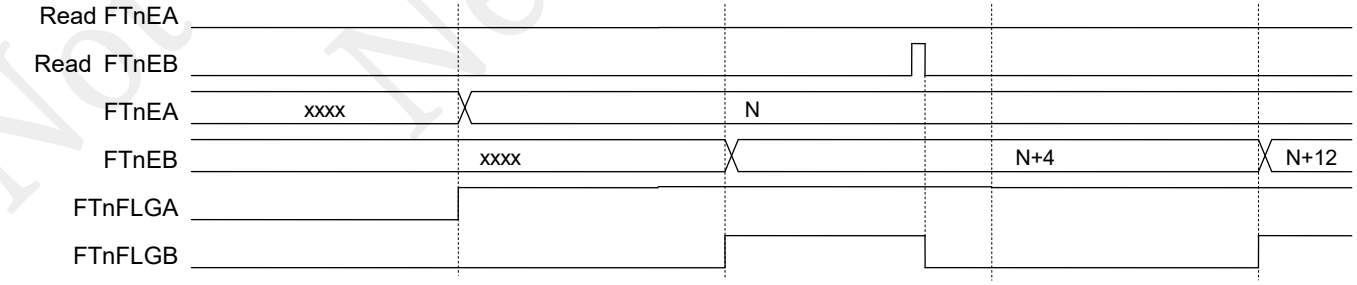


Figure 9-6 (c) Next trigger occurred without register read (FTnOST=1)

9.3.7 Event/Emergency Stop Trigger Control

9.3.7.1 Trigger Signal

FTMn can receive two types of trigger signal: event trigger and emergency stop trigger.
The event trigger is used as counter start/stop or trigger of capture. EXI0-7 (external interrupts), TIMER0-7 interrupts, or FTM0-3 triggers can be selected as the trigger source.
The emergency stop trigger is used to stop the timer operation. It stops the counter and sets output FTMnP/FTMnN to L. CMP0TGO/CMP1TGO interrupt, EXI0TGO, or EXI4TGO can be selected as the trigger source.

The analog filter output of the interrupt controller is connected to the EXI0-7TGO input.
The output of the sampling controller in the comparator is connected to the input from CMP0/1TGO.
The sampling can be selected using the comparator register.
The timer interrupt source and the FTM trigger source are set using the register of each timer.

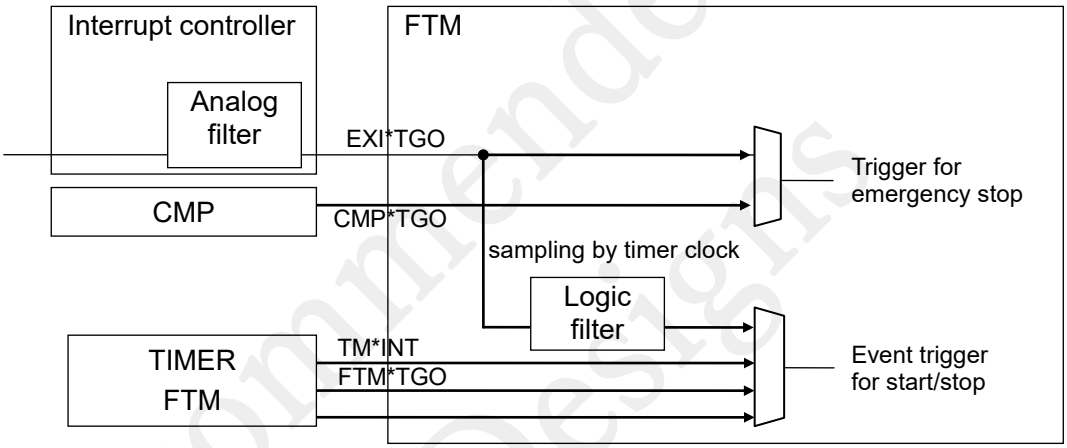


Figure 9-7 Input Path of Trigger Signal

9.3.7.2 Start/Stop Operations by Event Trigger

Here is the setting used to control the counter by event triggers.

1) FTnTRG0 setting
   Enable/Disable counter start/stop by event triggers
   Set whether or not to clear the counter at stop by an event trigger
   Set whether or not to accept the next counter start after stop by an event trigger
   Set the event trigger source (EXI0-7TGO, TIMER0-7INT, FTM0-3TGO)
2) FTnTRG1 setting
   Set the edge of the event trigger which generates counter start
   Set the edge of the event trigger which generates counter stop
3) Controlling FTnCON0
   Set FTnTGEN to "1" to enter the waiting state for event triggers.
   Then, set FTnRUN to "1" to start the counter by the software.
   Set FTnRUN to "0" during the counter operation to stop the counter by the software.

Because the trigger signal is sampled at FTnCK when the external input (EXInTGO) is selected as counter control by event triggers, the input pulse width should be set to Analog filter 200ns and three or more sampling clocks. Pulses shorter than three sampling clock may be or may not be removed. Note that the sampling is not performed when the timer interrupt is selected as the event trigger.

Figure 9-8 shows the sampling timing of the external input.

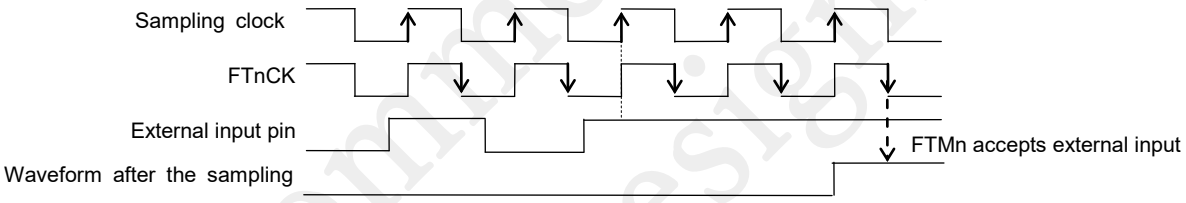
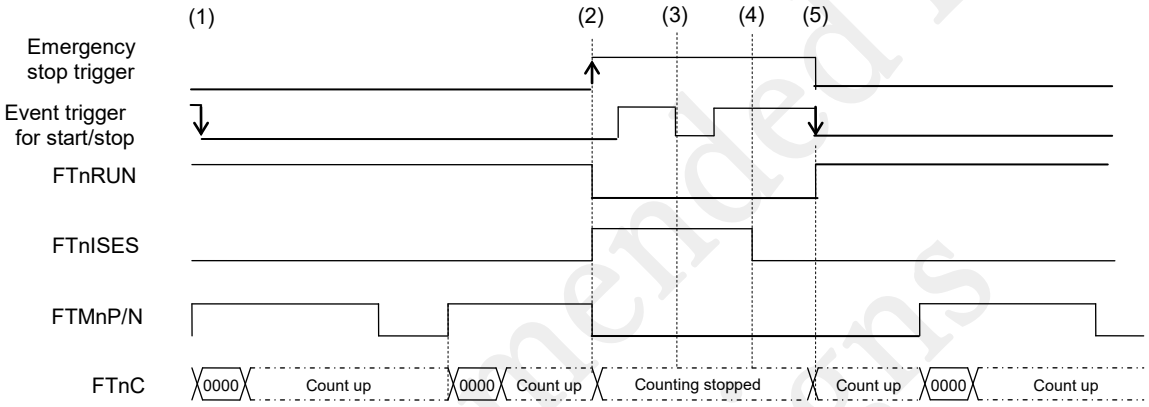


Figure 9-8 Sampling Timing of External Input

9.3.7.3 Emergency Stop Operation

When FTnEMGEN is set to "1", the emergency stop function is enabled. Set this bit after the trigger source is selected in FTnEST.
If an emergency stop trigger input (rising edge) is detected, the counter stops, the output is set to L, and an emergency stop interrupt occurs.
To restart the counter, clear the emergency stop interrupt status (write "1" to FTnICES) and "1" is set to run bit.
Figure 9-9 shows the operation timing at emergency stop.
After the emergency stop, the RUN bit is cleared to 0, the counter stops after one timer clock, and the STAT bit is cleared to 0. When the STAT bit is 1, setting the RUN to 1 is not accepted. Confirm that the STAT has changed to 0 after clearing the interrupt status before running the next RUN.



(1) The counter operation starts at an event trigger (falling edge).
(2) The counter stops at an emergency stop trigger (rising edge). An emergency stop interrupt occurs.
(3) The event trigger is disabled due to the emergency stop in progress.
(4) Clear the emergency stop interrupt to enable the operation.
(5) The counter operation restarts at an event trigger (falling edge).
(In this example, the pulse output restarts after one cycle because the counter is not cleared)

Figure 9-9 Operation Timing Diagram at Emergency Stop

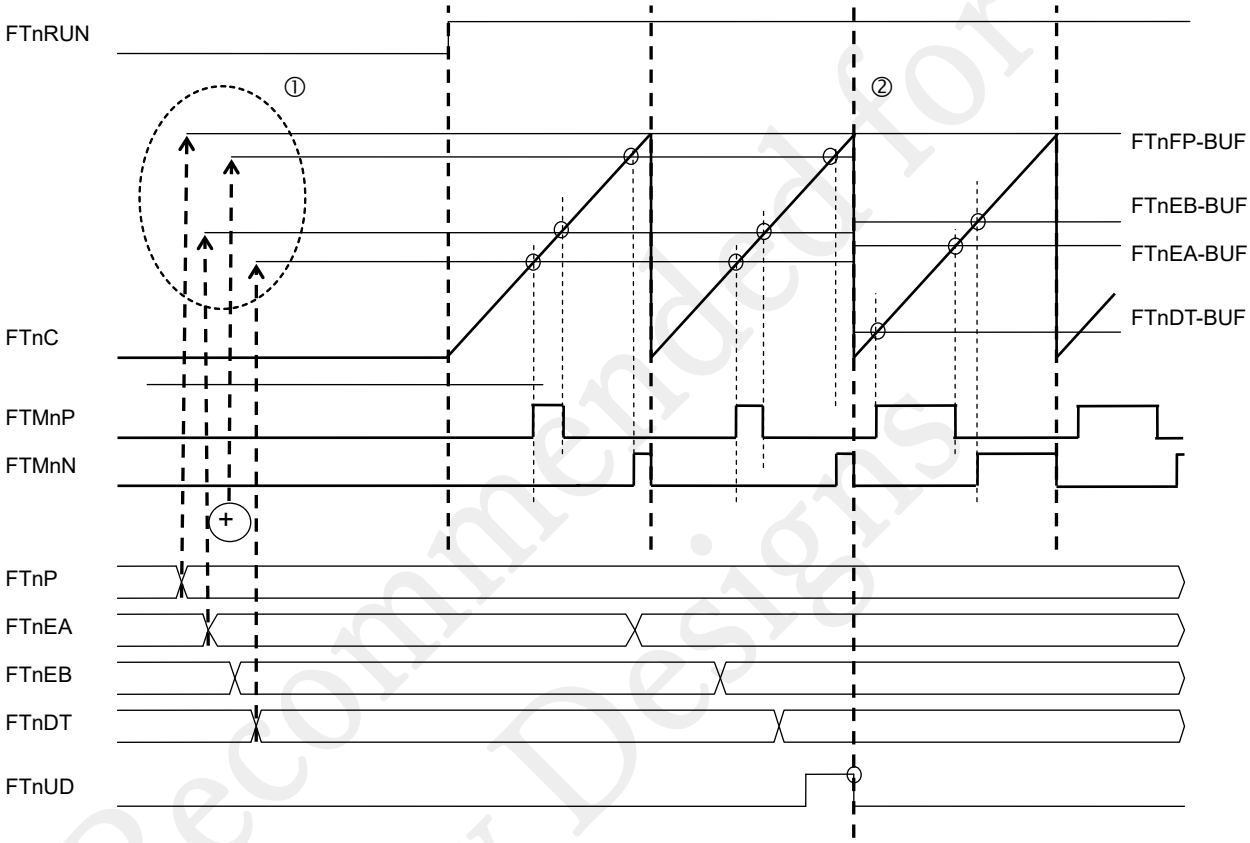
9.3.8 Output at Counter Stop

The FTMnP and FTMnN states depend on the setting of FTnSTPO when the counter stops by a software/Event trigger. If FTnSTPO is "0", FTMnP/FTMnN is set to "L" at the same time as stop. If the counter is restarted in this state, the FTMnP/FTMnN outputs keep "L" during that period, and they change according to the counter value from the next period.
When FTnSTPO is "1", FTMnP/FTMnN keep the state at stop. When the counter is restarted, their states change according to the counter value.
When the FTnEXCL bit of the FTnTRG0 register is set to "1" or the software clears the counter after counter stop, the counter value is counted up from "0000", and the output depends on the counter value.

9.3.9 Changing Period, Event A/B, and Dead Time during Operation

The period, event A/B, and dead time can be changed in the next cycle when the timer is counting.
To do so, set desired registers (FTnP, FTnEA, FTnEB, FTnDT, etc.), and then write "1" to the FTnUD bit of the FTnCON1 register to request the update. The values in the buffers for the period, event A/B, and dead time are updated at the beginning of the next period, and the FTnUD bit is set to "0".

Here is an example in the PWM2 mode (DTEN=1).



① Each buffer is updated at set timing during operation stopped.
② Each buffer is updated at the beginning of the next period where PFUD is set to "1" during operation.

Figure 9-10 Update Timing during Operation

9.3.10 Interrupt Source

This section describes the interrupt source and how to clear it.
When a target interrupt enable (FTnIE*) is set to "1", the interrupt status is enabled, and the interrupt controller is notified of the source.
Note that the emergency stop interrupt enable does not exist. When the emergency stop is enabled, its interrupt is also enabled.
If the interrupt status is set to "1" for a source, clear it by an appropriate processing.
When the interrupt vector is used, write "1" to FTnIR at the end of the interrupt processing (when exiting the interrupt vector).

Name	Mode	Status	How to clear
Period coincident interrupt	ALL	FTnISP	Write "1" to FTnICP
Event A coincident interrupt	TIMER/PWM1/PWM2	FTnISA	Write "1" to FTnICA
Capture A interrupt	CAPTURE	FTnISA	Write "1" to FTnICA or read FTnEA
Event B coincident interrupt	TIMER/PWM1	FTnISB	Write "1" to FTnICB
Capture B interrupt	CAPTURE	FTnISB	Write "1" to FTnICB or read FTnEB
Trigger stop interrupt	ALL	FTnISTS	Write "1" to FTnICTS
Trigger start interrupt	ALL	FTnISTR	Write "1" to FTnICTR
Emergency stop interrupt	ALL	FTnISES	Write "1" to FTnICES

The period coincident interrupt/event A coincident interrupt/event B coincident interrupt can be selected as the interrupt trigger output.

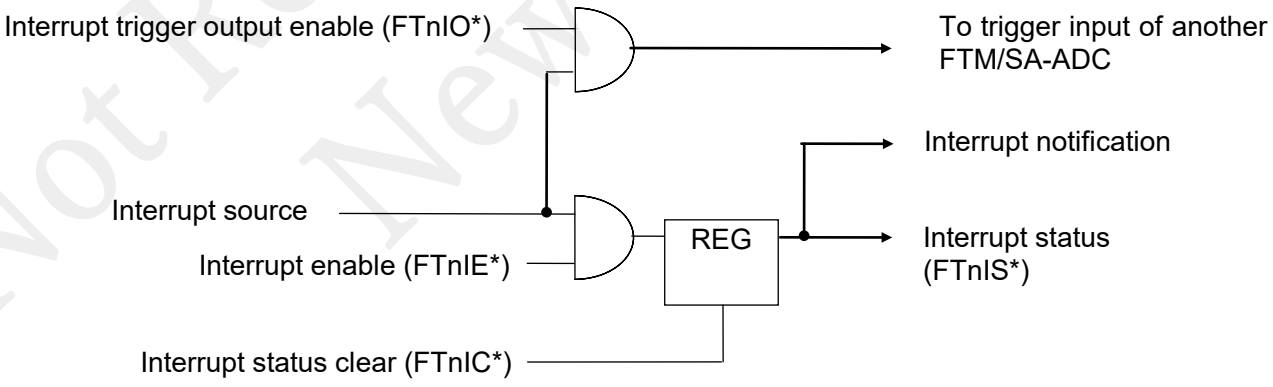


Figure 9-11 interrupt controlling

Chapter 10

Watchdog Timer

10 Watchdog Timer

10.1 Overview

Watchdog timer is free run counter that is used for detection of program abnormal behavior.
The watchdog timer start count automatically after system reset release and requests WDT interrupt when the first overflow occurs.
When the second overflow occurs, the watchdog timer generates a WDT reset signal and shifts the mode to a system reset mode.
For interrupts see Chapter 5, "Interrupts," and for WDT interrupt see Chapter 3, "Reset Function".

10.1.1 Features

- Free running (stop setting in DEEP-HALT mode is available)
- Count low-speed clock 128 period.
- One of four types of overflow periods (125ms, 500ms, 2s, and 8s @LSCLK=32.768kHz) selectable by software
- Requests a WDT interrupt (non-maskable interrupt) by the first overflow
- Reset generated by the second overflow

10.1.2 Configuration

Figure 10-1 shows the configuration of the watchdog timer.

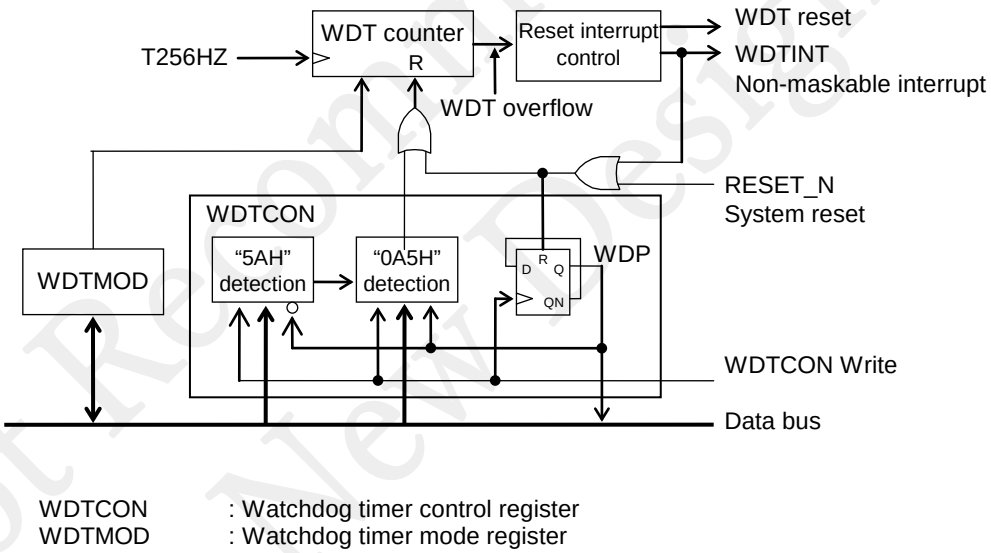


Figure 10-1 Configuration of Watchdog Timer

10.2 Description of Registers

10.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F00E	Watchdog timer control register	WDTCON	–	R/W	8	00
0F00F	Watchdog timer mode register	WDTMOD	–	R/W	8	82

10.2.2 Watchdog Timer Control Register (WDTCON)

Address: 0F00EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
WDTCON	d7	d6	d5	d4	d3	d2	d1	WDP/d0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

WDTCON is a special function register (SFR) to control the Watchdog Timer.
When write to WDTCON, the value of the internal pointer (WDP) is reversed .
WDT counter is cleared when "5AH" and "0A5H" is written to WDTCON in succession.
The value in WDP is read from bit0 when WDTCON is read. In this time "0" is read from bit7-bit1.
WDP is reset to "0" at system reset and at overflow.

For WDT counter clear, write "5AH" when WDP state is "0" and write "0A5H" when WDP state is "1".
If WDT state is different from above, WDT counter cannot be cleared, even if these clear data is written.

This register requires byte access always.

[Note]
When the WDT interrupt(WDTINT) is occurred by the WDT counter first overflow, the WDT counter and the internal pointer(WDP) are initialized for 1/2 clock period of low-speed clock(approximately 15.26us@32.768kHz). Therefore the writing to the WDTCON becomes invalid during the period and WDP is not reversed. I In processing clear WDT when WDT interrupt occur and system clock is in high-speed clock state, Confirm that WDP is reversed by writing to WDTCON and confirm the writing to WDTCON is done normally.

.

10.2.3 Watchdog Timer Mode Register (WDTMOD)

Address: 0F00FH
Access: R/W
Access size: 8 bits
Initial value: 82H

	7	6	5	4	3	2	1	0
WDTMOD	HLTEN	–	–	–	–	–	WDT1	WDT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	0	0	0	0	0	1	0

WDTMOD is a special function register to set the overflow period of theWDT counter.
This register requires byte access always.

Description of Bits

- **WDT1-0** (bits 1 to 0)

These bits are used to select an overflow period of the watchdog timer.
The WDT1 and WDT0 bits set a overflow period (T_{WOV}) of the WDT counter. It is selectable from the following.

WDT1	WDT0	Description
0	0	4096 counts at LSCLK (125 ms*)
0	1	16384 counts at LSCLK (500 ms*)
1	0	65536 counts at LSCLK (2 s*) (initial value)
1	1	262144 counts at LSCLK (8 s*)

*: where LSCLK = 32.768kHz.

- **HLTEN** (bits 7)

Set WDT cuount up fuction mode during DEEP-HALT mode.

HLTEN	Description
0	Stop counting up during DEEP-HALT mode
1	Keep counting up during DEEP-HALT mode（initial value）

10.3 Description of Operation

The WDT counter starts counting after the system reset has been released and the low-speed clock(LSCLK) oscillation start.
Write "5AH" when the internal pointer (WDP) is "0"and then the WDT counter is cleared by writing "0A5H" when WDP is "1".
WDP is reset to "0" at the time of system reset or when the WDT counter overflows and is inverted whenever data is written to WDTCON.
When the WDT counter cannot be cleared within the WDT counter overflow period (TWOV), a watchdog timer interrupt (WDTINT) occurs. If the WDT counter is not cleared even by the software processing performed following the watchdog timer interrupt and overflow occurs again, WDT reset occurs and the mode shifts to a system reset mode.
For the overflow period TWOV) of the WDT counter, one of 125ms, 500ms, 2s, and 8s can be selected by the watchdog mode register (WDTMOD).
Clear the WDT counter within the clear period of the WDT counter shown in Table 10-1.

Table 10-1 Clear Period of WDT Counter

WDT1	WDT0	T_{WOV}	T_{WCL}
0	0	4096 counts at LSCLK (125 ms*)	3968 counts at LSCLK (Approx. 121 ms*)
0	1	16384 counts at LSCLK (500 ms*)	16256 counts at LSCLK (Approx. 496 ms*)
1	0	65536 counts at LSCLK (2000 ms*)	65408 counts at LSCLK (Approx. 1996 ms*)
1	1	262144 counts at LSCLK (8000 ms*)	262016 count at LSCLK (Approx. 7996 ms*)

*: where LSCLK = 32.768kHz. T_{WOV} and T_{WCL} depends on a frequency of the LSCLK.

[Note]
WDT counter clock is T256HZ that is divided by 128 of LSCLK. Therfor, keep on supply the LSCLK during not reset and STOP-mode conditions.

・The time of Table 10-1 is changed with the frequency of the LSCLK to be used. It is calculable by the frequency of low speed crystal oscillator to be used as follows.

Ex)Operate by LSCLK=32.768kHz (set WDT1/WDT0=00)

T_{WOV} : 1 / ((32.768[kHz]) / 128 [dividing]) * 32 [clock] = 125 [msec]

Figure 10-2 shows an example of watchdog timer operation.

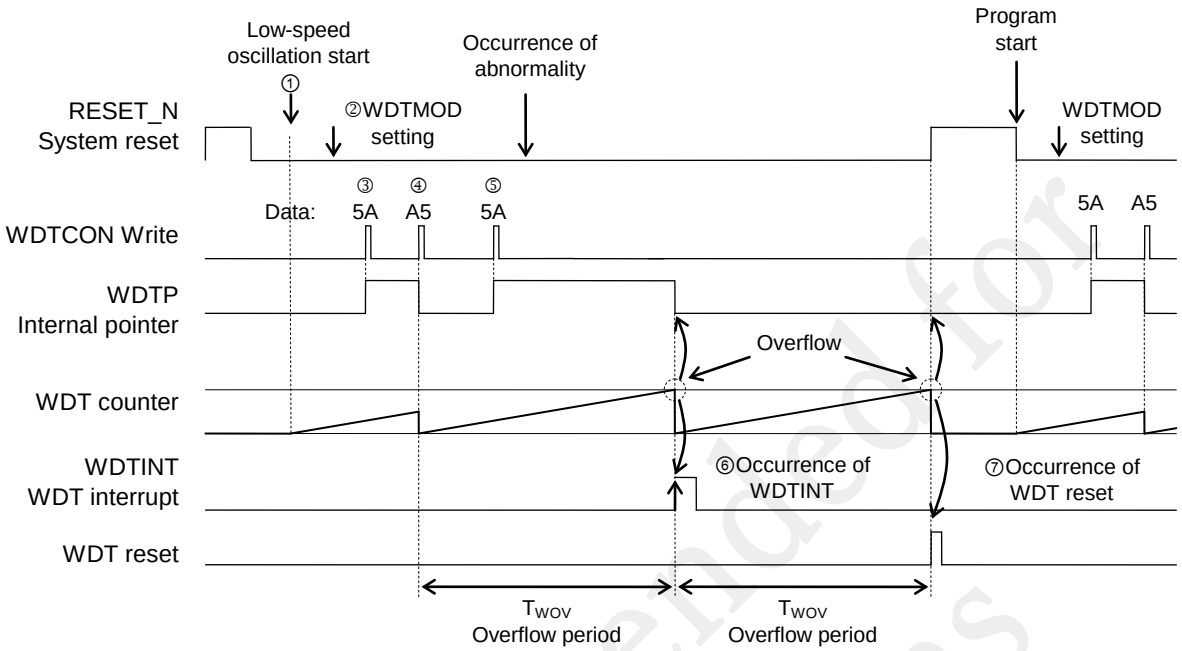


Figure 10-2 Example of Watchdog Timer Operation

① The WDT counter starts counting after the system reset has been released and the low-speed clock oscillation start.
② The overflow period of the WDT counter (T_{WOV}) is set to WDTMOD.
③ Write "5AH" to WDTCON. (Internal pointer 0→1)
④ Write "0A5H" to WDTCON and clear the WDT counter. (Internal pointer 1→0)
⑤ Write "5AH" to WDTCON. (Internal pointer 0→1)
⑥ If abnormalities occur and the writing of "0A5H" is not performed, WDT counter overflows. Watchdog timer interrupt occurs because the overflow is the first overflow after reset of WDT counter. In addition, during the period of the half clock of LSCLK, WDT counter and internal pointer are initialized. While it is initialized, the writing to WDTCON becomes invalid, and internal pointer doesn't turn over.
⑦ If the WDT counter is not cleared even by the software processing performed following a watchdog timer interrupt and the WDT counter overflows again, WDT reset occurs and the mode is shifted to a system reset mode.

[Note]
- In STOP mode, the watchdog timer operation also stops. When the WDT interrupt occurs, the HALT(DEEP-HALT, HALT-H, HALT) mode is released.
- The watchdog timer cannot detect all the abnormal operations. Even if the CPU loses control, the watchdog timer cannot detect the abnormality in the operation state in which the WDT counter is cleared.

10.3.1 The process example when not using Watchdog Timer

Watchdog timer cannot be stopped. Even when the watchdog timer function is not used as failsafe measures, it is necessary to clear WDT counter.
The example program which clears WDT counter at WDT interrupt occurs, and controls the system reset by WDT is shown.

The example of program description:

```
do
 {
    WDTCON = 0x5a;
 } while(WDP !=1)
    WDTCON = 0xa5;
```

Chapter 11

Synchronous Serial Port (SSIO)

11 Synchronous Serial Port

11.1 Overview

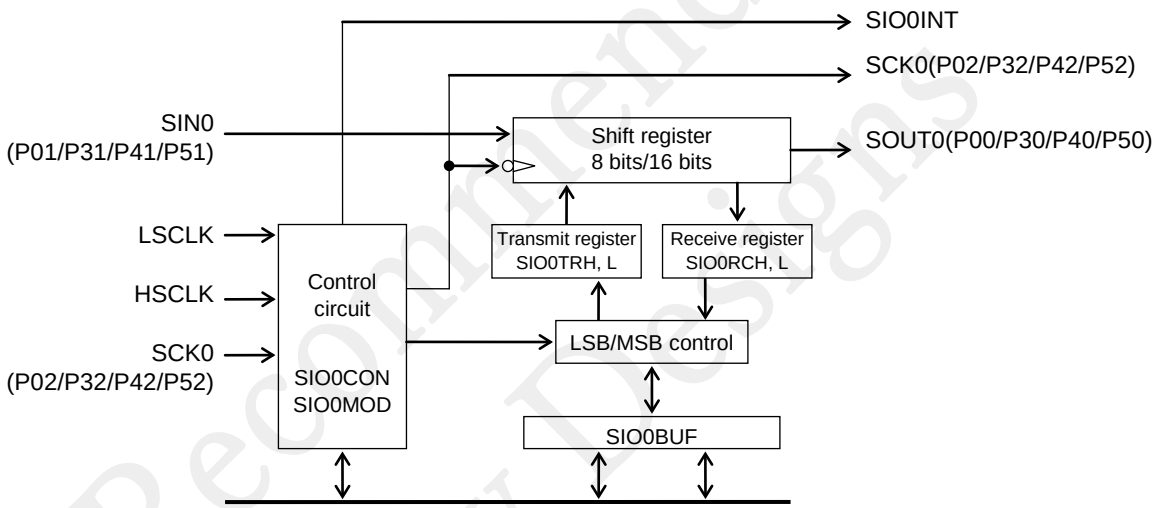
This LSI includes one channel of the 8/16-bit synchronous serial port (SSIO) and can also be used to control the device incorporated with the SPI interface by using one GPIO as the chip enable pin.

11.1.1 Features

- Master or slave selectable
- MSB first or LSB first selectable
- 8-bit length or 16-bit length selectable for the data length
- Selectable phase and polarity of clock

11.1.2 Configuration

Figure 11-1 shows the configuration of the synchronous serial port.



SIO0BUF: Serial port transmit/receive buffer
SIO0CON: Serial port control register
SIO0MOD: Serial port mode register

Figure 11-1 Configuration of Synchronous Serial Port

11.1.3 List of Pins

Pin name	I/O	Description
SIN0	I	Receive data input.
SCK0	I/O	Synchronous clock input/output.
SOUT0	O	Transmit data output.

11.2 Description of Registers

11.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F700	Serial port 0 transmit/receive buffer	SIO0BUFL	SIO0BUF	R/W	8/16	00
0F701		SIO0BUFH		R/W	8	00
0F702	Serial port 0 control register	SIO0CON	–	R/W	8	00
0F704	Serial port 0 mode register	SIO0MOD0	SIO0MOD	R/W	8/16	00
0F705		SIO0MOD1		R/W	8	00

11.2.2 Serial Port 0 Transmit/Receive Buffer (SIO0BUF)

Address: 0F700H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
SIO0BUFL	S0B7	S0B6	S0B5	S0B4	S0B3	S0B2	S0B1	S0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
SIO0BUFH	S0B15	S0B14	S0B13	S0B12	S0B11	S0B10	S0B9	S0B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0BUF are special function registers (SFRs) to write transmit data and to read receive data of the synchronous serial port 0.
When data is written in SIO0BUF, the data is written in the transmit registers (SIO0TRL and SIO0TRH) and when data is read from SIO0BUF, the contents of the receive registers (SIO0RCL and SIO0RCH) are read.

11.2.3 Serial Port 0 Control Register (SIO0CON)

Address: 0F702H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
-	–	–	–	–	–	–	–	S0EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0CON is a special function register (SFR) to control the synchronous serial port 0.

Description of Bits

- **S0EN** (bit 0)

The S0EN bit is used to specify start of synchronous serial communication. Writing a "1" to this bit starts 8-/16-bit data communication. This bit is set to "0" automatically when 8-/16-bit data communication is terminated.

S0EN	Description
0	Stops communication. (Initial value)
1	Starts communication

[Note]
Setting ports and SSIO should be completed before setting S0EN to "1".

11.2.4 Serial Port 0 Mode Register (SIO0MOD)

Address: 0F704H
Access: R/W
Access size: 8/16bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
SIO0MOD0	–	–	–	–	S0LG	S0MD1	S0MD0	S0DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
SIO0MOD1	–	–	S0NEG	S0CKT	–	S0CK2	S0CK1	S0CK0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SIO0MOD is a special function register (SFR) to set mode of the synchronous serial port 0.

Description of Bits

- **S0DIR** (bit 0)

The S0DIR is used to select LSB first or MSB first.

S0DIR	Description
0	LSB first (initial value)
1	MSB first

- **S0MD1-0** (bits 2 to 1)

The S0MD1 and S0MD0 bits are used to select transmit, receive, or transmit/receive mode of the synchronous serial port.

S0MD1	S0MD0	Description
0	0	Stops transmission/reception (initial value)
0	1	Receive mode
1	0	Transmit mode
1	1	Transmit/receive mode

- **S0LG** (bit 3)

The S0LG bit is used to specify the bit length of the transmit/receive buffer, 8-bit or 16-bit length.

S0LG	Description
0	8-bit length (initial value)
1	16-bit length

- **S0CK2-0** (bits 10 to 8)

The S0CK2-0 bits are used to select the transfer clock of the synchronous serial port. When the internal clock is selected, this LSI is set to master mode and when the external clock is selected, it is set to slave mode.

S0CK2	S0CK1	S0CK0	Description
0	0	0	1/1 LSCLK (initial value)
0	0	1	1/2 LSCLK
0	1	0	1/4 OSCLK
0	1	1	1/8 OSCLK
1	0	0	1/16 OSCLK
1	0	1	1/32 OSCLK
1	1	0	External clock 0 (SCK0)
1	1	1	reserved

- **S0CKT** (bit 12)

The S0CKT bit is used to select a transfer clock phase.

S0CKT	Description
0	Clock type 0: Clock is output with a “H” level being the default. (Initial value)
1	Clock type 1: Clock is output with a “L” level being the default.

- **S0NEG** (bit 13)

The S0NEG bit is used to select the positive or negative logic of the transfer clock.

S0NEG	Description
0	Positive logic (Initial value)
1	Negative logic

[Note]
- Do not change any of the SIO0MOD register settings during transmission/reception.
- SCK0 Max clock input frequency is 1/4 of SYSCLK or 2MHz at slave mode.
- SCK0 Max clock output frequency is 2MHz if using P02 as SCK0 in master mode.

11.3 Description of Operation

11.3.1 Transmit Operation

When "1" is written to the S0MD1 bit and "0" is written to the S0MD0 bit of the serial mode register (SIO0MOD), this LSI is set to a transmit mode.
When transmit data is written to the serial port transmit/receive buffer (SIO0BUF) and the S0EN bit of the serial port control register (SIO0CON) is set to "1", transmission starts. When transmission of 8/16-bit data terminates, a synchronous serial port interrupt (SIO0INT) occurs and the S0EN bit is set to "0".
Transmit data is output from SOUT0 pin.
When an internal clock is selected in the serial port mode register (SIO0MOD), the LSI is set to a master mode and when an external clock (SCK0) is selected, the LSI is set to a slave mode.
The serial port mode register (SIO0MOD) enables selection of MSB first/LSB first.
The transmit data output pin (SOUT0) and transfer clock input/output pin (SCK0) must be set to the tertiary functions.
Figures 11-2, 11-3, 11-4 and 11-5 show the transmit operation waveforms of the synchronous serial ports for "clock type 0 and positive-logic", "clock type 0 and negative-logic", "clock type 1 and positive-logic" and "clock type 1 and negative-logic", respectively (8-bit length, LSB first).

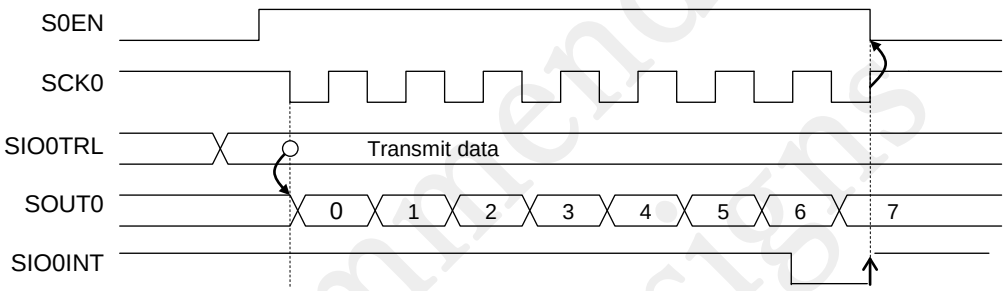


Figure 11-2 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8-bit Length, LSB first, Positive Logic)

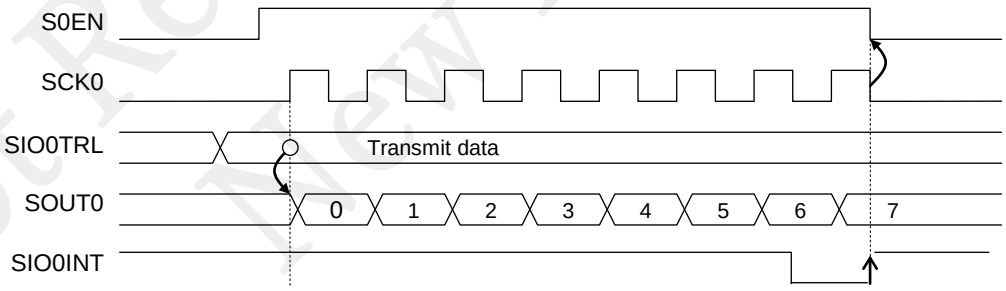


Figure 11-3 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8-bit Length, LSB first, Negative Logic)

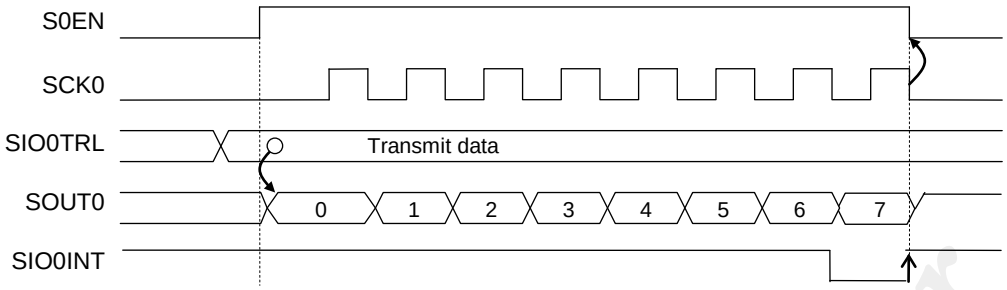


Figure 11-4 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8-bit Length, LSB first, Positive Logic)

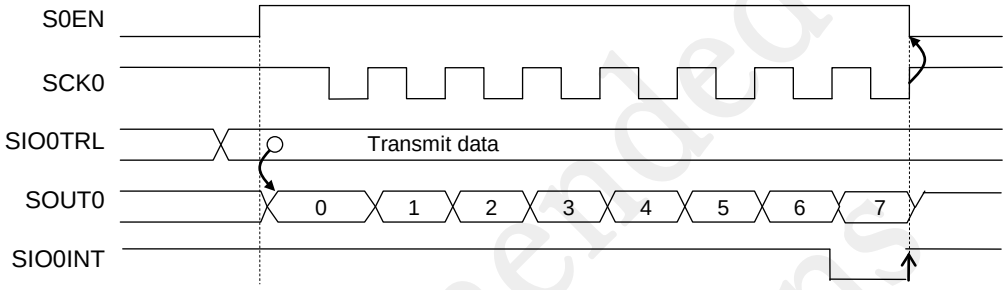


Figure 11-5 Transmit Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8-bit Length, LSB first, Negative Logic)

11.3.2 Receive Operation

When "0" is written to the S0MD1 bit and "1" is written to the S0MD0 bit of the serial mode register (SIO0MOD), this LSI is set to a receive mode.
When the S0EN bit of the serial port control register (SIO0CON) is set to "1", reception starts. When reception of 8/16-bit data terminates, a synchronous serial port interrupt (SIO0INT) occurs and the S0EN bit is set to "0".
Receive data is input from the SIN0 pin.
When an internal clock is selected in the serial port mode register (SIO0MD), the LSI is set to a master mode and when an external clock (SCK0) is selected, the LSI is set to a slave mode.
The serial port mode register (SIO0MOD) enables selection of MSB first or LSB first.
The receive data input pin (SIN0) and transfer clock input/output pin (SCK0) must be set to the tertiary function.
Figures 11-6,11-7,11-8 and 11-9 show the receive operation waveforms of the synchronous serial ports for "clock type 0 and positive-logic", "clock type 0 and negative-logic", "clock type 1 and positive-logic" and "clock type 1 and negative-logic", respectively (8-bit length, MSB first).

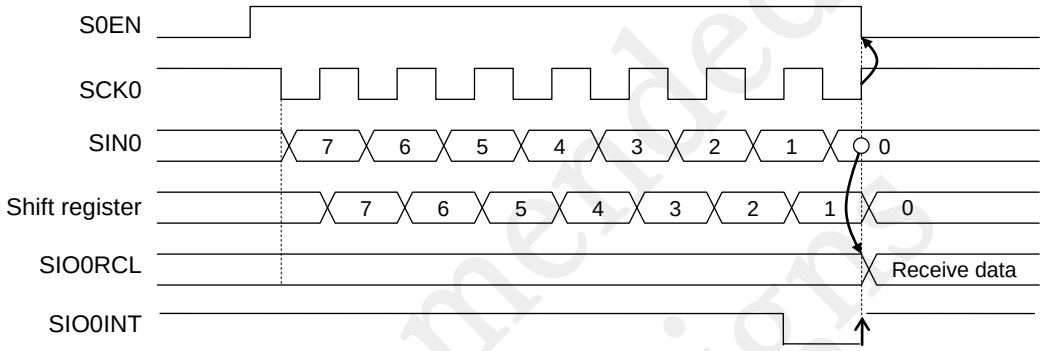


Figure 11-6 Receive Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8-bit Length, MSB first, Positive Logic)

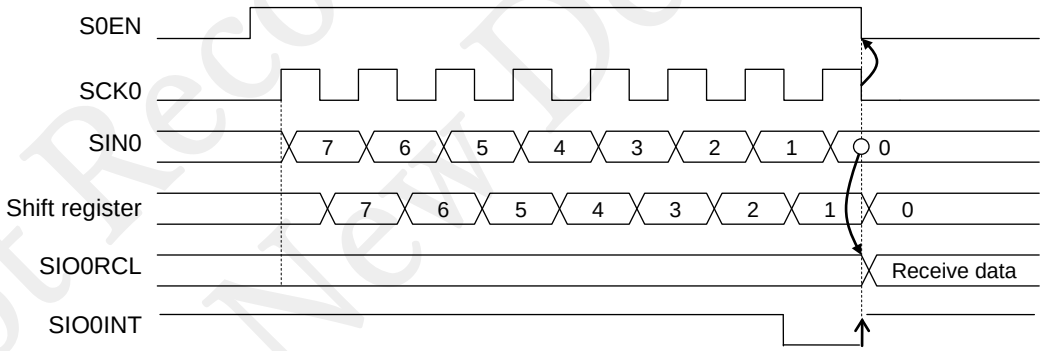


Figure 11-7 Receive Operation Waveforms of Synchronous Serial Port for Clock Type 0 (8-bit Length, MSB first, Negative Logic)

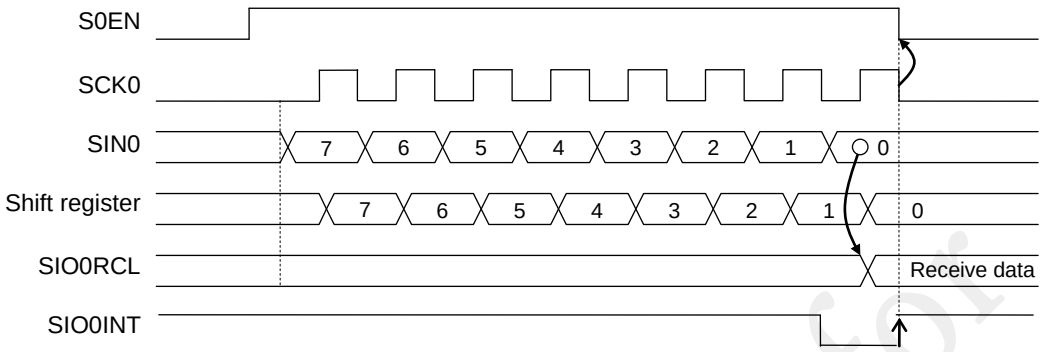


Figure 11-8 Receive Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8-bit Length, MSB first, Positive Logic)

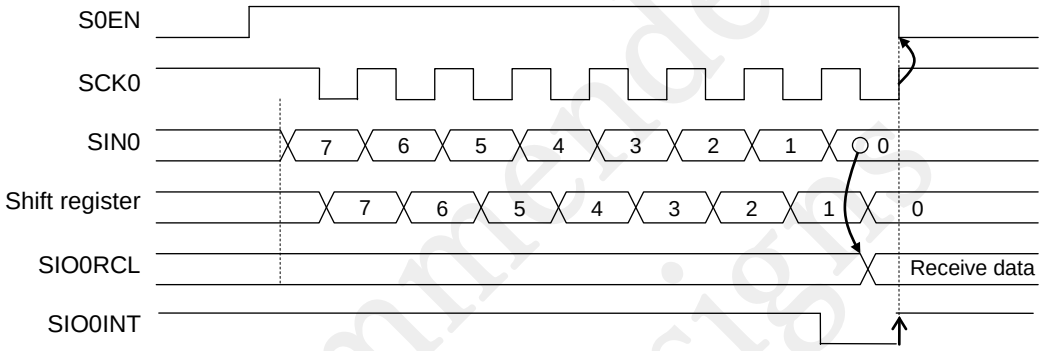


Figure 11-9 Receive Operation Waveforms of Synchronous Serial Port for Clock Type 1 (8-bit Length, MSB first, Negative Logic)

[Note]
When the SOUT0 pin is set to the tertiary function output in receive mode, a “H” level is output from the SOUT0 output pin.

11.3.3 Transmit/Receive Operation

When "1" is written to the S0MD1 bit and "1" is written to the S0MD0 bit of the serial mode register (SIO0MOD), this LSI is set to a transmit/receive mode.
When the S0EN bit of the serial port control register (SIO0CON) is set to "1", transmission/reception starts. When transmission/reception of 8/16-bit data terminates, a synchronous serial port interrupt (SIO0INT) occurs and the S0EN bit is set to "0".
Receive data is input from the SIN0 pin, and transmit data is output from the SOUT0 pin.
When an internal clock is selected in the serial port mode register (SIO0MD), the LSI is set to a master mode and when an external clock (SCK0) is selected, the LSI is set to a slave mode.
The serial port mode register (SIO0MOD) enables selection of MSB first or LSB first.
The receive data input pin (SIN0), the transmit data output pin (SOUT0), and transfer clock input/output pin (SCK0) must be set to the tertiary function.
Figure 11-10 shows the transmit/receive operation waveforms of the synchronous serial port (16-bit length, LSB first, clock types 0 and positive-logic).

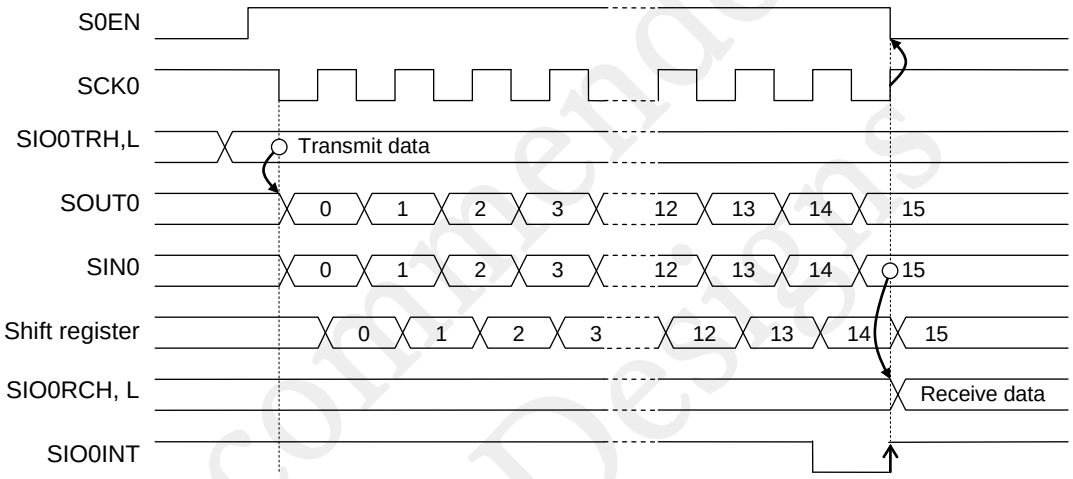


Figure 11-10 Transmit/Receive Operation Waveforms of Synchronous Serial Port (16-bit Length, LSB first, Clock Type 0 and positive-logic)

11.3.4 Pin Settings

To enable the SSIO function, the applicable bit of each related port register needs to be set. See Chapter 17, "Port 0", Chapter 20, "Port 3", Chapter 21, "Port 4", and Chapter 22, "Port 5" for details about the port registers.
For SIN0, SCK0 and SOUT0, the ports can be selected from several possibilities.
Be sure to select one of the following combinations of ports for SIN0/SCK0/SOUT0.

	SSIO pin	Combination 1	Combination 2	Combination 3	Combination 4
SSIO	SIN0,SCK0, SOUT0	P01,P02, P00	P31,P32, P30	P41,P42, P40	P51,P52, P50

Note that only one port can be selected as port.
If using P02 as SCK0 in master mode, SCK0 Max clock output frequency is 2MHz.

Chapter 12

Synchronous Serial Port with FIFO (SSIOF)

12 Synchronous Serial Port with FIFO (SSIOF)

12.1 General Description

The synchronous serial port with FIFO (SSIOF) can communicate with peripherals and other MCUs.
The use of SSIOF requires the function setting of the ports 2, 3, 4 and 5. For the port function setting, see Chapter 19 "Port 2", Chapter 20 "Port 3", Chapter 21 "Port 4", and Chapter 22 "Port 5".

12.1.1 Features

- Full-duplex data transfer
- Master or Slave mode can be selected
- Built-in 4-stage FIFO on each of transmit- and receive-sides
- For the transfer size, 8 bits (byte) or 16 bits (word) can be selected
- The number of received bytes (words) that cause interrupts can be set to 1 to 4.
- The number of untransmitted bytes (words) that cause interrupts can be set to 0 to 3.
- Either LSB first or MSB first can be selected
- The polarity and phase of the serial clock are selectable
- In Master mode, the OSCLK's 2 to 2046-division clocks can be selected as the sync clock (1023 types)
- In Master mode, the interval before/after transfer can be controlled
- State bit indicating transmission/receive complete and FIFO state
- Detects a mode fault error to avoid multi-master bus contention
- Detects a write overflow error if any further writing is attempted when the transmit FIFO is in the full state
- Generates an interrupt when the transmit/receive FIFO is in a specific state or when a cause such as mode fault error occurs

12.1.2 Configuration

Figure 12-1 shows the configuration of the SSIOF.

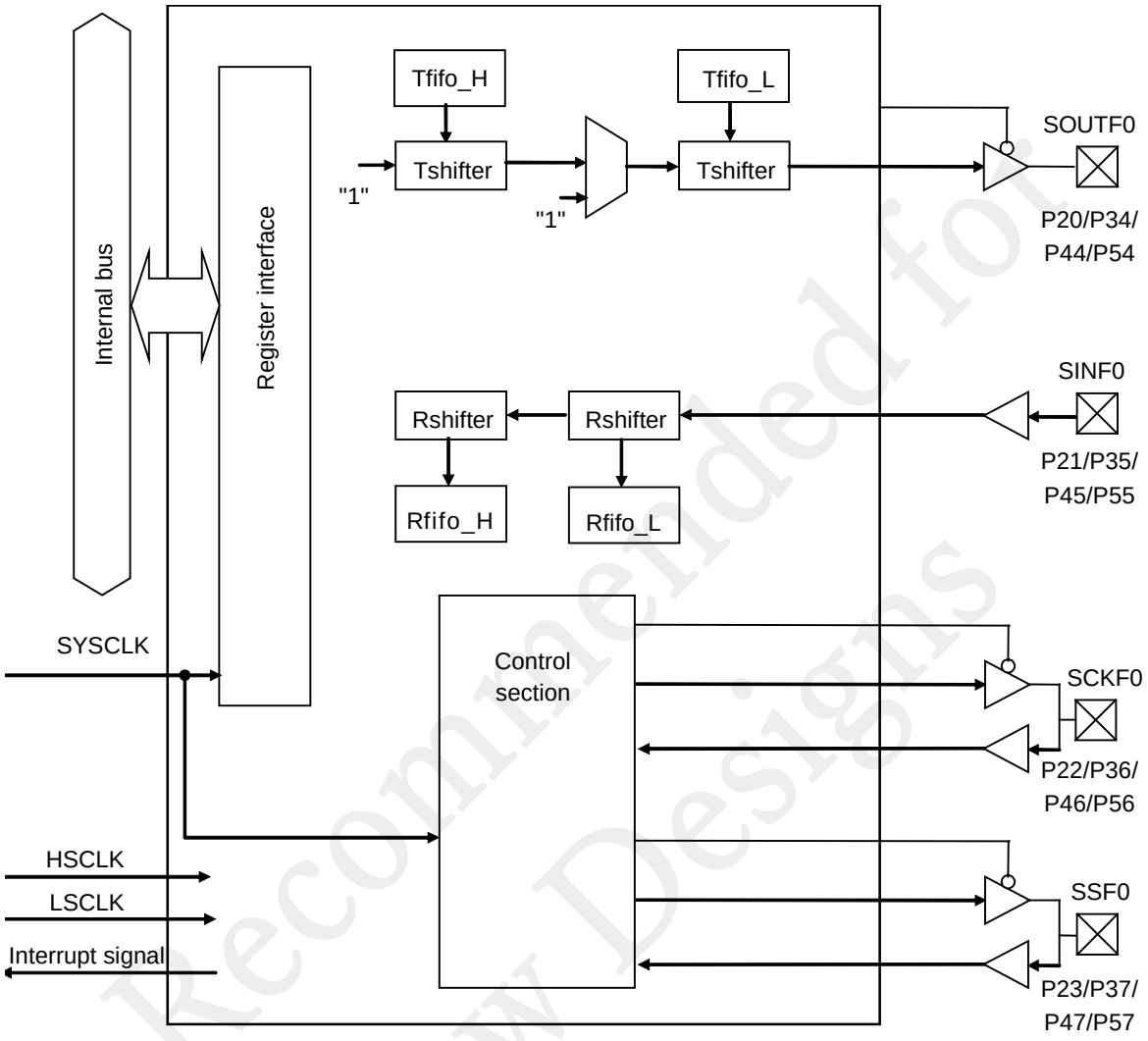


Figure 12-1 Configuration of SSIOF

12.1.3 List of Pins

Pin Name	I/O	Function
SOUTF0	O	Master serial output/slave serial output signal
SINF0	I	Master serial input/slave serial input signal
SCKF0	I/O	Baud rate clock
SSF0	I/O	Slave selection signal

12.2 Description of Registers

12.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F780	SIOF0 control register	SF0CTRLL	SF0CTRL	R/W	8/16	00
0F781		SF0CTRLH		R/W	8	00
0F782	SIOF0 interrupt control register	SF0INTCL	SF0INTC	R/W	8/16	00
0F783		SF0INTCH		R/W	8	00
0F784	SIOF0 transfer interval control register	-	SF0TRAC	R/W	16	0002
0F786	SIOF0 baud rate register	-	SF0BRR	R/W	16	5002
0F788	SIOF0 status register	SF0SRRL	SF0SRR	R	8/16	00
0F789		SF0SRRH		R	8	14
0F78A	SIOF0 status clear register	SF0SRCL	SF0SRC	W	8/16	00
0F78B		SF0SRCH		W	8	00
0F78C	SIOF0 FIFO status register	SF0FSRL	SF0FSR	R	8/16	00
0F78D		SF0FSRH		R	8	00
0F78E	SIOF0 write data register	SF0DWRL	SF0DWR	R/W	8/16	00
0F78F		SF0DWRH		R/W	8	00
0F790	SIOF0 read data register	SF0DRRL	SF0DRR	R	8/16	00
0F791		SF0DRRH		R	8	00

12.2.2 SIOF0 Control Register (SF0CTRL)

Address: 0F780H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
SF0CTRLL	–	SF0CPOL	SF0CPHA	SF0LSB	SF0MDFE	SF0SIZ	SF0MST	SF0SPE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
SF0CTRLH	–	–	–	–	SF0MOZ	SF0SOZ	SF0SSZ	SF0FICL
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SF0CTRL is a special function register (SFR) used to control the operation of the SSIOF.

Description of Bits

- **SF0SPE** (bit 0)
  SF0SPE sets whether or not to enable the transfer of the SSIOF.

SF0SPE	Description
0	Disable SSIOF transfer (initial value)
1	Enable SSIOF transfer

- **SF0MST** (bit 1)
  SF0MST sets the master/slave selection.

SF0MST	Description
0	Slave (initial value)
1	Master

- **SF0SIZ** (bit 2)
  SF0SIZ sets the transfer size.

SF0SIZ	Description
0	8 bits (initial value)
1	16 bits

- **SF0MDF** (bit 3)
  SF0MDF sets the mode fault control signal.
  The mode fault can be executed when MSTR = 1, MODFEN = 1, and not transferring.

SF0MDF	Description
0	The mode fault is not executed. (Initial value)
1	The mode fault is executed when not transferring.

- **SF0LSB** (bit 4)
  SF0LSB sets the data transfer order.

SF0LSB	Description
0	LSB first (initial value)
1	MSB first

- **SF0CPHA** (bit 5)
  SF0CPHA sets the serial clock phase.

SF0CPHA	Description
0	The data is sampled at the first edge and shifted at the second edge (initial value)
1	The data is shifted at the first edge and sampled at the second edge

- **SF0CPOL** (bit 6)
  SF0CPOL sets the serial clock polarity.

SF0CPOL	Description
0	Serial clock default is "0" ("0" during transmission/reception)(initial value)
1	Serial clock default is "1" ("1" during transmission/reception)

- **SF0FICL** (bit 8)
  SF0FICL sets the FIFO clearance. After clearance, set this to "0".

SF0FICL	Description
0	None (initial value)
1	Clear the receive/transmit byte (word) count

- **SF0SSZ** (bit 9)
  SF0SSZ sets the SSF0 output control.

SF0SSZ	Description
0	0/1 output (initial value)
1	Hi-Z

- **SF0SOZ** (bit 10)
  SF0SOZ sets the SOUTF0 output control when SSF0 = 1.

SF0SOZ	Description
0	0/1 output (initial value)
1	Hi-Z

- **SF0MOZ** (bit 11)
  SF0MOZ sets the SOUTF0, SCKF0 output control.

SF0MOZ	Description
0	0/1 output (initial value)
1	Hi-Z

12.2.3 SIOF0 Interrupt Control Register (SF0INTC)

Address: 0F782H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
SF0INTCL	–	–	–	SF0MFIE	SF0ORIE	SF0FIE	SF0RFIE	SF0TFIE
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
SF0INTCH	–	–	SF0RFIC1	SF0RFIC0	–	–	SF0TFIC1	SF0TFIC0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SF0INTC is a special function register (SFR) used to control the interrupt operation of the SSIOF.

Description of Bits

- **SF0TFIE** (bit 0)
  SF0TFIE sets whether or not to enable the transmission interrupt of the SSIOF.

SF0TFIE	Description
0	Interrupt disabled (initial value)
1	Interrupt enabled

- **SF0RFIE** (bit 1)
  SF0RFIE sets whether or not to enable the reception interrupt of the SSIOF.

SF0RFIE	Description
0	Interrupt disabled (initial value)
1	Interrupt enabled

- **SF0FIE** (bit 2)
  SF0FIE sets whether or not to enable the transfer end interrupt.

SF0FIE	Description
0	Interrupt disabled (initial value)
1	Interrupt enabled

- **SF0ORIE** (bit 3)
  SF0ORIE sets whether or not to enable the overrun error interrupt.

SF0ORIE	Description
0	Interrupt disabled (initial value)
1	Interrupt enabled

- **SF0MFIE** (bit 4)
  SF0MFIE sets whether or not to enable the SSIOF mode fault interrupt.

SF0MFIE	Description
0	Interrupt disabled (initial value)
1	Interrupt enabled

- **SF0TFIC1-0** (bits 9 to 8)
  SF0TFIC1-0 set the remaining byte count interrupt control for the transmit FIFO.

SF0TFIC1	SF0TFIC0	Description
0	0	An interrupt occurs when the number of remaining byte to transmit becomes 0 bytes (0 words) (initial value)
0	1	An interrupt occurs when the number of remaining byte to transmit becomes 1 byte (1 word)
1	0	An interrupt occurs when the number of remaining byte to transmit becomes 2 bytes (2 words)
1	1	An interrupt occurs when the number of remaining bytes to transmit becomes 3 bytes (3 words)

- **SF0RFIC1-0** (bits13 to 12)
  SF0RFIC1-0 set the receive FIFO interrupt control.

SF0RFIC1	SF0RFIC0	Description
0	0	An interrupt occurs when 1 byte (1 word) has been received (initial value)
0	1	An interrupt occurs when 2 bytes (2 words) have been received
1	0	An interrupt occurs when 3 bytes (3 words) have been received
1	1	An interrupt occurs when 4 bytes (4 words) have been received

12.2.4 SIOF0 Transfer Interval Control Register (SF0TRAC)

Address: 0F784H
Access: R/W
Access size: 16 bits
Initial value: 0002H

	7	6	5	4	3	2	1	0
-	SF0DTL7	SF0DTL6	SF0DTL5	SF0DTL4	SF0DTL3	SF0DTL2	SF0DTL1	SF0DTL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	1	0

	15	14	13	12	11	10	9	8
-	–	–	–	–	–	–	–	SF0DTL8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SF0TRAC is a special function register (SFR) used to set the minimum data transfer interval in Master mode. For details, see 12.3.7, "Transfer Interval Setting".

12.2.5 SIOF0 Baud Rate Register (SF0BRR)

Address: 0F786H
Access: R/W
Access size: 16 bits
Initial value: 5002H

	7	6	5	4	3	2	1	0
-	SF0BR7	SF0BR6	SF0BR5	SF0BR4	SF0BR3	SF0BR2	SF0BR1	SF0BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	1	0

	15	14	13	12	11	10	9	8
-	SF0LAG1	SF0LAG0	SF0LEAD1	SF0LEAD0	–	–	SF0BR9	SF0BR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	1	0	1	0	0	0	0

SF0BRR is a special function register (SFR) used to set the operation mode.
Do not change the setting of this register during transfer. Operation is not guaranteed if it is changed during transfer.

Description of Bits

- **SF0BR9-0** (bits 9 to 0)
  Sets the baud rate (f_{SCK})(setting enabled in Master mode).
  $f_{SCK}=f_{HLSCLK}/(2\times SF0BR9\text{-}0)$
  f_{HLSCLK}: HSCLK or LSCLK frequency

SF0BR[9:0]										Description
9	8	7	6	5	4	3	2	1	0	
0	0	0	0	0	0	0	0	0	0	2 dividing
0	0	0	0	0	0	0	0	0	1	2 dividing
0	0	0	0	0	0	0	0	1	0	4 dividing (initial value)
0	0	0	0	0	0	0	0	1	1	6 dividing
:										:
1	1	1	1	1	1	1	1	1	1	2046 dividing

[Note]
The maximum SSIOF transfer frequency is 4MHz. This setting should not exceed 4MHz.
If using P22 as SCKF0 in master mode, the max frequency is 2MHz.

- **SF0LEAD1-0** (bits 13 to 12)
  SF0LEAD1-0 set the SSF0 –SCKF0 delay interval (setting enabled only in Master mode).

SF0LEAD1	SF0LEAD0	Description
0	0	0.5 X SCK
0	1	0.5 X SCK (initial value)
1	0	1.0 X SCK
1	1	1.5 X SCK

- **SF0LAG1-0** (bits 15 to 14)
  SF0LAG1-0 set the SCKF0-SSF0(H) delay interval (setting enabled only in Master mode).

SF0LAG1	SF0LAG0	Description
0	0	0.5 X SCK
0	1	0.5 X SCK (initial value)
1	0	1.0 X SCK
1	1	1.5 X SCK

12.2.6 SIOF0 Status Register (SF0SRR)

Address: 0F788H
Access: R
Access size: 8/16 bits
Initial value: 1400H

	7	6	5	4	3	2	1	0
SF0SRRL	–	–	SF0SPIF	SF0MDF	SF0ORF	SF0FI	SF0RFI	SF0TFI
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
SF0SRRH	–	–	–	SF0RFE	SF0RFF	SF0TFE	SF0TFF	SF0WOF
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	1	0	1	0	0

SF0SRR is a special function register (SFR) used to indicate the data transfer state and error state of the SSIOF.

Description of Bits

- **SF0TFI** (bit 0)
  SF0TFI indicates a transmission interrupt.
  A transmission interrupt occurs if the remaining data in the transmit FIFO matches the byte count selected with SF0TFIC.

SF0TFI	Description
0	No interrupt request (initial value)
1	Interrupt request

- **SF0RFI** (bit 1)
  SF0RFI indicates a reception interrupt.
  If the number of data received in the receive FIFO is equal or more byte count selected with SF0RFIC , reception interrupt occur.

SF0RFI	Description
0	No interrupt request (initial value)
1	Interrupt request

- **SF0FI** (bit 2)
  SF0FI indicates a transfer end interrupt. (the transmit FIFO is empty and the transfer of the last one byte (one word) is finished)

SF0FI	Description
0	No interrupt request (initial value)
1	Interrupt request

- **SF0ORF** (bit 3)
  SF0ORF indicates the overrun error flag.

SF0ORF	Description
0	Normal (initial value)
1	An overrun error occurred (an interrupt is generated)

- **SF0MDF** (bit 4)
  SF0MDF indicates a mode fault.

SF0MDF	Description
0	Normal (initial value)
1	A mode fault occurs (an interrupt occurs)

- **SF0SPIF** (bit 5)
  SF0SPIF indicates the SSIOF one byte (word) transfer end.

SF0SPIF	Description
0	No end of transfer (initial value)
1	End of transfer

- **SF0WOF** (bit 8)
  SF0WOF indicates a write overflow.

SF0WOF	Description
0	Normal (initial value)
1	A write overflow occurred (No interrupt is generated)

- **SF0TFF** (bit 9)
  SF0TFF indicates the transmit FIFO Full.

SF0TFF	Description
0	Not Full (initial value)
1	Full (No interrupt is generated)

- **SF0TFE** (bit 10)
  SF0TFE indicates the transmit FIFO Empty.

SF0TFE	Description
0	Not Empty
1	Empty (No interrupt is generated) (initial value)

- **SF0RFF** (bit 11)
  SF0RFF indicates the receive FIFO Full.

SF0RFF	Description
0	Not Full (initial value)
1	Full (No interrupt is generated)

- **SF0RFE** (bit 12)
  SF0RFE indicates the receive FIFO Empty.

SF0RFE	Description
0	Not Empty
1	Empty (No interrupt is generated) (initial value)

12.2.7 SIOF0 Status Clear Register (SF0SRC)

Address: 0F78AH
Access: W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
SF0SRCL	–	–	SF0SPIFC	SF0MDFC	SF0ORFC	SF0FC	SF0RFC	SF0TFC
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
SF0SRCH	SF0IRQ	–	–	–	–	–	–	SF0WOFC
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

SF0SRC is a special function register (SFR) used to clear the data transfer state and error state of the SSIOF.

Description of Bits

- **SF0TFC** (bit 0)
  SF0TFC clears the interrupt request of the transmission interrupt. The interrupt request is cleared by writing "1". For the interrupt request, check on the SF0TFI bit of SF0SRR.

- **SF0RFC** (bit 1)
  SF0RFC clears the interrupt request of the receiving interrupt. The interrupt request is cleared by writing "1". For the interrupt request, check on the SF0RFI bit of SF0SRR.

- **SF0FC** (bit 2)
  SF0FC clears the interrupt request of the transfer end interrupt. The interrupt request is cleared by writing "1". For the interrupt request, check on the SF0FI bit of SF0SRR.

- **SF0ORFC** (bit 3)
  SF0ORFC clears the interrupt request of the overrun error flag. The interrupt request is cleared by writing "1". For the interrupt request, check on the SF0ORF bit of SF0SRR.

- **SF0MDFC** (bit 4)
  SF0MDFC clears the interrupt request of the mode fault. The interrupt request is cleared by writing "1". For the interrupt request, check on the SF0MDF bit of SF0SRR.

- **SF0SPIFC** (bit 5)
  SF0SPIFC clears the SSIOF1 byte (word) transfer end. The transfer end flag (SF0SPIF) is cleared by writing "1".

- **SF0WOFC** (bit 8)
  SF0WOFC clears a write overflow. The write overflow flag (SF0WOF) is cleared by writing "1".

- **SF0IRQ** (bit 15)
  When there is any unprocessed interrupt source, the interrupt request is issued again by writing "1".

[Note]
Write "1" to SF0IRQ bit while there is any unprocessed interrupt source and processing all the interrupt sources before exiting the interrupt vector will cause re-entry to the interrupt vector with no interrupt source after exiting the interrupt vector. Ensure to write "1" before exiting the interrupt vector.

12.2.8 SIOF0 FIFO Status Register (SF0FSR)

Address: 0F78CH
Access: R
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
SF0FSRL	-	-	-	-	-	SF0TFD2	SF0TFD1	SF0TFD0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
SF0FSRH	-	-	-	-	-	SF0RFD2	SF0RFD1	SF0RFD0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SF0FSR is a special function register (SFR) used to indicate the count transmitted and received by FIFO.

Description of Bits

- **SF0TFD2-0** (bits 2 to 0)
  SF0TFD2-0 indicate the untransmitted byte (word) count of the transmit FIFO.

SF0TFD2	SF0TFD1	SF0TFD0	Description
0	0	0	Empty (initial value)
0	0	1	1Byte/1Word
0	1	0	2Byte/2Word
0	1	1	3Byte/3Word
1	0	0	4Byte/4Word (Full)

- **SF0RFD2-0** (bits 10 to 8)
  SF0RFD2-0 indicate the byte (word) count received in the receive FIFO.

SF0RFD2	SF0RFD1	SF0RFD0	Description
0	0	0	Empty (initial value)
0	0	1	1Byte/1Word
0	1	0	2Byte/2Word
0	1	1	3Byte/3Word
1	0	0	4Byte/4Word (Full)

12.2.9 SIOF0 Write Data Register (SF0DWR)

Address: 0F78EH
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
SF0DWRL	SF0WD7	SF0WD6	SF0WD5	SF0WD4	SF0WD3	SF0WD2	SF0WD1	SF0WD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
SF0DWRH	SF0WD15	SF0WD14	SF0WD13	SF0WD12	SF0WD11	SF0WD10	SF0WD9	SF0WD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SF0DWR is an 8-bit (byte) or 16-bit (word) special function register (SFR) used to hold transmitted data.
Write access to this register should be:
8-bit write access to SF0DWRL for 8-bit transmission (SF0SIZ=0)
16-bit write access to SF0DWR for 16-bit transmission (SF0SIZ=1)
Operation is not guaranteed for other accesses.

12.2.10 SIOF0 Read Data Register (SF0DRR)

Address: 0F790H
Access: R
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
SF0DRRL	SF0RD7	SF0RD6	SF0RD5	SF0RD4	SF0RD3	SF0RD2	SF0RD1	SF0RD0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
SF0DRRH	SF0RD15	SF0RD14	SF0RD13	SF0RD12	SF0RD11	SF0RD10	SF0RD9	SF0RD8
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

SF0DRR is an 8-bit (byte) or 16-bit (word) special function register (SFR) used to hold received data.
Read access to this register should be:
8-bit read access to SF0DRRL for 8-bit reception (SF0SIZ=0)
16-bit read access to SF0DRR for 16-bit reception (SF0SIZ=1)
Other accesses are not guaranteed.

12.3 Description of Operation

12.3.1 Master Mode and Slave Mode

Master mode and Slave mode are provided as the transmit/receive mode. This is selected by the SF0MST bit of the SIOF0 control register.
SF0BR (baud rate), SF0LEAD (SSF0-SCKF0 delay interval), and SF0LAG (SCKF0-SSF0 delay interval) of the SIOF0 baud rate register and SF0DTL (minimum data transfer interval) of the SIOF0 transfer interval control register determine SCKF0 and SSF0 operations and are only valid during the master operation.
Each of SF0CPOL, SF0CPHA, SF0LSB, and SF0SIZ needs to have the same value for master and slave.

12.3.2 Control of Polarity and Phase of Serial Clock

SF0CPOL of the SIOF0 control register controls the clock polarity. SF0CPHA controls the clock phase and determines the shift timing of transmit data and the sampling timing of received data. The master and slave which communicate with each other must have the same setting values for SF0CPOL and SF0CPHA.

12.3.3 Data Transfer Timing When SF0CPHA Is "0"

Figure 12-2 shows the data transfer timing when SF0CPHA is "0". For the SCKF0, two cases are shown (SF0CPOL is "0" and "1"). SSF0 is the slave selection input in Slave mode.
In Master mode, the transfer is started when data is written to the SF0DWR register. In Slave mode, the transfer is started at the SSF0 falling edge. The received data is sampled at the rising-edge of SCKF0 in SF0CPOL is “0” and the falling-edge of SCKF0 in SF0CPOL is “1”. The transmitted data is shifted at the falling-edge of SCKF0 in SF0CPOL is “0” and the rising-edge of SCKF0 in SF0CPOL is “1”.

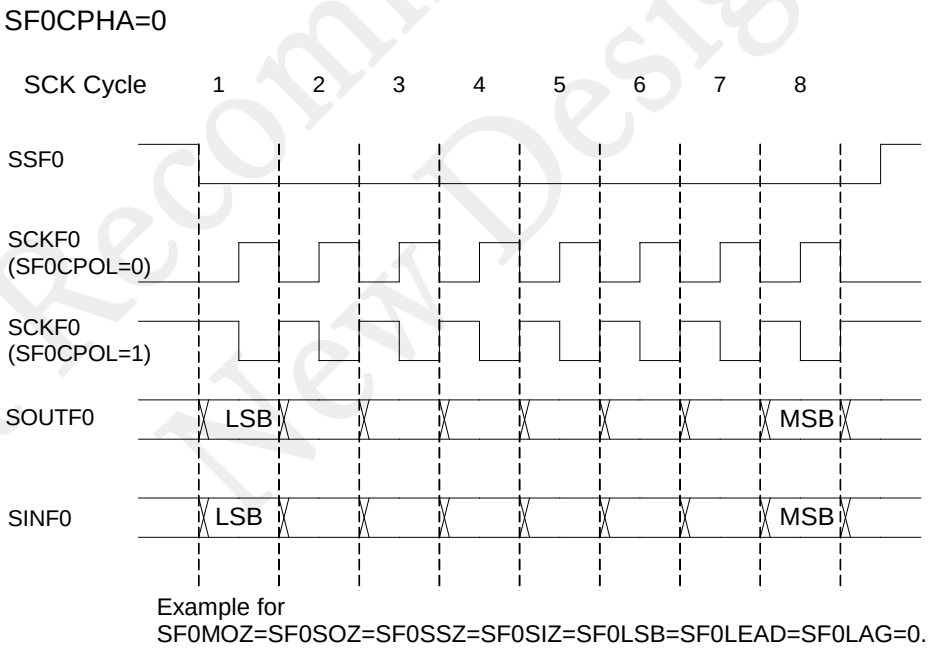


Figure 12-2 Clock Waveform When SF0CPHA = 0

12.3.4 Data Transfer Timing When SF0CPHA Is "1"

Figure 12-3 shows the data transfer timing when SF0CPHA is "1". For the SCKF0, two cases are shown (SF0CPOL is "0" and "1").
SSF0 is the slave selection input in Slave mode.
In Master mode, the transfer is started when data is written to SF0DWR. In Slave mode, the transfer is started at the first edge of SCKF0. The received data is sampled at the falling-edge of SCKF0 in SF0CPOL is “0” and the rising-edge of SCKF0 in SF0CPOL is “1”. The transmitted data is shifted at the rising-edge of SCKF0 in SF0CPOL is “0” and the falling-edge of SCKF0 in SF0CPOL is “1”.

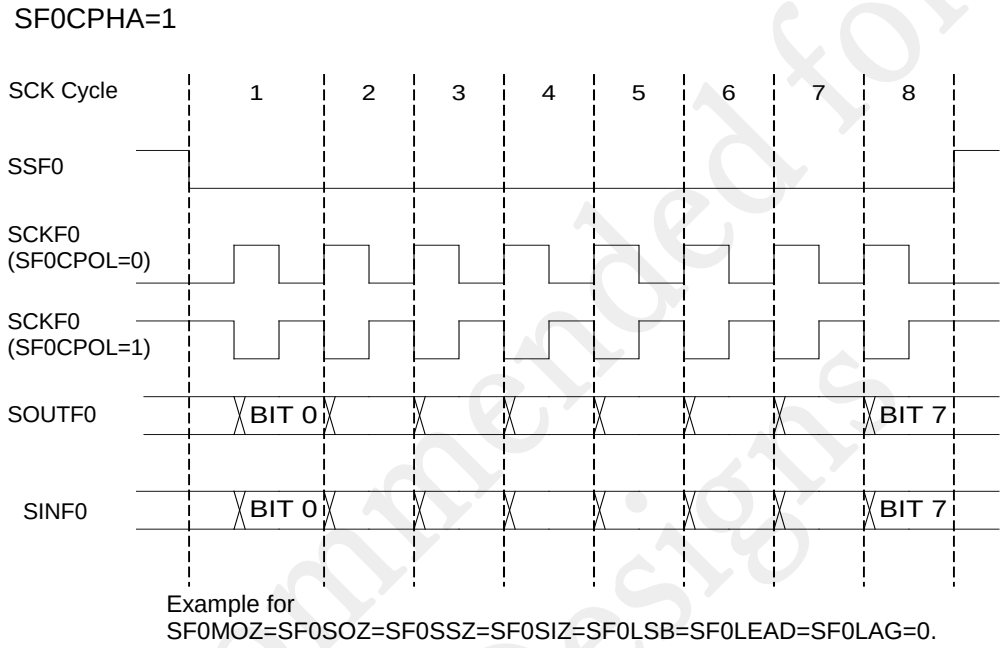


Figure 12-3 Clock Waveform When CPHA = 1

12.3.5 Serial Clock Baud Rate

The baud rate is selected by the SF0BR9-0 bit of SF0BRR. This is only valid in Master mode. The baud-rate clock SCKF0 is generated by dividing HSCLK or LSCLK.
The baud rate (f_{SCK}) is calculated as follows.

$f_{SCK}=f_{HLSCLK}/(2\times SF0BR9\text{-}0)$

f_{SCK} : Frequency of baud-rate clock
f_{HLSCLK} : Frequency of HSCLK or LSCLK
SF0BR : Value set in SF0BR9-0 of the SF0BRR register (1 to 1023)
If 0 is set the SF0BR register, it is processed as 1.

For SF0BR, it can be selected from 1023 dividing types (2 to 2046).

12.3.6 Transfer Size

The transfer size can be selected in 8 bits (byte) or 16 bits (word).
Transfer data read/write must be adjusted to the transfer size. As the number of FIFO stages is the same for both byte and word, the number of transfers is the same.
The master and slaves which communicate with each other must have the same value for SF0SIZ.

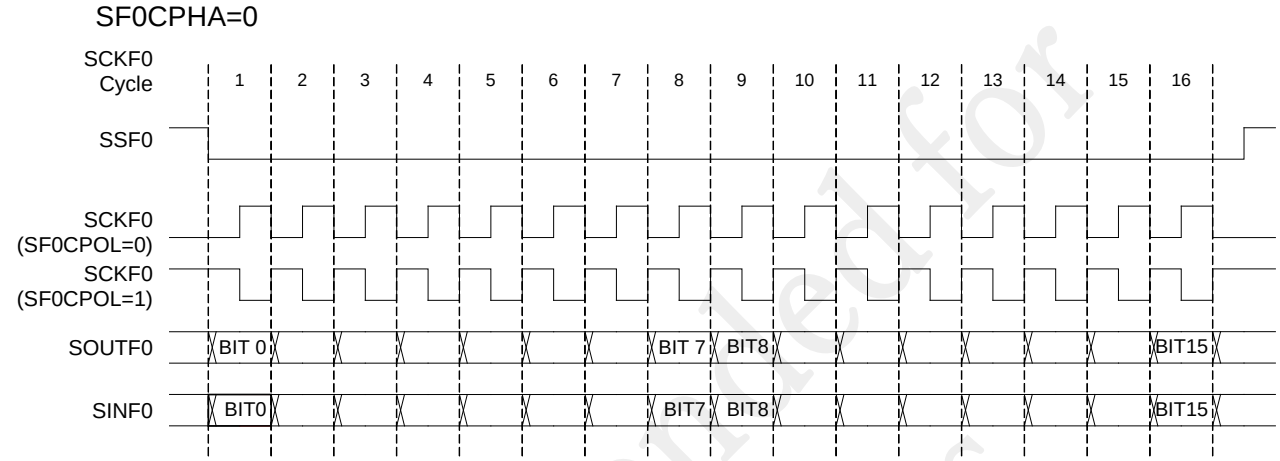


Figure 12-4 SSIOF Bus Waveform When Transfer Size Size SF0SIZ = 1 (16-Bit) and SF0CPHA = 0

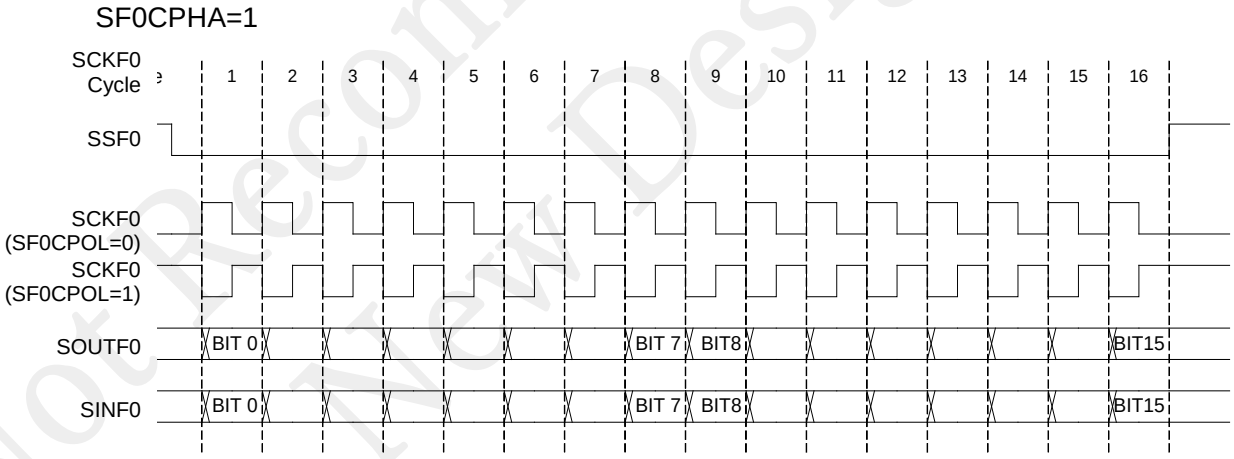


Figure 12-5 SSIOF Bus Waveform When Transfer Size SF0SIZ = 1 (16-Bit) and SF0CPHA = 1

12.3.7 Transfer Interval Setting

LEAD (SSF0-SCKF0 time), LAG (SCKF0-SSF0(H) time), and TDTL (SSF0(H)-SSF0(H)) can be set to adjust the speed to the slave. This setting is only valid in Master mode. It is ignored in Slave mode.
Setting during transferring is invalid.

(1) LEAD
A value from 0.5 to 1.5SCKF0 can be set.
(2) LAG
A value from 0.5 to 1.5SCKF0 can be set.
(3) TDTL
The minimum transfer interval can be controlled in SCKF0 clocks by setting SF0TRAC's SF0DTL.
If there is any transfer data in FIFO, the time set by this setting (SSF0) changes to H during byte/word transfer.
If there is no transfer data in FIFO, this is H until any transmitted data is written.
If SF0DTL is set to 0, the interval after transfer (TDTL) disappears and a continuous transfer is performed. SSF0 is held to L and returns to H after the transfer is finished.

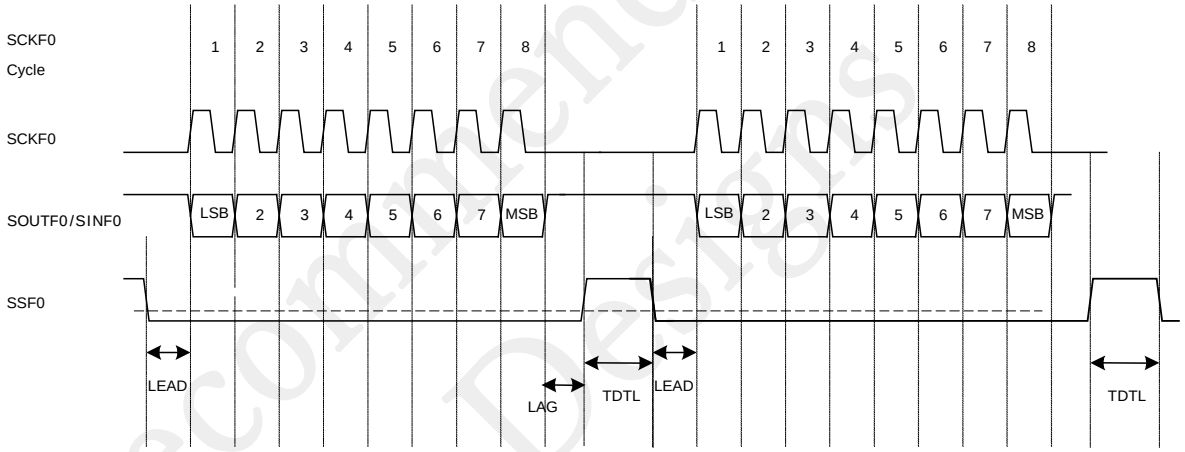


Figure 12-6 Transfer Interval (When SF0DTL Is Not "0")

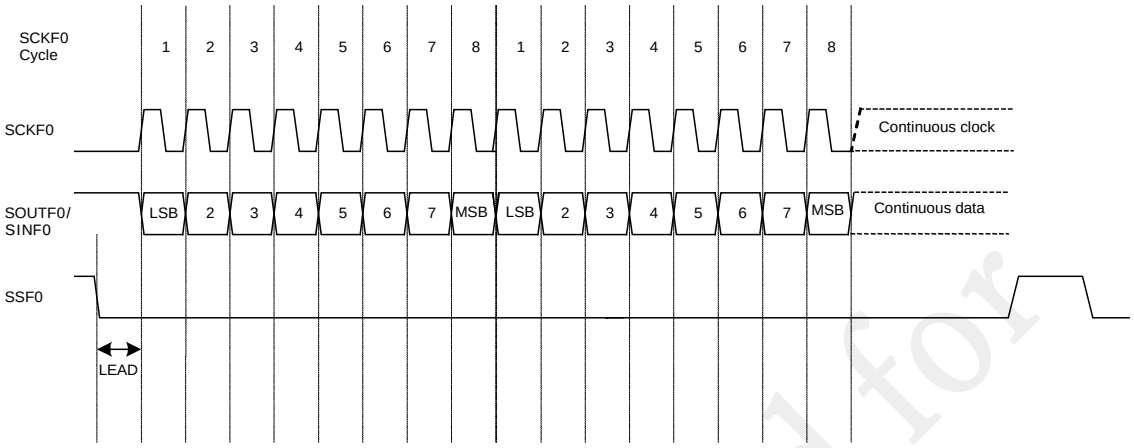


Figure 12-7 Transfer Interval (When SF0DTL Is "0")

12.3.8 Transmit Operation (Master Mode)

① Write the necessary values to SF0CTRL, SF0INTC, SF0BRR, and SF0TRAC, set the SF0MST bit to Master mode, and set the SF0SPE bit to enable the SSIOF transfer.
② When the transmitted data is written to SF0DWR, the transmit FIFO Empty flag changes to 0 (SF0TFE = 0). SSIOF starts the automatic transmission and outputs the transmitted data from LSB or MSB on the SOUTF0 pin according to the SF0LSB setting.
③ The sync clock, which was set by the SF0CPOL, SF0CPHA, and SF0BRR registers, is output from the SCKF0 pin.
④ Transmitted data can be written to SF0DWR successively. However, if further writing is performed when the transmit FIFO is in Full status (SF0TFF = 1), a write overflow occurs. (SF0WOF = 1, No interrupt is generated.)
⑤ The SF0SPIF bit is set each time the transfer of 1 byte is completed. (SF0SPIF=1)
⑥ A transmission interrupt occurs if the remaining data in the transmit FIFO matches the byte count selected with SF0TFIC. (SF0TFI=1)
⑦ If the transmit FIFO becomes empty and the transfer of the last byte is completed, a transfer completion interrupt is generated. (SF0FI=1)

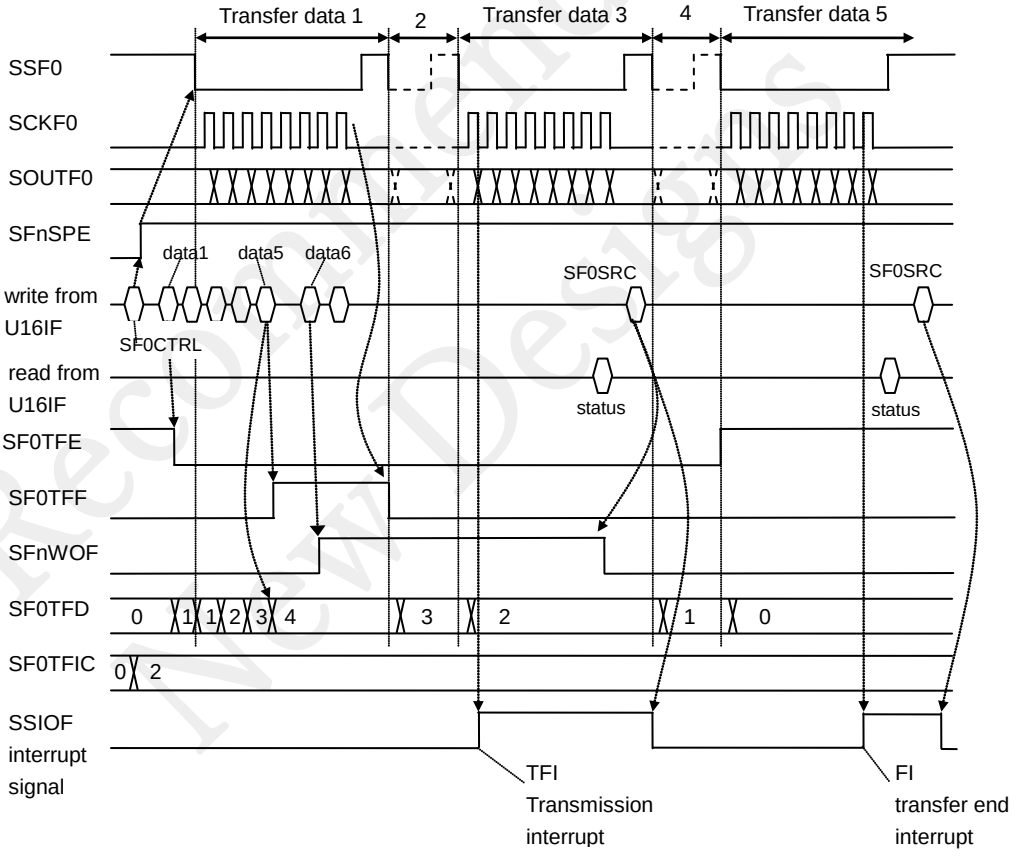


Figure 12-8 Master Mode (Transmit Operation)

12.3.9 Receive Operation (Master Mode)

The master mode of the synchronous serial with FIFO starts by setting data in a transmission buffer.
Data needs to be set into a transmission buffer even master mode reception only.

① Write the necessary values to SF0CTRL, SF0INTC, SF0BRR, and SF0TRAC, set the SF0MST bit to Master mode, and set the SF0SPE bit to enable the SSIOF transfer.
② When the data is written to SF0DWR, the SSIOF transfer is started.
③ The sync clock, which was set by the SF0CPOL, SF0CPHA, and SF0BRR0-1 registers, is output from the SCKF0 pin.
④ On the SINF0 pin, the received data is sampled from LSB or MSB according to the SF0LSB setting and stored in the receive FIFO. The receive FIFO Empty flag changes to 0 (RFE = 0).
⑤ The SF0SPIF bit is set each time the transfer of 1 byte is completed. (SF0SPIF=1)
⑥ If the number of data received in the receive FIFO is equal to or more than matches following the byte count selected with SF0RFIC of SF0CR, SF0RFI of SF0SRR is set to generate a reception interrupt.
⑦ When the receive FIFO becomes Full, the subsequent reception is disabled. If the reception is performed in this state, an overrun error interrupt is generated. (SF0ORF=1)
⑧ If the temporary data of transmit FIFO becomes empty and the transfer of the last byte is completed, a transfer completion interrupt is generated. (SF0FI=1)

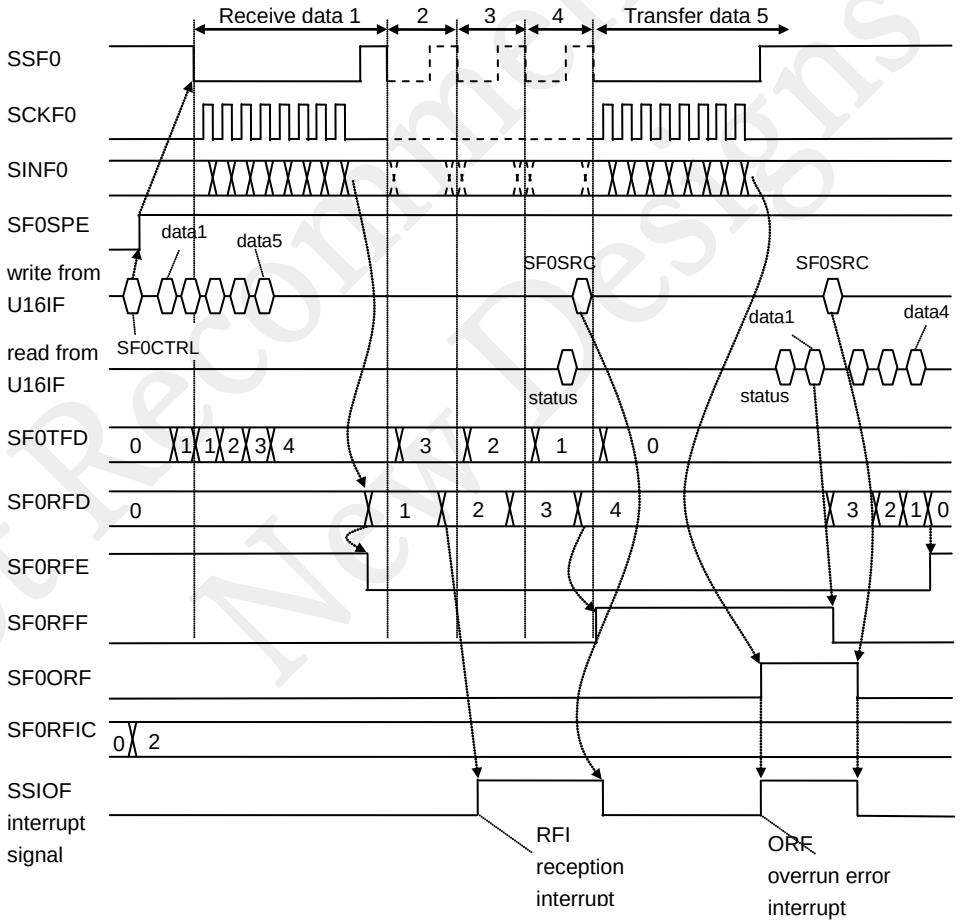


Figure 12-9 Master Mode (Receive Operation)

12.3.10 FIFO Operation

SSIOF includes the receive FIFO of 4 words and the transmit FIFO of 4 words. The FIFO state is indicated in the SF0TFF, SF0TFE, SF0RFF, and SF0RFE bits of SF0SRR, and the SF0TFD and SF0RFD bits of SF0FSR.
There are three FIFO states, Full (SF0TFF and SF0RFF), Empty (SF0TFE and SF0RFE), and Depth (SF0TFD and SF0RFD).

12.3.11 Write Overflow

If further writing is performed when the transmit FIFO is in Full status (SF0TFF = 1), a write overflow is set. (SF0WOF=1)
However, interrupt is not generated even when a write overflow occurs.
SF0WOF is cleared when SF0SRR is read.

12.3.12 Overrun Error

If further reception is performed when the receive FIFO is in Full status (SF0RFF = 1), an overrun error occurs. (SF0ORF=1)
If an overrun error occurs, the SF0ORF bit of SF0SRR is set, and an overrun error interrupt is generated. The newly received data is not held.
Read the content of the receive FIFO, clear the SF0RFF bit, then write "1" in the SF0ORFC bit to clear the SF0ORF bit.

12.3.13 FIFO Clear

The transmit/receive counter control of FIFO can be initialized to the initial setting state (SF0TFF=0, SF0TFE=1, SF0RFF=0, and SF0RFE=1 in the SF0SRR register and SF0TFD=000 and SF0RFD=000 in the SF0FSR register) by setting the SF0FICL bit of the SF0CTRL register to 1.
The SF0FICL bit of the SF0CTRL register needs to be 0, before next transfer operation.
Even if SF0FICL bit of SF0CTRL register is set to 1, the interrupt is not changed for SF0RFIC, SF0TFIC, SF0ORIE, SF0FIE, SF0RFIE, and SF0TFIE of the SF0INTC register, and SF0ORF, SF0FI, SF0RFI, and SF0TFI of the SF0SRR register.

This bit can be used to discard the data of FIFO when the communication is aborted.

12.3.14 Transfer When Slave Has Different Number of FIFO Transfer Bytes/Words

(1) The master sends data only when the transmitted data is already written in FIFO.
(2) As the slave's transmit data count is determined by the master, data is transferred as follows if the number of FIFO transfer bytes/words of slave is different from that of the master.
If the transmitted data is not written in the slave's FIFO, a 0xFF ((0xFFFF) for word) is sent, including the state after a reset.

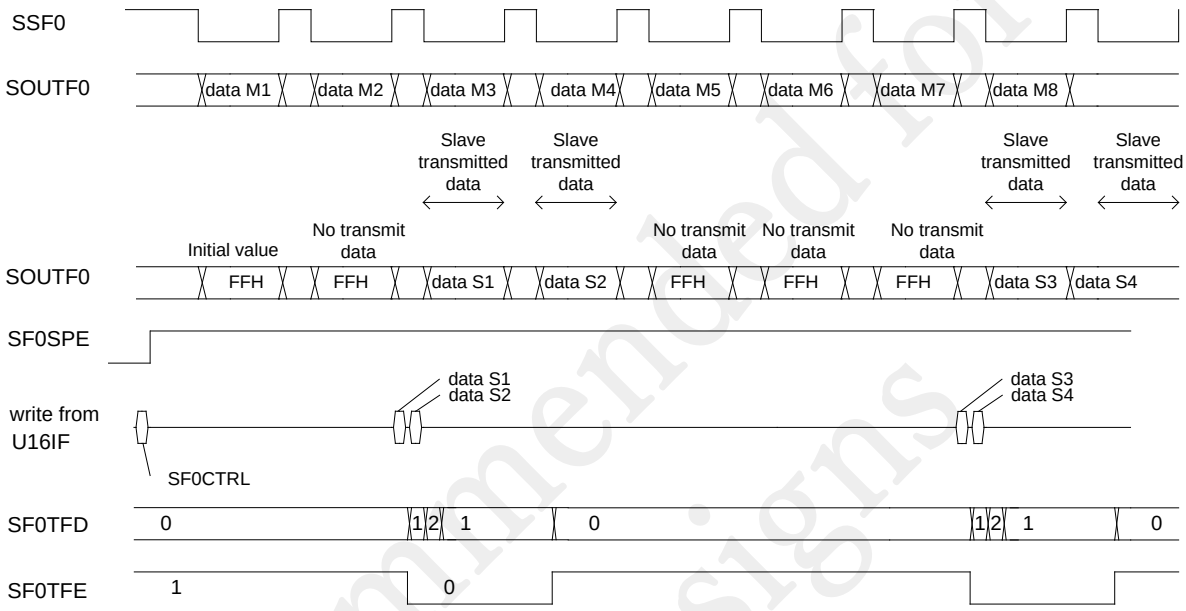


Figure 12-10 Transfer When Slave Has Different Number of FIFO Transfer Bytes/Words

12.3.15 Mode Fault (MDF)

A mode fault error occurs if the SSF0 signal becomes low level in Master mode. (SF0SRR's SF0MDF is set.) If this bit becomes 1, it indicates that there is risk of two or more masters competing for the bus.
When a mode fault error occurs, SSIOF performs the following operations since there is a risk of bus latch-up:

1. Automatically sets the SF0MST bit of SF0CTRL to 0 (slave).
2. Automatically sets the SF0SPE bit of SF0CTRL to 0 (disabled) to make the SSIOF unable to transfer.
3. Set SF0MDF of SF0SRR, and also generates an interrupt if the SF0MDFE bit of SF0CTRL is 1 (interrupt permitted).

The system should resolve the causes of the mode fault, and then clear SF0MDF according to the following steps:

1. Write 1 in SF0MDF to clear it.
2. Set SF0CTRL again.

Figure 12- shows the timing that allows a mode fault operation.

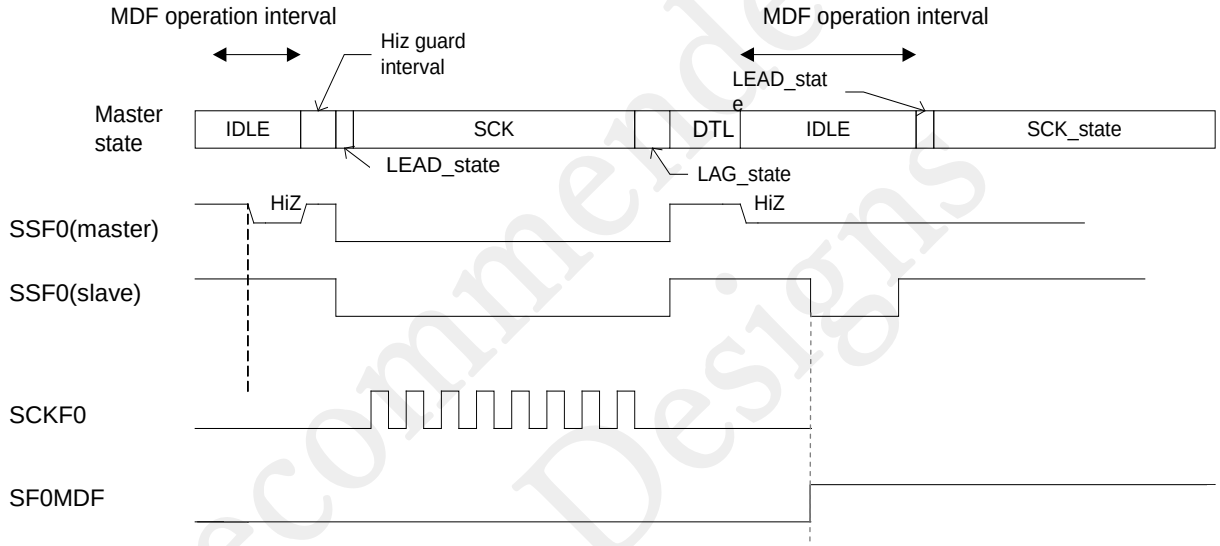


Figure 12-11 Timing That Allows Mode Fault Operation

12.3.16 Interrupt Source

12.3.16.1 SSIOF Interrupt Source

There are the following five types.

- Mode fault
  If a mode fault (multi-master bus contention) occurs, SF0MDF of SF0SRR is set and a mode fault interrupt is generated.
- Overrun
  If an overrun occurs, SF0ORF of SF0SRR is set, and an overrun error interrupt is generated.
- Transmit FIFO threshold
  If the remaining data of the transmit FIFO matches the byte count selected with SF0TFIC, SF0TFI of SF0SRR is set to generate a transmission interrupt.
- Receive FIFO threshold
  If the number of data received in the receive FIFO is equal to or more than following the byte count selected with SF0RFIC of SF0CR, SF0RFI of SF0SRR is set to generate a reception interrupt.
- End of transfer
  If the transmit FIFO becomes empty and the transfer of the last byte is finished, SF0FI of SF0SRR is set to generate a transfer end interrupt.

12.3.16.2 Clear SSIOF Interrupt

An interrupt request is cleared by writing 1 to each interrupt bit (SF0TFC, SF0RFC, SF0FC, SF0ORFC, SF0MDFC, SF0SPIFC, and SF0WOFC) of the SF0SRR.

12.3.16.3 SSIOF Interrupt Timing

Figure 12-12 shows the interrupt timing.
The remaining transmit byte count interrupt (TFI) generates an interrupt in 1 to 2 SYSCLK after the shift clock of the second bit.
For receive byte count interrupt (RFI), transfer completion interrupt (FI), and overrun (ORF), an interrupt is generated in 1 to 2 SYSCLK after the sampling clock at the MSB.
For MDF, an interrupt is generated at a mode fault occurrence.

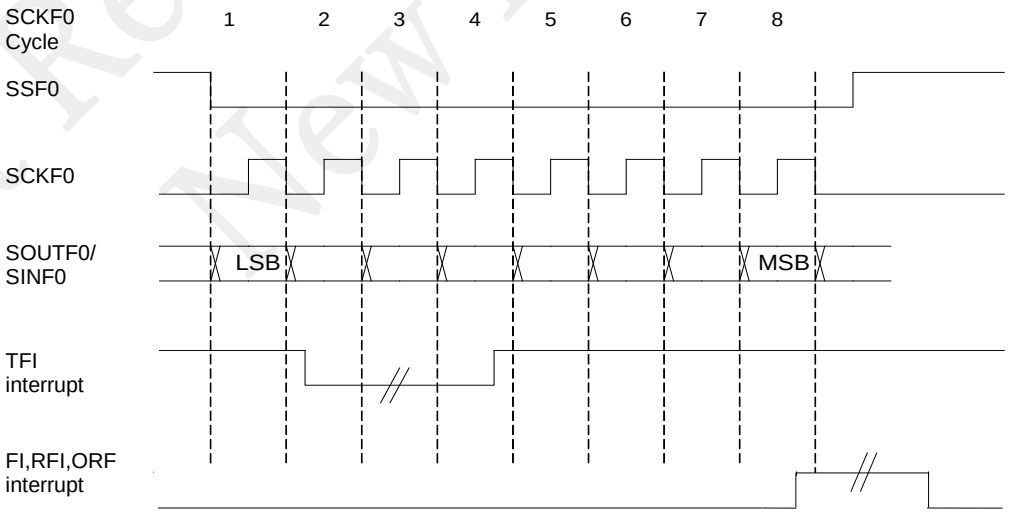


Figure 12-12 Interrupt Timing

12.3.16.4 Interrupt processing flow

Figure 12-13 show the processing flow in the receiving operation of the slave mode.

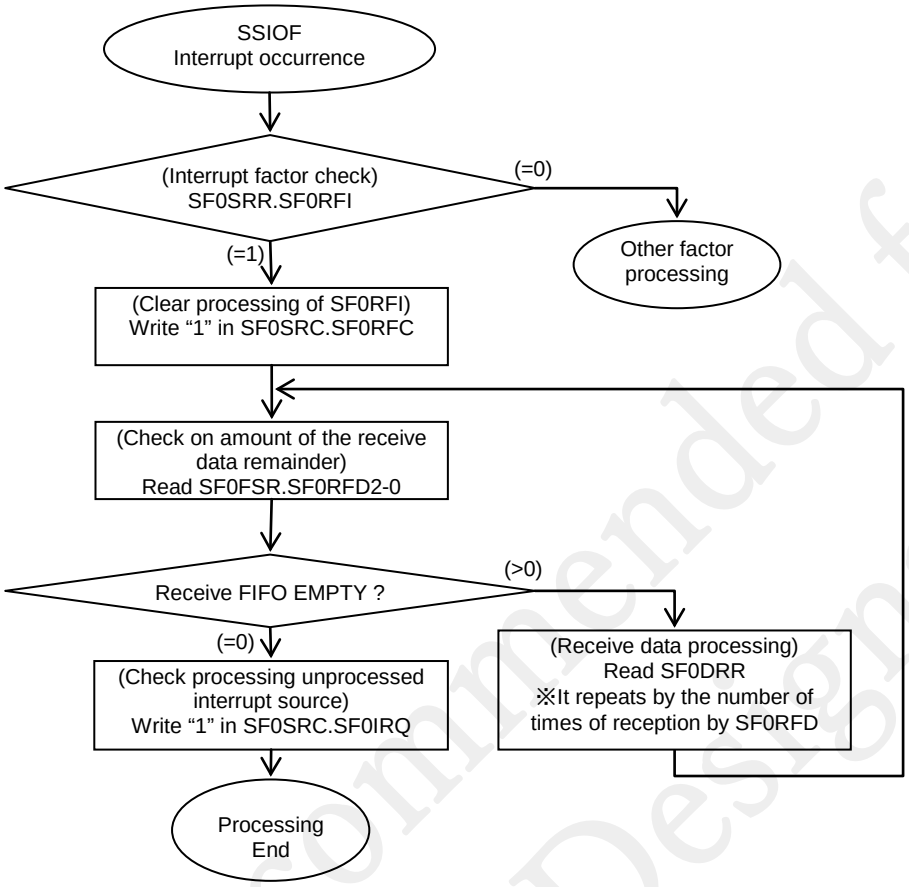


Figure 12-13 Example of the interrupt control flow

12.3.17 Hi-Z Operation

Figure 12-14 shows an example of using Hi-Z (SF0MOZ, SF0SOZ, and SF0SSZ).
The Hi-Z transmit interval of the master is limited to the IDLE time shown below.
To reduce the effect of noise in the Hi-Z state, "1"/"0" is fixed 1SCKF0 before the transmission starts (HiZ guard interval), and "1"/"0" is fixed during the DTL time of the transfer interval. If any of the SF0MOZ, SF0SOZ, and SF0SSZ bits is set to 1, the HiZ guard interval is inserted before the transmission starts.

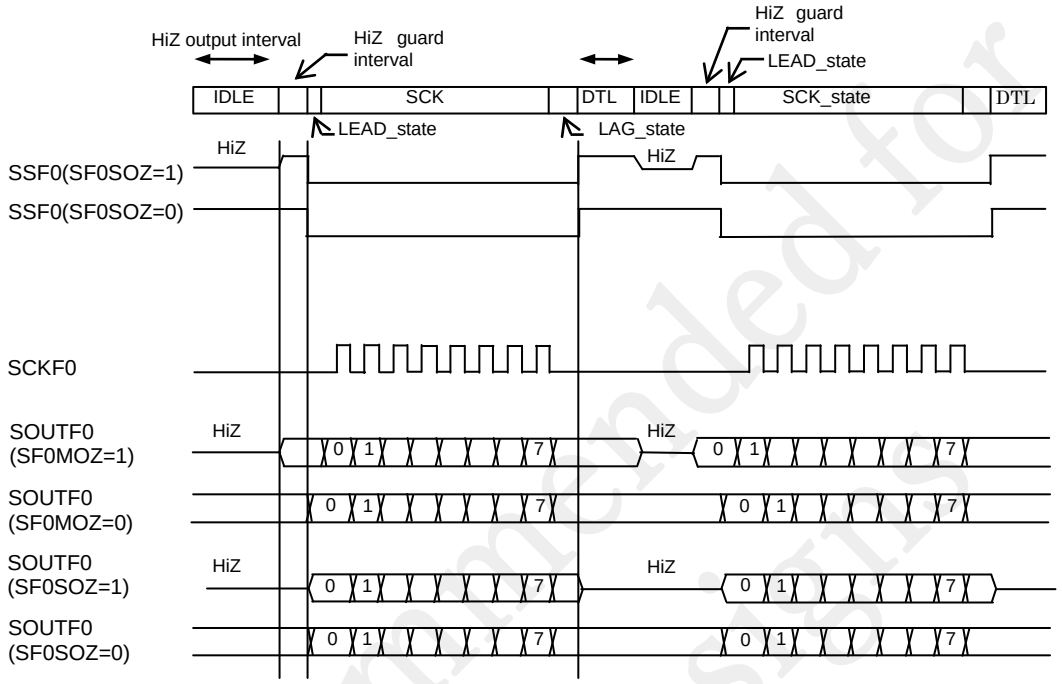


Figure 12-24 Hi-Z Operation

12.3.18 Interval from SF0MST Setting to Transfer Start

The SSIOF bus (SOUTF0, SCKF0, and SSF0) remains high impedance until Master mode is set.
After setting SF0MSTR, wait for at least 100ns before starting the transmission (SF0SPE = 1, or transfer started by data write).

12.3.19 Pin Settings

To enable the SSIOF function, the applicable bit of each related port register needs to be set. See Chapter 19, "Port 2", Chapter 20, "Port 3", Chapter 21, "Port 4", and Chapter 22, "Port 5" for details about the port registers. These settings should be completed before use.
For SOUTF0, SINF0, SCKF0 and SSF0, the ports can be selected from several possibilities.
Be sure to select one of the following combinations of ports for SOUTF0/SINF0/SCKF0/SSF0.

	SSIOF pin	Combination 1	Combination 2	Combination 3	Combination 4
SSIOF	SOUTF0,SINF0, SCKF0,SSF0	P20,P21, P22,P23	P34,P35, P36,P37	P44,P45, P46,P47	P54,P55, P56,P57

Note that only one port can be selected as port.
If using P22 as SCKF0 in master mode, the max clock output frequency is 2MHz.

Chapter 13

UART

13 UART

13.1 General Description

This LSI includes one channel of UART (Universal Asynchronous Receiver Transmitter), a full-duplex communication start-stop synchronous serial interface.
For input clocks, see Chapter 6, "Clock Generation Circuit".
To use the UART, it needs to set the secondary and quartic functions of the ports 0, 3, 4, and 5. For the port function setting, see Chapter 17 "Port 0", Chapter 20 "Port 3", Chapter 21 "Port 4", and Chapter 22 "Port5".

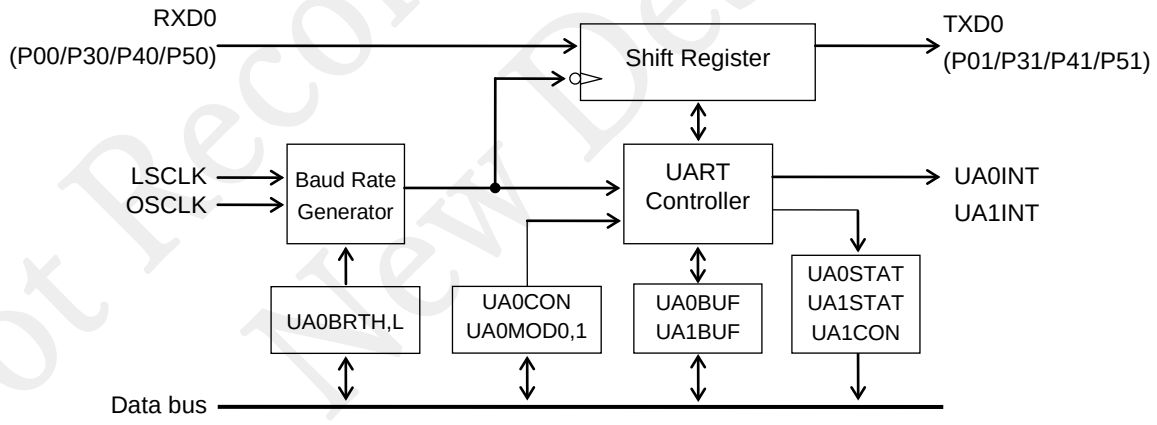
If The UART is used, Set to "0" the both of DUA0 and DUA1 bit of BLKCON2 register. If the both of these bits are "1", the UART is reset-state. For BLKCON2 register, see Chapter 4, "Power Management".

13.1.1 Features

- 5-bit/6-bit/7-bit/8-bit data length selectable.
- Odd parity, even parity, or no parity selectable.
- 1 stop bit or 2 stop bits selectable.
- Provided with parity error flag, overrun error flag, framing error flag, and transmit buffer status flag.
- Positive logic or negative logic selectable as communication logic.
- LSB first or MSB first selectable as a communication direction.
- Communication speed: Settable within the range of 4800bps to 115200bps.
- Built-in baud rate generator.

13.1.2 Configuration

Figure 13-1 shows the configuration of the UART.



UA0BUF	: UART0 receive buffer
UA1BUF	: UART0 transmit buffer
UA0BRTH,L	: UART0 baud rate registers H and L
UA0CON	: UART0 control register
UA0MOD	: UART0 mode register
UA0STAT	: UART0 receive status register
UA1STAT	: UART0 transmit status register
UA1CON	: UART0 transmit monitor register

Figure 13-1 Configuration of UART

13.1.3 List of Pins

Pin Name	I/O	Function
RXD0	I	UART0 data input pin
TXD0	O	UART0 data output pin

13.2 Description of Registers

13.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F710	UART0 receive buffer	UA0BUF	–	R/W	8	00
0F711	UART0 control register	UA0CON	–	R/W	8	00
0F712	UART0 mode register	UA0MOD0	UA0MOD	R/W	8/16	00
0F713		UA0MOD1		R/W	8	00
0F714	UART0 baud rate register	UA0BRTL	UA0BRT	R/W	8/16	FF
0F715		UA0BRTH		R/W	8	0F
0F716	UART0 receive status register	UA0STAT	–	R/W	8	00
0F718	UART0 transmit buffer	UA1BUF	–	R/W	8	00
0F719	UART0 transmit monitor register	UA1CON	–	R/W	8	00
0F71E	UART0 transmit status register	UA1STAT	–	R/W	8	00

13.2.2 UART0 Receive Buffer (UA0BUF)

Address: 0F710H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0BUF	U0B7	U0B6	U0B5	U0B4	U0B3	U0B2	U0B1	U0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0BUF is a special function register (SFR) used to store the received data.
Since data received at termination of reception is stored in UA0BUF, read the contents of UA0BUF using the UART0 interrupt at termination of reception. At continuous reception, UA0BUF is updated whenever reception terminates. Any write to UA0BUF is disabled after communication is started.
When the 5- to 7-bit data length is selected, unnecessary bits become "0".

13.2.3 UART0 Transmit Buffer (UA1BUF)

Address: 0F718H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1BUF	U1B7	U1B6	U1B5	U1B4	U1B3	U1B2	U1B1	U1B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1BUF is a special function register (SFR) used to store the transmitted data.
Write data to be transmitted in the UA1BUF. To transmit data consecutively, confirm the U1FUL flag of the transmit status register (UA1STAT) becomes "0", then write the next transmitted data to UA1BUF. Any value written to UA1BUF can be read. When the 5- to 7-bit data length is selected, unnecessary bits become invalid in the transmit mode.

13.2.4 UART0 Control Register (UA0CON)

Address: 0F711H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0CON	–	–	–	–	–	–	–	U0EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0CON is a special function register (SFR) used to start/stop communication of the UART.

Description of Bits

- **U0EN** (bit 0)
  The U0EN bit is used to specify the UART communication operation start. When U0EN is set to "1", UART communication starts. To terminate the communication, set the bit to "0" by software.

U0EN	Description
0	Stops communication. (Initial value)
1	Start communication

[Note]
Setting ports and UART should be completed before setting U0EN to “1”.

13.2.5 UART0 Transmit Monitor Register (UA1CON)

Address: 0F719H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1CON	–	–	–	–	–	–	–	U1EN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1CON is a special function register(SFR) which indicate UART transmission status.

Description of Bits

- **U1EN** (bit 0)
  The bit indicates transmission operating status .
  When a transmission is started, the bit becomes “1”,
  When a transmission is stopped, the bit becomes “0”.

U1EN	Description
0	stop transmit（initial value）
1	transmitting

13.2.6 UART0 Mode Register (UA0MOD)

Address: 0F712H
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
UA0MOD0	–	U0RSS	–	–	–	U0CK1	U0CK0	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
UA0MOD1	–	U0DIR	U0NEG	U0STP	U0PT1	U0PT0	U0LG1	U0LG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0MOD is a special function register (SFR) used to set the transfer mode of the UART.

Description of Bits

- **U0CK1-0** (bits 2 to 1)
  The U0CK1-0 bits are used to select the clock to be input to the baud rate generator of the UART0.

U0CK1	U0CK0	Description
0	0	LSCLK (initial value)
0	1	Prohibited
1	0	OSCLK
1	1	Prohibited

- **U0RSS** (bit 6)
  U0RSS is the bit that selects the UART0 received data input sampling timing.

U0RSS	Description
0	Value set in the UA0BRT registers/2 (initial value)
1	Value set in the UA0BRT registers/2-1

- **U0LG1-0** (bits 9 to 8)
  The U0LG1-0 bits are used to specify the data length in the communication of the UART.

U0LG1	U0LG0	Description
0	0	8-bit length (initial value)
0	1	7-bit length
1	0	6-bit length
1	1	5-bit length

- **U0PT1-0** (bits 11 to 10)
  The U0PT1-0 bits are used to select "even parity", "odd parity", or "no parity" in the communication of the UART.

U0PT1	U0PT0	Description
0	0	Even parity (initial value)
0	1	Odd parity
1	*	No parity bit

- **U0STP** (bit 12)
  The U0STP bit is used to select the stop bit length in the communication of the UART.

U0STP	Description
0	1 stop bit (initial value)
1	2 stop bit

- **U0NEG** (bit 13)
  The U0NEG bit is used to select positive logic or negative logic in the communication of the UART.

U0NEG	Description
0	Positive logic (initial value)
1	Negative logic

- **U0DIR** (bit 14)
  The U0DIR bit is used to select LSB first or MSB first in the communication of the UART.

U0DIR	Description
0	LSB first (initial value)
1	MSB first

[Note]
Always set UA0MOD while communication is stopped, and do not rewrite it during communication.

13.2.7 UART0 Baud Rate Register (UA0BRT)

Address: 0F714H
Access: R/W
Access size: 8/16 bit
Initial value: 0FFFH

	7	6	5	4	3	2	1	0
UA0BRTL	U0BR7	U0BR6	U0BR5	U0BR4	U0BR3	U0BR2	U0BR1	U0BR0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8
UA0BRTH	–	–	–	–	U0BR11	U0BR10	U0BR9	U0BR8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	1	1

UA0BRT is special function registers (SFRs) to set the count value of the baud rate generator which generates baud rate clocks.
For the relationship between the count value of the baud rate generator and baud rate, see Section 13.3.2, "Baud Rate".

[Note]
Always set UA0BRT while communication is stopped, and do not rewrite it during communication.

13.2.8 UART0 Receive Status Register (UA0STAT)

Address: 0F716H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA0STAT	–	–	–	–	–	U0PER	U0OER	U0FER
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA0STAT is a special function register (SFR) used to indicate the UART state in receive operations.
When any data is written to UA0STAT, all the flags are initialized to "0".

Description of Bits

- **U0FER** (bit 0)
  The U0FER bit is used to indicate occurrence of a framing error of the UART.
  When an error occurs in the start or stop bit, the U0FER bit is set to "1". U0FER is updated each time reception is completed.

U0FER	Description
0	No framing error (initial value)
1	With framing error

- **U0OER** (bit 1)
  The U0OER bit is used to indicate occurrence of an overrun error of the UART.
  If the received data in the transmit/receive buffer (UA0BUF) is received again before it is read, this bit is set to "1". Even if reception is stopped by the U0EN bit and then reception is restarted, this bit is set to "1" unless the previously received data is not read. Therefore, make sure that data is always read from the receive buffer even if the data is not required.

U0OER	Description
0	No overrun error (initial value)
1	Overrun error

- **U0PER** (bit 2)
  The U0PER bit is used to indicate occurrence of a parity error of the UART.
  When the parity of the received data and the parity bit attached to the data do not coincide, this bit is set to "1". U0PER is updated whenever data is received.

U0PER	Description
0	No parity error (initial value)
1	Parity error

13.2.9 UART0 Transmit Status Register (UA1STAT)

Address: 0F71EH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
UA1STAT	–	–	–	–	U1FUL	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UA1STAT is a special function register (SFR) used to indicate the UART state in transmit operations.
When any data is written to UA1STAT, all the flags are initialized to "0".

Description of Bits

- **U1FUL** (bit 3)
  U1FUL indicates the UART transmit buffer state.
  When the transmitted data is written in UA1BUF, this bit is set to "1" and when this transmitted data is transferred to the shift register, this bit is set to "0". To transmit the data consecutively, confirm the U1FUL flag becomes "0", then write the next transmitted data to the UA1BUF.

U1FUL	Description
0	No data in the transmit buffer (UA1BUF)(initial value)
1	Data present in the transmit buffer (UA1BUF)

13.3 Description of Operation

13.3.1 Transfer Data Format

In the transfer data format, one frame contains a start bit, a data bit, a parity bit, and a stop bit. In this format, 5 to 8 bits can be selected as data bit. For the parity bit, "with parity bit", "without parity bit", "even parity", or "odd parity" can be selected. For the stop bit, "1 stop bit" or "2 stop bits" are available and LSB first or MSB first selectable as a communication direction. For serial input/output logic, positive logic or negative logic can be selected.
All these options are set with the UART0 mode register (UA0MOD1).
Figure 13-2 and Figure 13-3 show the positive logic input/output format and negative logic input/output format, respectively.

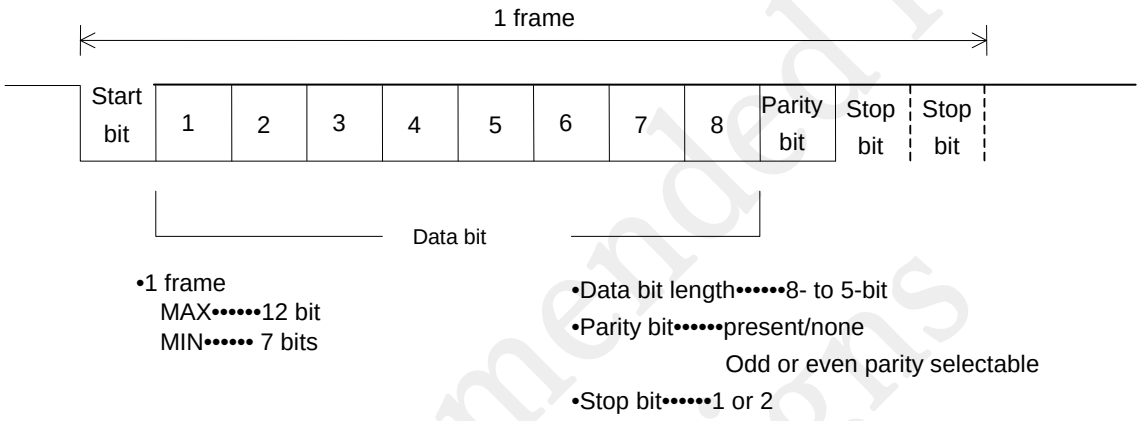


Figure 13-2 Positive Logic Input/Output Format

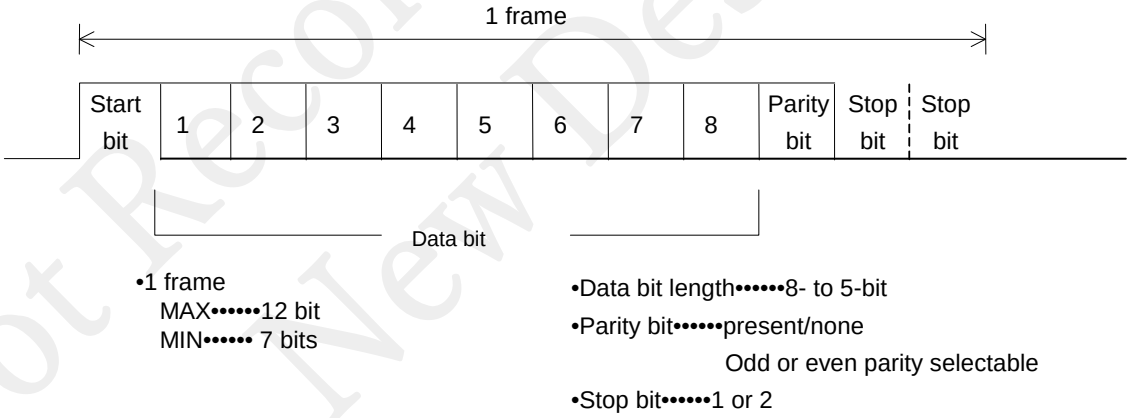


Figure 13-3 Negative Logic Input/Output Format

13.3.2 Baud Rate

Baud rates are generated by the baud rate generator.
The baud rate generator generates a baud rate by counting the clock selected by the baud rate clock selection bits (U0CK1, U0CK0) of the UART0 mode register 0 (UA0MOD0). The count value of the baud rate generator can be set by writing it in the UART0 baud rate register (UA0BRT). The maximum count is 4096.
The setting value of UA0BRT is expressed by the following equation.

$$UA0BRT = \frac{\text{Clock frequency (Hz)}}{\text{Baud rate (bps)}} - 1$$

Table 13-1 lists the count values for typical baud rates.

Table 13-1 Count Values for Typical Baud Rates

Baud rate	Baud rate generator clock selection	Baud rate generator counter value			Error*1
	Baud rate clock	Count value	Period of cycle	UA0BRT	
4800bps	16MHz	3333	Approx. 208us	0D04H	0.01%
9600bps		1667	Approx. 104us	0682H	-0.02%
19200bps		833	Approx. 52us	0340H	0.04%
38400bps		417	Approx. 26us	01A0H	-0.08%
57600bps		278	Approx. 17.4us	0115H	-0.08%
115200bps		139	Approx. 8.7us	008AH	-0.08%

*1:The error does not include the clock error. Use this in consideration of an error of Baud rate clock.

13.3.3 Transmitted Data Direction

Figure 13-4 shows the relationship between the transmit/receive buffer and the transmit/receive data.

Transmit:n=1, Receive:n=0

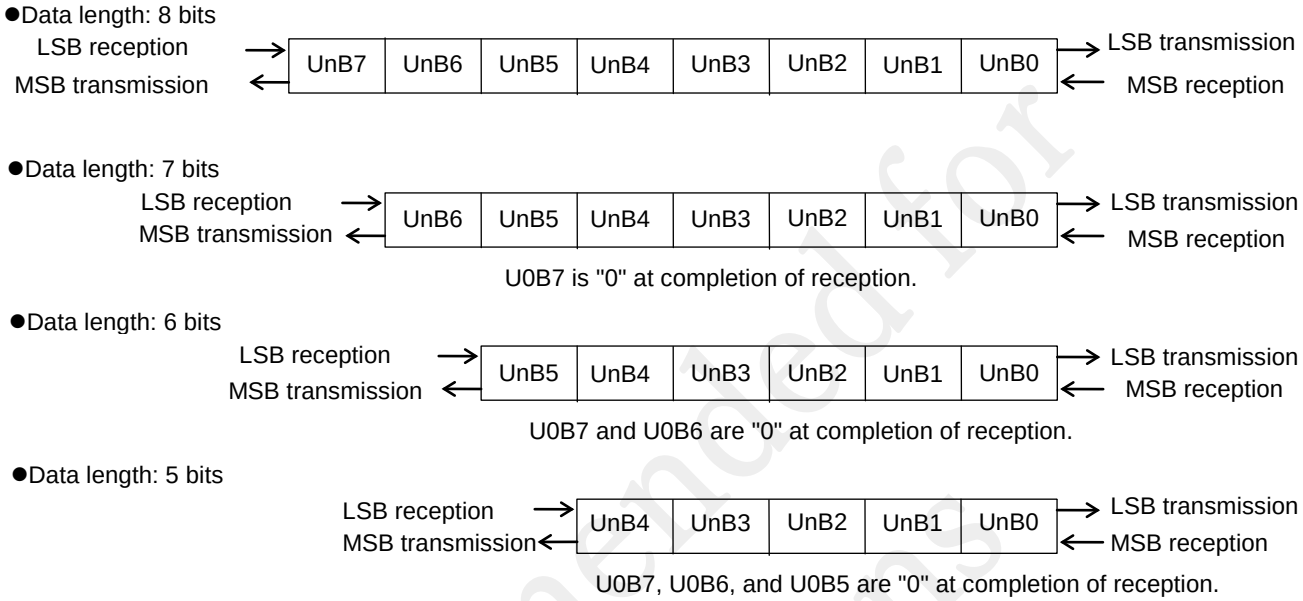


Figure 13-4 Relationship between Transmit/Receive Buffer and Transmit/Receive Data

13.3.4 Transmit Operation

Transmission is started by setting the U0EN bit of the UART0 control register (UA0CON) to "1" and set transfer data to UA1BUF. The order of UA0EN setting and UA1BUF setting does not matter.
Figure 13-5 shows the operation timing for transmission.

When the U0EN bit is set to "1" (①), the baud rate generator generates an internal transfer clock of the baud rate set and starts transmit operation.
The start bit is output to the TXD pin by the falling edge of the internal transfer clock (②). Subsequently, the transmitted data, a parity bit, and a stop bit are output.
When the start bit is output (②), a UART0 interrupt is requested. In the UART0 interrupt routine, the next data to be transmitted is written to the transmit buffer (UA1BUF).
When the next data to be transmitted is written to the transmit buffer (UA1BUF), the transmit buffer status flag (U1FUL) is set to "1" (③) and a UART transmission interrupt is requested on the falling edge of the internal transfer clock (④) after transmission of the stop bit. At this time if the UART transmission interrupt routine is terminated without writing the next data to the transmit buffer, the U1FUL bit is not set to "1" (⑤). The transmit operation stops when the stop bit is sent, the U1EN bit is reset to "0", and the UART transmission interrupt is requested.
The valid period for the next transmit data to be written to the transmit buffer is from the generation of an interrupt to the termination of stop bit transmission. (⑥)

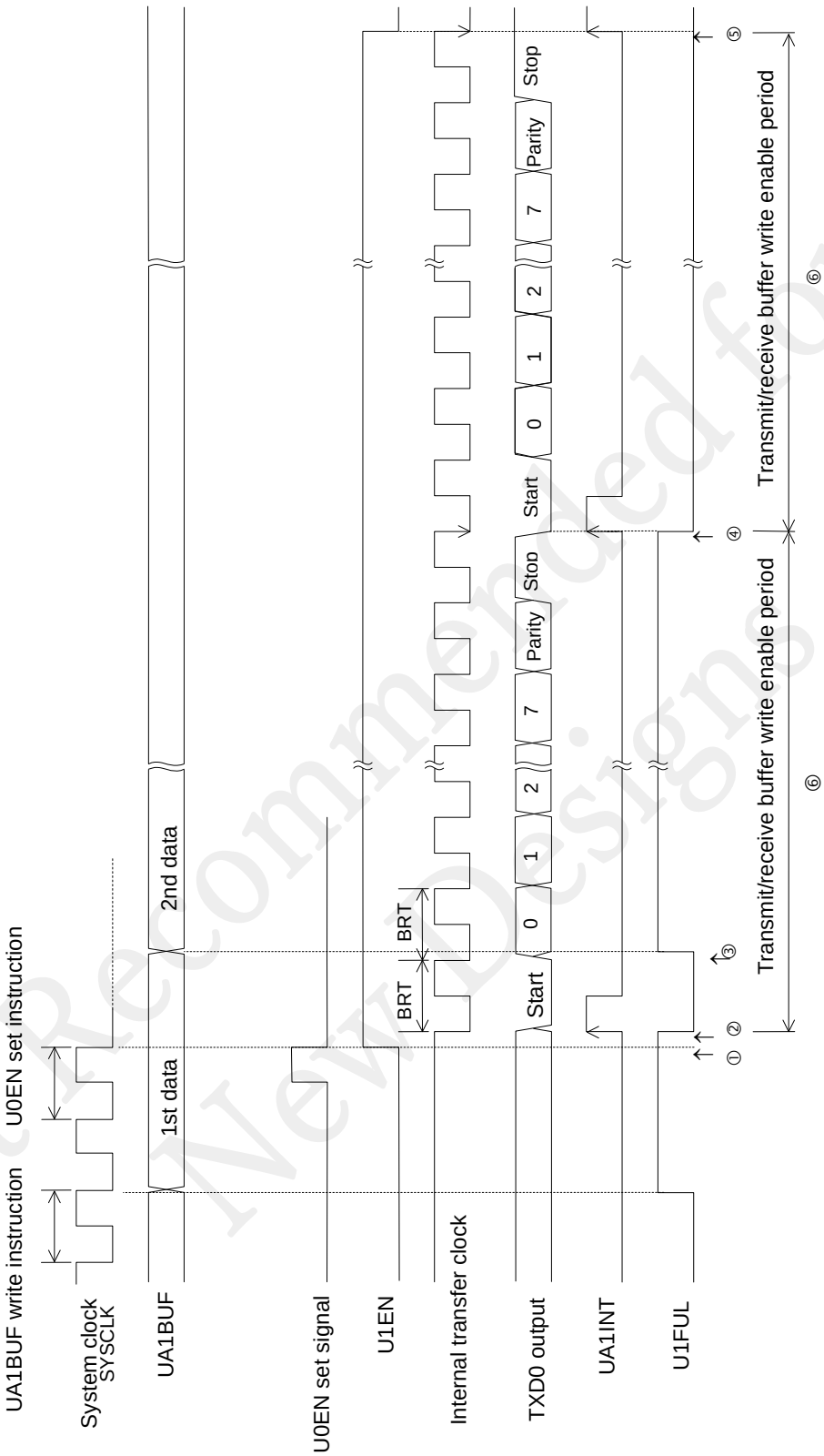


Figure 13-5 Operation Timing in Transmission

13.3.5 Receive Operation

Select the receive data pin using the U0RSEL bit of the UART0 mode register 0 (UA0MOD0). Reception is started by setting the U0EN bit of the UART0 control register (UA0CON) to "1".
Figure 13-6 shows the operation timing for reception.

When receive operation starts, the LSI checks the data sent to the input pin RXD and waits for the arrival of a start bit.
When detecting a start bit (②), the LSI generates the internal transfer clock of the baud rate set with the start bit detect point as a reference and performs receive operation.
The shift register shifts in the data input to RXD on the rising edge of the internal transfer clock. The data and parity bit are shifted into the shift register and 5- to 8- bit received data is transferred to the receive buffer (UA0BUF) concurrently with the falling edge of the internal transfer clock of ③.
The LSI requests a UART reception interrupt on the rising edge of the internal transfer clock subsequent to the internal transfer clock by which the received data was fetched (④) and checks for a stop bit error and a parity bit error. When an error is detected, the LSI sets the corresponding bit of the UART0 status register (UA0STAT) to "1".

Parity error : U0PER ="1"
Overrun error : U0OER ="1"
Framing error : U0FER ="1"

As shown in Figure 13-6, the rise of the internal transfer clock is set so that it may fall into the middle of the bit interval of the received data.
Reception continues until the U0EN bit is reset to "0" by the program. When the U0EN bit is reset to "0" during reception, the received data may be destroyed. When the U0EN bit is reset to "0" during the "U0EN reset enable period" in Figure 13-6, the received data is protected.

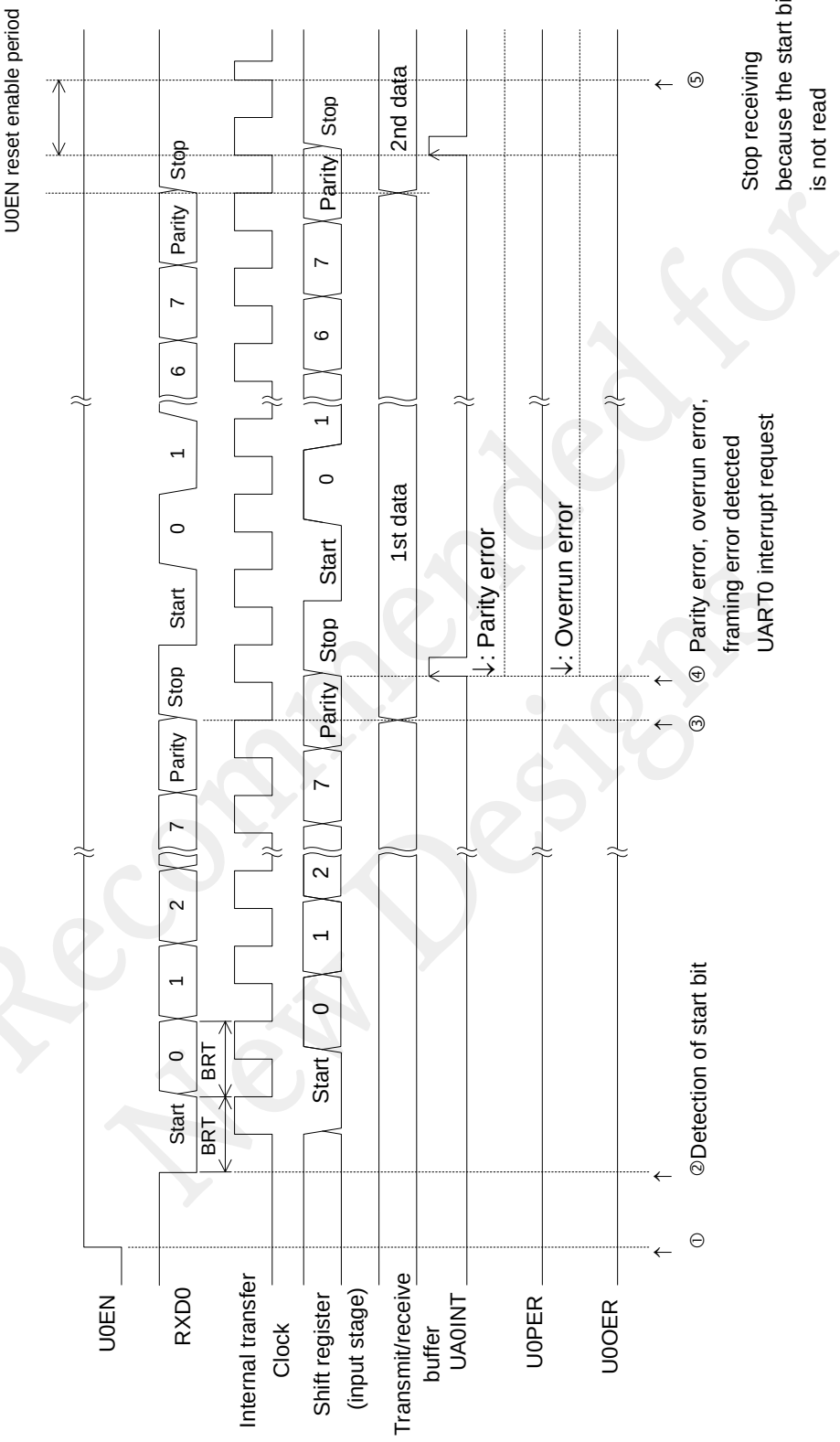


Figure 13-6 Operation Timing in Reception

13.3.5.1 Detection of Start Bit

The start bit is sampled with the baud rate generator clock (OSCLK). Therefore, the start bit detection may be delayed for one cycle of the baud rate generator clock at the maximum.
Figure 13-7 shows the start bit detection timing.

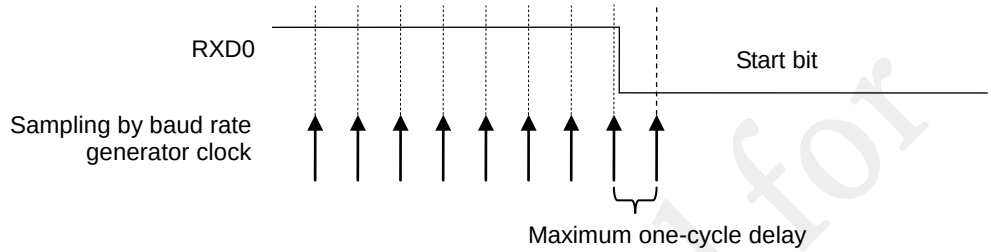
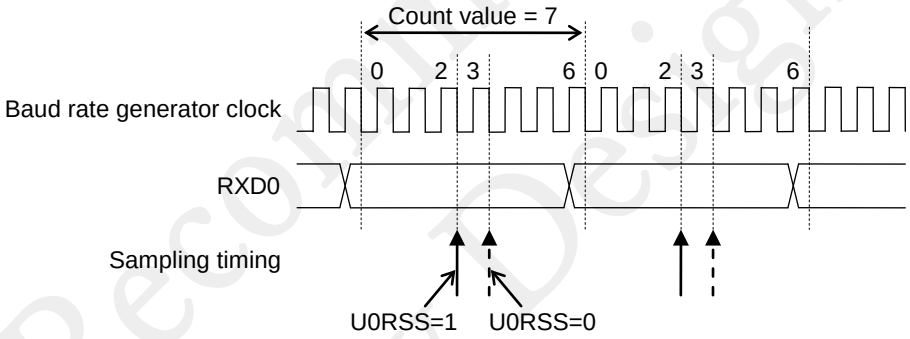


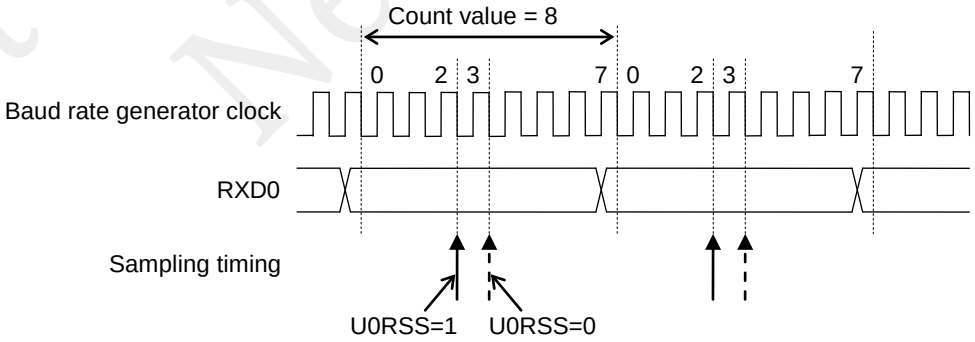
Figure 13-7 Start Bit Detection Timing (Positive Logic)

13.3.5.2 Sampling Timing

When the start bit is detected, the received data that was input to the RXD is sampled almost at the center of the baud rate, then loaded to the shift register.
The loading sampling timing of this shift register can be adjusted for one clock of the baud rate generator clock, using the U0RSS bit of the UART0 mode register (UA0MOD).
Figure 13-8 shows the relationship between the U0RSS bit and the sampling timing.



(1) When the baud rate generator count value is "7" (odd)



(2) When the baud rate generator count value is "8" (even)

Figure 13-8 Relationship between U0RSS Bit and Sampling Timing

13.3.5.3 Receive Margin

If there is an error between the sender baud rate and the baud rate generated by the baud rate generator of this LSI, the error accumulates until the last stop bit loading in one frame, decreasing the receive margin. Figure 13-9 shows the baud rate errors and receive margin waveforms.

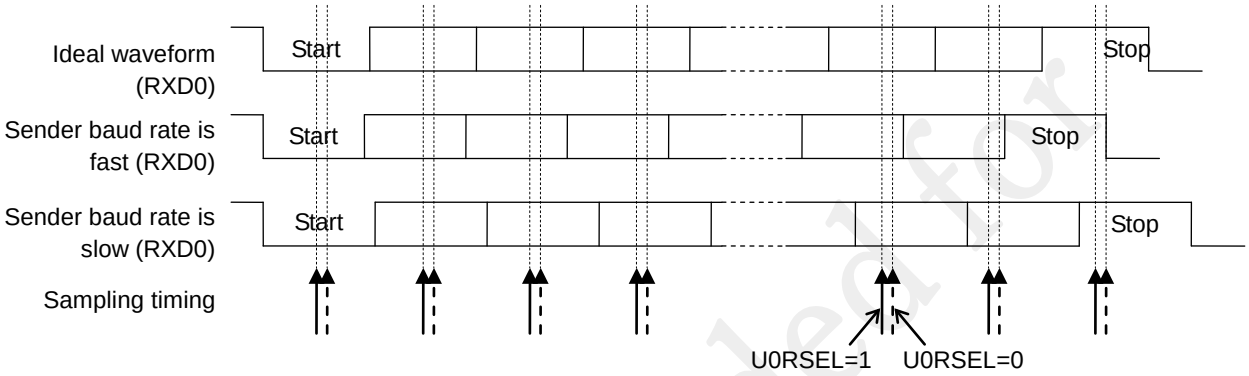


Figure 13-9 Baud Rate Error and Receive Margin

[Note]
In system designing, ensure a sufficient receive margin considering the baud rate difference between sender and receiver, start bit detection delay, distortion in receive data, and influence of noise.

Chapter 14

UART with FIFO (UARTF)

14 UART with FIFO (UARTF)

14.1 General Description

The UART with FIFO (UARTF) functions as the input/output interface, carries out serial-to-parallel conversion of the data sent from the peripheral devices, and also converts the parallel data sent from the CPU into serial data. The UART has a 4-byte FIFO for transmission and reception, capable of storing up to 4 bytes of data during transmission/reception in the FIFO mode.
Further, the receive FIFO generates 3 bits of error data for every byte of received data. The CPU can read out the UARTF state at any time. The information that can be read out consists of the type and status of the transfer operation under execution, and the statuses of errors such as parity, overrun, framing errors, and break interrupt, etc.

The I/O pins of the UARTF are assigned as the tertiary function of the ports 2, 3, 4, and 5. For the ports 2, 3, 4, and 5, see Chapter 19 "Port 2", Chapter 20 "Port 3", Chapter 21 "Port 4", and Chapter 22 "Port 5".

14.1.1 Features

- Full duplex buffer system
- All status reporting function
- 4-byte transmit and receive FIFOs
- Independent control of transmit, receive, line status data set interrupt and FIFO
- Programmable serial interface
  - 5-, 6-, 7-, and 8-bit characters
  - Odd parity, even parity, no parity generation and verification
  - 1, 1.5, or 2 stop bits
- Communication speed: Settable within the range of 2400bps to 115200bps.
- Built-in baud rate generator.

14.1.2 Configuration

Figure 14-1 shows the configuration of the UARTF.

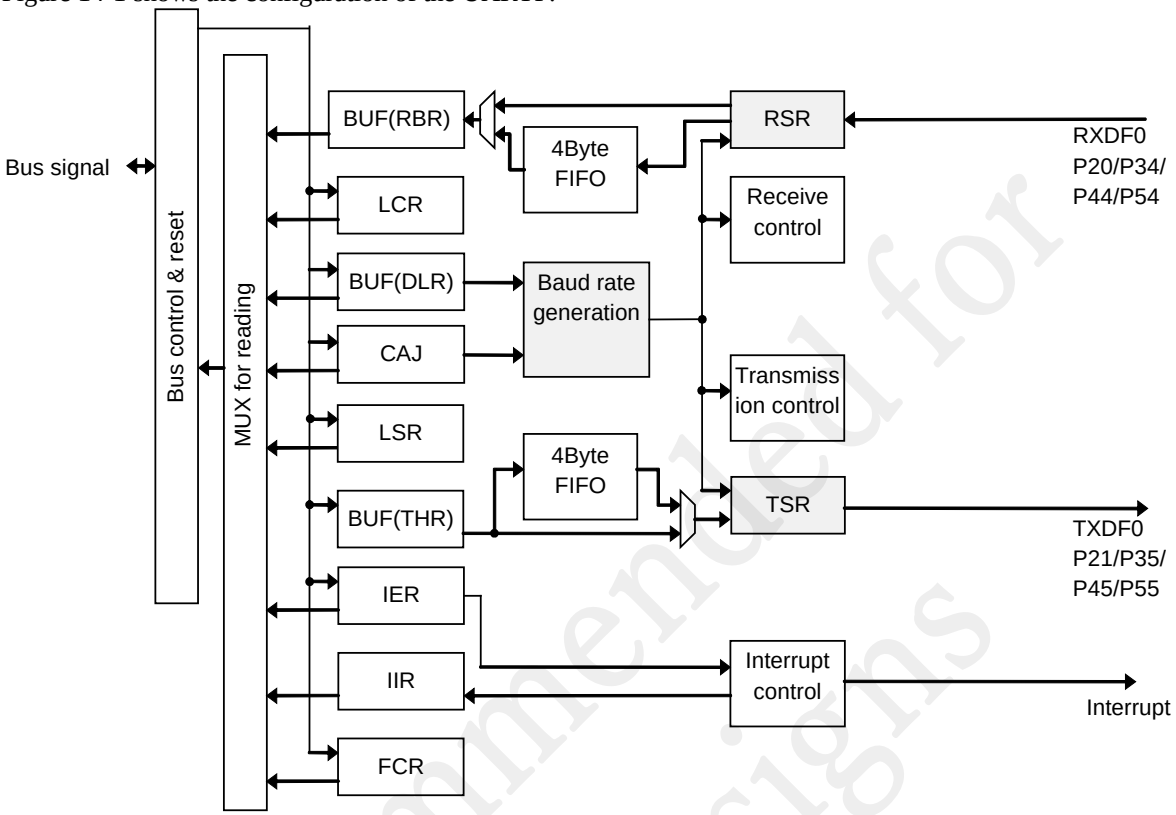


Figure 14-1 Configuration of UARTF

14.1.3 List of Pins

Pin Name	I/O	Function
RXDF0	I	UARTF0 data input pin
TXDF0	O	UARTF0 data output pin

14.2 Description of Registers

14.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F7C0	UARTF0 transmit/receive buffer	UAF0BUFL	UAF0BUF	R/W	8/16	xx
0F7C1		UAF0BUFH		R/W	8	00
0F7C2	UARTF0 interrupt enable register	UAF0IERL	UAF0IER	R/W	8/16	00
0F7C3		UAF0IERH		R/W	8	00
0F7C4	UARTF0 interrupt status register	UAF0IIRL	UAF0IIR	R	8/16	01
0F7C5		UAF0IIRH		R	8	00
0F7C6	UARTF0 mode register	UAF0MODL	UAF0MOD	R/W	8/16	00
0F7C7		UAF0MODH		R/W	8	00
0F7C8	UARTF0 line status register	UAF0LSRL	UAF0LSR	R	8/16	60
0F7C9		UAF0LSRH		R	8	00
0F7CA	UARTF0 clock adjustment register	UAF0CAJL	UAF0CAJ	R/W	8/16	0D
0F7CB		UAF0CAJH		R/W	8	00
0F7CC	UARTF0 interrupt request register	UAF0IRQL	UAF0IRQ	W	8/16	00
0F7CD		UAF0IRQH		W	8	00

14.2.2 UARTF0 Transmit/Receive Buffer (UAF0BUF)

Address: 0F7C0H
Access: R/W
Access size: 8/16 bits
Initial value: Undefined

	7	6	5	4	3	2	1	0
UAF0BUFL	UF0B7	UF0B6	UF0B5	UF0B4	UF0B3	UF0B2	UF0B1	UF0B0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	x	x	x	x	x	x	x	x

	15	14	13	12	11	10	9	8
UAF0BUFH	UF0B15	UF0B14	UF0B13	UF0B12	UF0B11	UF0B10	UF0B9	UF0B8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UAF0BUF is a special function register (SFR) that provides the following three functions.

(1) Read-only register for buffering received data: Receiver Buffer Register (RBR)
RBR is the register that holds received data from 5 to 8 bits depending on the character length.
The bit 0 of a data word is always the first serial data bit received. If data less than 8 bits is received, the data is entered in the right justified manner towards the LSB.
When the UART carries out parallel-to-serial or serial-to-parallel conversion operation, the register has the double buffer configuration so that read operations can be made.
RBR can be read by program when UF0DLAB of UAF0MOD is 0. When UAF0BUF is read, RBR can be read from UnB7-0. For UF0B15-8, 00H can be read.
The reset value is undefined.

(2) Write-only register for setting transmitted data: Transmitter Holding Register (THR)
THR is the register that holds transmitted data from 5 to 8 bits depending on the character length.
The bit 0 of the data word is always the first serial data bit that is transmitted.
When the UART carries out parallel-to-serial or serial-to-parallel conversion operation, the register has the double buffer configuration so that write operations can be made.
THR can be written by program when UF0DLAB of UAF0MOD is 0. When UAF0BUF is written, the UF0B7-0 data is written to THR. The UF0B15-8 data are invalid.

(3) 16-bit divisor latch for baud rate generator: Divisor Latch Resister (DLR)
DLR can be read/written by program when UF0DLAB of UAF0MOD is 1. For details, see "Baud rate clock generation".

	UF0DLAB = 0		UF0DLAB = 1	
	UAF0BUF[15:8]	UAF0BUF[7:0]	UAF0BUF[15:8]	UAF0BUF[7:0]
Read	00H	RBR	DLR[15:8]	DLR[7:0]
Write	Disabled	THR	DLR[15:8]	DLR[7:0]

14.2.3 UARTF0 Interrupt Enable Register (UAF0IER)

Address: 0F7C2H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
UAF0IERL	–	–	–	–	–	UF0ELSI	UF0ETBEI	UF0ERBFI
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
UAF0IERH	–	–	–	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UAF0IER is a special function register (SFR) used to set whether to enable/disable the UART interrupt source.

Description of Bits

- **UF0ERBFI** (bit 0)
  UF0ERBFI is used to set Enable/disable the received data read request interrupt (including character timeout interrupt in the FIFO mode).

UF0ERBFI	Description
0	Disable the received data read request interrupt (Includes the character timeout interrupt when FIFO is enabled) (initial value)
1	Enable the received data read request interrupt (Includes the character timeout interrupt when FIFO is enabled)

- **UF0ETBEI** (bit 1)
  UF0ETBEI is used to set Enable/disable the transmitted data write request interrupt.

UF0ETBEI	Description
0	Disable the transmitted data write request interrupt (initial value)
1	Enable the transmitted data write request interrupt

- **UF0ELSI** (bit 2)
  UF0ELSI is used to set Enable/disable the received data error interrupt.

UF0ELSI	Description
0	Disable the received data error interrupt (initial value)
1	Enable the received data error interrupt

14.2.4 UARTF0 Interrupt Status Register (UAF0IIR)

Address: 0F7C4H
Access: R
Access size: 8/16 bits
Initial value: 0001H

	7	6	5	4	3	2	1	0
UAF0IIRL	UF0FMD1	UF0FMD0	–	–	UF0IRID2	UF0IRID1	UF0IRID0	UF0IRP
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	1

	15	14	13	12	11	10	9	8
UAF0IIRH	–	–	–	–	–	–	–	–
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

UAF0IIR is a special function register (SFR) used to indicate the UART state in interrupt transmit/receive operations.
UAF0IIR stores information indicating that an interrupt with a certain priority level is pending, along with the type of that interrupt. IIR indicates the interrupt with the highest priority level that is pending.

Description of Bits

- **UF0IRP** (bit 0)
  UF0IRP indicates whether a UARTF0 interrupt was generated.

UF0IRP0	Description
0	Interrupt was generated
1	Interrupt was not generated (initial value)

- **UF0IRID2-0** (bits 3 to 1)
  UF0IRID2-0 indicate the interrupt source of the UARTF0 interrupt.
  LVL=1 is the highest priority. The highest-priority interrupt source is notified.

UF0IRID 2 to 0	LVL	Flag	Source	Reset Process
000	–	–	No interrupt source (initial value)	–
011	1	Received data error	Overrun error, parity error, framing error, break interrupt	Read UAF0LSR
010	2	Received data read request	FIFO disabled: The received data is available. FIFO enabled: Reached the Trigger level	Read RBR, or when FIFO drops below trigger level
110	2	Character timeout	At least one character is present in the receive FIFO, and no other character was placed into or read out within 4 character time.	Read RBR
001	3	Transmitted data write request	FIFO disabled: THR write enabled. FIFO enabled: The transmit FIFO data becomes empty.	Read UAF0IIR or write THR

- **UF0FMD1-0** (bits 7 to 6)
  UF0FMD1-0 indicate the FIFO mode.

UF0FMD1	**UF0FMD0**	Description
0	0	Non-FIFO mode (initial value)
0	1	Unused
1	0	Unused
1	1	FIFO mode

[Note]
These interrupt status may be hot before use. Therefore be setting ports then be clear all of these interrupt status and enable these interrupt.

14.2.5 UARTF0 Mode Register (UAF0MOD)

Address: 0F7C6H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
UAF0MODL	UF0DLAB	UF0BC	UF0PT2	UF0PT1	UF0PT0	UF0STP	UF0LG1	UF0LG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
UAF0MODH	UF0FTL1	UF0FTL0	–	–	–	UF0TFR	UF0RFR	UF0FEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UAF0MOD is a special function register (SFR) used to set the mode of the UART.

Description of Bits

- **UF0LG1-0** (bits 1 to 0)
  UF0LG1-0 specify the character length of UARTF0.

UF0LG1	UF0LG0	Description
0	0	5-bit length (initial value)
0	1	6-bit length
1	0	7-bit length
1	1	8-bit length

- **UF0STP** (bit 2)
  UF0STP selects the stop bit count of the character transmitted by UARTF0.

UF0STP	Description
0	1 stop bit (initial value)
1	1.5 stop bits (when character length = 5 bits) 2 stop bits (when character length = 6, 7, or 8 bits)

- **UF0PT2-0** (bits 5 to 3)
  UF0PT2-0 select the parity bit of UARTF0.

UF0PT2	UF0PT1	UF0PT0	Description
*	*	0	No parity bit (initial value)
0	0	1	Odd parity
0	1	1	Even parity
1	0	1	Parity bit fixed to "1"
1	1	1	Parity bit fixed to "0"

- **UF0BC** (bit 6)
  UF0BC selects the break control of UARTF0.
  Turning this to "1" brings the UARTF0 data output (TXDF0) to the spacing state (logical 0). The control by this bit is valid only on the TXDF0 pin. This means that TXDF0 is masked but the transmit operation continues internally. The use of the break control allows the CPU to send an alarm to the terminal of the computer communication system.

UF0BC	Description
0	Break control not implemented (initial value)
1	Break control implemented

- **UF0DLAB** (bit 7)
  UF0DLAB selects the access register of UAF0BUF.
  When this is "0", RBR and THR are accessible. When this is "1", DLR is accessible.

UF0DLAB	Description
0	RBR and THR of UAF0BUF are accessible (initial value)
1	DLR of UAF0BUF is accessible

- **UF0FEN** (bit 8)
  UF0FEN selects whether FIFO is enabled or disabled for UARTF0.

UF0FEN	Description
0	FIFO disabled (initial value)
1	FIFO enabled

[Note]
FIFO will be cleared when switching between FIFO enable/disable.

- **UF0RFR** (bit 9)
  UF0RFR instructs to reset the receive FIFO of UARTF0.

UF0RFR	Description
0	Receive FIFO normal operation (initial value)
1	Clears the receive FIFO

[Note]
When the receive clearance is selected, data being received is not cleared.

- **UF0TFR** (bit 10)
  UF0TFR selects to clear the transmit FIFO of UARTF0.

UF0TFR	Description
0	Transmit FIFO normal operation (initial value)
1	Clears the transmit FIFO

[Note]
When the transmit clearance is selected, data being transmitted is not cleared.

- **UF0FTL1-0** (bits 15 to 14)
  UF0FTL1-0 select the trigger level for the receive FIFO interrupt.

UF0FTL1	UF0FTL0	Description
0	0	1 byte (initial value)
0	1	2 bytes
1	0	3 bytes
1	1	4 bytes

14.2.6 UARTF0 Line Status Register (UAF0LSR)

Address: 0F7C8H
Access: R
Access size: 8/16 bits
Initial value: 0060H

	7	6	5	4	3	2	1	0
UAF0LSRL	UF0RFE	UF0TEMT	UF0THRE	UF0BI	UF0FER	UF0PER	UF0OER	UF0DR
R/W	R	R	R	R	R	R	R	R
Initial value	0	1	1	0	0	0	0	0

	15	14	13	12	11	10	9	8
UAF0LSRH	–	–	–	–	–	–	–	–
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

UAF0LSR is a special function register (SFR) used to display the status.
UAF0LSR is normally the first register read out by the CPU for determining the interrupt cause or for polling the status of the serial communication channel.
UF0OER, UF0PER, UF0FER, and UF0BI are error conditions, which generate a received data error interrupt (a LVL=1 interrupt in the IIR) if any of the states is detected. This interrupt is enabled by setting UF0ELSI of UARTF0IER to 1.

Description of Bits

- **UF0DR** (bit 0)
  UF0DR is set to 1 when the input character has been received and transmitted to RBR. This bit is cleared when the RBR data is read.

UF0DR	Description
0	No valid data in RBR (initial value)
1	There is valid data in RBR

- **UF0OER** (bit 1)
  UF0ER indicates that an overrun error occurred. The overrun error indicates that the CPU did not read the data in RBR before the next character was sent to RBR to overwrite the previous character. In FIFO mode, an overrun error occurs after the FIFO has become full when the next character is completely received. Reading UAF0LSR after an overrun error will clear the overrun error. The character during reception is overwritten instead of being transferred to FIFO. This bit is cleared when UAF0LSR is read.

UF0OER	Description
0	No overrun error (initial value)
1	Overrun error occurred

- **UF0PER** (bit 2)
  UF0PER indicates that a parity error occurred. This is enabled only when parity is enabled. This bit is cleared when UAF0LSR is read. In FIFO mode, this bit indicates that an error exists for the leading data. If a parity error occurs in the data that is not the leading data in the FIFO, it is not reflected to this bit.

UF0PER	Description
0	No parity error (initial value)
1	Parity error occurred

- **UF0FER** (bit 3)
  UF0FER indicates that a framing error occurred. A framing error indicates that there is no valid stop bit in the received character. This bit is set to "1" when the stop bit after the last data bit or after the parity bit is "0" (spacing level). This bit is cleared when UAF0LSR is read. In FIFO mode, the framing error is related to a specific character in the FIFO. This bit indicates that an error is present when that character comes to the beginning of the FIFO.

UF0FER	Description
0	No framing error (initial value)
1	Framing error occurred

- **UF0BI** (bit 4)
  UF0BI indicates that a break interrupt occurred. This bit is set to "1" when the input data is maintained in the spacing ("0") state during the transmission of one frame (start bit + data bit + parity bit + stop bit). This bit will be cleared when the CPU reads UAF0LSR. In FIFO mode, this is related to a specific character in the FIFO. This bit reflects the break interrupt state when the break character comes to the beginning of the FIFO. The CPU erases the error if the related character comes to the beginning of the FIFO before the first reading of UAF0LSR. When a break interrupt occurs, only one zero character will be loaded into the FIFO.

UF0BI	Description
0	No break interrupt (initial value)
1	Break interrupt occurred

- **UF0THRE** (bit 5)
  UF0THRE indicates that preparations have been made for calling a new character to be transmitted by the UART. This bit is set to "1" when the character is transferred from THR to the shift register for transmission (TSR). This bit is cleared to "0" by writing to THR. This bit will not be cleared by reading out the UAF0LSR register. In FIFO mode, this bit is set when the transmit FIFO is empty. This bit is cleared when one byte is written to the transmit FIFO. If the THRE interrupt is enabled by UF0ETBEI of UAF0IER, THRE initiates the third-order priority interrupt to UAF0IIR.

UF0THRE	Description
0	Transmit data still present in the THR
1	THR ready for transmission (initial value)

- **UF0TEMT** (bit 6)
  UF0TEMT is set to "1" when both THR and the shift register for transmission (TSR) are empty. When a character is loaded into THR, this bit is cleared to "0" and remains "0" until the character is transferred from TXDF0. This bit is not cleared to "0" by reading UAF0LSR.
  In FIFO mode, this bit is set to "1" when both the transmit FIFO and the shift register are empty.

UF0TEMT	Description
0	Transmitted data remains in either THR or TSR
1	Both THR and TSR are empty (initial value)

- **UF0RFE** (bit 7)
  UF0RFE is always 0 when FIFO is disabled. In the FIFO enable, this bit is set to "1" if any of parity, framing, and break interrupt data errors exists within FIFO. This bit will be cleared when the data causing the error is read out from the RBR, or when the data causing the error is cleared by the FIFO clear and then reading out the UAF0LSR.

UF0RFE	Description
0	No data error in FIFO mode (initial value)
1	A parity error, framing error, or break interrupt occurred in FIFO mode

14.2.7 UARTF0 Clock Adjustment Register (UAF0CAJ)

Address: 0F7CAH
Access: R/W
Access size: 8/16 bits
Initial value: 000DH

	7	6	5	4	3	2	1	0
UAF0CAJL	–	–	–	UF0CAJ4	UF0CAJ3	UF0CAJ2	UF0CAJ1	UF0CAJ0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	1	1	0	1

	15	14	13	12	11	10	9	8
UAF0CAJH	–	–	–	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

UAF0CAJ is a special function register (SFR) used to adjust the base clock for the baud rate clock of UARTF0.

Description of Bits

- **UF0CAJ4-0** (bits 4 to 0)
  Adjusts the base clock for the baud rate clock of UARTF0.
  Each setting of different clocks of SYSCLK is as below.

SYSCLK	UF0CAJ4	UF0CAJ3	UF0CAJ2	UF0CAJ1	UF0CAJ0
16.000MHz	0	1	1	0	1
8.000MHz					
4.000MHz					
8.192MHz	0	1	0	1	0
4.096MHz					

[Note]
When using UARTF0, always set SYSCLK to 4MHz or more. If SYSCLK is 4MHz or less, it does not work normally.
For details, see 0 "Baud rate clock generation".

14.2.8 UARTF0 Interrupt Request Register (UAF0IRQ)

Address: 0F7CCH
Access: W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
UAF0IRQL	–	–	–	–	–	–	–	UF0IRQ
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
UAF0IRQH	–	–	–	–	–	–	–	–
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

UAF0IRQ is a special function register (SFR) used to issue an interrupt request again if there is an unprocessed interrupt source.

Description of Bits

- **UF0IRQ** (bit 0)
  When there is any unprocessed interrupt source, the interrupt request is issued again by writing "1".

  [Note]
  Writing "1" to this bit while there is any unprocessed interrupt source and processing all the interrupt sources before exiting the interrupt vector will cause re-entry to the interrupt vector with no interrupt source after exiting the interrupt vector. Ensure to write "1" immediately before exiting the interrupt vector.

14.3 Description of Operation

The UART is programmed with UAF0IER, UAF0MOD, DLR(UAF0BUF), and UAF0CAJ. These registers define the character length, number of stop bits, parity, baud rate, etc.
Though the registers can be written in any order, UAF0IER needs to be written to last because it controls the interrupt enable. Once the UART is programmed to be operable, these registers can be updated any time when the UART is not transmitting or receiving data.

14.3.1 Data Transmission

Figure 14-2 shows the transmission timing.

Writing data to THR will transfer the contents through the transmit FIFO to the transmit shift register. Within 16 baud rate clocks after the THRE bit rise is detected, the start bit is sent, followed by the data one bit at a time from the least significant bit. When the data to be transmitted is 7-bit, the most significant bit will not be sent.
If parity is enabled by UF0PT2-0 of UAF0MOD, then the parity bit is sent. This is followed by the stop bit which indicates the end of transmitting one frame of data.
After the data is transmitted, the UF0THRE bit of UAF0LSR is set to "1" to indicate that it is ready for the next transmission. This bit is cleared when one byte is written to the transmit FIFO. Also, if the THRE interrupt is enabled by UF0ETBEI of UAF0IER, THRE initiates a LVL=3 interrupt to UAF0IIR. If THRE is the interrupt source indicated in UAF0IR, this bit is cleared by reading the UAF0IIR register.

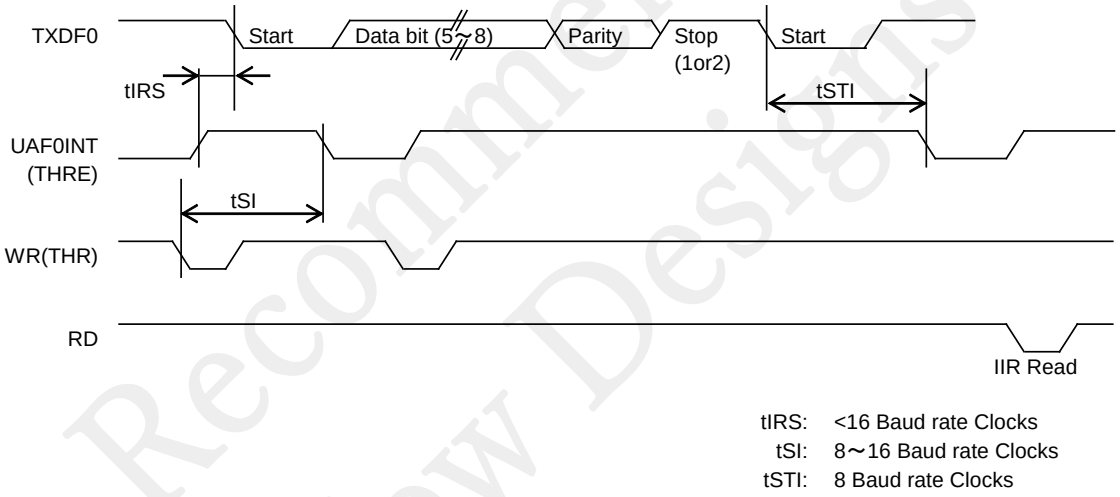


Figure 14-2 Transmission Timing

[Note]
Even if the Transmit FIFO is empty, some transition processing might not be completed.
Before stop the high-speed clock (shift to STOP, DEEP-HALT, HALT-H), confirm the transmit shift register (TSR) becomes empty by UF0TEMT of UAF0LSR register first.
And then wait for 1.5bit transmission time regardless of the setting of Parity and Stop bit.

14.3.2 Data Reception

Figure 14-4 shows the reception timing. Figure 14-5 shows the timing when the first byte in the receive FIFO is read, and Figure 14-6 the reception timing when the remaining bytes in the receive FIFO are read.

The sampling clock is obtained by dividing the baud rate clock by 8.
First, when the start bit is detected from RXDF0, subsequent data is obtained and transferred to the receive shift register. The data in the receive shift register is transferred to RBR through the receive FIFO.
When the data reaches RBR, UF0DR of UAF0LSR is set to "1" to indicate there is valid data in RBR. This bit is cleared by reading the data in RBR.

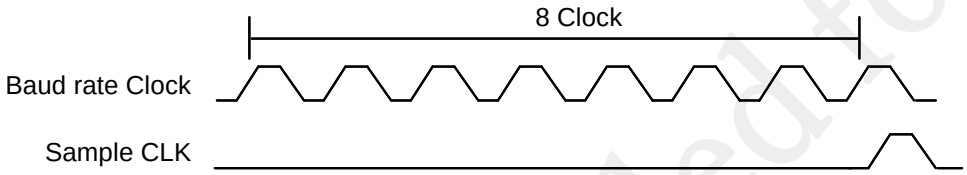


Figure 14-3 Relation between Baud Rate Clock and Sample CLK

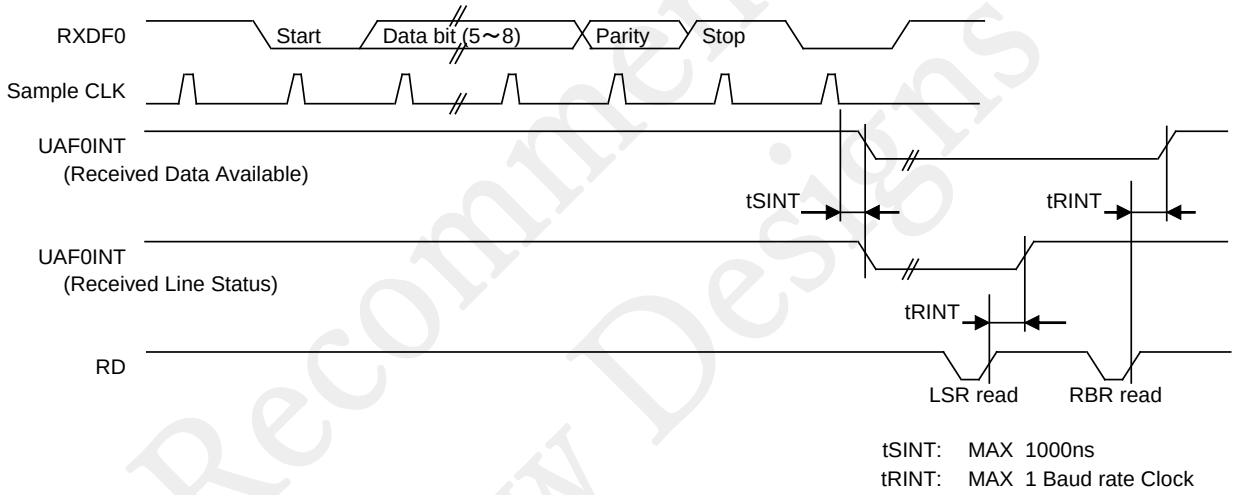


Figure 14-4 Reception Timing

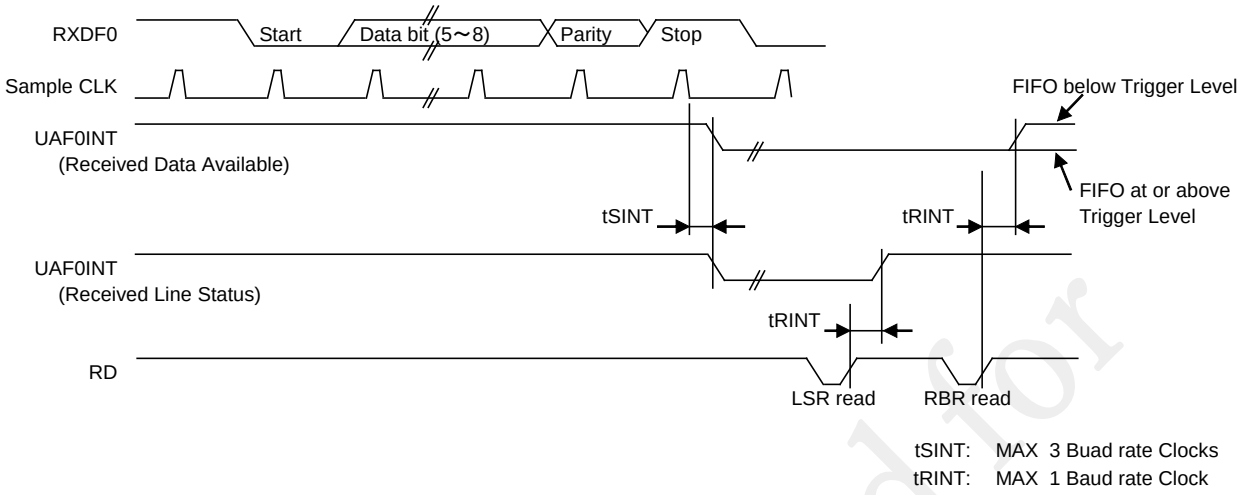


Figure 14-5 First Byte of Receive FIFO (Set RBR)

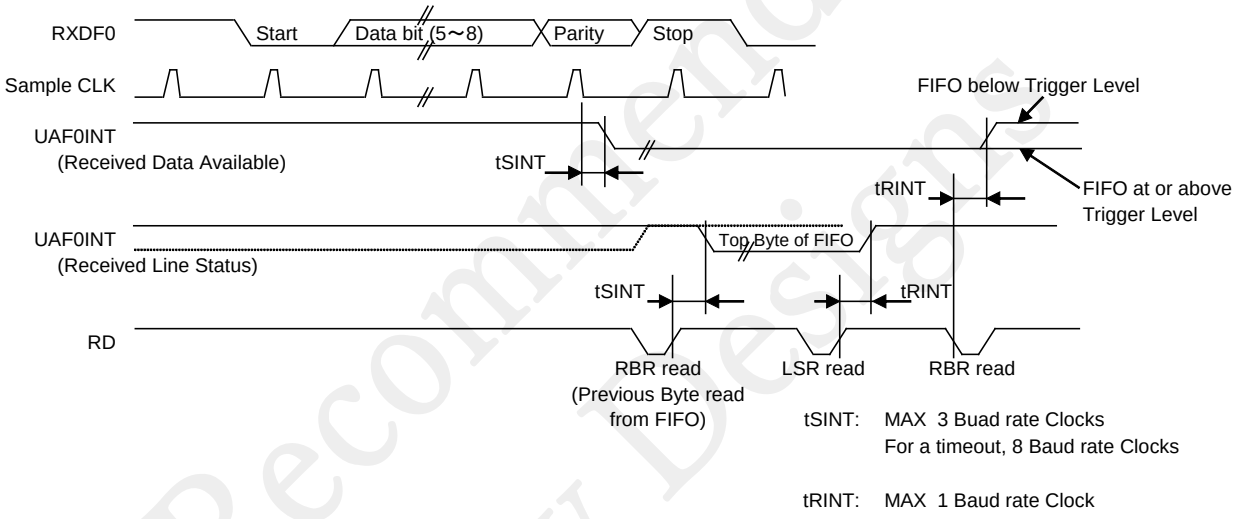


Figure 14-6 Remaining Bytes in Receive FIFO

14.3.3 Baud Rate Clock Generation

A baud rate is obtained by the following expression:

Baud rate frequency = SYSCLK x (UAF0CAJ-1)/UAF0CAJ/(DLR[15:0] x 16)

Although actually available baud rate for communication depends on the software processing, a 115200bps baud rate can be used for communication with the DLR=8 setting in an ideal state of 16MHz SYSCLK.
Make sure that the margin of error between the actual and set baud rates is within a few percent.

[Note]
Divisor (DLR[15:0]) cannot be set to 1. Set a value of 0 (stop) or greater than 2.

The following table shows the relation among SYSCLK, DLR, and baud rates.

Baud rate (bps)	SYSCLK	DLR (Hex)	error*1 (%)
2400	16MHz	0181	0.09 to 0.10
4800		00C0	-0.16
9600		0060	-0.16
19200		0030	-0.16
38400		0018	-0.16
57600		0010	-0.18 to 0.08
115200		0008	-0.21 to 0.08

*1: The error does not include the clock error. User this in consideration of an error of SYSCLK.

14.3.4 FIFO Mode

When the receive FIFO and reception interrupt are both enabled, reception interrupts are generated as follows:

(A) If the number of characters present within the FIFO exceeds the programmed trigger level, a received data read request interrupt is generated. This interrupt is immediately cleared when the number of characters present within the FIFO drops below the trigger level.

(B) As with the received data read request interrupt, the UAnIIR received data read request display is set to "1" if the number of characters present within the FIFO exceeds the trigger level, and cleared to "0" if it drops below the trigger level.

(C) The received data error interrupt has a higher priority than the received data read request interrupt.

(D) The received data read request flag is set to "1" as soon as the data is transferred from the receive shift register to the FIFO, and cleared to "0" when the FIFO becomes empty.

When the receive FIFO and the reception interrupt are both enabled, a character timeout interrupt is generated as follows.

(A) A character timeout interrupt is generated when the following conditions are met.

- There is at least one character present in the FIFO.
- An amount of time required to transfer at least 4 characters has elapsed since a character was last received (if 2 stop bits are specified, the time after the first stop bit is calculated).
- An amount of time required to transfer at least 4 characters has elapsed since the receive FIFO was last read.

For example, if 1 start bit + 8 character bits + 1 parity bit + 2 stop bits is specified, and the transfer speed is 300 baud, the said amount of time will be approximately 160 ms.

(B) SYSCLK is used to calculate the character time.

(C) When a character is read out from the FIFO, the character timeout interrupt and the timer used for timeout detection will be cleared.

(D) When no character timeout interrupt is generated, the timeout detection timer will be cleared when a character is read out from the FIFO or a new character is received.

The transmission interrupt is generated as follows when the transmitter section and the transmit FIFO interrupts have been enabled.

(A) If the transmit FIFO is empty, a transmitted data write request interrupt occurs. This interrupt is cleared when a character is written to the transmit FIFO or when UAnIIR is read out.

(B) When the following conditions are met, the transmitted data write request interrupt will be delayed for an amount of time equivalent to "time required to transmit one character – time when last stop bit occurred".

- There was a period when only one character was present in the FIFO after THRE (transmitted data write request) was last set.
- THRE was set.

[Note]
Even if the Transmit FIFO is empty, some transition processing might not be completed.
Before stop the high-speed clock (shift to STOP, DEEP-HALT, HALT-H), confirm the transmit shift register (TSR) becomes empty by UF0TEMT of UAF0LSR register first.
And then wait for 1.5bit transmission time regardless of the setting of Parity and Stop bit.

14.3.5 FIFO Polled Mode

If FIFO is enabled and UF0ELSI, UF0ETBEI, and UF0ERBFI of UAF0IER are "0", the UART operates in the FIFO polled mode. Since the receiver section and transmitter section can be controlled separately, either one (or both) can be set to FIFO polled mode. In FIFO polled mode, the states of the receiver and transmitter sections must be checked by reading out the UAnLSR (since no interrupt is generated).

- A state in which at least one character is present in the receive FIFO can be confirmed by the value "1" set to UF0DR.
- When UF0PER is cleared to "0", an interrupt will not be generated even if an error is detected while receiving a character. The error state will not be indicated on the UAF0IIR value. Therefore, the error type must be checked with the UF0BI, UF0FER, UF0PER, and UF0OER values.
- It can be known that the transmit FIFO is empty by the fact that UF0THRE has been set to "1".
- A state in which the transmit FIFO and transmit shift register are both empty can be confirmed by the value "1" set to UF0TEMT.
- A state in which the character associated with an error at the time of reception is present in the receive FIFO can be confirmed by the value "1" set to UF0RFE.

In FIFO polled mode, FIFO will operate; however, trigger level and timeout detection will not be performed (since they are only notified by interrupts).

14.3.6 Error Status

(a) Overrun error

An overrun error indicates that the data in RBR was not read before the next character was sent to RBR to overwrite the previous character.
At this time, UF0OER of UAF0LSR is set.

(b) Parity error

A parity error indicates that the parity of the received data and the received parity bit did not match. At this time, UF0PER of UAF0LSR is set.
Note that, this error will only occur when parity is enabled.
In FIFO mode, this bit indicates that an error exists for the leading data. If a parity error occurs in the data that is not the leading data in the FIFO, it is not reflected to UF0PER of UAF0LSR.

(c) Framing error

A framing error indicates that there is no valid stop bit in the received character. This error will occur when the stop bit after the last data bit or after the parity bit is "0" (spacing level).
At this time, UF0FER of UAF0LSR is set.
In FIFO mode, this is related to a specific character in the FIFO. UF0FER indicates that an error is present when that character comes to the beginning of the FIFO.

(d) Break interrupt

A break interrupt indicates that the input data received was maintained in the spacing ("0") state during the transmission of one frame (start bit + data bit + parity bit + stop bit).
At this time, UF0BI of the UAF0LSR register is set.
In FIFO mode, this is related to a specific character in the FIFO. UF0BI indicates that the break character is present at the beginning of the FIFO.

14.3.7 Reset By Block Control Register

If using DUAF0 bit of BLKCON23 register as block reset, a sequence is the following:

1) Set DUAF0 bit to 1.
   If it is in the UARTF is transmission state, the TXD output will become indetermination.
2) Set DUAF0 bit to 0 again. The block reset is completed in this time. When reset is completed, TXD becomes H.
3) Place 2 blanks (for example 2 NOP instructions), before a next instruction to access to some registers of this block.

Chapter 15

I^2C Bus Interface

15 I²C Bus Interface

15.1 General Description

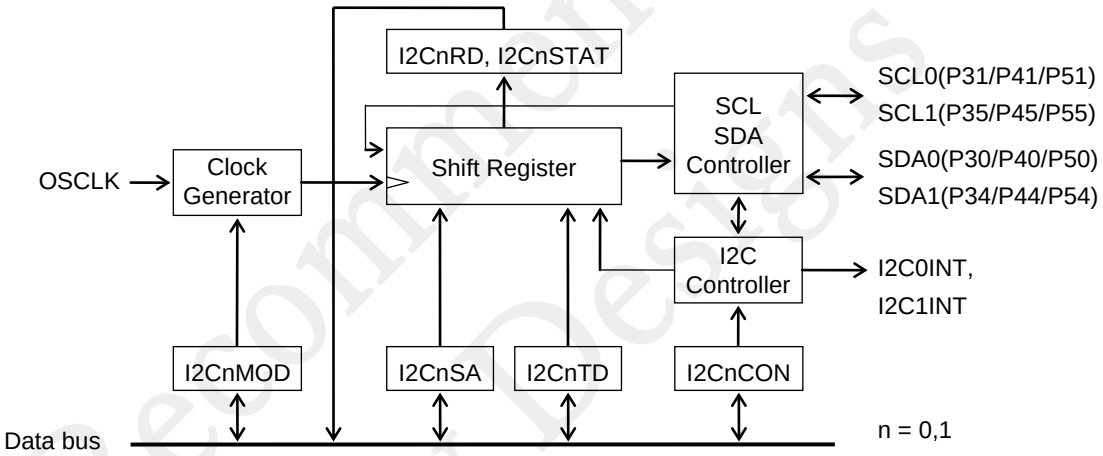
The I²C bus interface operates as the master device of I²C bus and can communicate with the slave device.
This LSI includes two channels of I²C bus interface.
The I²C bus interface data I/O pin and the I²C bus interface clock I/O pin are assigned as the secondary function of the ports 3, 4, and 5. For the ports 3, 4, and 5, see Chapter 20 “Port 3”, Chapter 21 “Port 4”, and Chapter 22 “Port 5”.

15.1.1 Features

- Master function (Multi-master, stretch is not supported)
- Communication speeds supported include standard mode (100kbps) and fast mode (400kbps).
- 7-bit address format (10-bit address can be supported)

15.1.2 Configuration

Figure 15-1 shows the configuration of the I²C bus interface.



I2CnRD : I²C bus n receive data register
I2CnSA : I²C bus n slave address register
I2CnTD : I²C bus n transmit data register
I2CnCON : I²C bus n control register
I2CnMOD : I²C bus n mode register
I2CnSTAT : I²C bus n status register

Figure 15-1 Configuration of I²C Bus Interface

15.1.3 List of Pins

Pin name	I/O	Function
SDAn	I/O	I²C bus interface data I/O pin
SCLn	I/O	I²C bus interface clock I/O pin

15.2 Description of Registers

15.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F740	I^2C bus 0 receive data register	I2C0RD	–	R	8	00
0F742	I^2C bus 0 slave address register	I2C0SA	–	R/W	8	00
0F744	I^2C bus 0 transmit data register	I2C0TD	–	R/W	8	00
0F746	I^2C bus 0 control register	I2C0CON0	I2C0CON	R/W	8/16	00
0F747		I2C0CON1		R/W	8	00
0F748	I^2C bus 0 mode register	I2C0MODL	I2C0MOD	R/W	8/16	00
0F749		I2C0MODH		R/W	8	02
0F74A	I^2C bus 0 status register	I2C0STAL	I2C0STA	R	8/16	00
0F74B		I2C0STAH		R	8	00
0F750	I^2C bus 1 receive data register	I2C1RD	–	R	8	00
0F752	I^2C bus 1 slave address register	I2C1SA	–	R/W	8	00
0F754	I^2C bus 1 transmit data register	I2C1TD	–	R/W	8	00
0F756	I^2C bus 1 control register	I2C1CON0	I2C1CON	R/W	8/16	00
0F757		I2C1CON1		R/W	8	00
0F758	I^2C bus 1 mode register	I2C1MODL	I2C1MOD	R/W	8/16	00
0F759		I2C1MODH		R/W	8	02
0F75A	I^2C bus 1 status register	I2C1STAL	I2C1STA	R	8/16	00
0F75B		I2C1STAH		R	8	00

15.2.2 I²C Bus n Receive Data Register (I2CnRD : n=0,1)

Address: 0F740H(I2C0RD), 0F750H(I2C1RD)
Access: R
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2CnRD	I2nR7	I2nR6	I2nR5	I2nR4	I2nR3	I2nR2	I2nR1	I2nR0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

I2CnRD is a read-only special function register (SFR) to store the received data.
I2CnRD is updated after completion of each reception.

Description of Bits

- **I2nR7-0** (bits 7 to 0)
  The I2nR7-0 bits are used to store the received data. The signal input to the SDA pin is received at transmission of a slave address and at data transmission/reception in sync with the rising edge of the signal on the SCL pin. Since data that has been output to the SDA and SCL pins is received not only at data reception but also at slave address data transmission and data transmission, it is possible to check whether transmit data has certainly been transmitted.

15.2.3 I²C Bus n Slave Address Register (I2CnSA : n=0,1)

Address: 0F742H(I2C0SA), 0F752H(I2C1SA)
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2CnSA0	I2nA6	I2nA5	I2nA4	I2nA3	I2nA2	I2nA1	I2nA0	I2nRW
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2CnSA is a special function register (SFR) to set the address and the transmit/receive mode of the slave device.

Description of Bits

- **I2nRW** (bit 0)
  The I2nRW bit is used to select the data transmit mode (write) or data receive mode (read).

I2nRW	Description
0	Data transmit mode (initial value)
1	Data receive mode

- **I2nA6-0** (bits 7 to 1)
  The I2nA6-0 bits are used to set the address of the communication partner.

15.2.4 I²C Bus n Transmit Data Register (I2CnTD : n=0,1)

Address: 0F744H(I2C0TD), 0F754H(I2C1TD)
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
I2CnTD0	I2nT7	I2nT6	I2nT5	I2nT4	I2nT3	I2nT2	I2nT1	I2nT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2CnTD is a special function register (SFR) used to set the transmitted data.

Description of Bits

- **I2nT7-0** (bits 7 to 0)
  The I2nT7-0 bits are used to set the transmit data.

15.2.5 I²C Bus n Control Register (I2CnCON : n=0,1)

Address: 0F746H(I2C0CON0/I2C0CON), 0F747H(I2C0CON1),
0F756H(I2C1CON0/I2C1CON), 0F757H(I2C1CON1)
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
I2CnCON0	I2nACT	–	–	–	–	I2nRS	I2nSP	I2nST
R/W	R/W	R/W	R/W	R/W	R/W	W	W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
I2CnCON1	–	–	–	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

I2CnCON is a special function register (SFR) to control transmit and receive operations.

Description of Bits

- **I2nST** (bit 0)
  The I2nST bit is used to control the communication operation of the I²C bus interface. When the I2nST bit is set to "1", communication starts. When "1" is overwritten to the I2nST bit in a control register setting wait state after transmission/reception of acknowledgment, communication restarts. When the I2nST bit is set to "0", communication is stopped forcibly.
  The I2nST bit can be set to "1" only when the I²C bus interface is in an operation enable state (I2nEN = "1").
  When the I2nSP bit is set to "1", the I2nST bit is set to "0".

I2nST	Description
0	Stops communication (initial value)
1	Start communication

- **I2nSP** (bit 1)
  The I2nSP bit is a write-only bit used to request a stop condition. When the I2nSP bit is set to "1", the bus shifts to the stop condition and communication stops. When the I2nSP bit is read, "0" is always read.

I2nSP	Description
0	No stop condition request (initial value)
1	Stop condition request

- **I2nRS** (bit 2)
  The I2nRS bit is a write-only bit used to request a restart. When this bit is set to "1" during data communication, the I^2C bus shifts to the restart condition and communication restarts from the slave address. I2nRS can be set to "1" only while communication is active (I2nST ="1"). When the I2nRS bit is read, "0" is always read.

I2nRS	Description
0	No restart request (initial value)
1	Restart request

- **I2nACT** (bit 7)
  The I2nACT bit is used to set the acknowledge signal to be output at completion of reception.

I2nACT	Description
0	Acknowledgment data "0" (initial value)
1	Acknowledgment data "1"

15.2.6 I²C Bus n Mode Register (I2CnMOD : n=0,1)

Address: 0F748H(I2C0MODL/I2C0MOD), 0F749H(I2C0MODH),
0F758H(I2C1MODL/I2C1MOD), 0F759H(I2C1MODH)
Access: R/W
Access size: 8/16 bits
Initial value: 0200H

	7	6	5	4	3	2	1	0
I2CnMODL	–	–	–	–	I2nDW1	I2nDW0	I2nMD	I2nEN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
I2CnMODH	–	–	–	–	–	–	I2nCD1	I2nCD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	1	0

*) I2CnMODH can always read “00H” at the time of I2CnEN=0
I2CnMOD is a special function register (SFR) used to set the operation mode.

Description of Bits

- **I2nEN** (bit 0)
  The I2nEN bit is used to enable the operation of the I²C bus interface. Only when I2nEN is “1”, the I2nST bit can be set and the I2Cn bus becomes available. When I2nEN is set to “0”, all the SFRs related to I²C bus n (I2CnMODH register is excluded) are initialized.

I2nEN	Description
0	Stops I²C operation (initial value)
1	Enables I²C operation

[Note]
Setting ports should be completed before setting I2nEN to “1”.

- **I2nMD** (bit 1)
  The I2nMD bit is used to set the communication speed of the I²C bus interface. Standard mode or fast mode can be selected. The communication speed varies depending on the setting value of the SYSC2, SYSC1, and SYSC0 bits of the frequency control register (FCON0). For details, see “Table 15-1 Relationship between OSCLK and Communication Speeds”.

I2nMD	Description
0	Standard mode (initial value)/100 kbps
1	Fast mode/400 kbps

[Note]
This is set so that the communication speed becomes 100kbps/400kbps when the operating frequency of I²C is 4MHz. Set the operating frequency of I²C in I2nCD0 and I2nCD1.

- **I2nDW1-0** (bits 3 to 2)
  The I2nDW1-0 bits are used to set the communication speed reduction rate of the I^2C bus interface. Set this bit so that the communication speed does not exceed 100kbps/400kbps.

I2nDW1	I2nDW0	Description
0	0	No communication speed reduction (initial value)
0	1	10% communication speed reduction
1	0	20% communication speed reduction
1	1	30% communication speed reduction

- **I2nCD1-0** (bits 9 to 8)
  The I2nCD1-0 bits are used to set the operating frequency of I^2C. Set a frequency division value of OSCLK. Make sure that the clock input to I^2C is 4MHz or less. Proper operation cannot be guaranteed if the frequency division value exceeds 4MHz. Table 15-1 shows the relationship between the setting values of OSCLK, I2nCD1, and I2nCD0 and the communication speed.

I2nCD1	I2nCD0	Description
0	0	OSCLK
0	1	1/2OSCLK
1	0	1/4OSCLK (initial value)
1	1	Setting prohibited

Table 15-1 Relationship between OSCLK and Communication Speeds

OSCLK	I2nCD1	I2nCD0	I2C operating frequency	Standard mode	Fast mode
16MHz	0	0	Setting prohibited	–	–
	0	1	Setting prohibited	–	–
	1	0	4MHz	100kbps	400kbps
	1	1	Setting prohibited	–	–
8MHz	0	0	Setting prohibited	–	–
	0	1	4MHz	100kbps	400kbps
	1	0	2MHz	50kbps	200kbps
	1	1	Setting prohibited	–	–
4MHz	0	0	4MHz	100kbps	400kbps
	0	1	2MHz	50kbps	200kbps
	1	0	1MHz	25kbps	100kbps
	1	1	Setting prohibited	–	–

[Note]
Do not change this bit during I^2C communication. Operation is not guaranteed if it is changed.

15.2.7 I²C Bus n Status Register (I2CnSTAT : n=0,1)

Address: 0F74AH(I2C0STAL/I2C0STAT), 0F74BH(I2C0STAH)
0F75AH(I2C1STAL/I2C1STAT), 0F75BH(I2C1STAH)
Access: R
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
I2CnSTAL	–	–	–	–	–	I2nER	I2nACR	–
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
I2CnSTAH	–	–	–	–	–	–	–	–
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

I2CnSTAT is a read-only special function register (SFR) to indicate the state of the I²C bus interface.

Description of Bits

- **I2nACR** (bit 1)
  The I2nACR bit is used to store the acknowledgment signal received. Acknowledgment signals are received each time the slave address is received and data transmission or reception is completed. The I2nACR bit is set to "0" when the I2nEN bit of I2CnMOD is "0".

I2nACR	Description
0	Receives acknowledgment "0" (initial value)
1	Receives acknowledgment "1"

- **I2nER** (bit 2)
  The I2nER bit is a flag to indicate a transmit error. When the value of the bit transmitted and the value of the SDA pin do not coincide, this bit is set to "1". The SDA pin output continues until the subsequent byte data communication terminates, even if the I2nER bit is set to "1".
  The I2nER bit is set to "0" when a write operation to I2CnCON is performed. The I2nER bit is set to "0" when the I2nEN bit of I2CnMOD is set to "0".

I2nER	Description
0	No transmit error (initial value)
1	Transmit error

15.3 Description of Operation

15.3.1 Communication Operation Mode

Communication is started when communication mode is selected by using the I²C bus n mode register (I2CnMOD), the I²C function is enabled by using the I2nEN bit, a slave address and a data communication direction are set in the I²C bus n slave address register (I2CnSA), and "1" is written to the I2nST bit of the I²C bus n control register (I2CnCON).

15.3.1.1 Start Condition

When "1" is written to the I2nST bit of the I²C bus n control register (I2CnCON) while communication is stopped (the I2nST bit is "0"), communication is started and the start condition waveform is output to the SDA and SCL pins.
After execution of the start condition, the LSI shifts to the slave address transmit mode.

15.3.1.2 Restart Condition

When "1" is written to the I2nRS and I2nST bits of the I²C bus n control register (I2CnCON) during communication (the I2nST bit is "0"), the restart condition waveform is output to the SDA and SCL pins.
After execution of the restart condition, the LSI shifts to the slave address transmit mode.

15.3.1.3 Slave Address Transmit Mode

In slave address transmit mode, the values (slave address and data communication direction) of the I²C bus n slave address register (I2CnSA) are transmitted in MSB first, and finally, the acknowledgment signal is received in the I2nACR bit of the I²C bus n status register (I2CnSTAT).
At completion of acknowledgment reception, the LSI shifts to the I²C bus n control register (I2CnCON) setting wait state (control register setting wait state).
The value of I2CnSA output from the SDA pin is stored in I2CnRD.

15.3.1.4 Data Transmit Mode

In data transmit mode, the value of I2CnTD is transmitted in MSB first, and finally, the acknowledgment signal is received in the I2nACR bit of the I²C bus n status register (I2CnSTAT).
At completion of acknowledgment reception, the LSI shifts to the I²C bus n control register (I2CnCON) setting wait state (control register setting wait state).
The value of I2CnTD output from the SDA pin is stored in I2CnRD.

15.3.1.5 Data receive mode

In data receive mode, the value input in the SDA pin is received synchronously with the rising edge of the serial clock output to the SCL pin, and finally, the value of the I2nACT bit of the I²C bus n control register (I2CnCON) is output.
At completion of acknowledgment transmission, the LSI shifts to the I²C bus n control register (I2CnCON) setting wait state (control register setting wait state).
The data received is stored in I2CnRD after the acknowledgment signal is output. The acknowledgment signal output is received in the I2nACR bit of the I²C bus n status register (I2CnSTAT).

15.3.1.6 Control Register Setting Wait State

When the LSI shifts to the control register setting wait state, an I^2C bus n interface interrupt (I2CnINT) is generated.
In the control register setting wait state, the transmit error flag (I2nER) of the I^2C bus n status register (I2CnSTAT) and acknowledgment receive data (I2nACR) are confirmed and at data reception, the contents of I2CnRD are read in the CPU and the next operation mode is selected.
When "1" is written to the I2nST bit in the control register setting wait state, the LSI shifts to the data transmit or receive mode. When "1" is written to the I2nSP bit, the LSI shifts to the stop condition. When "1" is written to the I2nRS bit, the LSI shifts to the restart condition.

15.3.1.7 Stop Condition

In the stop condition, the stop condition waveform is output to the SDA and SCL pins. After the stop condition waveform is output, an I^2C bus n interface interrupt (I2CnINT) is generated.

15.3.2 Communication Operation Timing

Figures 15-2 to 15-4 show the operation timing and control method for each communication mode.

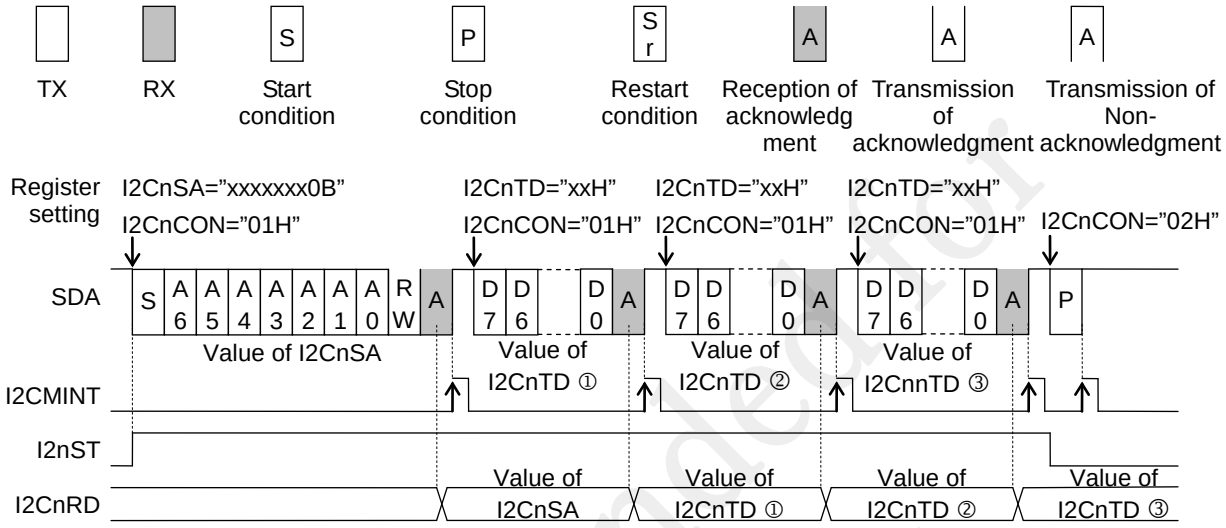


Figure 15-2 Operation Timing in Data Transmit Mode (Write)

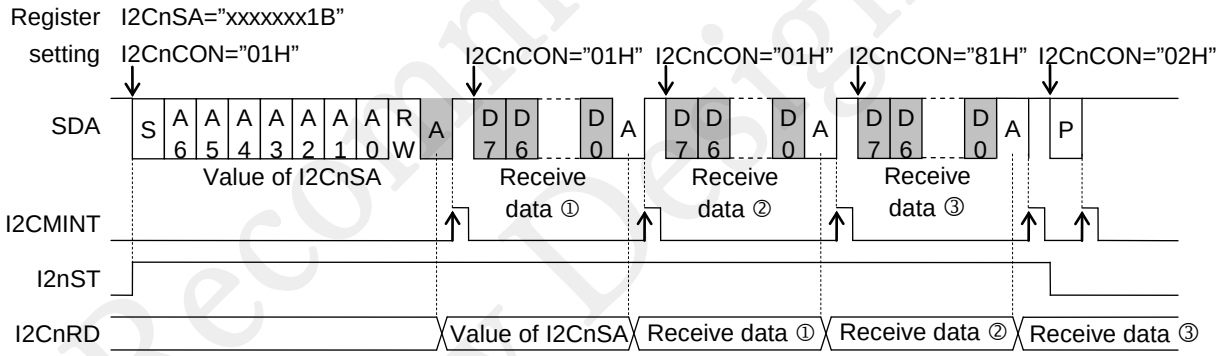


Figure 15-3 Operation Timing in Data Receive Mode (Read)

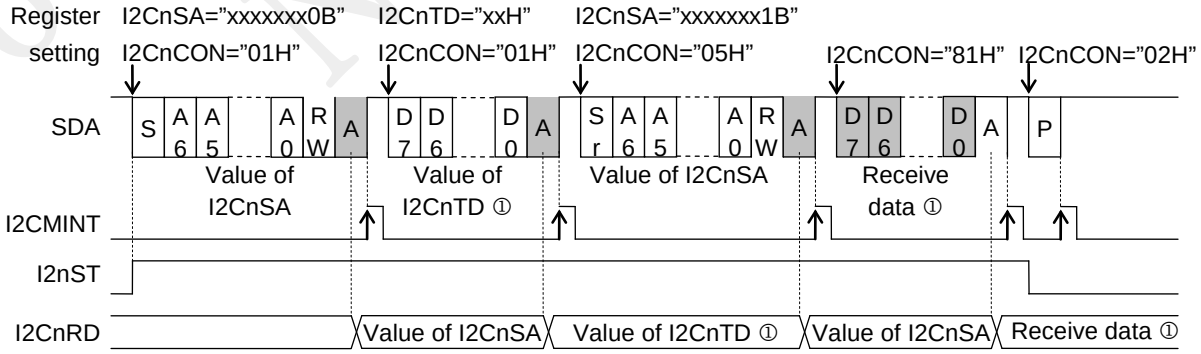


Figure 15-4 Operation Timing at Data Transmit/Receive Mode (Write/Read) Switching

Figure 15-5 shows the operation timing and control method when an acknowledgment error occurs.

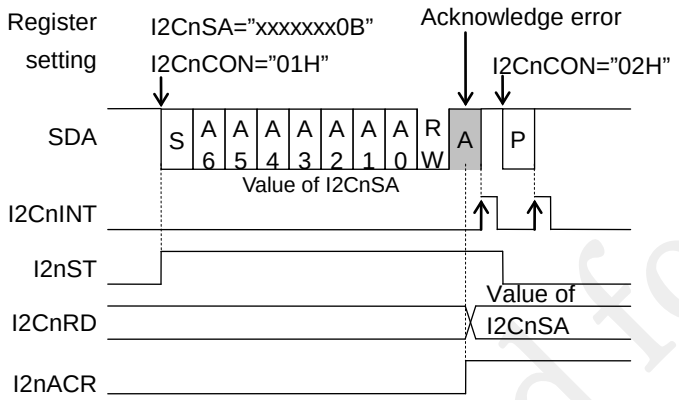


Figure 15-5 Operation Suspend Timing at Occurrence of Acknowledgment Error

When the values of the transmitted bit and the SDA pin do not coincide, the I2nER bit of the I²C bus n status register (I2CnSTAT) is set to "1" and the SDA pin output is disabled until termination of the subsequent byte data communication.
Figure 15-6 shows the operation timing and control method when transmission fails.

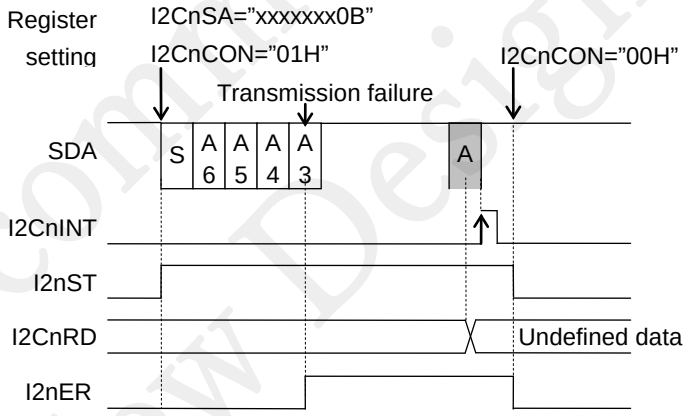


Figure 15-6 Operation Timing When Transmission Fails

15.3.3 Operation Waveforms

Figure 15-7 shows the operation waveforms of the SDA and SCL signals. Table 15-2 shows the relationship between communication speeds and 1/m OSCLK clock counts.

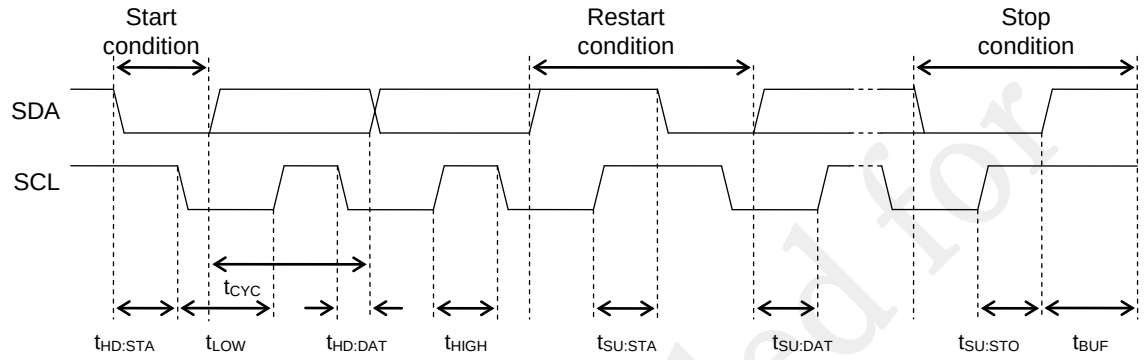


Figure 15-7 Operation Waveforms of SDA and SCL Signals

Table 15-2 Relationship between Communication Speeds and OSCLK Clock Counts

Communication speed (I2nSP)	Speed reduction (I2nDW1,0)	t_{CYC}	$t_{HD:STA}$	t_{LOW}	$t_{HD:DAT}$	t_{HIGH}	$t_{SU:STA}$	$t_{SU:DAT}$	$t_{SU:STO}$	t_{BUF}
Standard mode 100kbps	No reduction	40φ	18φ	22φ	4φ	18φ	22φ	18φ	18φ	22φ
	10% reduction	44φ	20φ	24φ	4φ	20φ	24φ	20φ	20φ	24φ
	20% reduction	48φ	22φ	26φ	4φ	22φ	26φ	22φ	22φ	26φ
	30% reduction	52φ	24φ	28φ	4φ	24φ	28φ	24φ	24φ	28φ
Fast mode 400kbps	No reduction	10φ	4φ	6φ	2φ	4φ	6φ	4φ	4φ	6φ
	10% reduction	11φ	4φ	7φ	2φ	4φ	7φ	5φ	4φ	7φ
	20% reduction	12φ	5φ	7φ	2φ	5φ	7φ	5φ	5φ	7φ
	30% reduction	13φ	5φ	8φ	2φ	5φ	8φ	6φ	5φ	8φ

φ: Clock cycle of 1/m OSCLK
m: Depends on the setting of the I2nCD1 and I2nCD0 bits of the I2CnMOD register.

[Note]
The 1/m OSCLK clock count is set so that the communication speed may be set to 100 kbps/400kbps when 1/m OSCLK is 4MHz.

15.3.4 Pin Settings

To enable the I^2C function, the applicable bit of each related port register needs to be set. See Chapter 20, "Port 3", Chapter 21, "Port 4", and Chapter 22, "Port 5" for details about the port registers.
For SCLn and SDAn, the ports can be selected from several possibilities.
Be sure to select one of the following combinations of ports for SCL/SDA.

	I^2C pin	Combination 1	Combination 2	Combination 3
I^2C0	SCL0,SDA0	P31,P30	P41,P40	P51,P50
I^2C1	SCL1,SDA1	P35,P34	P45,P44	P55,P54

Moreover, being able to select as a port is only in one port.

Chapter 16

Port XT

16 Port XT

16.1 General Description

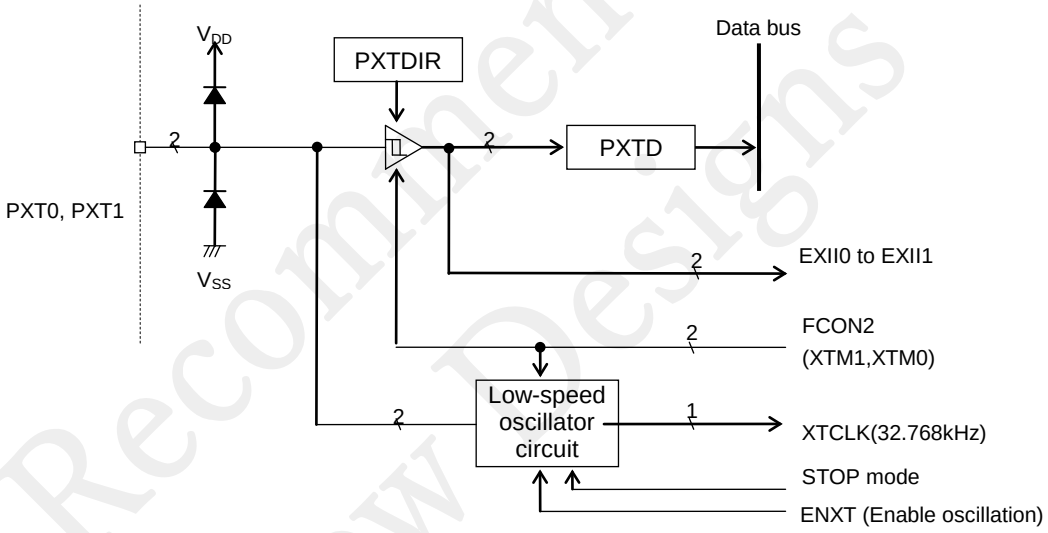
This LSI includes a 2-bit input port, port XT (PXT0, PXT1).
It can function as an external interrupt input, a low-speed crystal oscillation pin, or an external clock input pin.
When it is used as a low-speed crystal oscillation pin, the PXT1 pin functions as an output pin if the crystal oscillation mode is selected with the XTM1 to XTM0 bits of the FCON2 register. For details of the FCON2 register, low-speed crystal oscillation, and external clock input, see Chapter 6, "Clock Generation Circuit".

16.1.1 Features

- Can be used as a high-impedance input.
- Can be used as an external interrupt pin (EXII0 to EXII1), a low-speed crystal oscillation pin, or an external clock input pin.

16.1.2 Configuration

Figure 16-1 shows the configuration of the port XT.



PXTD : Port XT data register
PXTDIR : Port XT direction register

Figure 16-1 Configuration of Port XT

16.1.3 List of Pins

Pin name	I/O	Primary function
PXT0/EXII0/XT0	I	Input port, External interrupt pin Low-speed crystal oscillation pin
PXT1/EXII1/XT1/ LSCLKI	I/O	Input port, External interrupt pin Low-speed crystal oscillation pin, External low-speed clock input pin

16.2 Description of Registers

16.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F208	Port XT data register	PXTD	–	R	8	Depends on pin state
0F209	Port XT direction register	PXTDIR	–	R/W	8	00

16.2.2 Port XT Data Register (PXTD)

Address: 0F208H
Access: R
Access size: 8 bits
Initial value: Depends on pin state

	7	6	5	4	3	2	1	0
PXTD	–	–	–	–	–	–	PXT1D	PXT0D
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	x	x

PXTD is a read-only special function register (SFR) used to read the input level of the port XT pin.

Description of Bits

- **PXT1-0D** (bits 1 to 0)
  The PXT1-0D bits are used to read the input level of the port XT pin.

PXT1D	Description
0	Input level of the PXT1 pin: “L”
1	Input level of the PXT1 pin: “H”

PXT0D	Description
0	Input level of the PXT0 pin: “L”
1	Input level of the PXT0 pin: “H”

16.2.3 Port XT Direction Register (PXTDIR)

Address: 0F209H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
PXTDIR	–	–	–	–	–	–	–	PXT01DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

PXTD is a special function register (SFR) used to enable the input port function of the port XT pin.

Description of Bits

- **PXT01DIR** (bit 0)
  The PXTDIR bit is used to enable the input port function of the port XT pin.

PXT01DIR	Description
0	Input port function of the PXT0 and PXT1 pins disabled (initial value)
1	Input port function of the PXT0 and PXT1 pins enabled

[Note]
If the input port function is enabled in this bit, both the PXT0 and PXT1 pins can be used as input port function.
These pins do not have the pull-up/pull-down function. If only one of them is used, fix the unused pin to V_{DD} or Vss outside the LSI.

16.3 Description of Operation

16.3.1 Input Port Function

In the initial state after system reset, input is disabled for both the pins of the port XT.
When the pins of the port XT are set to the input state by the port XT direction register (PXTDIR), their input level can be read by reading the port XT data register (PXTD).

16.3.2 Primary Function Other Than Input Port

The low-speed crystal oscillation pin, external clock input pin, or external interrupt is assigned to the port XT as the primary function other than the input port.
When the XTM1 and XTM0 bits of the frequency control register 0 (FCON2) are set to the crystal oscillation mode, the low-speed crystal oscillation mode or the external clock input mode is selected.
In the low-speed crystal oscillation mode, both the PXT0 and PXT1 pins are used as the pins for crystal oscillation.
In the external clock input mode, the PXT1 pin is used as the input pin of the external clock. In this case, the PXT0 pin is in the input-disabled state.
To use the port XT as the low-speed crystal oscillation pin or the external clock input pin, set the appropriate port to the input port disabled state.
To use the port XT as the external interrupt input (EXII0 to EXII1), set the appropriate port to the input port enabled state, and configure the setting to use the port as the external interrupt with the external interrupt mode register (EXI01SEL).

	PXTDIR setting	FCON2 setting	PXT0 pin	PXT1 pin
Crystal oscillation	0	1	Crystal oscillation	Crystal oscillation
External clock	0	3	Input disabled	External clock input
Input port/ External Interrupt	1	2	General-purpose input pin/ External Interrupt	General-purpose input pin/ External Interrupt

Chapter 17

Port 0

17 Port 0

17.1 Overview

This LSI includes Port 0 (P00 to P05), which is a 6-bit input/output port.
These ports can also be used as the SA-ADC, RC-ADC, SSIO, UART, FTM output pins.
See the following chapters for reference:

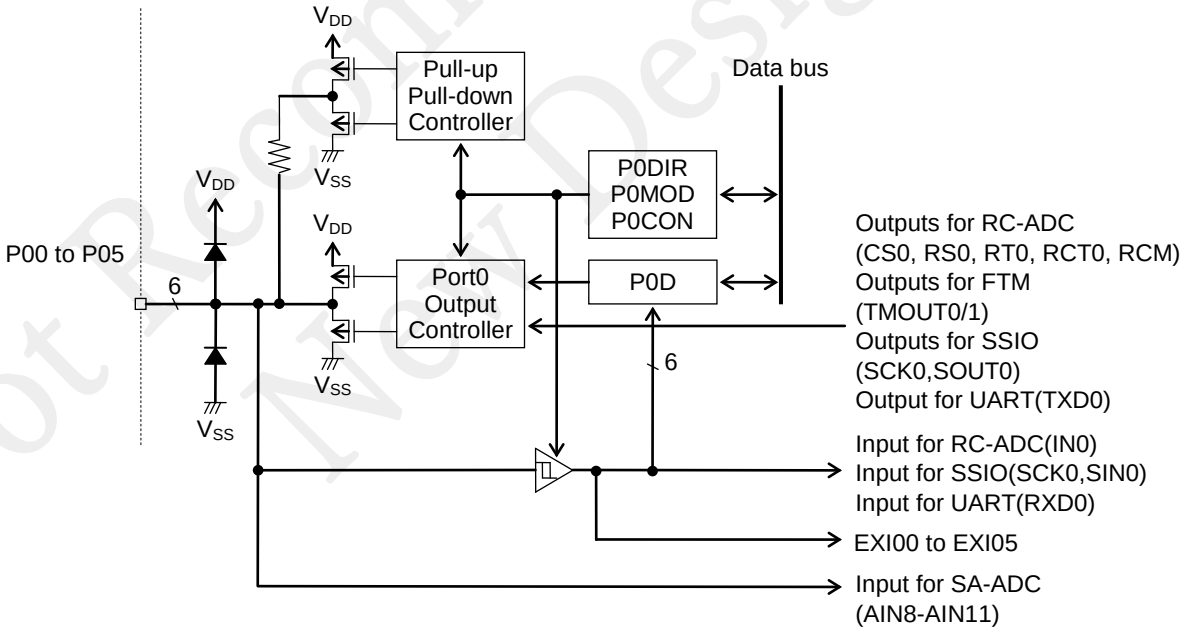
FTM:	Chapter 9 "Function Timer"
SSIO:	Chapter 11"Synchronous Serial Port"
UART:	Chapter 13"UART"
SA-ADC:	Chapter 25 "Successive approximate type A/D converter"
RC-ADC:	Chapter 24 "RC Oscillation Type A/D Converter"

17.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode for each bit.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode for each bit.
- External interrupt inputs(EXI00,EXI01,EXI02,EXI03,EXI04,EXI05), the SA-ADC input pins (AIN8, AIN9, AIN10, AIN11), The RC-ADC (channel 0) oscillation pins (IN0, CS0, RS0, RT0, RCT0, RCM), the SSIO pins (SCK0, SOUT0, SIN0), the UART pins (TXD0, RXD0), FTM output pin (TMOUT0, TMOUT1) can be used as the secondary or tertiary or fourthly functions.

17.1.2 Configuration

Figure 17-1 shows the configuration of Port 0.



P0D	: Port 0 data register
P0DIR	: Port 0 direction register
P0CON	: Port 0 control register
P0MOD	: Port 0 mode register

Figure 17-1 Configuration of Port 0

17.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Fourthly function
P00/EXI00/AIN8/ IN0/ SOUT0/ RXD0	I/O	Input/output port/ External Interrupt/ SA-ADC AIN8	Oscillation waveform input pin for RC-ADC IN0	SSIO data output SOUT0	UART data input RXD0
P01/EXI01/AIN9/ CS0/ SIN0/ TXD0	I/O	Input/output port/ External Interrupt/ SA-ADC AIN9	Reference capacitor connection pin for RC-ADC CS0	SSIO data input SIN0	UART data output TXD0
P02/EXI02/AIN10 RCT0/ SCK0/ TMOUT0	I/O	Input/output port/ External Interrupt/ SA-ADC AIN10	Resistor/capacitor sensor connection pin for measurement for RC-ADC RCT0	SSIO clock input/output SCK0	FTM output TMOUT0
P03/EXI03/AIN11/ RS0/ TMOUT1	I/O	Input/output port/ External Interrupt/ SA-ADC AIN11	Reference resistor connection pin for RC-ADC RS0	–	FTM output TMOUT1
P04/EXI04/ RT0	I/O	Input/output port/ External Interrupt	Resistor sensor connection pin for measurement for RC-ADC RT0	–	–
P05/EXI05/ RCM	I/O	Input/output port/ External Interrupt	RC oscillation monitor pin for RC-ADC RCM	–	–

17.2 Description of Registers

17.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F210	Port 0 data register	P0D	–	R/W	8	00
0F211	Port 0 direction register	P0DIR	–	R/W	8	00
0F212	Port 0 control register	P0CON0	P0CON	R/W	8/16	00
0F213		P0CON1		R/W	8	00
0F214	Port 0 mode register	P0MOD0	P0MOD	R/W	8/16	00
0F215		P0MOD1		R/W	8	00

17.2.2 Port 0 Data Register (P0D)

Address: 0F210H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P0D	–	–	P05D	P04D	P03D	P02D	P01D	P00D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P0D is a special function register (SFR) to set the value to be output to the Port 0 pin or to read the input level of the Port 0. In output mode, the value of this register is output to the Port 0 pin. The value written to P0D is readable. In input mode, the input level of the Port 0 pin is read when P0D is read. Output mode or input mode is selected by using the port 0 direction register (P0DIR) described later.

Description of Bits

- **P05-P00D** (bits 5 to 0)
  The P05-00D bits are used to set the output value of the Port 0 pin in output mode and to read the pin level of the Port 0 pin in input mode.

P00D	Description
0	Output or input level of the P00 pin: "L"
1	Output or input level of the P00 pin: "H"

P01D	Description
0	Output or input level of the P01 pin: "L"
1	Output or input level of the P01 pin: "H"

P02D	Description
0	Output or input level of the P02 pin: "L"
1	Output or input level of the P02 pin: "H"

P03D	Description
0	Output or input level of the P03 pin: "L"
1	Output or input level of the P03 pin: "H"

P04D	Description
0	Output or input level of the P04 pin: "L"
1	Output or input level of the P04 pin: "H"

P05D	Description
0	Output or input level of the P05 pin: "L"
1	Output or input level of the P05 pin: "H"

17.2.3 Port 0 Direction Register (P0DIR)

Address: 0F211H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P0DIR	–	–	P05DIR	P04DIR	P03DIR	P02DIR	P01DIR	P00DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P0DIR is a special function register (SFR) to select the input/output mode of Port 0.

Description of Bits

- **P05-00DIR** (bits 5 to 0)
  The P05-00DIR pins are used to set the input/output direction of the Port 0 pin.

P00DIR	Description
0	P00 pin: Output (initial value)
1	P00 pin: Input

P01DIR	Description
0	P01 pin: Output (initial value)
1	P01 pin: Input

P02DIR	Description
0	P02 pin: Output (initial value)
1	P02 pin: Input

P03DIR	Description
0	P03 pin: Output (initial value)
1	P03 pin: Input

P04DIR	Description
0	P04 pin: Output (initial value)
1	P04 pin: Input

P05DIR	Description
0	P05 pin: Output (initial value)
1	P05 pin: Input

17.2.4 Port 0 Control Register (P0CON)

Address: 0F212H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
P0CON0	–	–	P05C0	P04C0	P03C0	P02C0	P01C0	P00C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
P0CON1	–	–	P05C1	P04C1	P03C1	P02C1	P01C1	P00C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P0CON0 and P0CON1 are special function registers (SFRs) to select input/output state of the Port 0 pin. The input/output state is different between input mode and output mode. Input or output is selected by using the P0DIR register.

Description of Bits

- **P05-00C1**(bits 5 to 0)**, P05-00C0** (bit13 to 8)
  The P05-00C0 pins and the P05-00C1 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P00 pin		When output mode is selected (P00DIR bit = "0")	When input mode is selected (P00DIR bit = "1")
P00C1	**P00C0**	Description	
0	0	P00 pin: High-impedance output (initial value)	P00 pin: High-impedance input
0	1	P00 pin: P-channel open drain output	P00 pin: Input with a pull-down resistor
1	0	P00 pin: N-channel open drain output	P00 pin: Input with a pull-up resistor
1	1	P00 pin: CMOS output	P00 pin: High-impedance input

Setting of P01 pin		When output mode is selected (P01DIR bit = "0")	When input mode is selected (P01DIR bit = "1")
P01C1	**P01C0**	Description	
0	0	P01 pin: High-impedance output (initial value)	P01 pin: High-impedance input
0	1	P01 pin: P-channel open drain output	P01 pin: Input with a pull-down resistor
1	0	P01 pin: N-channel open drain output	P01 pin: Input with a pull-up resistor
1	1	P01 pin: CMOS output	P01 pin: High-impedance input

Setting of P02 pin		When output mode is selected (P02DIR bit = "0")	When input mode is selected (P02DIR bit = "1")
P02C1	**P02C0**	Description	
0	0	P02 pin: High-impedance output (initial value)	P02 pin: High-impedance input
0	1	P02 pin: P-channel open drain output	P02 pin: Input with a pull-down resistor
1	0	P02 pin: N-channel open drain output	P02 pin: Input with a pull-up resistor
1	1	P02 pin: CMOS output	P02 pin: High-impedance input

Setting of P03 pin		When output mode is selected (P03DIR bit = "0")	When input mode is selected (P03DIR bit = "1")
P03C1	**P03C0**	Description	
0	0	P03 pin: High-impedance output (initial value)	P03 pin: High-impedance input
0	1	P03 pin: P-channel open drain output	P03 pin: Input with a pull-down resistor
1	0	P03 pin: N-channel open drain output	P03 pin: Input with a pull-up resistor
1	1	P03 pin: CMOS output	P03 pin: High-impedance input

Setting of P04 pin		When output mode is selected (P04DIR bit = "0")	When input mode is selected (P04DIR bit = "1")
P04C1	**P04C0**	Description	
0	0	P04 pin: High-impedance output (initial value)	P04 pin: High-impedance input
0	1	P04 pin: P-channel open drain output	P04 pin: Input with a pull-down resistor
1	0	P04 pin: N-channel open drain output	P04 pin: Input with a pull-up resistor
1	1	P04 pin: CMOS output	P04 pin: High-impedance input

Setting of P05 pin		When output mode is selected (P05DIR bit = "0")	When input mode is selected (P05DIR bit = "1")
P05C1	**P05C0**	Description	
0	0	P05 pin: High-impedance output (initial value)	P05 pin: High-impedance input
0	1	P05 pin: P-channel open drain output	P05 pin: Input with a pull-down resistor
1	0	P05 pin: N-channel open drain output	P05 pin: Input with a pull-up resistor
1	1	P05 pin: CMOS output	P05 pin: High-impedance input

17.2.5 Port 0 Mode Register (P0MOD)

Address: 0F214H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
P0MOD0	–	–	P05MD0	P04MD0	P03MD0	P02MD0	P01MD0	P00MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
P0MOD1	–	–	P05MD1	P04MD1	P03MD1	P02MD1	P01MD1	P00MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P0MOD0 and P0MOD1 are special function registers (SFRs) to select the primary, secondary, or tertiary function of Port 0.

Description of Bits

- **P00MD1-0** (bit 8,0)
  The P00MD1-0 bits are used to select the primary or secondary or tertiary or fourthly function of the P00 pin.

P00MD1	P00MD0	Description
0	0	General-purpose input/output mode / External Interrupt (initial value)
0	1	RC oscillation waveform input pin for RC-ADC (IN0)
1	0	SSIO data output (SOUT0)
1	1	UART data input (RXD0)

- **P01MD1-0** (bit 9,1)
  The P01MD1-0 bits are used to select the primary or secondary or tertiary or fourthly function of the P01 pin.

P01MD1	P01MD0	Description
0	0	General-purpose input/output mode / External Interrupt (initial value)
0	1	Reference capacitor connection pin for RC-ADC (CS0)
1	0	SSIO data input (SIN0)
1	1	UART data output (TXD0)

- **P02MD1-0** (bit 10,2)
  The P02MD1-0 bits are used to select the primary or secondary or tertiary or fourthly function of the P02 pin.

P02MD1	P02MD0	Description
0	0	General-purpose input/output mode / External Interrupt (initial value)
0	1	Resistor/capacitor sensor connection pin for measurement for RC-ADC (RCT0)
1	0	SSIO clock input/output (SCK0)
1	1	FTM output (TMOUT0)

- **P03MD1-0** (bit 11,3)
  The P03MD1-0 bits are used to select the primary or secondary or fourthly function of the P03 pin.

P03MD1	P03MD0	Description
0	0	General-purpose input/output mode / External Interrupt (initial value)
0	1	Reference resistor connection pin for RC-ADC (RS0)
1	0	Prohibited
1	1	FTM output (TMOUT1)

- **P04MD1-0** (bit 12,4)
  The P04MD1-0 bits are used to select the primary, secondary of the P04 pin.

P04MD1	P04MD0	Description
0	0	General-purpose input/output mode / External Interrupt (initial value)
0	1	Resistor/capacitor sensor connection pin for measurement for RC-ADC (RT0)
1	0	Prohibited
1	1	Prohibited

- **P05MD1-0** (bit 13,5)
  The P05MD1-0 bits are used to select the primary or secondary function of the P05 pin.

P05MD1	P05MD0	Description
0	0	General-purpose input/output mode / External Interrupt (initial value)
0	1	RC oscillation monitor pin for RC-ADC (RCM)
1	0	Prohibited
1	1	Prohibited

[Note]
If any bit combination out of the above is set to "Prohibited" and the corresponding bit of the port 0 is specified to output mode (selected in port0 control register), status of corresponding pin is fixed, regardless the contents of Port0 register (P0D)

High-impedance output mode: High-impedance
P-channel open drain output mode: High-impedance
N-channel open drain output mode: Fixed to "L"
CMOS output mode: High-impedance: Fixed to "L"

17.3 Description of Operation

17.3.1 Input/Output Port Functions

For each pin of Port 0, either output or input is selected by setting the Port 0 direction register (P0DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 0 control registers 0 and 1 (P0CON0 and P0CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 0 control registers 0 and 1 (P0CON0 and P0CON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port 0 depending on the value set by the Port 0 data register (P0D).
In input mode, the input level of each pin of Port 0 can be read from the Port 0 data register (P0D).

17.3.2 Primary Function except for Input/Output Port

Port 0 is assigned to the SA-ADC input pins (AIN8, AIN9, AIN10, AIN11), External interrupts (EXI00, EXI01, EXI02, EXI03, EXI04, EXI05).
When used as the SA-ADC input pins, set the applicable port to the high impedance output state.
When used as the External interrupts, set the applicable port to the input state.

17.3.3 Secondary ,Tertiary and Fourthly Functions

Secondary, tertiary and fourthly functions are assigned to Port 0 as the RC-ADC (channel 0) oscillation pins (IN0, CS0, RS0, RT0, RCT0, RCM), the SSIO pins (SIN0, SOUT0,SCK0), the UART pins (RXD0, TXD0), FTM output pins(TMOUT0,TMOUT1). These pins can be used in a secondary or tertiary or fourthly function mode by setting the P05MD0 to P00MD0 bits and the P05MD1 to P00MD1 bits of the Port 0 mode registers (P0MOD0, P0MOD1).
When used as the RC-ADC, set the P00 to P05 to the high impedance input state and RC-ADC mode.

Chapter 18

Port 1

18 Port 1

18.1 Overview

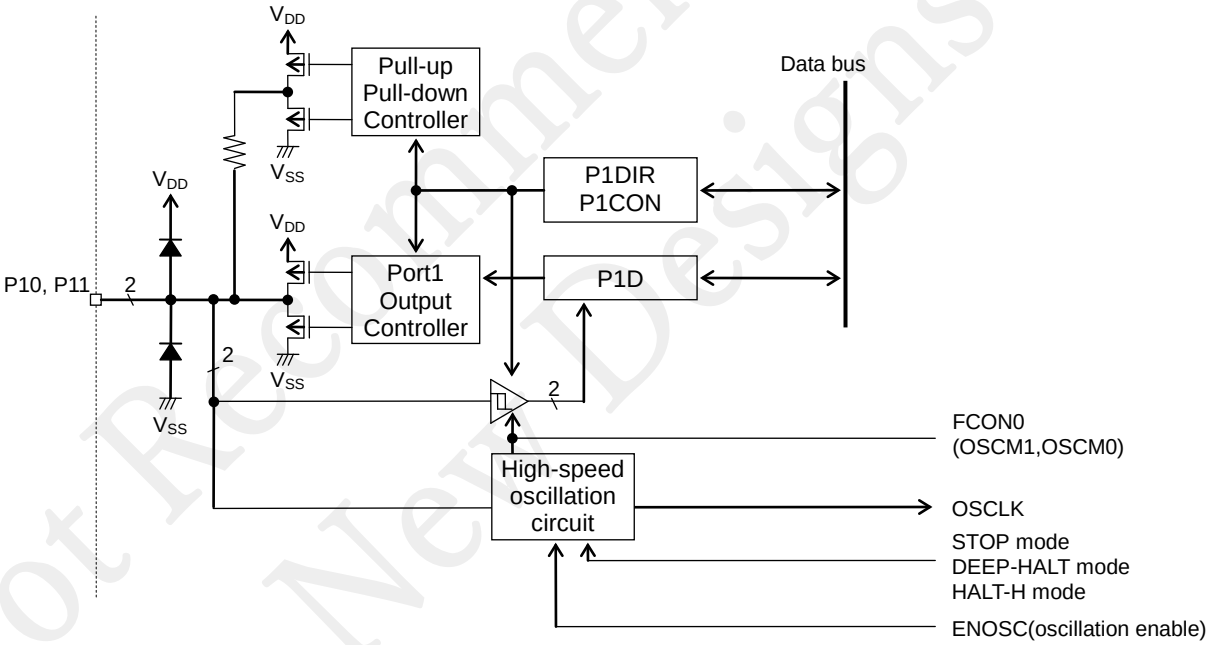
This LSI incorporates a 2-bit input port, Port 1 (P10, P11).
Port 1 can have a high-speed oscillation pin or an external clock input pin. When the port is used as a high-speed oscillation pin, the P11 pin functions as an output pin if crystal/ceramic oscillation mode is selected with the OSCM1–0 bits of the FCON0 register.
For high-speed oscillation and external clock input, see Chapter 6, "Clock Generation Circuit".

18.1.1 Features

- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit.
- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode for each bit.
- Allows selection of a high-speed crystal/ceramic oscillation pin or an external clock input pin.

18.1.2 Configuration

Figure 18-1 shows the configuration of Port 1.



P1D : Port 1 data register
P1DIR : Port 1 direction register
P1CON : Port 1 control register

Figure 18-1 Configuration of Port 1

18.1.3 List of Pins

Pin name	I/O	Primary function
P10/OSC0	I/O	Input /output port High-speed crystal/ceramic oscillation pin
P11/OSC1/ CLKIN	I/O	Input /output port High-speed crystal/ ceramic oscillation pin/ external clock input pin

18.2 Description of Registers

18.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F218	Port 1 data register	P1D	–	R/W	8	00
0F219	Port 1 direction register	P1DIR	–	R/W	8	00
0F21A	Port 1 control register	P1CON0	P1CON	R/W	8/16	00
0F21B		P1CON1		R/W	8	00

18.2.2 Port 1 Data Register (P1D)

Address: 0F218H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P1D	–	–	–	–	–	–	P11D	P10D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P1D is a special function register (SFR) to set the value to be output to the Port 1 pin or to read the input level of the Port 1. In output mode, the value of this register is output to the Port 1 pin. The value written to P1D is readable. In input mode, the input level of the Port 1 pin is read when P1D is read. Output mode or input mode is selected by using the port mode register (P1DIR) described later.

Description of Bits

- **P11-10D** (bits 1 to 0)
  The P11-10D bits are used to read the input level of the Port 1 pin.

P10D	Description
0	Input level of the P10 pin: "L"
1	Input level of the P10 pin: "H"

P11D	Description
0	Input level of the P11 pin: "L"
1	Input level of the P11 pin: "H"

18.2.3 Port 1 Direction Register (P1DIR)

Address: 0F219H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P1DIR	–	–	–	–	–	–	P11DIR	P10DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P0DIR is a special function register (SFR) to select the input/output mode of Port 0.

Description of Bits

- **P11-10DIR** (bits 1 to 0)
  The P11-10DIR pins are used to set the input/output direction of the Port 1 pin.

P10DIR	Description
0	P10 pin: Output (initial value)
1	P10 pin: Input

P11DIR	Description
0	P11 pin: Output (initial value)
1	P11 pin: Input

18.2.4 Port 1 Control Register (P1CON)

Address: 0F21AH
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
P1CON0	–	–	–	–	–	–	P11C0	P10C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
P1CON1	–	–	–	–	–	–	P11C1	P10C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P1CON0 and P1CON1 are special function registers (SFRs) to select input/output state of the Port 1 pin. The input/output state is different between input mode and output mode. Input or output is selected by using the P1DIR register.

Description of Bits

- **P11-10C0**(bits 1 to 0)**, P11-00C1** (bits 9 to 8)
  The P11-10C1 pins and the P11-10C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P10 pin		Description	
P10C1	P10C0	When output mode selected (P10DIR = 0)	When input mode selected (P10DIR = 1)
0	0	P10 pin: High-impedance output (initial value)	P10 pin: high-impedance input mode (initial value)
0	1	P10 pin: P-channel open drain output	P10 pin: input mode with a pull-down resistor
1	0	P10 pin: N-channel open drain output	P10 pin: input mode with a pull-up resistor
1	1	P10 pin: CMOS output	P10 pin: high-impedance input mode

Setting of P11 pin		Description	
P11C1	P11C0	When output mode selected (P11DIR = 0)	When input mode selected (P11DIR = 1)
0	0	P11 pin: High-impedance output (initial value)	P11 pin: high-impedance input mode (initial value)
0	1	P11 pin: P-channel open drain output	P11 pin: input mode with a pull-down resistor
1	0	P11 pin: N-channel open drain output	P11 pin: input mode with a pull-up resistor
1	1	P11 pin: CMOS output	P11 pin: high-impedance input mode

18.3 Description of Operation

18.3.1 Input/Output Port Function

For each pin of Port 1, either output or input is selected by setting the Port 1 direction register (P1DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 1 control registers 0 and 1 (P1CON0 and P1CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 1 control registers 0 and 1 (P1CON0 and P1CON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port 1 depending on the value set by the Port 1 data register (P1D).
In input mode, the input level of each pin of Port 1 can be read from the Port 1 data register (P1D).

18.3.2 Other Function

A high-speed crystal/ceramic oscillation pin or an external clock input pin is assigned to Port 1 as a secondary function. Select high-speed crystal/ceramic oscillation mode or external clock input mode by using the high-speed clock mode select function of the OSCM1 and 0 bits of the frequency control register 0 (FCON0). In crystal/ceramic oscillation mode, both P10 and P11 pins are used as the pins for crystal/ceramic oscillation.
In external clock input mode, the P11 pin is used as the input pin of external clock.

Chapter 19

Port2

19 Port 2

19.1 Overview

This LSI includes Port 2 (P20 to P23) which is an 4-bit input/output port.
This port can have external interrupts, SA-ADC, RC-ADC, SSIOF, UARTF and FTIMER output functions as secondary, tertiary and quartic functions.
See the following chapters for reference:

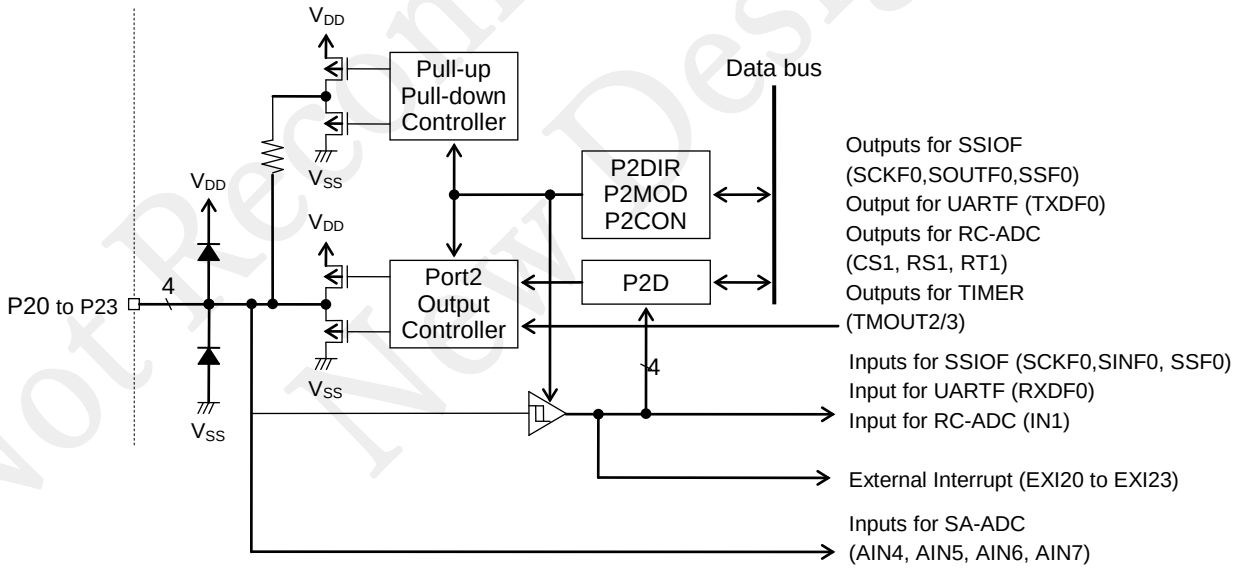
FTM:	Chapter 9 "Function Timer"
SSIOF:	Chapter 12 "SSIO with FIFO"
UARTF:	Chapter 14 "UART with FIFO"
RC-ADC:	Chapter 24 "RC Oscillation type A/D converter"
SA-ADC:	Chapter 25 "Successive approximate type A/D converter"

19.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- External interrupt inputs(EXI20,EXI21,EXI22,EXI23), the SA-ADC inputs (AIN4, AIN5, AIN6, AIN7), RC-ADC (channel 1) oscillation pins (IN1, CS1, RS1, RT1), SSIO with FIFO pins (SINF0, SCKF0, SOUTF0, SSF0), UART with FIFO pins (RXDF0, TXDF0), TIMER output pin (TMOUT2, TMOUT3) .

19.1.2 Configuration

Figure 19-1 shows the configuration of Port 2.



P2D	: Port 2 data register
P2DIR	: Port 2 direction register
P2CON	: Port 2 control register
P2MOD	: Port 2 mode register

Figure 19-1 Configuration of Port 2

19.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Fourthly function
P20/EXI20/AIN4/ IN1/ SOUTF0/ RXDF0	I/O	Input/output port External interrupt SA-ADC AIN4	RC oscillation waveform input pin for RC-ADC IN1	SSIOF data output SOUTF0	UARTF data input RXDF0
P21/EXI21/AIN5/ CS1/ SINF0/ TXDF0	I/O	Input/output port External interrupt SA-ADC AIN5	Reference capacitor connection pin for RC-ADC CS1	SSIOF data input SINF0	UARTF data output TXDF0
P22/EXI22/AIN6/ RS1/ SCKF0/ TMOUT2	I/O	Input/output port External interrupt SA-ADC AIN6	Reference resistor connection pin for RC-ADC RS1	SSIOF clock input/output SCKF0	FTM output TMOUT2
P23/EXI23/AIN7/ RT1/ SCKF0/ TMOUT1	I/O	Input/output port External interrupt SA-ADC AIN7	Resistor sensor connection pin for measurement for RC-ADC RT1	SSIOF enable input/output SSF0	FTM output TMOUT3

19.2 Description of Registers

19.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F220	Port 2 data register	P2D	–	R/W	8	00
0F221	Port 2 direction register	P2DIR	–	R/W	8	00
0F222	Port 2 control register	P2CON0	P2CON	R/W	8/16	00
0F223		P2CON1		R/W	8	00
0F224	Port 2 mode register	P2MOD0	P2MOD	R/W	8/16	00
0F225		P2MOD1		R/W	8	00

19.2.2 Port 2 Data Register (P2D)

Address: 0F220H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2D	–	–	–	–	P23D	P22D	P21D	P20D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2D is a special function register (SFR) to set the value to be output to the Port 2 pin or to read the input level of the Port 2. In output mode, the value of this register is output to the Port 2 pin. The value written to P2D is readable. In input mode, the input level of the Port 2 pin is read when P2D is read. Output mode or input mode is selected by using the port mode register (P2DIR) described later.

Description of Bits

- **P23-20D** (bits 3 to 0)
  The P23-20D bits are used to set the output value of the Port 2 pin in output mode and to read the pin level of the Port 2 pin in input mode.

P20D	Description
0	Output or input level of the P20 pin: "L"
1	Output or input level of the P20 pin: "H"

P21D	Description
0	Output or input level of the P21 pin: "L"
1	Output or input level of the P21 pin: "H"

P22D	Description
0	Output or input level of the P22 pin: "L"
1	Output or input level of the P22 pin: "H"

P23D	Description
0	Output or input level of the P23 pin: "L"
1	Output or input level of the P23 pin: "H"

19.2.3 Port 2 Direction Register (P2DIR)

Address: 0F221H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P2DIR	–	–	–	–	P23DIR	P22DIR	P21DIR	P20DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2DIR is a special function register (SFR) to select the input/output mode of Port 2.

Description of Bits

- **P23-20DIR** (bits 3 to 0)
  The P23-20DIR pins are used to set the input/output direction of the Port 2 pin.

P20DIR	Description
0	P20 pin: Output (initial value)
1	P20 pin: Input

P21DIR	Description
0	P21 pin: Output (initial value)
1	P21 pin: Input

P22DIR	Description
0	P22 pin: Output (initial value)
1	P22 pin: Input

P23DIR	Description
0	P23 pin: Output (initial value)
1	P23 pin: Input

19.2.4 Port 2 Control Register (P2CON)

Address: 0F222H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
P2CON0	–	–	–	–	P23C0	P22C0	P21C0	P20C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
P2CON1	–	–	–	–	P23C1	P22C1	P21C1	P20C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2CON0 and P2CON1 are special function registers (SFRs) to select input/output state of the Port 2 pin. The input/output state is different between input mode and output mode. Input or output is selected by using the P2DIR register.

Description of Bits

- **P23-20C1** (bits 3 to 0)**, P23-20C0** (bits 11 to 8)
  The P27-20C1 pins and the P27-20C0 pins are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.

Setting of P20 pin		When output mode is selected (P20DIR bit = "0")	When input mode is selected (P20DIR bit = "1")
P20C1	**P20C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P21 pin		When output mode is selected (P21DIR bit = "0")	When input mode is selected (P21DIR bit = "1")
P21C1	**P21C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P22 pin		When output mode is selected (P22DIR bit = "0")	When input mode is selected (P22DIR bit = "1")
P22C1	**P22C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P23 pin		When output mode is selected (P23DIR bit = "0")	When input mode is selected (P23DIR bit = "1")
P23C1	**P23C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

19.2.5 Port 2 Mode Register (P2MOD)

Address: 0F224H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
P2MOD0	–	–	–	–	P23MD0	P22MD0	P21MD0	P20MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
P2MOD1	–	–	–	–	P23MD1	P22MD1	P21MD1	P20MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P2MOD0 and P2MOD1 are special function registers (SFRs) to select the primary, secondary, or tertiary function of Port 2.

Description of Bits

- **P20MD1-0** (bit 8,0)
  The P20MD1-0 bits are used to select the primary, secondary, or tertiary function of the P20 pin.

P20MD1	P20MD0	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	RC oscillation waveform input pin for RC-AD (IN1)
1	0	SSIOF data output (SOUTF0)
1	1	UARTF data input (RXDF0)

- **P21MD1-0** (bit 9,1)
  The P21MD1-0 bits are used to select the primary, secondary, or tertiary function of the P21 pin.

P21MD1	P21MD0	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	Reference capacitor connection pin for RC-ADC (CS1)
1	0	SSIOF data input (SINF0)
1	1	USRTF data output (TXDF0)

- **P22MD1-0** (bit 10,2)
  The P22MD1-0 bits are used to select the primary, secondary, or tertiary function of the P22 pin.

P22MD1	P22MD0	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	Reference resistor connection pin for RC-ADC (RS1)
1	0	SSIOF clock input/output (SCKF0)
1	1	FTM output mode (TMOUT2)

- **P23MD1-0** (bit 11,3)
  The P23MD1-0 bits are used to select the primary, secondary, or tertiary function of the P23 pin.

P23MD1	P23MD0	Description
0	0	General-purpose input/output mode / External interrupt (initial value)
0	1	Resistor sensor connection pin for measurement for RC-ADC (RT1)
1	0	SSIOF enable input/output (SSF0)
1	1	FTM output mode (TMOUT3)

[Note]
If any bit combination out of the above is set to "Prohibited" and the corresponding bit of the Port 2 is specified to output mode (selected in Port 2 control register), status of corresponding pin is fixed, regardless the contents of Port 2 register (P2D)

High-impedance output mode: High-impedance
P-channel open drain output mode: High-impedance
N-channel open drain output mode: Fixed to "L"
CMOS output mode: High-impedance: Fixed to "L"

19.3 Description of Operation

19.3.1 Input/Output Port Functions

For each pin of Port 2, either output or input is selected by setting the Port 2 direction register (P2DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 2 control registers 0 and 1 (P2CON0 and P2CON1).
In input mode, high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor can be selected by setting the Port 2 control registers 0 and 1 (P2CON0 and P2CON1).
At a system reset, high-impedance output mode is selected as the initial state.
In output mode, "L" or "H" level is output to each pin of Port 2 depending on the value set by the Port 2 data register (P2D).
In input mode, the input level of each pin of Port 2 can be read from the Port 2 data register (P2D).

19.3.2 Primary Function except for Input/Output Port

Port 2 is assigned to the SA-A/DC input pins (AIN4, AIN5, AIN6, AIN7), External interrupts (EXI20, EXI21, EXI22, EXI23).
When used as the SA-ADC input pins, set the applicable port to the high impedance output state.
When used as the External interrupts, set an applicable port to the input state.

19.3.3 Secondary, Tertiary and Fourthly Functions

Secondary, tertiary and fourthly functions are assigned to Port 2 as the SSIOF pins (SCKF0, SINF0, SOUTF0, SSF0), UARTF pins (RXDF0, TXDF0), RC-ADC (channel 1) oscillation pins (IN1, CS1, RS1, RT1), FTIMER output pin (TMOUT2, TMOUT3),. These pins can be used in a secondary or tertiary or fourthly function mode by setting the P23MD0 to P20MD0 bits and the P23MD1 to P20MD1 bits of the Port 2 mode registers (P2MOD0, P2MOD1).
When used as the RC-ADC, set the P20 to P23 to the high impedance input state and RC-ADC mode.

Chapter 20

Port 3

20 Port 3

20.1 General Description

This LSI includes an 8-bit input/output port, port 3 (P30 to P37).
It can function as an external interrupt, a successive approximation type A/D converter input, and a comparator input, as well as an I^2C bus, a buzzer output, a synchronous serial port, a synchronous serial port with FIFO, a UART, a UART with FIFO, and a timer out output pin as the secondary, tertiary, or quartic function.

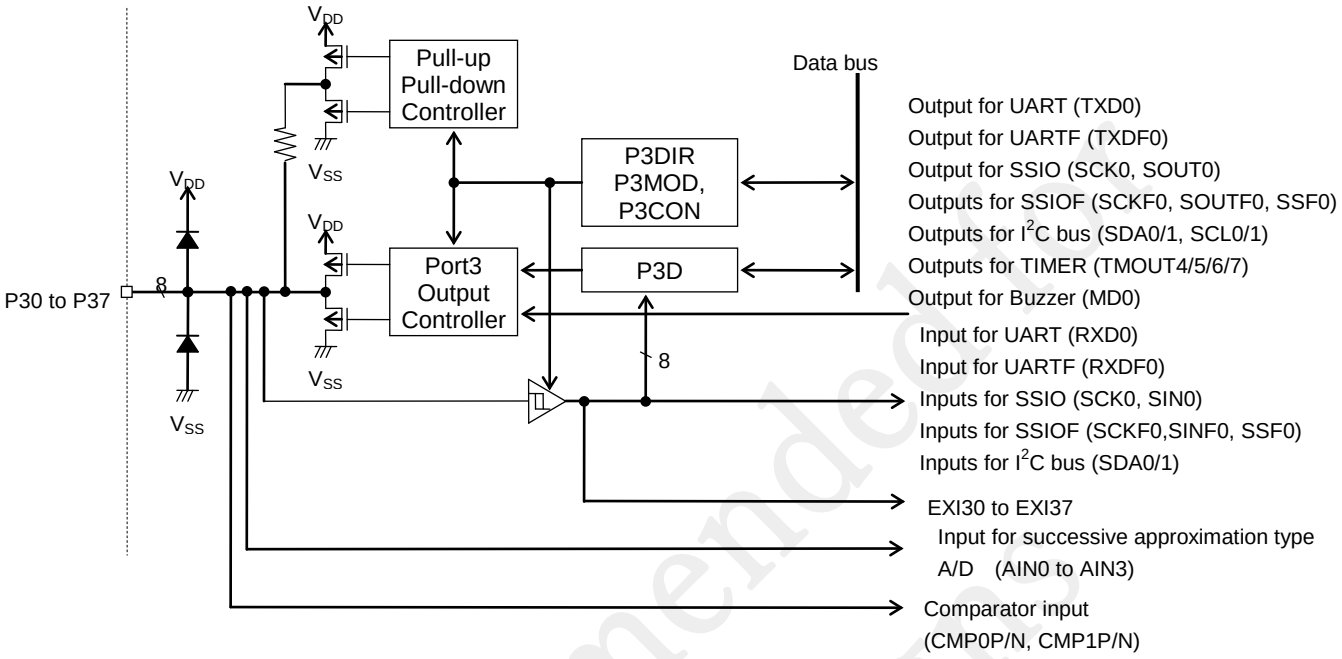
FTM:	Chapter 9 “Function Timer”
SSIO:	Chapter 11 “Synchronous Serial Port”
SSIOF:	Chapter 12 “SSIO with FIFO”
UART:	Chapter 13 “UART”
UARTF:	Chapter 14 “UART with FIFO”
I^2C :	Chapter 15 “I^2C Bus Interface”
MELODY:	Chapter 23 “Melody Driver”
SA-ADC:	Chapter 25 “Successive approximate type A/D converter”
COMP :	Chapter 26 “Analog Comparator”

20.1.1 Features

- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- Can be used as an external interrupt pin (EXI30, EXI31, EXI32, EXI33, EXI34, EXI35, EXI36, EXI37), a successive approximation type A/D converter pin (AIN0/1/2/3), a comparator input (CMP0P/N, CMP1P/N), an I^2C bus pin (SDA0/1, SCL0/1), a buzzer output (MD0), a synchronous serial port pin (SIN0, SCK0, SOUT0), a synchronous serial port with FIFO pin (SINF0, SCKF0, SOUTF0, SSF0), a UART pin (RXD0, TXD0), a UART with FIFO pin (RXDF0, TXDF0), or a timer out pin (TMOUT4/5/6/7).

20.1.2 Configuration

Figure 20-1 shows the configuration of Port 3.



P3D : Port 3 data register
P3DIR : Port 3 direction register
P3CON : Port 3 control register
P3MOD : Port 3 mode register

Figure 20-1 Configuration of Port 3

20.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Quartic function
P30/EXI30/CMP0P/ SDA0/ SOUT0/ RXD0	I/O	I/O port External interrupt Comparator + side input 0	I^2C data I/O SDA0	Synchronous serial data output SOUT0	UART data input RXD0
P31/EXI31/CMP0M/ SCL0/ SIN0/ TXD0	I/O	I/O port External interrupt Comparator - side input 0	I^2C clock output SCL0	Synchronous serial data input SIN0	UART data output TXD0
P32/EXI32/CMP1P/ SCK0/ TMOUT4	I/O	I/O port External interrupt Comparator + side input1	–	Synchronous serial clock output SCK0	FTM output TMOUT4
P33/EXI33/CMP1M/ MD0 TMOUT5	I/O	I/O port External interrupt Comparator - side input 1	Melody/Buzzer output MD0	–	FTM output TMOUT5
P34/EXI34/ AIN0/ SDA1/ SOUTF0/ RXDF0	I/O	I/O port External interrupt Successive approximation type A/D converter input AIN0	I^2C data I/O SDA1	Synchronous serial data with FIFO output SOUTF0	UART with FIFO data input RXDF0
P35/EXI35/ AIN1/ SCL1/ SINF0/ TXDF0	I/O	I/O port External interrupt Successive approximation type A/D converter input AIN1	I^2C clock output SCL1	Synchronous serial data with FIFO input SINF0	UART with FIFO data output TXDF0
P36/EXI36/ AIN2/ SCKF0/ TMOUT6	I/O	I/O port External interrupt Successive approximation type A/D converter input AIN2	–	Synchronous serial clock with FIFO output SCKF0	FTM output TMOUT6
P37/EXI37/ AIN3/ SSF0/ TMOUT7	I/O	I/O port External interrupt Successive approximation type A/D converter input AIN3	–	Synchronous serial chip with FIFO select output SSF0	FTM output TMOUT7

20.2 Description of Registers

20.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F228	Port 3 data register	P3D	–	R/W	8	00
0F229	Port 3 direction register	P3DIR	–	R/W	8	00
0F22A	Port 3 control register	P3CON0	P3CON	R/W	8/16	00
0F22B		P3CON1		R/W	8	00
0F22C	Port 3 mode register	P3MOD0	P3MOD	R/W	8/16	00
0F22D		P3MOD1		R/W	8	00

20.2.2 Port 3 Data Register (P3D)

Address: 0F228H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3D	P37D	P36D	P35D	P34D	P33D	P32D	P31D	P30D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3D is a special function register (SFR) to set the value to be output to the Port 3 pin or to read the input level of the Port 3. In output mode, the value of this register is output to the Port 3 pin. The value written to P3D is readable. In input mode, the input level of the Port 3 pin is read when P3D is read.
Output mode or input mode is selected by using the port mode register (P3DIR) described later.

Description of Bits

- **P37-30D** (bits 7 to 0)
  The P37-30D bits are used to set the output value of the Port 3 pin in output mode and to read the pin level of the Port 3 pin in input mode.

P30D	Description
0	Output or input level of the P30 pin: ”L”
1	Output or input level of the P30 pin: ”H”

P31D	Description
0	Output or input level of the P31 pin: ”L”
1	Output or input level of the P31 pin: ”H”

P32D	Description
0	Output or input level of the P32 pin: ”L”
1	Output or input level of the P32 pin: ”H”

P33D	Description
0	Output or input level of the P33 pin: ”L”
1	Output or input level of the P33 pin: ”H”

P34D	Description
0	Output or input level of the P34 pin: ”L”
1	Output or input level of the P34 pin: ”H”

P35D	Description
0	Output or input level of the P35 pin: ”L”
1	Output or input level of the P35 pin: ”H”

P36D	Description
0	Output or input level of the P36 pin: ”L”
1	Output or input level of the P36 pin: ”H”

P37D	Description
0	Output or input level of the P37 pin: ”L”
1	Output or input level of the P37 pin: ”H”

20.2.3 Port 3 Direction Register (P3DIR)

Address: 0F229H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P3DIR	P37DIR	P36DIR	P35DIR	P34DIR	P33DIR	P32DIR	P31DIR	P30DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3DIR is a special function register (SFR) to select the input/output mode of Port 3.

Description of Bits

- **P37-30DIR** (bits 7 to 0)
  The P37-30DIR bits are used to set the input/output mode of the port 3 pin.

P30DIR	Description
0	P30 pin: Output (initial value)
1	P30 pin: Input

P31DIR	Description
0	P31 pin: Output (initial value)
1	P31 pin: Input

P32DIR	Description
0	P32 pin: Output (initial value)
1	P32 pin: Input

P33DIR	Description
0	P33 pin: Output (initial value)
1	P33 pin: Input

P34DIR	Description
0	P34 pin: Output (initial value)
1	P34 pin: Input

P35DIR	Description
0	P35 pin: Output (initial value)
1	P35 pin: Input

P36DIR	Description
0	P36 pin: Output (initial value)
1	P36 pin: Input

P37DIR	Description
0	P37 pin: Output (initial value)
1	P37 pin: Input

[Note]
The P34 to P37 pins are assigned to successive approximation type A/D converter input or comparator input. If it is used as a successive approximation type A/D converter input or comparator input, set the appropriate port to the output mode.

20.2.4 Port 3 Control Register (P3CON)

Address: 0F22AH
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
P3CON0	P37C0	P36C0	P35C0	P34C0	P33C0	P32C0	P31C0	P30C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
P3CON1	P37C1	P36C1	P35C1	P34C1	P33C1	P32C1	P31C1	P30C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3CON0 and P3CON1 are special function registers (SFRs) used to select the output state of the port 3 pin. The output state is different between input mode and output mode. Input or output is selected by using the P3DIR register.

Description of Bits

- **P37-30C0**(bits 7 to 0)**, P37-30C1** (bits 15-8)
  The P37-30C1 and P37-30C0 bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.
  To perform the direct LED drive, select N-channel open drain output mode.

Setting of P30 pin		When output mode is selected (P30DIR bit = "0")	When input mode is selected (P30DIR bit = "1")
P30C1	**P30C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P31 pin		When output mode is selected (P31DIR bit = "0")	When input mode is selected (P31DIR bit = "1")
P31C1	**P31C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P32 pin		When output mode is selected (P32DIR bit = "0")	When input mode is selected (P32DIR bit = "1")
P32C1	**P32C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P33 pin		When output mode is selected (P33DIR bit = "0")	When input mode is selected (P33DIR bit = "1")
P33C1	**P33C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P34 pin		When output mode is selected (P34DIR bit = "0")		When input mode is selected (P34DIR bit = "1")
		When 1st function is selected (P34MD1,P34MD0="00")	When 2nd/3rd/4th function is selected (P34MD1,P34MD0≠"00")	
P34C1	**P34C0**	Description		
0	0	High-impedance output (initial value)	N-channel open drain output	High-impedance input
0	1	P-channel open drain output	CMOS output	Input with a pull-down resistor
1	0	N-channel open drain output	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	CMOS output	High-impedance input

Setting of P35 pin		When output mode is selected (P35DIR bit = "0")		When input mode is selected (P35DIR bit = "1")
		When 1st function is selected (P35MD1,P35MD0="00")	When 2nd/3rd/4th function is selected (P35MD1,P35MD0≠"00")	
P35C1	**P35C0**	Description		
0	0	High-impedance output (initial value)	N-channel open drain output	High-impedance input
0	1	P-channel open drain output	CMOS output	Input with a pull-down resistor
1	0	N-channel open drain output	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	CMOS output	High-impedance input

Setting of P36 pin		When output mode is selected (P36DIR bit = "0")		When input mode is selected (P36DIR bit = "1")
		When 1st function is selected (P36MD1,P36MD0="00")	When 2nd/3rd/4th function is selected (P36MD1,P36MD0≠"00")	
P36C1	**P36C0**	Description		
0	0	High-impedance output (initial value)	N-channel open drain output	High-impedance input
0	1	P-channel open drain output	CMOS output	Input with a pull-down resistor
1	0	N-channel open drain output	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	CMOS output	High-impedance input

Setting of P37 pin		When output mode is selected (P37DIR bit = "0")		When input mode is selected (P37DIR bit = "1")
		When 1st function is selected (P37MD1,P37MD0="00")	When 2nd/3rd/4th function is selected (P37MD1,P37MD0≠"00")	
P37C1	**P37C0**	Description		
0	0	High-impedance output (initial value)	N-channel open drain output	High-impedance input
0	1	P-channel open drain output	CMOS output	Input with a pull-down resistor
1	0	N-channel open drain output	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	CMOS output	High-impedance input

[Note]

The P34 to P37 pins are assigned to successive approximation type A/D converter input or comparator input. If it is used as a successive approximation type A/D converter input or comparator input, set the appropriate port to the high-impedance output mode.

20.2.5 Port 3 Mode Register (P3MOD)

Address: 0F22CH
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
P3MOD0	P37MD0	P36MD0	P35MD0	P34MD0	P33MD0	P32MD0	P31MD0	P30MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
P3MOD1	P37MD1	P36MD1	P35MD1	P34MD1	P33MD1	P32MD1	P31MD1	P30MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P3MOD0 and P3MOD1 are special function registers (SFRs) used to select the primary, secondary, tertiary, or quartic function of the port 3.

Description of Bits

- **P30MD1-0** (bits 8,0)
  The P30MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P30 pin.

P30MD1	P30MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	I^2C bus data input/output mode (SDA0)
1	0	Synchronous serial port data output mode (SOUT0)
1	1	UART data input mode (RXD0)

- **P31MD1-0** (bits 9,1)
  The P31MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P31 pin.

P31MD1	P31MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	I^2C bus clock output mode (SCL0)
1	0	Synchronous serial port data input mode (SIN0)
1	1	UART data output mode (TXD0)

- **P32MD1-0** (bits 10,2)
  The P32MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P32 pin.

P32MD1	P32MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	Prohibited
1	0	Synchronous serial port clock input/output mode (SCK0)
1	1	FTM output mode (TMOUT4)

- **P33MD1-0** (bits 11,3)
  The P33MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P33 pin.

P33MD1	P33MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	Buzzer output mode (MD0)
1	0	Prohibited
1	1	FTM output mode (TMOUT5)

- **P34MD1-0** (bits 12,4)
  The P34MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P34 pin.

P34MD1	P34MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	I^2C bus data input/output mode (SDA1)
1	0	Synchronous serial port with FIFO data output mode (SOUTF0)
1	1	UART with FIFO data input mode (RXDF0)

- **P35MD1-0** (bits 13,5)
  The P35MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P35 pin.

P35MD1	P35MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	I^2C bus clock output mode (SCL1)
1	0	Synchronous serial port with FIFO data input mode (SINF0)
1	1	UART with FIFO data output mode (TXDF0)

- **P36MD1-0** (bits 14,6)
  The P36MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P36 pin.

P36MD1	P36MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	Prohibited
1	0	Synchronous serial port with FIFO clock input/output mode (SCKF0)
1	1	FTM output mode (TMOUT6)

- **P37MD1-0** (bits 15,7)
  The P37MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P37 pin.

P37MD1	P37MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	Prohibited
1	0	Synchronous serial port with FIFO chip select input/output mode (SSF0)
1	1	FTM output mode (TMOUT7)

[Note]

When the pin is set to "Prohibited" and the output mode is selected (by the Port 3 control register), the Port 3 output pin state is fixed as follows regardless of the data of the port data register P3D:

When high-impedance output is selected: Output pin is high-impedance
When P-channel open drain output is selected: Output pin is high-impedance
When N-channel open drain output is selected: Output pin is fixed to "L"
When CMOS output is selected: Output pin is fixed to "L"

The P34 to P37 pins are assigned to successive approximation type A/D converter input or comparator. If it is used as a successive approximation type A/D converter input or comparator, set the appropriate port to the general-purpose input/output mode.

20.3 Description of Operation

20.3.1 Input/Output Port Functions

For each pin of Port 3, either output or input is selected by setting the Port 3 direction register (P3DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 3 control registers 0 and 1 (P3CON0 and P3CON1).
In the input mode, set the port 3 control registers 0 and 1 (P3CON0 and P3CON1) to select any of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor.
At a system reset, high-impedance output mode is selected as the initial status.
In output mode, "L" or "H" level is output to each pin of Port 3 depending on the value set by the Port 3 data register (P3D).
In input mode, the input level of each pin of Port 3 can be read from the Port 3 data register (P3D).

20.3.2 Primary Function Other Than Input/Output Port

The successive approximation type A/D converter input (AIN0 to AIN3), comparator input (CMP0P/N, CMP1P/N), or external interrupt input (EXI30 to EXI37) can be assigned to the port 3 as the primary function other than the input/output port.
To use the port as the successive approximation type A/D converter input (AIN0 to AIN3) or comparator input (CMP0P/N, CMP1P/N), set the appropriate port as high-impedance output.
To use the port as the external interrupt input (EXI30 to EXI37), set the appropriate port to the input state.

20.3.3 Secondary to Quartic Functions

The I2C bus pin (SDA0/1, SCL0/1), buzzer output (MD0), synchronous serial port pin (SIN0, SCK0, SOUT0), synchronous serial port with FIFO pin (SINF0, SCKF0, SOUTF0, SSF0), UART pin (RXD0, TXD0), UART with FIFO pin (RXDF0, TXDF0), and FTM output pin (TMOUT4/5/6/7) are assigned to the port 3 as the secondary, tertiary, or quartic function. Each of them can be used as the tertiary or quartic function by setting the P37MD0 to P30MD0 and P37MD1 to P30MD1 bits of the port 3 mode register (P3MOD0, P3MOD1).

Chapter 21

Port 4

21 Port 4

21.1 General Description

This LSI includes an 8-bit input/output port, port 4 (P40 to P47).
It can function as an external interrupt, as well as an I^2C bus, a buzzer output, low/high speed clock output, a synchronous serial port, a synchronous serial port with FIFO, a UART, a UART with FIFO, and a timer out output pin as the secondary, tertiary, or quartic function.

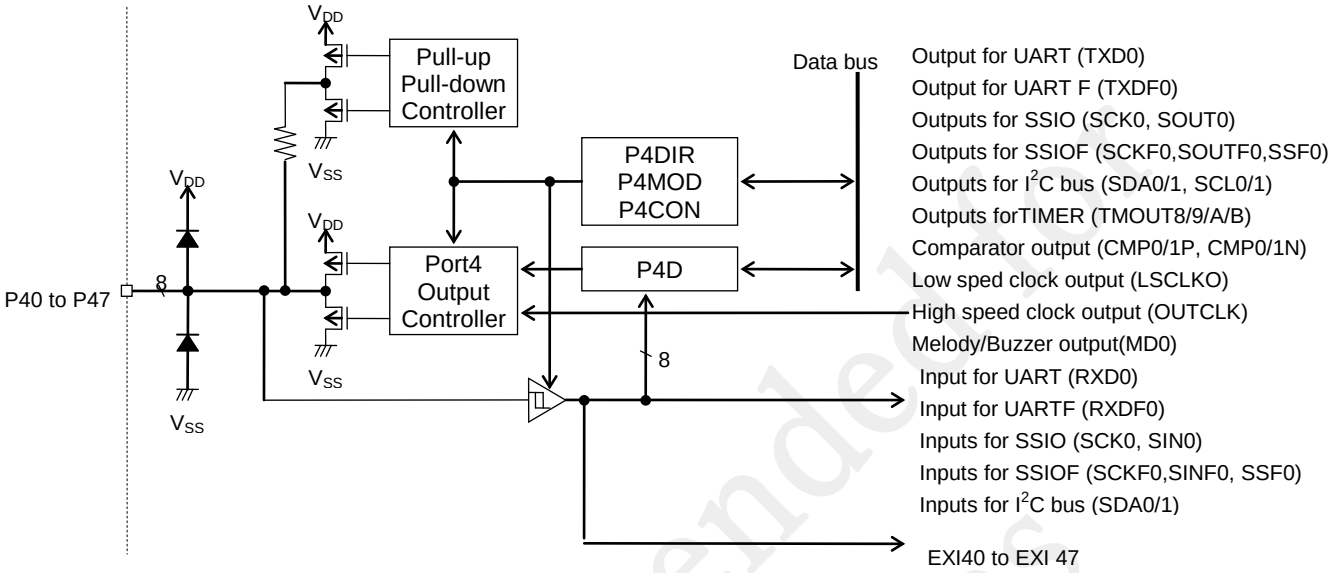
CLOCK :	Chapter 6 “Clock Generation Circuit”
TIMER:	Chapter 8 “Timers”
FTM:	Chapter 9 “Function Timer”
SSIO:	Chapter 11 “Synchronous Serial Port”
SSIOF:	Chapter 12 “SSIO with FIFO”
UART:	Chapter 13 “UART”
UARTF:	Chapter 14 “UART with FIFO”
I^2C :	Chapter 15 “I^2C Bus Interface”
MELODY:	Chapter 23 “Melody Driver”

21.1.1 Features

- Direct LED drive is available.
- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- Can be used as an external interrupt pin (EXI40, EXI41, EXI42, EXI43, EXI44, EXI45, EXI46, EXI47), Timer clock input (TMCKI0/1, TMCKI2/3), a Low speed clock output pin (LSCLKO), a high speed clock output pin (OUTCLK), an I^2C bus pin (SDA0/1, SCL0/1), a buzzer output (MD0), a synchronous serial port pin (SIN0, SCK0, SOUT0), a synchronous serial port with FIFO pin (SINF0, SCKF0, SOUTF0, SSF0), a UART pin (RXD0, TXD0), a UART with FIFO pin (RXDF0, TXDF0), or a FTM output pin (TMOUT8/9/A/B).

21.1.2 Configuration

Figure 21-1 shows the configuration of Port 4.



P4D : Port 4 data register
P4DIR : Port 4 direction register
P4CON : Port 4 control register
P4MOD : Port 4 mode register

Figure 21-1 Configuration of Port 4

21.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Quartic function
P40/EXI40/LED/ SDA0/ SOUT0/ RXD0	I/O	I/O port External interrupt LED direct drive	I^2C data I/O SDA0	Synchronous serial data output SOUT0	UART data input RXD0
P41/EXI41/LED/ SCL0/ SIN0/ TXD0	I/O	I/O port External interrupt LED direct drive	I^2C clock output SCL0	Synchronous serial data input SIN0	UART data output TXD0
P42/EXI42/ SCK0/ TMOUT8	I/O	I/O port External interrupt	–	Synchronous serial clock output SCK0	FTM output TMOUT8
P43/EXI43/ MD0/ TMOUT9	I/O	I/O port External interrupt	Melody/Buzzer output MD0	–	FTM output TMOUT9
P44/EXI44/ SDA1/ SOUTF0/ RXDF0	I/O	I/O port External interrupt	I^2C data I/O SDA1	Synchronous serial data with FIFO output SOUTF0	UART with FIFO data input RXDF0
P45/EXI45/ SCL1/ SINF0/ TXDF0	I/O	I/O port External interrupt	I^2C clock output SCL1	Synchronous serial data with FIFO input SINF0	UART with FIFO data output TXDF0
P46/EXI46/ LSCLKO/ SCKF0/ TMOUTA	I/O	I/O port External interrupt	Low speed clock output LSCLKO	Synchronous serial clock with FIFO output SCKF0	FTM output TMOUTA
P47/EXI47/ OUTCLK/ SSF0/ TMOUTB	I/O	I/O port External interrupt	High speed clock output OUTCLK	Synchronous serial chip with FIFO select output SSF0	FTM output TMOUTB

21.2 Description of Registers

21.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F230	Port 4 data register	P4D	–	R/W	8	00
0F231	Port 4 direction register	P4DIR	–	R/W	8	00
0F232	Port 4 control register	P4CON0	P4CON	R/W	8/16	00
0F233		P4CON1		R/W	8	00
0F234	Port 4 mode register	P4MOD0	P4MOD	R/W	8/16	00
0F235		P4MOD1		R/W	8	00

21.2.2 Port 4 Data Register (P4D)

Address: 0F230H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4D	P47D	P46D	P45D	P44D	P43D	P42D	P41D	P40D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4D is a special function register (SFR) to set the value to be output to the Port 4 pin or to read the input level of the Port 4. In output mode, the value of this register is output to the Port 4 pin. The value written to P4D is readable. In input mode, the input level of the Port 4 pin is read when P4D is read.
Output mode or input mode is selected by using the port mode register (P4DIR) described later.

Description of Bits

- **P47-40D** (bits 7 to 0)
  The P47-40D bits are used to set the output value of the Port 4 pin in output mode and to read the pin level of the Port 4 pin in input mode.

P40D	Description
0	Output or input level of the P40 pin: ”L”
1	Output or input level of the P40 pin: ”H”

P41D	Description
0	Output or input level of the P41 pin: ”L”
1	Output or input level of the P41 pin: ”H”

P42D	Description
0	Output or input level of the P42 pin: ”L”
1	Output or input level of the P42 pin: ”H”

P43D	Description
0	Output or input level of the P43 pin: ”L”
1	Output or input level of the P43 pin: ”H”

P44D	Description
0	Output or input level of the P44 pin: ”L”
1	Output or input level of the P44 pin: ”H”

P45D	Description
0	Output or input level of the P45 pin: ”L”
1	Output or input level of the P45 pin: ”H”

P46D	Description
0	Output or input level of the P46 pin: ”L”
1	Output or input level of the P46 pin: ”H”

P47D	Description
0	Output or input level of the P47 pin: ”L”
1	Output or input level of the P47 pin: ”H”

21.2.3 Port 4 Direction Register (P4DIR)

Address: 0F231H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P4DIR	P47DIR	P46DIR	P45DIR	P44DIR	P43DIR	P42DIR	P41DIR	P40DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4DIR is a special function register (SFR) to select the input/output mode of Port 4.

Description of Bits

- **P47-40DIR** (bits 7-0)
  The P47-40DIR bits are used to set the input/output mode of the port 4 pin.

P40DIR	Description
0	P40 pin: Output (initial value)
1	P40 pin: Input

P41DIR	Description
0	P41 pin: Output (initial value)
1	P41 pin: Input

P42DIR	Description
0	P42 pin: Output (initial value)
1	P42 pin: Input

P43DIR	Description
0	P43 pin: Output (initial value)
1	P43 pin: Input

P44DIR	Description
0	P44 pin: Output (initial value)
1	P44 pin: Input

P45DIR	Description
0	P45 pin: Output (initial value)
1	P45 pin: Input

P46DIR	Description
0	P46 pin: Output (initial value)
1	P46 pin: Input

P47DIR	Description
0	P47 pin: Output (initial value)
1	P47 pin: Input

21.2.4 Port 4 Control Register (P4CON)

Address: 0F232H
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
P4CON0	P47C0	P46C0	P45C0	P44C0	P43C0	P42C0	P41C0	P40C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
P4CON1	P47C1	P46C1	P45C1	P44C1	P43C1	P42C1	P41C1	P40C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4CON0 and P4CON1 are special function registers (SFRs) used to select the output state of the port 4 pin. The output state is different between input mode and output mode. Input or output is selected by using the P4DIR register.

Description of Bits

- **P47-40C0**(bits 7 to 0)**, P47-40C1** (bits 15 to 8)
  The P47-40C0 and P47-40C1 bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.
  To perform the direct LED drive, select N-channel open drain output mode.

Setting of P40 pin		When output mode is selected (P40DIR bit = "0")	When input mode is selected (P40DIR bit = "1")
P40C1	**P40C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P41 pin		When output mode is selected (P41DIR bit = "0")	When input mode is selected (P41DIR bit = "1")
P41C1	**P41C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P42 pin		When output mode is selected (P42DIR bit = “0”)	When input mode is selected (P42DIR bit = “1”)
P42C1	**P42C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P43 pin		When output mode is selected (P43DIR bit = “0”)	When input mode is selected (P43DIR bit = “1”)
P43C1	**P43C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P44 pin		When output mode is selected (P44DIR bit = “0”)	When input mode is selected (P44DIR bit = “1”)
P44C1	**P44C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P45 pin		When output mode is selected (P45DIR bit = “0”)	When input mode is selected (P45DIR bit = “1”)
P45C1	**P45C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P46 pin		When output mode is selected (P46DIR bit = “0”)	When input mode is selected (P46DIR bit = “1”)
P46C1	**P46C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P47 pin		When output mode is selected (P47DIR bit = “0”)	When input mode is selected (P47DIR bit = “1”)
P47C1	**P47C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

21.2.5 Port 4 Mode Register (P4MOD)

Address: 0F234H
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
P4MOD0	P47MD0	P46MD0	P45MD0	P44MD0	P43MD0	P42MD0	P41MD0	P40MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
P4MOD1	P47MD1	P46MD1	P45MD1	P44MD1	P43MD1	P42MD1	P41MD1	P40MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P4MOD0 and P4MOD1 are special function registers (SFRs) used to select the primary, secondary, tertiary, or quartic function of the port 4.

Description of Bits

- **P40MD1-0** (bits 8, 0)
  The P40MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P40 pin.

P40MD1	P40MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	I^2C bus data input/output mode (SDA0)
1	0	Synchronous serial port data output mode (SOUT0)
1	1	UART data input mode (RXD0)

- **P41MD1-0** (bits 9, 1)
  The P41MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P41 pin.

P41MD1	P41MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	I^2C bus clock output mode (SCL0)
1	0	Synchronous serial port data input mode (SIN0)
1	1	UART data output mode (TXD0)

- **P42MD1-0** (bits 10, 2)
  The P42MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P42 pin.

P42MD1	P42MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	Prohibited
1	0	Synchronous serial port clock input/output mode (SCK0)
1	1	FTM output mode (TMOUT8)

- **P43MD1-0** (bits 11, 3)
  The P43MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P43 pin.

P43MD1	P43MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	Melody/Buzzer output mode (MD0)
1	0	Prohibited
1	1	FTM output mode (TMOUT9)

- **P44MD1-0** (bits 12, 4)
  The P44MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P44 pin.

P44MD1	P44MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	I^2C bus data input/output mode (SDA1)
1	0	Synchronous serial port with FIFO data output mode (SOUTF0)
1	1	UART with FIFO data input mode (RXDF0)

- **P45MD1-0** (bits 13, 5)
  The P45MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P45 pin.

P45MD1	P45MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	I^2C bus clock output mode (SCL1)
1	0	Synchronous serial port with FIFO data input mode (SINF0)
1	1	UART with FIFO data output mode (TXDF0)

- **P46MD1-0** (bits 14, 6)
  The P46MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P46 pin.

P46MD1	P46MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	Low speed clock output mode(LSCLKO)
1	0	Synchronous serial port with FIFO clock input/output mode (SCKF0)
1	1	FTM output mode (TMOUTA)

- **P47MD1-0** (bits 15, 7)
  The P47MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P47 pin.

P47MD1	P47MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	High speed clock output mode (OUTCLK)
1	0	Synchronous serial port with FIFO chip select input/output mode (SSF0)
1	1	FTM output mode (TMOUTB)

[Note]
When the pin is set to "Prohibited" and the output mode is selected (by the Port 4 control register), the Port 4 output pin state is fixed as follows regardless of the data of the port data register P4D:

When high-impedance output is selected: Output pin is high-impedance
When P-channel open drain output is selected: Output pin is high-impedance
When N-channel open drain output is selected: Output pin is fixed to "L"
When CMOS output is selected: Output pin is fixed to "L"

21.3 Description of Operation

21.3.1 Input/Output Port Functions

For each pin of Port 4, either output or input is selected by setting the Port 4 direction register (P4DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 4 control registers 0 and 1 (P4CON0 and P4CON1).
In the input mode, set the port 4 control registers 0 and 1 (P4CON0 and P4CON1) to select any of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor.
At a system reset, high-impedance output mode is selected as the initial status.
In output mode, "L" or "H" level is output to each pin of Port 4 depending on the value set by the Port 4 data register (P4D).
In input mode, the input level of each pin of Port 4 can be read from the Port 4 data register (P4D).

21.3.2 Primary Function Other Than Input/Output Port

The external interrupt input (EXI40 to EXI47) can be assigned to the port 4 as the primary function other than the input/output port.

21.3.3 Secondary to Quartic Functions

The I2C bus pin (SDA0/1, SCL0/1), Melody/Buzzer output (MD0), low speed clock(LSCLKO), high speed clock (OUTCLK), synchronous serial port pin (SIN0, SCK0, SOUT0), synchronous serial port with FIFO pin (SINF0, SCKF0, SOUTF0, SSF0), UART pin (RXD0, TXD0), UART with FIFO pin (RXDF0, TXDF0), and timer out output pin (TMOUT8/9/A/B) are assigned to the port 4 as the secondary, tertiary, or quartic function. Each of them can be used as the tertiary or quartic function by setting the P47MD0 to P40MD0 and P47MD1 to P40MD1 bits of the port 4 mode register (P4MOD0, P4MOD1).

Output frequency of High speed clock output can be selected by frequency control register 0 (FCON0) OUTC2 to OUTC0. See Chapter 6 "Clock Generation Circuit".

Chapter 22

Port 5

22 Port 5

22.1 General Description

This LSI includes an 8-bit input/output port, port 5 (P50 to P57).
It can function as an external interrupt, a timer clock input, as well as an I^2C bus, a buzzer output, a synchronous serial port, a synchronous serial port with FIFO, a UART, a UART with FIFO, and a timer out output pin as the secondary, tertiary, or quartic function.

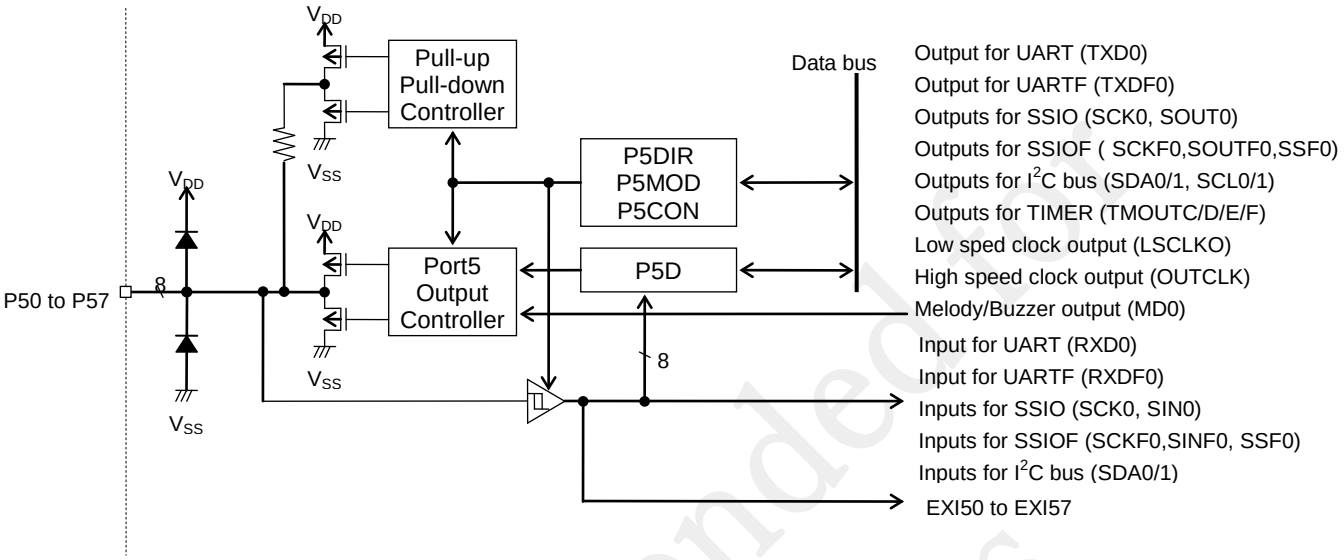
CLOCK :	Chapter 6 “Clock Generation Circuit”
TIMER:	Chapter 8 “Timers”
FTM:	Chapter 9 “Function Timer”
SSIO:	Chapter 11 “Synchronous Serial Port”
SSIOF:	Chapter 12 “SSIO with FIFO”
UART:	Chapter 13 “UART”
UARTF:	Chapter 14 “UART with FIFO”
I^2C :	Chapter 15 “I^2C Bus Interface”
MELODY:	Chapter 23 “Melody Driver”

22.1.1 Features

- Direct LED drive is available.
- Allows selection of high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output for each bit in output mode.
- Allows selection of high-impedance input, input with a pull-down resistor, or input with a pull-up resistor for each bit in input mode.
- Can be used as an external interrupt pin (EXI50, EXI51, EXI52, EXI53, EXI54, EXI55, EXI56, EXI57), Timer clock input (TMCKI4/5, TMCKI6/7), a Low speed clock output pin (LSCLKO), a high speed clock output pin (OUTCLK), an I^2C bus pin (SDA0/1, SCL0/1), a buzzer output (MD0), a synchronous serial port pin (SIN0, SCK0, SOUT0), a synchronous serial port with FIFO pin (SINF0, SCKF0, SOUTF0, SSF0), a UART pin (RXD0, TXD0), a UART with FIFO pin (RXDF0, TXDF0), or a FTM output pin (TMOUTC/D/E/F).

22.1.2 Configuration

Figure 22-1 shows the configuration of Port 5.



P5D : Port 5 data register
P5DIR : Port 5 direction register
P5CON : Port 5 control register
P5MOD : Port 5 mode register

Figure 22-1 Configuration of Port 5

22.1.3 List of Pins

Pin name	I/O	Primary function	Secondary function	Tertiary function	Quartic function
P50/EXI50/ SDA0/ SOUT0/ RXD0	I/O	I/O port External interrupt	I^2C data I/O SDA0	Synchronous serial data output SOUT0	UART data input RXD0
P51/EXI51/ SCL0/ SIN0/ TXD0	I/O	I/O port External interrupt	I^2C clock output SCL0	Synchronous serial data input SIN0	UART data output TXD0
P52/EXI52/ LED/ SCK0/ TMOUTC	I/O	I/O port External interrupt LED direct drive	–	Synchronous serial clock output SCK0	FTM output TMOUTC
P53/EXI53/ LED/ MD0/ TMOUTD	I/O	I/O port External interrupt LED direct drive	Melody/Buzzer output MD0	–	FTM output TMOUTD
P54/EXI54/ SDA1/ SOUTF0/ RXDF0	I/O	I/O port External interrupt	I^2C data I/O SDA1	Synchronous serial data with FIFO output SOUTF0	UART with FIFO data input RXDF0
P55/EXI55/ SCL1/ SINF0/ TXDF0	I/O	I/O port External interrupt	I^2C clock output SCL1	Synchronous serial data with FIFO input SINF0	UART with FIFO data output TXDF0
P56/EXI56/ LSCLK/ SCKF0/ TMOUTE	I/O	I/O port External interrupt	Low speed clock output LSCLKO	Synchronous serial clock with FIFO output SCKF0	FTM output TMOUTE
P57/EXI57/ OUTCLK/ SSF0/ TMOUTF	I/O	I/O port External interrupt	High speed clock output OUTCLK	Synchronous serial chip with FIFO select output SSF0	FTM output TMOUTF

22.2 Description of Registers

22.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F238	Port 5 data register	P5D	–	R/W	8	00
0F239	Port 5 direction register	P5DIR	–	R/W	8	00
0F23A	Port 5 control register	P5CON0	P5CON	R/W	8/16	00
0F23B		P5CON1		R/W	8	00
0F23C	Port 5 mode register	P5MOD0	P5MOD	R/W	8/16	00
0F23D		P5MOD1		R/W	8	00

22.2.2 Port 5 Data Register (P5D)

Address: 0F238H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P5D	P57D	P56D	P55D	P54D	P53D	P52D	P51D	P50D
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5D is a special function register (SFR) to set the value to be output to the Port 5 pin or to read the input level of the Port 5. In output mode, the value of this register is output to the Port 5 pin. The value written to P5D is readable. In input mode, the input level of the Port 5 pin is read when P5D is read.
Output mode or input mode is selected by using the port mode register (P5DIR) described later.

Description of Bits

- **P57-50D** (bits 7 to 0)
  The P57-50D bits are used to set the output value of the Port 5 pin in output mode and to read the pin level of the Port 5 pin in input mode.

P50D	Description
0	Output or input level of the P50 pin: ”L”
1	Output or input level of the P50 pin: ”H”

P51D	Description
0	Output or input level of the P51 pin: ”L”
1	Output or input level of the P51 pin: ”H”

P52D	Description
0	Output or input level of the P52 pin: ”L”
1	Output or input level of the P52 pin: ”H”

P53D	Description
0	Output or input level of the P53 pin: ”L”
1	Output or input level of the P53 pin: ”H”

P54D	Description
0	Output or input level of the P54 pin: ”L”
1	Output or input level of the P54 pin: ”H”

P55D	Description
0	Output or input level of the P55 pin: ”L”
1	Output or input level of the P55 pin: ”H”

P56D	Description
0	Output or input level of the P56 pin: ”L”
1	Output or input level of the P56 pin: ”H”

P57D	Description
0	Output or input level of the P57 pin: ”L”
1	Output or input level of the P57 pin: ”H”

22.2.3 Port 5 Direction Register (P5DIR)

Address: 0F239H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
P5DIR	P57DIR	P56DIR	P55DIR	P54DIR	P53DIR	P52DIR	P51DIR	P50DIR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5DIR is a special function register (SFR) to select the input/output mode of Port 5.

Description of Bits

- **P57-50DIR** (bits 7 to 0)
  The P57-50DIR bits are used to set the input/output mode of the port 5 pin.

P50DIR	Description
0	P50 pin: Output (initial value)
1	P50 pin: Input

P51DIR	Description
0	P51 pin: Output (initial value)
1	P51 pin: Input

P52DIR	Description
0	P52 pin: Output (initial value)
1	P52 pin: Input

P53DIR	Description
0	P53 pin: Output (initial value)
1	P53 pin: Input

P54DIR	Description
0	P54 pin: Output (initial value)
1	P54 pin: Input

P55DIR	Description
0	P55 pin: Output (initial value)
1	P55 pin: Input

P56DIR	Description
0	P56 pin: Output (initial value)
1	P56 pin: Input

P57DIR	Description
0	P57 pin: Output (initial value)
1	P57 pin: Input

[Note]
The P50 to P57 pins are assigned to successive approximation type A/D converter input. If it is used as a successive approximation type A/D converter input, set the appropriate port to the output mode.

22.2.4 Port 5 Control Register (P5CON)

Address: 0F23AH
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
P5CON0	P57C0	P56C0	P55C0	P54C0	P53C0	P52C0	P51C0	P50C0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
P5CON1	P57C1	P56C1	P55C1	P54C1	P53C1	P52C1	P51C1	P50C1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5CON0 and P5CON1 are special function registers (SFRs) used to select the output state of the port 5 pin. The output state is different between input mode and output mode. Input or output is selected by using the P5DIR register.

Description of Bits

- **P57-50C0** (bits 7 to 0)**, P57-50C1** (bits 15 to 8)
  The P57-50C0 and P57-50C1 bits are used to select high-impedance output, P-channel open drain output, N-channel open drain output, or CMOS output in output mode and to select high-impedance input, input with a pull-down resistor, or input with a pull-up resistor in input mode.
  To perform the direct LED drive, select N-channel open drain output mode.

Setting of P50 pin		When output mode is selected (P50DIR bit = “0”)	When input mode is selected (P50DIR bit = “1”)
P50C1	**P50C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P51 pin		When output mode is selected (P51DIR bit = “0”)	When input mode is selected (P51DIR bit = “1”)
P51C1	**P51C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P52 pin		When output mode is selected (P52DIR bit = “0”)	When input mode is selected (P52DIR bit = “1”)
P52C1	**P52C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P53 pin		When output mode is selected (P53DIR bit = “0”)	When input mode is selected (P53DIR bit = “1”)
P53C1	**P53C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P54 pin		When output mode is selected (P54DIR bit = “0”)	When input mode is selected (P54DIR bit = “1”)
P54C1	**P54C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P55 pin		When output mode is selected (P55DIR bit = “0”)	When input mode is selected (P55DIR bit = “1”)
P55C1	**P55C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P56 pin		When output mode is selected (P56DIR bit = “0”)	When input mode is selected (P56DIR bit = “1”)
P56C1	**P56C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

Setting of P57 pin		When output mode is selected (P57DIR bit = “0”)	When input mode is selected (P57DIR bit = “1”)
P57C1	**P57C0**	Description	
0	0	High-impedance output (initial value)	High-impedance input
0	1	P-channel open drain output	Input with a pull-down resistor
1	0	N-channel open drain output	Input with a pull-up resistor
1	1	CMOS output	High-impedance input

[Note]
The P50 to P53 pins are assigned to successive approximation type A/D converter input. If it is used as a successive approximation type A/D converter input, set the appropriate port to the high-impedance output mode.

22.2.5 Port 5 Mode Register (P5MOD)

Address: 0F23CH
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
P5MOD0	P57MD0	P56MD0	P55MD0	P54MD0	P53MD0	P52MD0	P51MD0	P50MD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
P5MOD1	P57MD1	P56MD1	P55MD1	P54MD1	P53MD1	P52MD1	P51MD1	P50MD1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

P5MOD0 and P5MOD1 are special function registers (SFRs) used to select the primary, secondary, tertiary, or quartic function of the port 5.

Description of Bits

- **P50MD1-0** (bits 8, 0)
  The P50MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P50 pin.

P50MD1	P50MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	I^2C bus data input/output mode (SDA0)
1	0	Synchronous serial port data output mode (SOUT0)
1	1	UART data input mode (RXD0)

- **P51MD1-0** (bits 9, 1)
  The P51MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P51 pin.

P51MD1	P51MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	I^2C bus clock output mode (SCL0)
1	0	Synchronous serial port data input mode (SIN0)
1	1	UART data output mode (TXD0)

- **P52MD1-0** (bits 10, 2)
  The P52MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P52 pin.

P52MD1	P52MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	Prohibited
1	0	Synchronous serial port clock input/output mode (SCK0)
1	1	FTM output mode (TMOUTC)

- **P53MD1-0** (bits 11, 3)
  The P53MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P53 pin.

P53MD1	P53MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	Buzzer output mode (MD0)
1	0	Prohibited
1	1	FTM output mode (TMOUTD)

- **P54MD1-0** (bits 12, 4)
  The P54MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P54 pin.

P54MD1	P54MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	I^2C bus data input/output mode (SDA1)
1	0	Synchronous serial port with FIFO data output mode (SOUTF0)
1	1	UART with FIFO data input mode (RXDF0)

- **P55MD1-0** (bits 13, 5)
  The P55MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P55 pin.

P55MD1	P55MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	I^2C bus clock output mode (SCL1)
1	0	Synchronous serial port with FIFO data input mode (SINF0)
1	1	UART with FIFO data output mode (TXDF0)

- **P56MD1-0** (bits 14, 6)
  The P56MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P56 pin.

P56MD1	P56MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	Low speed clock output mode(LSCLKO)
1	0	Synchronous serial port with FIFO clock input/output mode (SCKF0)
1	1	FTM output mode (TMOUTE)

- **P57MD1-0** (bits 15, 7)
  The P57MD1-0 bits are used to select the primary, secondary, tertiary, or quartic function of the P57 pin.

P57MD1	P57MD0	Description
0	0	General-purpose input/output mode, External interrupt mode (initial value)
0	1	High speed clock output mode (OUTCLK)
1	0	Synchronous serial port with FIFO chip select input/output mode (SSF0)
1	1	FTM output mode (TMOUTF)

[Note]
When the pin is set to “Prohibited” and the output mode is selected (by the Port 5 control register), the Port 5 output pin state is fixed as follows regardless of the data of the port data register P5D:

When high-impedance output is selected: Output pin is high-impedance
When P-channel open drain output is selected: Output pin is high-impedance
When N-channel open drain output is selected: Output pin is fixed to “L”
When CMOS output is selected: Output pin is fixed to “L”

22.3 Description of Operation

22.3.1 Input/Output Port Functions

For each pin of Port 5, either output or input is selected by setting the Port 5 direction register (P5DIR).
In output mode, high-impedance output mode, P-channel open drain output mode, N-channel open drain output mode, or CMOS output mode can be selected by setting the Port 5 control registers 0 and 1 (P5CON0 and P5CON1).
In the input mode, set the port 5 control registers 0 and 1 (P5CON0 and P5CON1) to select any of high-impedance input mode, input mode with a pull-down resistor, or input mode with a pull-up resistor.
At a system reset, high-impedance output mode is selected as the initial status.
In output mode, "L" or "H" level is output to each pin of Port 5 depending on the value set by the Port 5 data register (P5D).
In input mode, the input level of each pin of Port 5 can be read from the Port 5 data register (P5D).

22.3.2 Primary Function Other Than Input/Output Port

The external interrupt input (EXI50 to EXI57) can be assigned to the port 5 as the primary function other than the input/output port.

22.3.3 Secondary to Quartic Functions

The I2C bus pin (SDA0/1, SCL0/1), buzzer output (MD0), Low speed clock output (LSCLKO), High speed clock output (OUTCLK), synchronous serial port pin (SIN0, SCK0, SOUT0), synchronous serial port with FIFO pin (SINF0, SCKF0, SOUTF0, SSF0), UART pin (RXD0, TXD0), UART with FIFO pin (RXDF0, TXDF0), and timer out output pin (TMOUTC/D/E/F) are assigned to the port 5 as the secondary, tertiary, or quartic function. Each of them can be used as the tertiary or quartic function by setting the P57MD0 to P50MD0 and P57MD1 to P50MD1 bits of the port 5 mode register (P5MOD0, P5MOD1).

Output frequency of High speed clock output can be selected by frequency control register 0 (FCON0) OUTC2 to OUTC0. See Chapter 6 "clock generation circuit".

Chapter 23

Melody Driver

23 Melody Driver

23.1 Overview

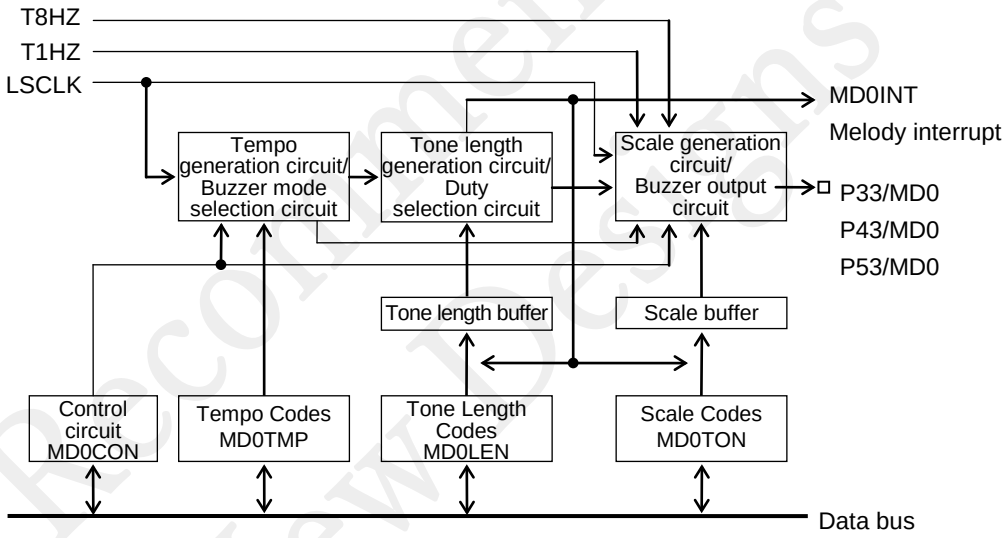
This LSI includes one channel of the melody driver.
To use the melody driver, the secondary function of Port 3 or Port 4 or Port 5 should be set. For the respective port setting, see Chapter 20, "Port 3", Chapter 21, "Port 4" and Chapter 22, "Port 5". For the clock to be used in this block, see Chapter 6, "Clock Generation Circuit".

23.1.1 Features

- In melody output mode, 29 scales (melody audio frequency: 508Hz to 10.922kHz), 63 tone lengths, and 15 tempos are available.
- In buzzer output mode, 4 output modes, 8 frequencies, and 15 duty levels (7 duty levels when buzzer frequency = 4.096kHz) are available.

23.1.2 Configuration

Figure 23-1 shows the configuration of the melody driver.



MD0CON : Melody 0 control register
MD0TMP : Melody 0 tempo code register
MD0TON : Melody 0 scale code register
MD0LEN : Melody 0 tone length code register

Figure 23-1 Configuration of Melody Driver

23.1.3 List of Pins

Pin name	I/O	Function
MD0	O	Melody 0 signal output pin

23.2 Description of Registers

23.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F8C0	Melody 0 control register	MD0CON	–	R/W	8	00
0F8C1	Melody 0 tempo code register	MD0TMP	–	R/W	8	00
0F8C2	Melody 0 scale/tone length code register	MD0TON	MD0TL	R/W	8/16	00
0F8C3		MD0LEN		R/W	8	00

23.2.2 Melody 0 Control Register (MD0CON)

Address: 0F8C0H
Access: R/W
Access size: 8 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
MD0CON	–	–	–	–	–	–	BZMD	M0RUN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

MD0CON is a special function register (SFR) to control the melody and the buzzer.

Description of Bits

- **M0RUN** (bit 0)
  The M0RUN bit is used to control start/stop of the MD0 output.

M0RUN	Description
0	Stops MD0 output. (Initial value)
1	Starts MD0 output.

- **BZMD** (bit 1)
  The BZMD bit is used to select melody mode or buzzer mode.

BZMD	Description
0	Melody mode (initial value)
1	Buzzer mode

23.2.3 Melody 0 Tempo Code Register (MD0TMP)

Address: 0F8C1H
Access: R/W
Access size: 8 bit
Initial value: 00H

	7	6	5	4	3	2	1	0
MD0TMP	–	–	–	–	M0TM3	M0TM2	M0TM1	M0TM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

MD0TMP is a special function register (SFR) to set the tempo code of a melody in the melody mode, or a buzzer output waveform type in the buzzer mode.

Description of Bits

- **M0TM3-0** (bits 3 to 0)

When melody mode is selected (BZMD bit = "0")				
M0TM3	**M0TM2**	**M0TM1**	**M0TM0**	Description
0	0	0	0	♪ =480 (initial value)
0	0	0	1	♪ =480
0	0	1	0	♪ =320
0	0	1	1	♪ =240
0	1	0	0	♪ =192
0	1	0	1	♪ =160
0	1	1	0	♪ ≅137
0	1	1	1	♪ =120
1	0	0	0	♪ ≅107
1	0	0	1	♪ =96
1	0	1	0	♪ ≅87
1	0	1	1	♪ =80
1	1	0	0	♪ ≅74
1	1	0	1	♪ ≅69
1	1	1	0	♪ =64
1	1	1	1	♪ =60

When buzzer mode is selected (BZMD bit = "1")				
M0TM3	**M0TM2**	**M0TM1**	**M0TM0**	Description
*	*	0	0	Intermittent sound 1 output (initial value)
*	*	0	1	Intermittent sound 2 output
*	*	1	0	Single sound output
*	*	1	1	Continuous sound output

[Note]
For melody output, use the low speed clock(LSCLK).

23.2.4 Melody 0 Scale/Tone Length Code Register (MD0TL)

Address: 0F8C2H
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
MD0TON	–	M0TN6	M0TN5	M0TN4	M0TN3	M0TN2	M0TN1	M0TN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
MD0LEN	–	–	M0LN5	M0LN4	M0LN3	M0LN2	M0LN1	M0LN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

MD0TL is a special function register (SFR) to set the scale code and tone length of a melody when melody mode is selected, and a buzzer output frequency and duties when buzzer mode is selected.

Description of Bits

- **M0TN6-0** (bits 6 to 0)

When melody mode is selected (BZMD bit = “0”)	
M0TN6 to 0	Description
	Sets the corresponding scale code.

For scale codes, see Section 23.3.4, "Scale Codes".

When buzzer mode is selected (BZMD bit = “1”)				
M0TN6 to M0TN3	**M0TN2**	**M0TN1**	**M0TN0**	Description
*	0	0	0	4.096 kHz (initial value)
*	0	0	1	2.048kHz
*	0	1	0	1.024kHz
*	0	1	1	683Hz
*	1	0	0	512Hz
*	1	0	1	410Hz
*	1	1	0	341Hz
*	1	1	1	293Hz

[Note]
In buzzer mode, the M0TN6 to M0TN3 bits are not used (Don't care).

- **M0LN5-0** (bits 13 to 8)

When melody mode is selected (BZMD bit = “0”)	
M0LN5 to M0LN0	Description
	Sets the corresponding tone length code.

For tone length codes, see Section 23.3.3, "Tone Length Codes".

When buzzer mode is selected (BZMD bit = “1”)						
M0LN5 to L0LN4	**M0LN3**	**M0LN2**	**M0LN1**	**M0LN0**	Description	
					Buzzer frequency = 4.096kHz	Buzzer frequency ≠ 4.096kHz
*	0	0	0	0	1/8 DUTY (initial value)	1/16 DUTY (initial value)
*	0	0	0	1	1/8DUTY	1/16DUTY
*	0	0	1	0	1/8DUTY	2/16DUTY
*	0	0	1	1	1/8DUTY	3/16DUTY
*	0	1	0	0	2/8DUTY	4/16DUTY
*	0	1	0	1	2/8DUTY	5/16DUTY
*	0	1	1	0	3/8DUTY	6/16DUTY
*	0	1	1	1	3/8DUTY	7/16DUTY
*	1	0	0	0	4/8DUTY	8/16DUTY
*	1	0	0	1	4/8DUTY	9/16DUTY
*	1	0	1	0	5/8DUTY	10/16DUTY
*	1	0	1	1	5/8DUTY	11/16DUTY
*	1	1	0	0	6/8DUTY	12/16DUTY
*	1	1	0	1	6/8DUTY	13/16DUTY
*	1	1	1	0	7/8DUTY	14/16DUTY
*	1	1	1	1	7/8DUTY	15/16DUTY

[Note]
In buzzer mode, values of the M0LN5 and M0LN4 bits are not used (Don't care).

23.3 Description of Operation

23.3.1 Operation of Melody Output

Melody is output in the following procedure.

(1) Select melody mode by setting the BZMD bit of the melody 0 control register (MD0CON) to “0”.
(2) Set a melody tempo in the melody 0 tempo code register (MD0TMP).
(3) Set a tone length code in the melody 0 tone length code register (MD0LEN).
(4) Set a scale code in the melody 0 scale code register (MD0TON).
(5) When the M0RUN bit of the melody 0 control register (MD0CON) is set to “1”, the tone length code and scale code are transferred to the tone length buffer and scale buffer and melody output is started from the MD0 pin. At the same time, a melody 0 interrupt (MD0INT) is requested. When an interrupt occurs and program is passed to the interrupt routine, the interrupt request flag is cleared.

The melody 0 signal output pin (MD0) is assigned as the secondary function of Port 3 or Port 4 or Port 5. For the secondary function of Port 3 or Port 4 or Port 5, see Chapter 20, "Port 3" or Chapter 21, "Port 4", Chapter 22, "Port 5".

In the software processing after melody 0 interrupt, the tone length code and the scale code of the note that are output next are set to MD0LEN and MD0TON, respectively. When there is no next note to be output, rest data “00H” is set in MD0TON, the M0RUN bit is set to “0” by the software processing after the next melody 0 interrupt, and melody output is terminated.

By setting the M0RUN bit to “0”, melody can be terminated forcibly during melody output.

Figure 23-2 shows the operation waveform of the melody driver.

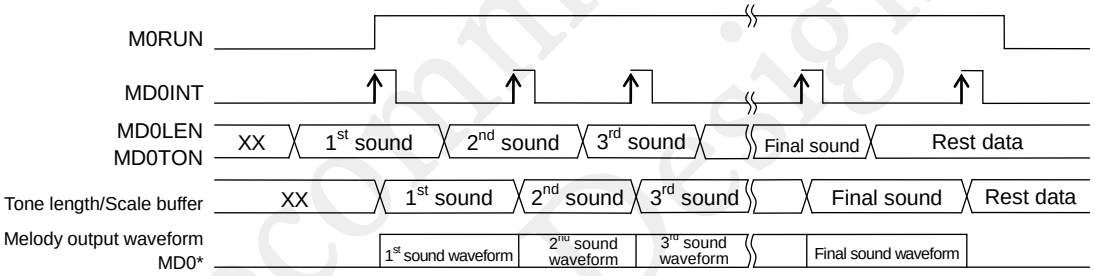


Figure 23-2 Operation Waveform of Melody Driver

23.3.2 Example of Using Melody Circuit

Figure 23-3 shows an example of a melody notation, and Table 23-1 shows note codes of melody examples.

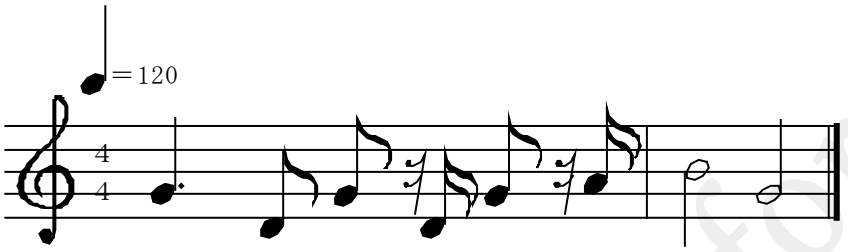


Figure 23-3 Example of Melody Notation

Table 23-1 Note Codes of Melody Examples

Note	Note code													
	MD0LEN						MD0TON							Hexadecimal
	5	4	3	2	1	0	6	5	4	3	2	1	0	
G^2	1	0	1	1	1	1	0	1	0	1	0	0	1	2F29H
D^2	0	0	1	1	1	1	0	1	1	0	1	1	0	0F36H
G^2	0	0	1	1	1	1	0	1	0	1	0	0	1	0F29H
—	0	0	0	1	1	1	0	0	0	0	0	0	0	0700H
D^2	0	0	0	1	1	1	0	1	1	0	1	1	0	0736H
G^2	0	0	1	1	1	1	0	1	0	1	0	0	1	0F29H
—	0	0	0	1	1	1	0	0	0	0	0	0	0	0700H
A^2	0	0	0	1	1	1	0	1	0	0	1	0	0	0724H
B^2	1	1	1	1	1	1	0	1	0	0	0	0	0	3F20H
G^2	1	1	1	1	1	1	0	1	0	1	0	0	1	3F29H

23.3.3 Tempo Codes

A tempo code is set in the melody 0 tempo code register (MD0TMP).
Table 23-2 shows the correspondence between tempos (number of counts for one minute) and tempo codes.
The tempo when all the bits are set to "0" is equal to the shortest tone length (the tempo when the only M0TP0 bit is set to "1").

Table 23-2 Correspondence between Tempos and Tempo Codes

Tempo	Tempo code (MD0TMP)				
	M0TP3	M0TP2	M0TP1	M0TP0	M0TP3□0
♩ = 480	0	0	0	0	0H
♩ = 480	0	0	0	1	1H
♩ = 320	0	0	1	0	2H
♩ = 240	0	0	1	1	3H
♩ = 192	0	1	0	0	4H
♩ = 160	0	1	0	1	5H
♩ ≅ 137	0	1	1	0	6H
♩ = 120	0	1	1	1	7H
♩ ≅ 107	1	0	0	0	8H
♩ = 96	1	0	0	1	9H
♩ ≅ 87	1	0	1	0	AH
♩ = 80	1	0	1	1	BH
♩ ≅ 74	1	1	0	0	CH
♩ ≅ 69	1	1	0	1	DH
♩ = 64	1	1	1	0	EH
♩ = 60	1	1	1	1	FH

23.3.4 Tone Length Codes

A tone length code is set in the melody 0 tone length code register (MD0LEN).
Table 23-3 shows the correspondence between tone lengths and tone length codes.
The tone length when all the bits are set to "0" is equal to the shortest tone length (the tone length when the only M0LN0 bit is set to "1").

Table 23-3 Correspondence between Tone Lengths and Tone Length Codes

Tone length	Tone length code (MD0LEN)						
	M0LN5	M0LN4	M0LN3	M0LN2	M0LN1	M0LN1	M0LN5□0
	1	1	1	1	1	1	3FH
	1	0	1	1	1	1	2FH
	0	1	1	1	1	1	1FH
	0	1	0	1	1	1	17H
	0	0	1	1	1	1	0FH
	0	0	1	0	1	1	0BH
	0	0	0	1	1	1	07H
	0	0	0	1	0	1	05H
	0	0	0	0	1	1	03H
	0	0	0	0	1	0	02H
	0	0	0	0	0	1	01H

The tone length set by a tone length code and a tempo code is expressed by the following equation.

Tone length = 1.953125 x (TP + 1) x (LN + 1) ms ,
where TP is an integer of 1 to 15, and LN is an integer of 1 to 63.

The bit correspondence between TP and tempo codes is expressed by the following equation.

$TP = 2^3M0TP3 + 2^2M0TP2 + 2^1M0TP1 + 2^0M0TP0$

The bit correspondence between LN and tone length codes is expressed by the following equation.

$LN = 2^5M0LN5 + 2^4M0LN4 + 2^3M0LN3 + 2^2M0LN2 + 2^1M0LN1 + 2^0M0LN0$

23.3.5 Scale Codes

A scale code is set in the melody 0 scale code register (MD0TON).
In the melody driver, a frequency that can be output is expressed by the following equation.

$$\frac{65536}{(TN + 1)} \text{ Hz} \quad \text{(where TN is an integer of 4 to 127.)}$$

The bit correspondence between TN and scale codes is expressed by the following equation.

$$TN = 2^6M0TN6 + 2^5M0TN5 + 2^4M0TN4 + 2^3M0TN3 + 2^2M0TN2 + 2^1M0TN1 + 2^0M0TN0$$

Table 23-4 shows the correspondence between scales and scale codes.
When the M0TN6 to M0TN2 bits are set to "0", scale becomes a rest. The rest length is set by the tone length code (MD0LEN).

Table 23-4 Correspondence between Scales and Scale Codes

Scale	Frequency (Hz)	Scale code (MD0TON)							
		M0TN6	M0TN5	M0TN4	M0TN3	M0TN2	M0TN1	M0TN0	M0TN6□0
C^1	529	1	1	1	1	0	1	1	7BH
Cis^1	560	1	1	1	0	1	0	0	74H
D^1	590	1	1	0	1	1	1	0	6EH
Dis^1	624	1	1	0	1	0	0	0	68H
E^1	662	1	1	0	0	0	1	0	62H
F^1	705	1	0	1	1	1	0	0	5CH
Fis^1	745	1	0	1	0	1	1	1	57H
G^1	790	1	0	1	0	0	1	0	52H
Gis^1	840	1	0	0	1	1	0	1	4DH
A^1	886	1	0	0	1	0	0	1	49H
Ais^1	936	1	0	0	0	1	0	1	45H
B^1	993	1	0	0	0	0	0	1	41H
C^2	1057	0	1	1	1	1	0	1	3DH
Cis^2	1111	0	1	1	1	0	1	0	3AH
D^2	1192	0	1	1	0	1	1	0	36H
Dis^2	1260	0	1	1	0	0	1	1	33H
E^2	1338	0	1	1	0	0	0	0	30H
F^2	1394	0	1	0	1	1	1	0	2EH
Fis^2	1490	0	1	0	1	0	1	1	2BH
G^2	1560	0	1	0	1	0	0	1	29H
Gis^2	1680	0	1	0	0	1	1	0	26H
A^2	1771	0	1	0	0	1	0	0	24H
Ais^2	1872	0	1	0	0	0	1	0	22H
B^2	1986	0	1	0	0	0	0	0	20H
C^3	2114	0	0	1	1	1	1	0	1EH
D^3	2341	0	0	1	1	0	1	1	1BH
Dis^3	2521	0	0	1	1	0	0	1	19H
E^3	2621	0	0	1	1	0	0	0	18H
Fis^3	2979	0	0	1	0	1	0	1	15H

23.3.6 Operations of Buzzer Output

A buzzer sound is output in the following procedure.
(1) Select a buzzer mode by setting the BZMD bit of the melody 0 control register (MD0CON) to "1".
(2) Select a buzzer output mode using the melody 0 tempo code register (MD0TMP).
(3) Select a duty of the High level width of the buzzer output waveform using the melody 0 tone length code register (MD0LEN).
(4) Set the buzzer output frequency in the melody 0 scale code register (MD0TON).
(5) When the M0RUN bit of the melody 0 control register (MD0CON) is set to "1", the waveform equivalent to the buzzer sound that is set from the MD0 pin is output.
Figure 23-4 shows the output waveform of each buzzer output mode.

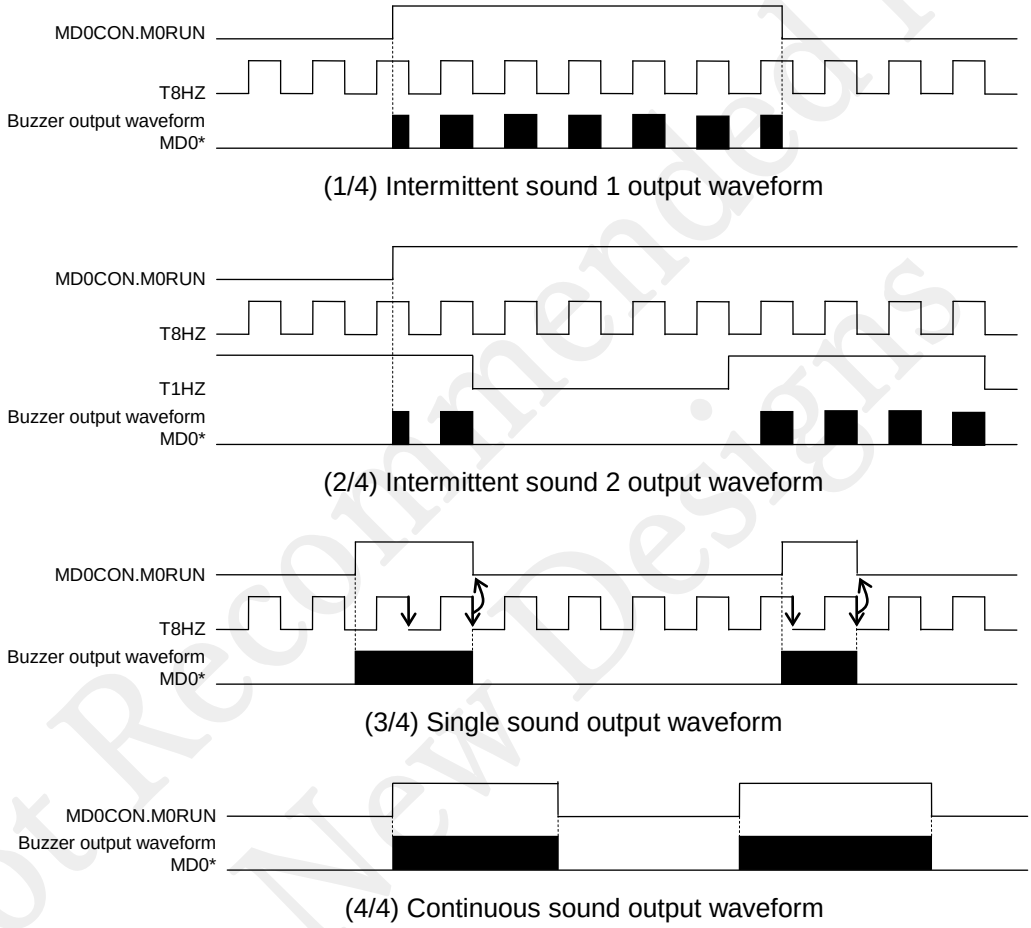


Figure 23-4 Output Waveform of Each Buzzer Output Mode

Chapter 24

RC Oscillation type A/D Converter (RC-ADC)

24 RC Oscillation Type A/D Converter (RC-ADC)

24.1 General Description

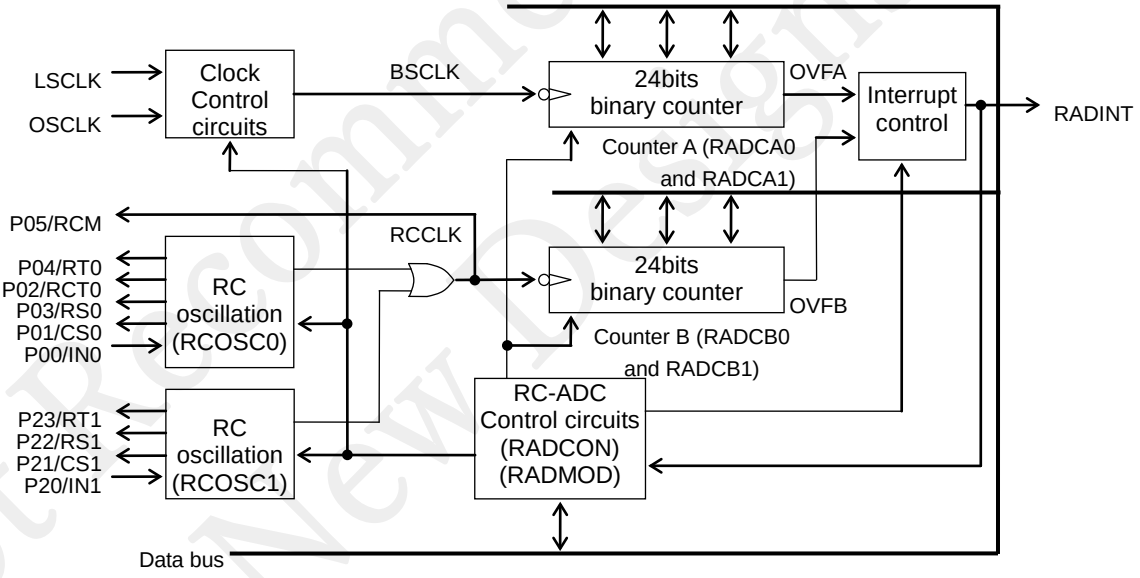
The RC oscillation type A-D Converter (RC-ADC) converts resistance values or capacitance values to digital values by counting the oscillator clock whose frequency changes according to the resistor or capacitor connected to the RC oscillator circuits. By using a thermistor or humidity sensor as a resistor, a thermometer or hygrometer can be formed.
In addition, a different sensor for each of the two channels of RC-ADC's RC oscillator circuit can be used to broaden RC-ADC applications; for example, the converter can be used for expansion of measurement range or measurement at two points.
For input clocks, see Chapter 6, "Clock Generation Circuit".

24.1.1 Features

- 2-channel system by time division

24.1.2 Configuration

The RC-ADC consists of two RC oscillator circuits to form two channels, Counter A (RADCA0 and RADCA1) and Counter B (RADCB0 and RADCB1) as 24-bit binary counters, and an RC-ADC control circuit (RADCON, RADMOD). Figure 24-1 shows the configuration of the RC-ADC.



RADMOD : RC-ADC mode register
RADCON : RC-ADC control register
RADCA0, 1 : RC-ADC counter A register
RADCB0, 1 : RC-ADC counter B register

Figure 24-1 Configuration of RC-ADC

24.1.3 List of Pins

Pin name	I/O	Function
IN0	I	Channel 0 oscillation input pin
CS0	O	Channel 0 reference capacitor connection pin
RS0	O	Channel 0 reference resistor connection pin
RCT0	O	Pin for connection with a resistive/capacitive sensor for measurement on Channel 0
RT0	O	Pin for connection with a resistive sensor for measurement on Channel 0
RCM	O	RC oscillation monitor pin Used as the secondary function of the P05 pin.
IN1	I	Channel 1 oscillation input pin
CS1	O	Channel 1 reference capacitor connection pin
RS1	O	Channel 1 reference resistor connection pin
RT1	O	Channel 1 resistive sensor for measurement connection pin

24.2 Description of Registers

24.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F800	RC-ADC counter A register 0	RADCA0L	RADCA0	R/W	8/16	00
0F801		RADCA0H		R/W	8	00
0F802	RC-ADC counter A register 1	RADCA1L	RADCA1	R/W	8/16	00
0F803		RADCA1H		R/W	8	00
0F804	RC-ADC counter B register 0	RADCB0L	RADCB0	R/W	8/16	00
0F805		RADCB0H		R/W	8	00
0F806	RC-ADC counter B register 1	RADCB1L	RADCB1	R/W	8/16	00
0F807		RADCB1H		R/W	8	00
0F808	RC-ADC mode register	RADMODL	RADMOD	R/W	8/16	00
0F809		RADMODH		R/W	8	00
0F80A	RC-ADC control register	RADCONL	RADCON	R/W	8/16	00
0F80B		RADCONH		R/W	8	00

24.2.2 RC-ADC Counter A Register 0 (RADCA0)

Address: 0F800H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
RADCA0L	RAA7	RAA6	RAA5	RAA4	RAA3	RAA2	RAA1	RAA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
RADCA0H	RAA15	RAA14	RAA13	RAA12	RAA11	RAA10	RAA9	RAA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

24.2.3 RC-ADC Counter A Register 1 (RADCA1)

Address: 0F802H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
RADCA1L	RAA23	RAA22	RAA21	RAA20	RAA19	RAA18	RAA17	RAA16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
RADCA1H	–	–	–	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

RADCA0 and RADCA1 are special function registers (SFRs) used to read from and write to the Counter A of the RC-ADC. RADCA0 and RADCA1 are 24-bit binary counters.

[Note]
When A/D conversion starts after data is written, the value that has been written is read during A/D conversion (RARUN = 1).
When A/D conversion terminates (RARUN = 0), the count value is read.

24.2.4 RC-ADC Counter B Register 0 (RADCB0)

Address: 0F804H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
RADCB0L	RAB7	RAB6	RAB5	RAB4	RAB3	RAB2	RAB1	RAB0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
RADCB0H	RAB15	RAB14	RAB13	RAB12	RAB11	RAB10	RAB9	RAB8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

24.2.5 RC-ADC Counter B Register 1 (RADCB1)

Address: 0F806H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
RADCB1L	RAB23	RAB22	RAB21	RAB20	RAB19	RAB18	RAB17	RAB16
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
RADCB1H	–	–	–	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

RADCB0 and RADCB1 are special function registers (SFRs) used to read from and write to the Counter B of the RC-ADC. RADCB0 and RADCB1 are 24-bit binary counters.

[Note]
When A/D conversion starts after data is written, the value that has been written is read during A/D conversion (RARUN = 1).
When A/D conversion terminates (RARUN = 0), the count value is read.

24.2.6 RC-ADC Mode Register (RADMOD)

Address: 0F808H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
RADMODL	RACK2	RACK1	RACK0	RADI	OM3	OM2	OM1	OM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
RADMODH	–	–	–	–	–	–	–	RAMD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

RADMOD is a special function register (SFR) used to select the A/D conversion mode of the RC-ADC.

Description of Bits

- **OM3-0** (bits 3 to 0)
  The OM3–0 bits are used to select an oscillation mode for the RC oscillator circuits.

OM3	OM2	OM1	OM0	Description
0	0	0	0	IN0 pin external clock input mode (initial value)
0	0	0	1	RS0-CS0 oscillation mode
0	0	1	0	RT0-CS0 oscillation mode
0	0	1	1	RT0-1-CS0 oscillation mode
0	1	0	0	RS0-CT0 oscillation mode
0	1	0	1	RS1–CS1 oscillation mode
0	1	1	0	RT1–CS1 oscillation mode
0	1	1	1	IN1 pin external clock input mode
1	*	*	*	Prohibited

- **RADI** (bit 4)
  The RADI bit is used to choose whether to generate the RC-ADC interrupt request signal (RADINT) by an overflow at Counter A or Counter B.

RADI	Description
0	Generates an interrupt request by Counter A overflow (initial value)
1	Generates an interrupt request by Counter B overflow

- **RACK2-0** (bits 7 to 5)
  The RACK2-0 bits are used to select the base clock of Counter A (BSCLK).

RACK2	RACK1	RACK0	Description
0	0	0	LSCLK (initial value)
0	0	1	OSCLK
0	1	0	1/2OSCLK
0	1	1	1/4OSCLK
1	0	0	1/8OSCLK
1	0	1	1/16OSCLK
1	1	0	1/32OSCLK
1	1	1	1/64OSCLK

- **RAMD0** (bit 8)
  The RAMD0 bit is selected to the range of the supply voltage(V_{DD}) of RC-ADC.

RAMD0	Description
0	V_{DD}=1.8V-3.6V (initial value)
1	V_{DD}=2.7V-5.5V

24.2.7 RC-ADC Control Register (RADCON)

Address: 0F80AH
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
RADCONL	–	–	–	–	–	–	–	RARUN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
RADCONH	–	–	–	–	–	–	–	–
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

RADCON is a special function register (SFR) used to control A/D conversion operation of the RC-ADC.

Description of Bits

- **RARUN** (bit 0)
  The RARUN bit is used to start or stop A/D conversion of the RC-ADC. Set RARUN to "1" to start the A/D conversion, and "0" to stop it. If Counter A or Counter B overflows with RARUN set to “1”, the bit is automatically reset to “0”.
  RARUN is set to "0" at system reset.

RARUN	Description
0	Stops A/D conversion (initial value)
1	Starts A/D conversion

[Note]
If the RARUN is set to "0" to stop the conversion, set DRAD of BLKCON4 to "1" to stop the operation once. To start it again, set DRAD of BLKCON4 to "0", set registers again, and then set RARUN to "1".

24.3 Description of Operation

Counter A (RADCA0 and RADCA1) is a 24-bit binary counter for counting the base clock (BSCLK), which is used as the standard of time. Counter A can count up to 0FFFFFFH.
Counter B (RADCB0 and RADCB1) is a 24-bit binary counter for counting the oscillator clock (RCCLK) of the RC oscillator circuits. Counter B can count up to 0FFFFFFH.
Counters A and B are provided with overflow flags (OVFA and OVFB, respectively). Each overflow output generates an RC-ADC interrupt request signal (RADINT). RADI bit of RC-ADC mode register(RADMOD) selects which of the counter A side or the counter B side generates the interrupt by overflow.
The overflow of Counter A is selected by setting RADI to “0”.
The overflow of Counter B is selected by setting RADI to “1”

The RARUN bit of the RC-ADC control register (RADCON) is used to start or stop RC-ADC conversion operation. When RARUN is set to “0”, the oscillator circuits stop, so that counting will not be performed. When RARUN is set to “1”, RC oscillation starts. The count of the oscillation clock(RCCLK) and the count of the base clock(BSCLK) are started by counter B and counter A.

The RC oscillation section has a total of eight types of oscillation modes based on the two oscillator circuits of RCOSC0 and RCOSC1. These modes are selected by the RC-ADC mode register (RADMOD).
When RC oscillation circuit (RCOSC0) is used, set “P00 to P04” to secondary function. When ROSC1 is used, set “P20 to P23” to secondary function. When RC monitor pin (RCM), which outputs RC oscillation waveform, is used, set P05 to secondary function.
For the RC oscillator circuit configuration, see "24.1.2 Configuration". For the secondary functions of Port 0, see Chapter 17, “Port 0”. For the secondary functions of Port 2, see Chapter 19, “Port 2”.

24.3.1 RC Oscillator Circuits

RC-ADC performs A/D conversion by converting the oscillation frequency ratio between a reference resistor (or capacitor) and a resistive sensor (or capacitive sensor) such as a thermistor to digital data.
By making RC oscillation occur both on the reference side and on the sensor side with the reference capacitor the error factor that the RS oscillator circuit itself is eliminated, thereby making it possible to perform the A/D conversion of the characteristics of the sensor itself.
Also, by calculating the ratio between the oscillation frequency on the reference side and that on the sensor side and then calculating the correlation between the calculated ratio and temperatures that the sensor characteristics have in advance, a temperature can be obtained based on that calculated ratio.
Table 24-1 lists the eight types of oscillation modes, one of which is selected by the RC-ADC mode register (RADMOD) OM3–0 bits.

Table 24-1 Oscillation Modes from Which Selection Is Made by OM3–0 Bits

mode No.	RADMOD				RCOSC0 output pin				RCOSC1 output pin			mode	
	OM3	OM2	OM1	OM0	RS0	RT0	RCT0	CS0	RS1	RT1	CS1		
0	0	0	0	0	Z	Z	Z	Z	Z	Z	Z	IN0 External clock input mode	
1	0	0	0	1	1/0	Z	Z	0/1	Z	Z	Z	RS0–CS0 oscillation	RCOSC0 oscillation mode
2	0	0	1	0	Z	1/0	Z	0/1	Z	Z	Z	RT0–CS0 oscillation	
3	0	0	1	1	Z	Z	1/0	0/1	Z	Z	Z	RT_{0-1}–CS0 oscillation	
4	0	1	0	0	1/0	Z	0/1	Z	Z	Z	Z	RS0–CT0 oscillation	
5	0	1	0	1	Z	Z	Z	Z	1/0	Z	0/1	RS1–CS1 oscillation	RCOSC1 oscillation mode
6	0	1	1	0	Z	Z	Z	Z	Z	1/0	0/1	RT1–CS1 oscillation	
7	0	1	1	1	Z	Z	Z	Z	Z	Z	Z	IN1 External clock input mode	
8	1	*	*	*	Z	Z	Z	Z	Z	Z	Z	(Prohibited)	

Note) * : Indicates arbitrary.
Z : Indicates high-impedance output.
1/0, 0/1 : Indicates active output.
(Prohibited) : The oscillator clock is not supplied even by setting the RARUN bit to "1" or by starting A/D conversion.

In Table 24-1, mode No.0 and mode No.7 are modes where external clocks to be input to the IN0 or IN1 pin are used for measurement with the RC oscillator circuit stopped.
As shown in Table 24-1, the two oscillator circuits, RCOSC0 and RCOSC1, are so specified that they cannot operate concurrently in order to prevent interference in oscillation from occurring when they oscillate concurrently.
The relationship between an oscillation frequency f_{RCCLK} and an RC constant is expressed by the following equation:

$$\frac{1}{f_{RCCLK}} = t_{RCCLK} = k_{RCCLK} \cdot R \cdot C$$

The t_{RCCLK} is the period of the oscillator clock, k_{RCCLK} the proportional constant, and R x C the product of capacitances CS, CT, (CS+CVR) and (CT+CVR) and resistances RS and RT. The value of k_{RCCLK} slightly changes depending on the value of the supply voltage VDD, RI, R, or C.
Table 24-2 lists the typical k_{RCCLK} values.

Table 24-2 Typical Values of the Proportional Constant k_{RCCLK} of RC Oscillator Circuits

VDD (V)	CSn, CTn (pF)	CVRn (pF)	RSn, RTn (kΩ)	k_{RCCLK} (Typ.)
3	560	820	100	1.2
	560	820	10	1.2

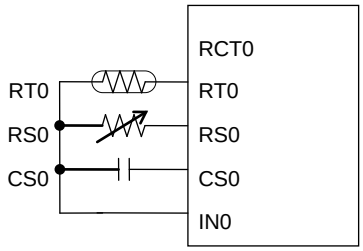
Note) n = 0, 1, 0-1

[Note]

•Pins that are to be used for the RC-ADC function must be configured as secondary function input or output using the mode register (P0MOD0, P0MOD1, P2MOD0, P2MOD1) of the corresponding port.

•All the Port 3 pins except P05/RCM (see Section 24.1.3, “List of Pins”) are configured as pins dedicated to the RC-ADC function during A/D conversion. Therefore, the Port 0 pins except P05 cannot be used as their primary functions in oscillation mode No. 0, 1, 2, 3 or 4, which is selected by the RADMOD register. In the same way, the P20 to P23 pins of Port 2 cannot be used as their primary functions in oscillation mode No. 5, 6 or 7.

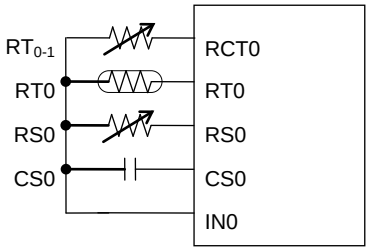
Figures 24-2 to 24-5 show the oscillator circuit configurations, the modes of oscillation for each configuration, and the OM3–0 bit settings.



OM3	OM2	OM1	OM0	oscillation mode
0	0	0	1	Oscillates with the reference resistor RS0 and CS0
0	0	1	0	Oscillates with the sensor RT0 and CS0

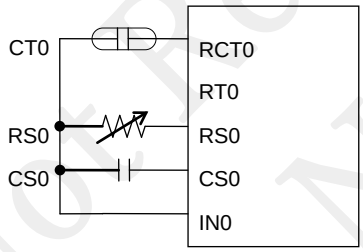
Figure 24-2 When RCOSC0 Is Used for Measurement with One Resistive Sensor

[Note]
The unused pin RCT0 shown in the figure 24-2 is configured as a pin dedicated to the RC-ADC function during A/D conversion. Therefore, RCT0 cannot be used as a primary function port (P02) during A/D conversion.



OM3	OM2	OM1	OM0	oscillation mode
0	0	0	1	Oscillates with the reference resistor RS0 and CS0
0	0	1	0	Oscillates with the sensor RT0 and CS0
0	0	1	1	Oscillates with the reference resistor RT_{0-1} and CS0

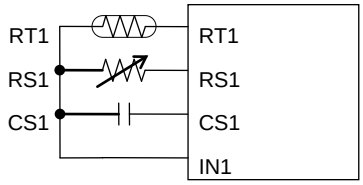
Figure 24-3 When RCOSC0 Is Used for Measurement with One Resistive Sensor
(Two points are adjusted with two reference resistors)



OM3	OM2	OM1	OM0	oscillation mode
0	0	0	1	Oscillates with the reference resistor RS0 and CS0
0	1	0	0	Oscillates with the sensor RS0 and CT0

Figure 24-4 When RCOSC0 Is Used for Measurement with One Capacitive Sensor

[Note]
The unused pin RT0 shown in the figure 24-4 is configured as a pin dedicated to the RC-ADC function during A/D conversion. Therefore, RT0 cannot be used as a primary function port (P04) during A/D conversion.



OM3	OM2	OM1	OM0	oscillation mode
0	1	0	1	Oscillates with the reference resistor RS1 and CS1
0	1	1	0	Oscillates with the sensor RT1 and CS1

Figure 24-5 When RCOSC1 Is Used for Measurement with One Resistive Sensor

24.3.2 Counter A/B Reference Modes

There are the following two modes of RC-ADC conversion operation:

- Counter A reference mode (RADMOD RADI = "0")
  In this mode, a gate time is determined by Counter A and the base clock (BSCLK), which is used as the time reference, then the RC oscillator clock (RCCLK) is counted by Counter B within the gate time to make the content of Counter B the A/D conversion value.
  The A/D conversion value is proportional to RC oscillation frequency.

- Counter B reference mode (RADMOD RADI = "1")
  In this mode, a gate time is determined by Counter B and the RC oscillator clock (RCCLK), and the base clock (BSCLK), which is used as the time reference, is counted by Counter A within the gate time to make the content of Counter A the A/D conversion value.
  The A/D conversion value is inverse proportional to RC oscillation frequency.

(1) Operation in Counter A reference mode
Figure 25-6 shows the operation timing in Counter A reference mode.
Following is an example of operation procedure in Counter A reference mode:

①Preset to Counter A (RADCA0 and RADCA1) the value obtained by subtracting the count value "nA0" from the maximum value + 1 (1000000H). The product of the count value "nA0" and the BSCLK clock cycle indicates the gate time.
②Preset "000000H" in Counter B (RADCB0 and RADCB1).
③Set the OM3–OM0 bits of RADMOD to desired oscillation mode. (See Table 24-1)
④Set the RADI bit of RADMOD to "0" to specify generating of an interrupt request signal by Counter A overflow.
⑤Set the RARUN bit of RADCON to "1" to start A/D conversion.

Counter A starts counting of the base clock (BSCLK) when RARUN is set to "1" and the RCON signal (signal synchronized with the fall of the base clock) is set to "1". When Counter A overflows, the RARUN bit is automatically reset to "0" (⑥) and counting is terminated. At the same time, an RC-ADC interrupt request (RADINT) occurs (⑦).

When the RCON signal is set to "1", the RC oscillator circuit starts operation and Counter B starts counting of the RC oscillator clock (RCCLK). When the RARUN bit is reset to "0" due to overflow of Counter A, RC oscillation stops and Counter B stops counting.
The final count value "nB0" of Counter B is the RCCLK count value during the gate time "nA0 x t_{BSCLK}" and is expressed by the following expression:

$$nB0 \cong nA0 \bullet \frac{t_{BSCLK}}{t_{RCCLK}} \propto f_{RCCLK}$$

The t_{BSCLK} indicates the BSCLK period and t_{RCCLK} the RCCLK period. That is, "nB0" is a value proportional to the RC oscillation frequency f_{RSCLK}.

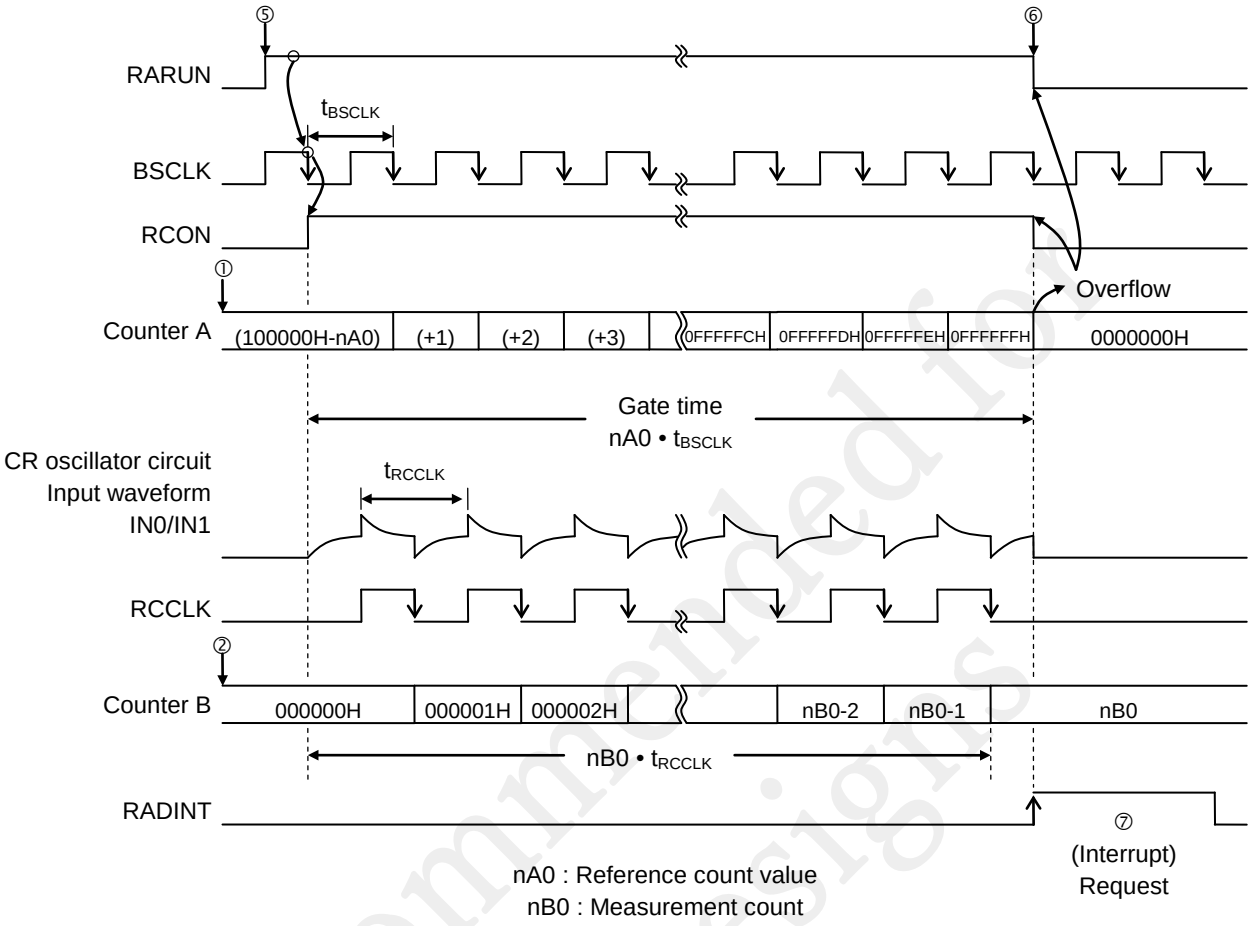


Figure 24-6 Operation Timing in Counter A Reference Mode

(2) Operation in Counter B reference mode

Figure 24-7 shows the operation timing in Counter B reference mode.
Following is an example of operation procedure in Counter B reference mode:

①Preset to Counter B (RADCB0 and RADCB1) the value obtained by subtracting the count value "nB1" from the maximum value + 1 (1000000H). The product of the count value "nB1" and the RCCLK clock cycle indicates the gate time.
②Preset "000000H" in Counter A (RADCA0 and RADCA1).
③Set the OM3–OM0 bits of RADMOD to desired oscillation mode. (See Table 24-1)
④Set the RADI bit of RADMOD to "1" to specify generating of an interrupt request signal by Counter B overflow.
⑤Set the RARUN bit of RADCON to "1" to start A/D conversion.

When the RARUN bit is set to "1" and the RCON signal (signal synchronized with the fall of the base clock) is set to"1", the RC oscillator circuit starts operation and Counter B starts counting of the RC oscillator clock (RCCLK). When Counter B overflows, the RARUN bit is automatically reset (⑥) and conversion operation terminates. At the same time, an RC-ADC interrupt request (RADINT) occurs. (⑦)

When the RCON signal is set to "1", Counter A starts counting of the base clock (BSCLK). When the RARUN bit is reset due to overflow of Counter B, Counter A stops counting.
The final count value "nA1" of Counter A is the CLK count value during the gate time "nB1 x t_{RCCLK}" and is expressed by the following expression:

$$nA1 \cong nB1 \bullet \frac{t_{RCCLK}}{t_{BSCLK}} \propto \frac{1}{f_{RCCLK}}$$

That is, "nA1" is a value inversely proportional to the RC oscillation frequency f_{RCCLK}.

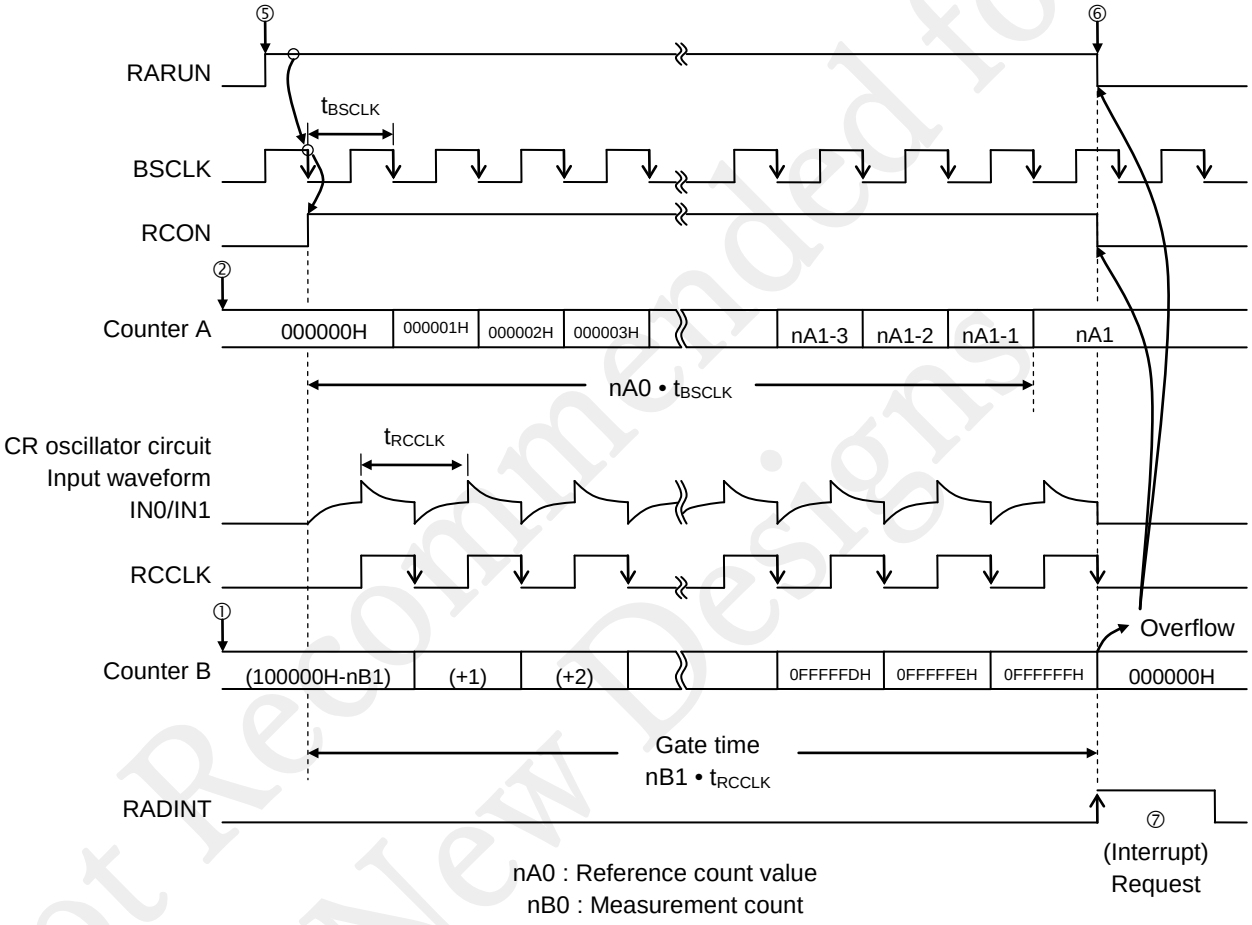


Figure 24-7 Operation Timing in Counter B Reference Mode

24.3.3 Example of Use of RC Oscillation Type A/D Converter

This section describes the method of performing A/D conversion for sensor values in Counter A and B reference modes by taking temperature measurement by a thermistor as an example.
Figure 24-8 shows the configuration of 1-thermistor RC oscillator circuit using RCOSC0.

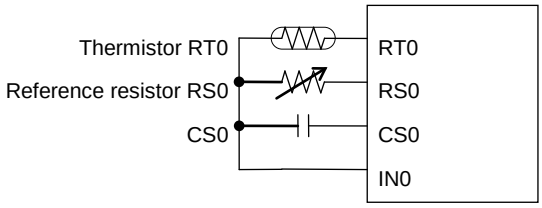


Figure 24-8 Configuration of 1-Thermistor RC Oscillator Circuit Using RCOSC0

Figure 24-9 shows the temperature characteristics of the thermistor resistance RT0.

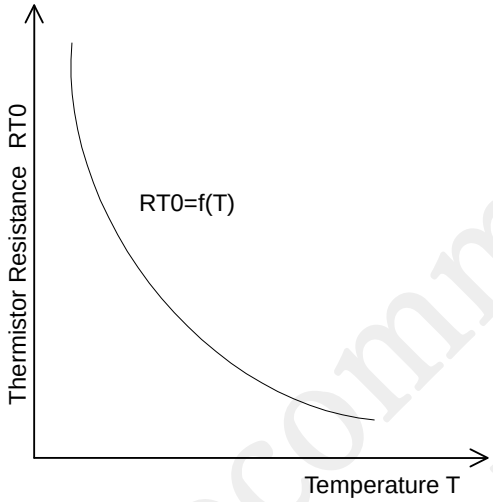


Figure 24-9 Temperature Characteristics of Thermistor

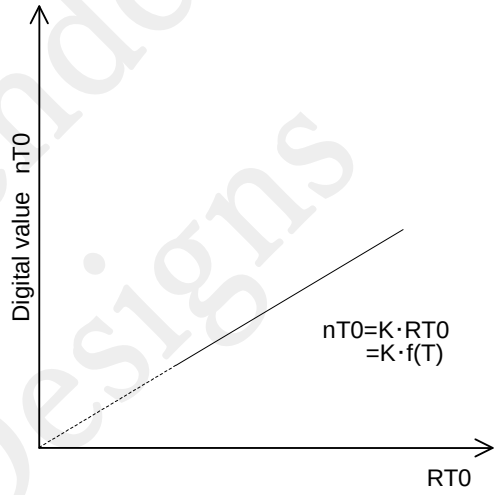


Figure 24-10 A/D Conversion Characteristics (Ideal characteristics when nT0 is proportional to RT0)

RT0 is expressed as a function of temperature T by the following equation:

RT0 = f (T)

Figure 24-10 shows the ideal characteristics of A/D conversion with the assumption that RT0 is an analog quantity. In the ideal characteristics, the A/D conversion value nT0 will purely depend on RT0 only. Assuming that nT0 is proportional to RT0, let proportional constant be K, then nT0 has the following relationship with temperature T:

nT0 = K•RT0 = K•f (T) ... Expression A

Therefore, temperature T can be expressed as a digital value by performing the conversion processing that accord with the characteristics shown in Figure 24-9 for nT0 by software.

To convert from an RT0 value to a digital value, the ratio is used between a) the RC oscillation frequency by the thermistor connected to the RT0 pin and the capacitor connected to the CS0 pin and b) the oscillation frequency by the reference resistor (which ideally should have no temperature characteristics) connected to the RS0 pin and the capacitor connected to the CS0 pin. This is for making the conditions other than resistance equal to eliminate the error factor in RC oscillation characteristics.
As shown in Figures 24-9 and 24-11, the RT0 value depends on temperature T and the RS0 value is assumed to be constant regardless of temperature T. It is ideal if the characteristics of the oscillation frequency f_{OSC} to temperature T using these resistances will be like the solid lines in Figures 24-12 and 24-13; however, in reality, it would appear that they will be like the dotted lines due to error factors such as IC temperature characteristics. Since the condition of f_{RCCLK} (RT0) and that of f_{RCCLK} (RS0) are the same except for the resistances, the error ratios are almost the same; therefore, errors can almost be eliminated by using the ratio between f_{RCCLK} (RT0) and f_{RCCLK} (RS0).

The ratio between f_{RCCLK} (RT0) and f_{RCCLK} (RS0) is equivalent to the above-mentioned A/D conversion value nT0 that should ideally depend only on RT0.

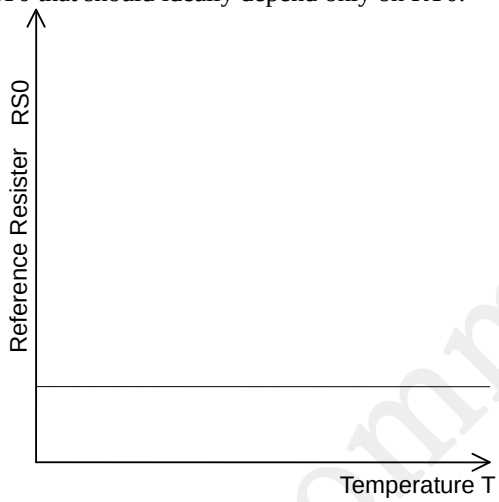


Figure 24-11 Temperature Characteristics of Reference Resistor

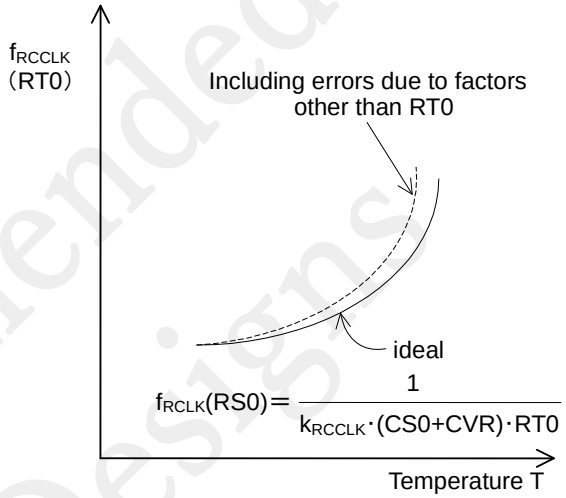


Figure 24-12 Oscillation Characteristics of Thermistor

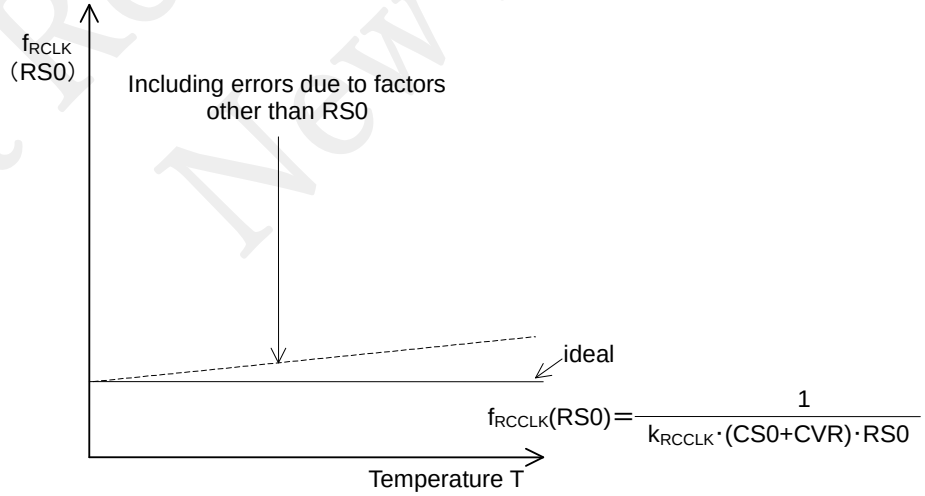


Figure 24-13 Oscillation Characteristics of Reference Resistor

Figure 24-14 shows, as an example of method, a timing diagram of one cycle of conversion from analog value RT0 to a digital value, that is, A/D conversion.

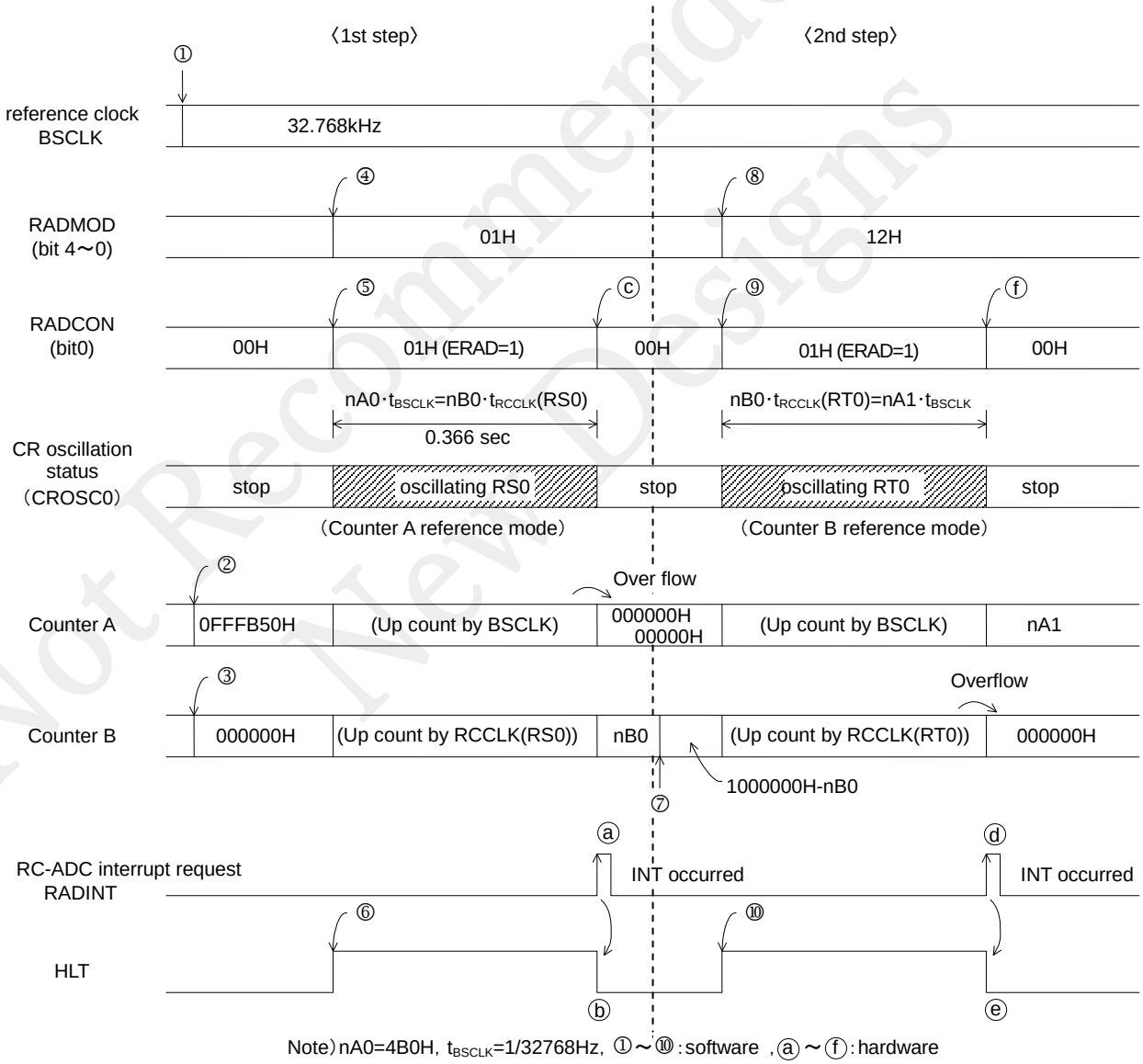
Basically, one A/D conversion cycle must consist of two steps, as shown in Figure 24-14. The reason for requiring two steps is that the reference resistor and the thermistor must first be oscillated separately and then the ratio between the oscillation frequencies of them is used, as described above.
In the example below, operation for these two steps is performed using the following combination:

- First step = RC oscillation with RS0 in Counter A reference mode
- Second step = RC oscillation with RT0 in Counter B reference mode

Besides this, there would be several possible A/D conversion methods.
In the above method, the operation time (gate time) for the second step fluctuates depending on the value of thermistor RT0. To avoid the fluctuation of the operation time, using a method that uses the following combination is recommended:

- First step = RC oscillation with RS0 in Counter B reference mode
- Second step = RC oscillation with RT0 in Counter A reference mode

A/D conversion procedure is explained below by taking Figure 24-14 as an example.



Note）nA0=4B0H, t_{BSCLK}=1/32768Hz, ①〜⑩：software ,ⓐ〜ⓕ：hardware

Figure 24-14 Timing Diagram for 1 Cycle of A/D Conversion (Example)

<First step>

①Set the base clock to LSCLK (32.768kHz). (Write “00H” in FCON0.)
②Preset “1000000H – nA0” in Counter A.
③Preset “000000H” in Counter B.
④Write “01H” in RADMOD to select Counter A reference mode and the oscillation mode that uses reference resistance RS0.
⑤Write “01H” in RADCON to start A/D conversion operation.
⑥Write “1” in the HLT bit of SBYCON (see Chapter 4, “MCU”) to set the device to HALT mode.

[Note]
In this example, nA0 is set to 4B0H because the gate time “nA0 x tBSCLK” in oscillation mode with reference resistor RS0 is set to 0.366 second. The value of nA0 is related to how much the margin of the quantization error of the A/D conversion is: the greater the nA0 value is, the smaller the margin of error becomes.
To reduce noise contamination to the RC oscillator circuit caused by CPU operation, it is recommended to constantly put the device into HALT mode during operation of RC oscillation.

From this point of time, the RC oscillator circuit (RCOSC0) continues oscillation for about 0.366 second with the reference resistance RS0. Then, when Counter A overflows, the RADINT signal is set to “1” and an RC-ADC interrupt request is generated. (Section a). Also, the generation of interrupt request releases HALT mode (section b) and at the same time, A/D conversion operation stops. (Section c, RARUN bit = "0"). At this time, Counter A is set to “000000H”.
The content of Counter B at this time is expressed by the following expression:

$$nB0 = nA0 \bullet \frac{t_{BSCLK}}{t_{RCCLK}\ (RS0)} \quad \text{... Expression B}$$

That completes the operations in First Step.

<Second step>

⑦Calculate “1000000H – nB0” from the content of Counter B “nB0” and set the obtained value in Counter B.
At this point, Counter A needs to be cleared; however, no processing is required since the counter is already set to “000000H”.
⑧Write “12H” in RADMOD to select Counter B reference mode and the oscillation mode that uses thermistor RT0.
⑨Write “01H” in RADCON to start A/D conversion operation.
⑩Write “1” in the HLT bit of SBYCON (see Chapter 4, “MCU”) to set the device to HALT mode.

The RC oscillator circuit (RCOSC0) oscillates with thermistor RT0 from this point until Counter B overflows. This period is equal to the product of “nB0” obtained in the First Step and the oscillation period t_{RCCLK} (RT0) using RT0.
When Counter B overflows, the RADINT signal is set to “1” and an RC-ADC interrupt request is generated. (Section d). Also, the generation of interrupt request releases HALT mode (section e) and at the same time, A/D conversion operation stops. (Section f, RARUN bit = "0").
This completes the operations in Second Step.

The content of Counter A at this time becomes the A/D conversion value nA1, which is expressed by the following expression:

$$nA1 = nB0 \bullet \frac{t_{RCCLK}(RT0)}{t_{BSCLK}} \quad \text{... Expression C}$$

From expressions B and C, nA1 is expressed by the following expression:

$$nA1 = nA0 \bullet \frac{t_{RCCLK}(RT0)}{t_{RCCLK}(RS0)} \quad \text{... Expression D}$$

The t_{RCCLK} (RS0) is the oscillator clock period by reference resistor RS0 and t_{RCCLK} (RT0) the oscillator clock period by thermistor RT0.
Since the oscillation period is expressed by "$t_{RCCLK} = k_{RCCLK}$ x R x C", t_{RCCLK} (RS0) and t_{RCCLK} (RT0) are expressed by the following expressions:

$$t_{RCCLK}(RS0) = k_{RCCLK} \bullet (CS0+CVR) \bullet RS0$$

$$t_{RCCLK}(RT0) = k_{RCCLK} \bullet (CS0+CVR) \bullet RT0 \quad \text{... Expression E}$$

When expression E is substituted for expression D, nA1 will be:

$$nA1 = nA0 \bullet \frac{RT0}{RS0}$$

Since “nA0” (“4B0H” in this example) and RS0 are constants whose values are fixed, “nA1” is a digital value proportional to RT0. This very “nA1” corresponds to “nT0” in expression A.

That concludes the description of the A/D conversion method using a thermistor. “nA1” that has been obtained must further be converted to a value such as a temperature indication value for thermometer by program according to the temperature-to-resistance characteristics of the thermistor.

24.3.4 Monitoring RC Oscillation

The RC oscillator clock (RCCLK) can be output using the secondary function of the P05. See Chapter 17, “Port 0,” for the details of the secondary function of P05.
Monitoring RC oscillation is useful for checking the characteristics of the RC oscillator circuit. That is, the relationship between a sensor, such as a thermistor, and the oscillation frequency can be measured. For instance, the coefficient for conversion from the above-described nA1 value to a temperature indication value can be obtained by checking the relationship between the ambient temperature of a thermistor-incorporated RC oscillator circuit, the oscillation frequency with thermistor RT0, and the oscillation frequency with reference resistor RS0.

[Note]
P05 (RCM) is a monitor pin for oscillation clock. The Channel 0 and Channel 1 share the monitor pin.
Use P05 (RCM) pin for the evaluation purpose and disable the output while operating in an actual application to minimize the noise.

Chapter 25

Successive Approximation Type A/D Converter (SA-ADC)

25 Successive Approximation Type A/D Converter (SA-ADC)

25.1 General Description

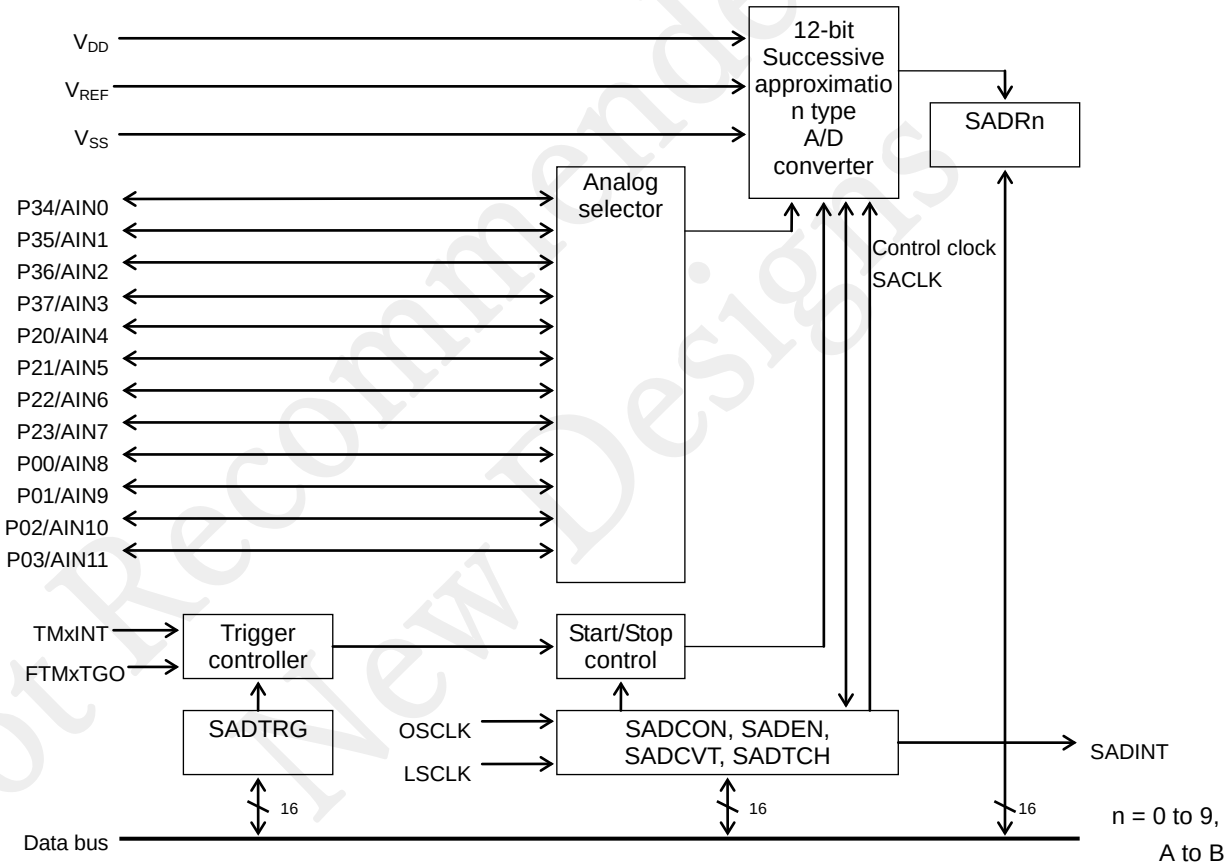
The successive approximation type A-D converter (SA-ADC) has 12 channels with a built-in function supporting an electrostatic capacity type switch (touch sensor supported) in addition to the normal A/D conversion.

25.1.1 Features

- Built-in sample/hold 12-bit successive approximation type A-D converter, which enables channel selection from multiple channels.
- Supports to start the A/D conversion using the timer.(trigger mode)
- Touch sensor supported.

25.1.2 Configuration

Figure 25-1 shows the configuration of SA-ADC.



SADRn : SA-ADC result register n
SADCON0/1: SA-ADC control register 0/1
SADEN : SA-ADC enable register
SADCVT : SA-ADC accuracy control register
SADTRG : SA-ADC trigger register
SADTCH : SA-ADC touch sensor register

Figure 25-1 Configuration of SA-ADC

25.1.3 List of Pins

Pin name	I/O	Function
P34/AIN0	I	Successive approximation type A/D converter input pin 0 Use as P34 pin primary function
P35/AIN1	I	Successive approximation type A/D converter input pin 1 Use as P35 pin primary function
P36/AIN2	I	Successive approximation type A/D converter input pin 2 Use as P36 pin primary function
P37/AIN3	I	Successive approximation type A/D converter input pin 3 Use as P37 pin primary function
P20/AIN4	I	Successive approximation type A/D converter input pin 4 Use as P20 pin primary function
P21/AIN5	I	Successive approximation type A/D converter input pin 5 Use as P21 pin primary function
P22/AIN6	I	Successive approximation type A/D converter input pin 6 Use as P22 pin primary function
P23/AIN7	I	Successive approximation type A/D converter input pin 7 Use as P23 pin primary function
P00/AIN8	I	Successive approximation type A/D converter input pin 8 Use as P00 pin primary function
P01/AIN9	I	Successive approximation type A/D converter input pin 9 Use as P01 pin primary function
P02/AIN10	I	Successive approximation type A/D converter input pin 10 Use as P02 pin primary function
P03/AIN11	I	Successive approximation type A/D converter input pin 11 Use as P03 pin primary function
V_{REF}	I	Reference voltage input pin for the successive approximation type A/D converter

25.2 Description of Registers

25.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F820	SA-ADC result register 0	SADR0L	SADR0	R	8/16	00
0F821		SADR0H		R	8	00
0F822	SA-ADC result register 1	SADR1L	SADR1	R	8/16	00
0F823		SADR1H		R	8	00
0F824	SA-ADC result register 2	SADR2L	SADR2	R	8/16	00
0F825		SADR2H		R	8	00
0F826	SA-ADC result register 3	SADR3L	SADR3	R	8/16	00
0F827		SADR3H		R	8	00
0F828	SA-ADC result register 4	SADR4L	SADR4	R	8/16	00
0F829		SADR4H		R	8	00
0F82A	SA-ADC result register 5	SADR5L	SADR5	R	8/16	00
0F82B		SADR5H		R	8	00
0F82C	SA-ADC result register 6	SADR6L	SADR6	R	8/16	00
0F82D		SADR6H		R	8	00
0F82E	SA-ADC result register 7	SADR7L	SADR7	R	8/16	00
0F82F		SADR7H		R	8	00
0F830	SA-ADC result register 8	SADR8L	SADR8	R	8/16	00
0F831		SADR8H		R	8	00
0F832	SA-ADC result register 9	SADR9L	SADR9	R	8/16	00
0F833		SADR9H		R	8	00
0F834	SA-ADC result register A	SADRAL	SADRA	R	8/16	00
0F835		SADRAH		R	8	00
0F836	SA-ADC result register B	SADRBL	SADRB	R	8/16	00
0F837		SADRBH		R	8	00
0F840	SA-ADC control register 0	SADCON0	–	R/W	8	22
0F841	SA-ADC control register 1	SADCON1		R/W	8	00
0F842	SA-ADC enable register	SADENL	SADEN	R/W	8/16	00
0F843		SADENH		R/W	8	00
0F844	SA-ADC touch sensor register	SADTCHL	SADTCH	R/W	8/16	00
0F845		SADTCHH		R/W	8	00
0F846	SA-ADC trigger register	SADTRGL	SADTRG	R/W	8/16	00
0F847		SADTRGH		R/W	8	00
0F848	SA-ADC accuracy control register	SADCVTL	SADCVT	R/W	8/16	FF
0F849		SADCVTH		R/W	8	FF

25.2.2 SA-ADC Result Register n (SADRn) n=0 to 9, A, B

Address: 0F820H(SADR0L/SADR0), 0F821H(SADR0H), 0F822H(SADR1L/SADR1), 0F823H(SADR1H), 0F824H(SADR2L/SADR2), 0F825H(SADR2H), 0F826H(SADR3L/SADR3), 0F827H(SADR3H), 0F828H(SADR4L/SADR4), 0F829H(SADR4H), 0F82AH(SADR5L/SADR5), 0F82BH(SADR5H), 0F82CH(SADR6L/SADR6), 0F82DH(SADR6H), 0F82EH(SADR7L/SADR7), 0F82FH(SADR7H), 0F830H(SADR8L/SADR8), 0F831H(SADR8H), 0F832H(SADR9L/SADR9), 0F833H(SADR9H), 0F834H(SADRAL/SADRA), 0F835H(SADRAH), 0F836H (SADRBL/SADRB), 0F837H (SADRBH)

Access: R

Access size: 8/16 bits

Initial value: 0000H

	7	6	5	4	3	2	1	0
SADRnL	SARn7	SARn6	SARn5	SARn4	SARn3	SARn2	SARn1	SARn0
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
SADRnH	–	–	–	–	SARnB	SARnA	SARn9	SARn8
R/W	R	R	R	R	R	R	R	R
Initial value	0	0	0	0	0	0	0	0

n = 0 to 9, A, B

SADRn is a special function register (SFR) used to store SA-ADC conversion results on channel n.
SADRn is updated after A/D conversion.

Description of Bits

- **SARnB-0** (bits 11 to 0)
  Stores the A/D conversion result (12 bits) of the channel n.

25.2.3 SA-ADC Control Register 0(SADCON0)

Address: 0F840H
Access: R/W
Access size: 8 bits
Initial value: 22H

	7	6	5	4	3	2	1	0
SADCON0	–	–	SACD1	SACD0	–	SATCM	SACK	SALP
R/W	RW	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	1	0	0	0	1	0

SADCON0 is a special function register (SFR) used to control the operation of the SA-ADC.

Description of Bits

- **SALP** (bit 0)
  This bit is used to select whether A/D conversion is performed once only for each channel or consecutively. When this bit is set to "0", A/D conversion is performed once only for each channel. And when it is set to "1", A/D conversion is performed consecutively according to the settings of the SA-ADC enable register (SADEN).
  Consecutive A/D conversion cannot be used in the trigger mode (SAST0 bit of SADTRG register is “1”). Therefore, set SALP to “0”.

SALP	Description
0	Single A/D conversion only (initial value)
1	Consecutive A/D conversion

- **SACK** (bit 1)
  This bit is used to set the clock used for the A/D conversion.
  When SACK is set to “0”, A/D conversion is preceded by using LSCLK. When SACK is set to “1”, A/D conversion is performed by using OSCSK. If OSCLK is selected, set the SACD0 and SACD1 bits to make the input clock into SA-ADC 4MHz or less.
  If selecting the touch sensor conversion, set SACK to “1”.

SACK	Description
0	LSCLK
1	OSCLK (initial value)

- **SATCM** (bit 2)
  This bit is used to select the touch sensor supported A/D conversion.
  By setting SATCM to “1”, the channel, which was selected by SADTCH, is A/D converted by the touch sensor support.

SATCM	Description
0	Touch sensor unsupported A/D conversion (initial value)
1	Touch sensor supported A/D conversion

- **SACD1-0** (bits 5 to 4)
  The SACD1-0 bits are used to set the counter frequency dividing of the SA-ADC conversion time. This setting is the dividing value of the clock selected by the SACK bit. The clock to be input to the SA-ADC should be 4MHz or less when OSCLK is selected, or 32.768kHz or less when LSCLK is selected. Proper operation cannot be guaranteed if the frequency division value exceeds 4MHz when OSCLK is selected, or 32.768kHz when the low-speed clock is selected.
  This counter is designed to have an optimal conversion time for 4MHz when OSCLK is selected, or 32.768kHz when LSCLK is selected. Therefore, the conversion time is extended according to the frequency ratio. Table 25-1 shows the relationship between the setting values of OSCLK, SACD1, and SACD0 when OSCLK is selected.

SACD1	SACD0	Description
0	0	non-dividing
0	1	2-dividing
1	0	4-dividing (initial value)
1	1	Prohibited

Table 25-1 Relationship between OSCLK and SACD0 and SACD1 Bits

OSCLK	SACD1	SACD0
16MHz	1	0
8MHz	0	1
4MHz	0	0

[Note]
Do not change this bit during SA-ADC conversion. Operation is not guaranteed if it is changed.

25.2.4 SA-ADC Control Register1 (SADCON1)

Address: 0F841H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
SADCON1	–	–	–	–	–	–	–	SARUN
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADCON is a special function register (SFR) used to control the operation of the SA-ADC.

Description of Bits

- **SARUN** (bit 0)
  This bit is used to start or stop the SA-ADC conversion. Set this bit to "1" to start the A/D conversion, and "0" to stop it.
  When SALP is “0” and then A/D conversion on the channel with the largest channel number among the selected ones is terminated, the SARUN bit is automatically set to “0”. In the case of a trigger mode, the control by the software isn’t possible. This bit is set to “1” when the A/D conversion starts by the trigger event, and when conversion is finished, it becomes “0”.
  In addition, don’t start A/D conversion in a state with all bits of SA-ADC enable register (SADEN) as “0”. If the A/D conversion is started in this state, the A/D conversion circuit does not work.

SARUN	Description
0	Stops conversion (initial value)
1	Starts conversion

25.2.5 SA-ADC Enable Register (SADEN)

Address: 0F842H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
SADENL	SACH7	SACH6	SACH5	SACH4	SACH3	SACH2	SACH1	SACH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
SADENH	–	–	–	–	SACHB	SACHA	SACH9	SACH8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADEN is a special function register (SFR) used to choose A/D conversion channel(s).

Description of Bits

- **SACHn** (bit 11 to 0)
  The SACHn bits are used to select channel(s) on which A/D conversion is performed.
  If both channel 1 and channel 0 are set to "1", A/D conversion is performed on channel 0 first, and then channel 1.
  Do not start the A/D conversion with all SACHB-SACH0 set to "0". If the A/D conversion is started in this state, the A/D conversion circuit does not work.

SACHn	Description
0	Stops conversion on channel n (initial value)
1	Performs conversion on channel n

n = 0 to 9, A, B

25.2.6 SA-ADC Touch Sensor Register (SADTCH)

Address: 0F844H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
SADTCHL	SATCH7	SATCH6	SATCH5	SATCH4	SATCH3	SATCH2	SATCH1	SATCH0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
SADTCHH	–	–	–	–	SATCHB	SATCHA	SATCH9	SATCH8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADTCH is a special function register (SFR) used to select channels to be operated in the touch sensor supported mode.

Description of Bits

- **SATCHn** (bit 11 to 0)
  The SATCHn bits are used to select channel(s) on which A/D conversion is performed.

SATCHn	Description
0	Touch sensor mode disable (initial value)
1	Touch sensor mode enable

n = 0 to 9, A, B

[Note]
•Even if SATCHn is set to "1" for a bit which is not set to "1" by SADEN, the A/D conversion is not performed.

25.2.7 SA-ADC Trigger Register (SADTRG)

Address: 0F846H
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
SADTRGL	–	–	–	–	–	–	–	SAST0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
SADTRGH	–	–	–	SASTS4	SASTS3	SASTS2	SASTS1	SASTS0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

SADTRG is a special function register (SFR) used to select the external trigger for the A/D conversion.

Description of Bits

- **SAST0** (bit 0)
  Selects the A/D conversion start mode.

SAST0	Description
0	Normal mode (initial value) Start A/D conversion by setting SARUN of SADCON registers “1” from software.
1	Trigger mode : SARUN is set to “1” by the trigger event selected by SASTS, and then A/D conversion is started. Even if a trigger event occurs during A/D conversion (when SARUN is set to “1”), it is ignored and the A/D conversion in process is continued. In addition, In addition, SARUN cannot be controlled by consecutive A/D conversion nor software.

- **SASTS4-0** (bits 12 to 8)
  This bit is used to select a trigger event for the A/D conversion.

SASTS4	SASTS3	SASTS2	SASTS1	SASTS0	Description
0	0	0	0	0	TM0INT
0	0	0	0	1	TM1INT
0	0	0	1	0	TM2INT
0	0	0	1	1	TM3INT
0	0	1	0	0	TM4INT
0	0	1	0	1	TM5INT
0	0	1	1	0	TM6INT
0	0	1	1	1	TM7INT
0	1	*	*	*	Setting prohibited
1	0	0	0	0	FTM0TGO
1	0	0	0	1	FTM1TGO
1	0	0	1	0	FTM2TGO
1	0	0	1	1	FTM3TGO
1	0	1	*	*	Setting prohibited
1	1	*	*	*	Setting prohibited

[Note]
•The timer interrupt request (TM0-7INT) is an interrupt request signal independent of the interrupt enabled/disabled setting of the interrupt enable register. The multifunction timer trigger output(FTM0-3TGO) is a signal for event trigger.
•If a prohibited setting is specified, the A/D conversion is not started by any trigger event.

25.2.8 SA-ADC Accuracy Control Register (SADCVT)

Address: 0F848H
Access: R/W
Access size: 8/16 bits
Initial value: FFFFH

	7	6	5	4	3	2	1	0
SADCVTL	SADCT7	SADCT6	SADCT5	SADCT4	SADCT3	SADCT2	SADCT1	SADCT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

	15	14	13	12	11	10	9	8
SADCVTH	SAPCT4	SAPCT3	SAPCT2	SAPCT1	SAPCT0	SACPT2	SACPT1	SACPT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	1	1	1	1	1	1	1	1

SADCVT is a special function register (SFR) used to select the conversion time of the A/D conversion.

SADCVT releate to SACK of SADCON0 and SATCM. Please set SADCVT according to the following table.

SACK	SATCM	SAPCT4-0	SACPT2-0	SADCT7-0
0	0	00H	00H	01H
0	1	Setting prohibited	Setting prohibited	Setting prohibited
1	0	00H	03H	78H
1	1	15H	03H	78H

25.3 Description of Operation

25.3.1 Setting of A/D Conversion Channels

According to the table 25-2, set a bit corresponding to each channel on which the A/D conversion is performed.

table 25-2, Setting channel

SADCON0 SATCM bits	SADEN SACHn bits	SADTCH SATCHn bits	SA-ADC operation
0	0	0	No operation
0	0	1	No operation
0	1	0	Non-touch sensor mode
0	1	1	No operation
1	0	0	No operation
1	0	1	No operation
1	1	0	No operation
1	1	1	Touch sensor mode

Do not start the A/D conversion with all SACHB-SACH0 set to “0” in the SA-ADC enable register (SADEN). If the A/D conversion is started in this state, an interrupt is not output and the SARUN bit remains as "1".

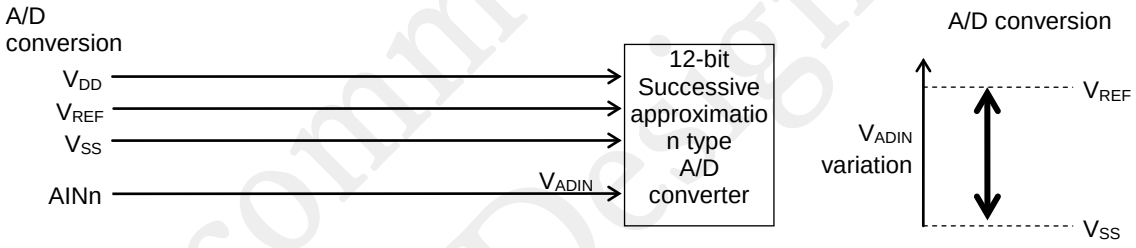


Figure 25-2 A/D Conversion Pins and Conversion Range

25.3.2 Operation of the Successive Approximation Type A/D Converter

For direct input, operate SA-ADC in the following procedure.

(1) Normal mode

1. Wait until the oscillation of the clock used for the A/D conversion is started and stabilized.
   When LSCLK is selected, it is revealed that the oscillation is stabilized by the fact that T128HZ of the low-speed time base counter register (LTBR) is set to "1".
   When OSCLK is selected and the high-speed crystal/ceramic oscillation mode, it is revealed that the oscillation is stabilized by the fact that the HOSST bit of the FCON01 register is set to "1".
2. Set the SA-ADC control register 0 (SADCON0), SA-ADC enable register (SADEN), and SA-ADC accuracy control register (SADCVT).
3. When the bit 2 (SATCM) of the SA-ADC control register 0 (SADCON0) is set to "0" then the bit 0 (SARUN) of the SA-ADC control register 1 (SADCON1) to "1", the SA-ADC circuit starts operating to perform A/D conversion on the channels selected in the SA-ADC enable register (SADEN) from a lower channel number.
4. A/D conversion results are stored in the applicable SA-ADC result registers (SADRn), and when A/D conversion of the largest channel number is completed, a SA-ADC conversion termination interrupt (SADINT) is generated.

(2) Trigger mode

1. Wait until the oscillation of the clock used for the A/D conversion is started and stabilized.
   When LSCLK is selected, it is revealed that the oscillation is stabilized by the fact that T128HZ of the low-speed time base counter register (LTBR) is set to "1".
   When OSCLK is selected and the high-speed crystal/ceramic oscillation mode, it is revealed that the oscillation is stabilized by the fact that the HOSST bit of the FCON01 register is set to "1".
2. Set the SA-ADC control register 0 (SADCON0), SA-ADC enable register (SADEN), and SA-ADC accuracy control register (SADCVT), where set SALP bit of SADCON0 register.
3 After trigger event source is selected by SA-ADC trigger register (SADTRG), and SAST0 bit is set to "1", the trigger mode is begun.
4. If occur trigger event , the bit 0 (SARUN) of the SA-ADC control register 1 (SADCON1) to "1", the SA-ADC circuit starts operating to perform A/D conversion on the channels selected in the SA-ADC enable register (SADEN) from a lower channel number.
5. A/D conversion results are stored in the applicable SA-ADC result registers (SADRn), and when A/D conversion of the largest channel number is completed, a SA-ADC conversion termination interrupt (SADINT) is generated.

Even if the channel is switched during A/D conversion, it is held as selected at the start of A/D conversion until an A/D conversion termination interrupt occurs.
Figure 25-3 shows the operation when channels 0 and 1 are selected.

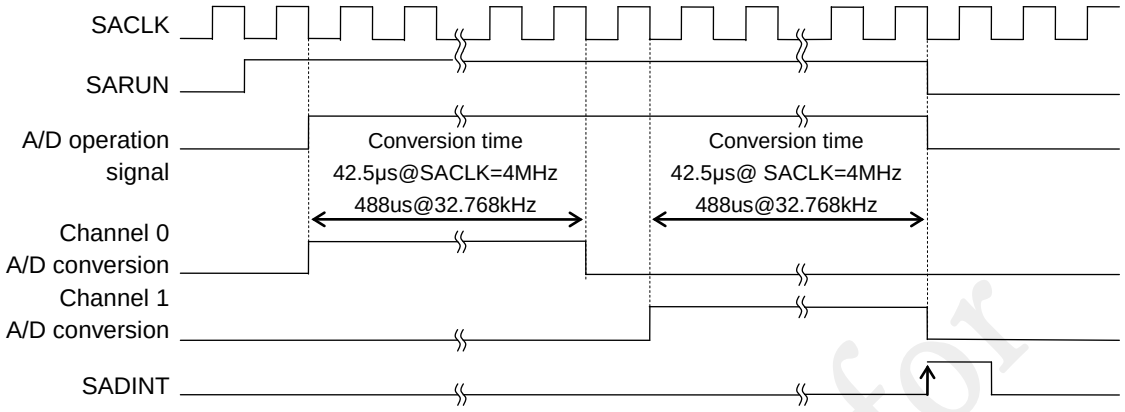


Figure 25-3 Operation Timing Diagram of SA-ADC

25.3.3 Capacitive Touch sensor mode operation

To operate SA-ADC, complete the following procedure.

1. Wait until the oscillation of the clock used for the A/D conversion is started and stabilized.
   In the high-speed crystal/ceramic oscillation mode, it is revealed that the oscillation is stabilized by the fact that the HOSST bit of the FCON01 register is set to ”1”.
2. Set the SA-ADC control register 0 (SADCON0), SA-ADC enable register (SADEN), SA-ADC accuracy control register (SADCVT), and SA-ADC touch sensor register (SADTCH).
3. When the bit 2 (SATCH) of the SA-ADC control register 0 (SADCON0) is set to “1” then the bit 0 (SARUN) of the SA-ADC control register 1 (SADCON1) to “1”, the SA-ADC circuit starts operating. The touch sensor supported A/D conversion is performed on the channels selected in the SA-ADC enable register (SADEN) from a lower channel number.
4. A/D conversion results are stored in the applicable SA-ADC result registers (SADRn), and when A/D conversion of the largest channel number is completed, a SA-ADC conversion termination interrupt (SADINT) is generated.

Figure 25-4 shows the operation when channels 0 and 1 are selected.

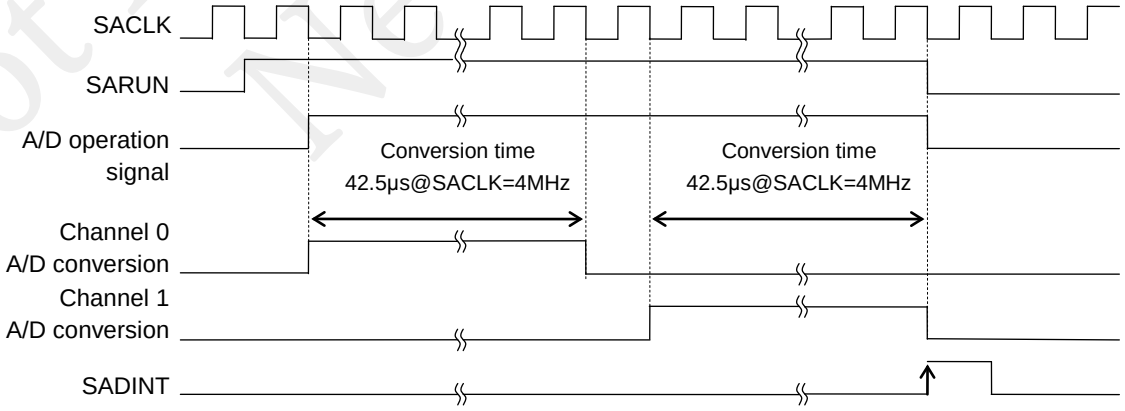


Figure 25-4 Operation Timing Diagram of SA-ADC

25.3.4 Notes on Use of SA-ADC

SA-ADC has an internal capacitor of 51.2pF(Typ), which is charged by the voltage input from AINn (n=0 to 11). It is possible to charge it by connecting an external capacitor of 0.47uF or more regardless of the input impedance.
Figure 25-5 shows the connection of SA-ADC.
If an external capacitor of less than 0.47uF is used, the measurement accuracy decreases.

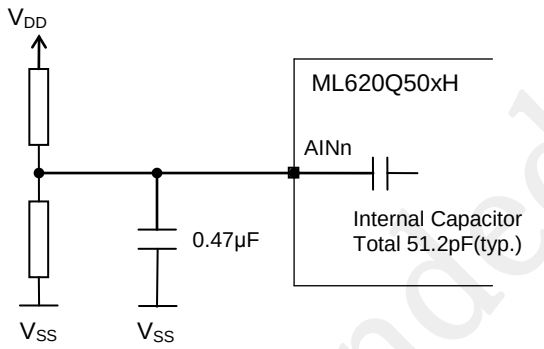


Figure 25-5 Connection of SA-ADC

Chapter 26

Analog Comparator

26 Analog Comparator

26.1 Overview

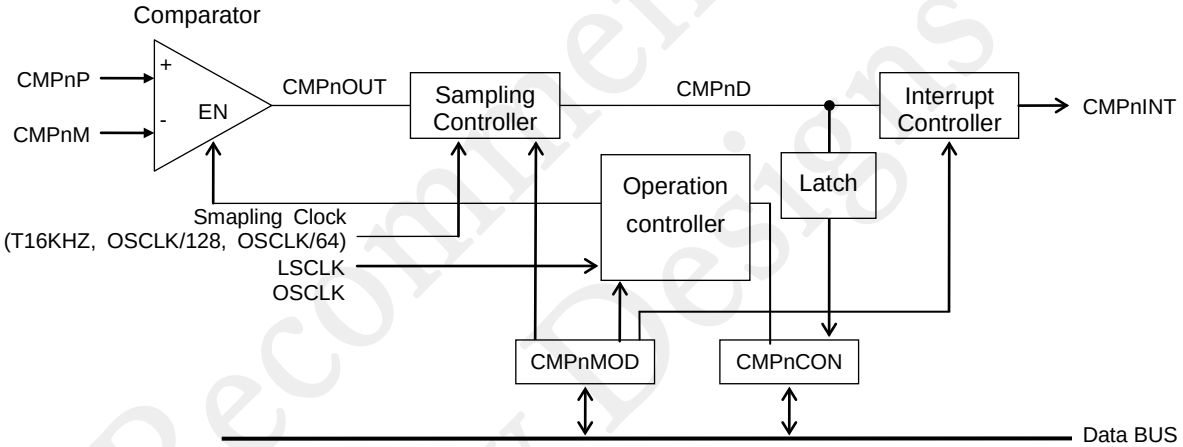
An analog comparator compares 2 input voltage and generate an interrupt corresponding to the comparison result.
This LSI has two channel analog comparator, can compare the voltages (differential input) supplied to two input pins (CMPnP and CMPnM, n=0, 1).

26.1.1 Features

- The comparator output can generate an interrupt.
- Allows selection of falling-edge interrupt mode, rising-edge interrupt mode, or both-edge interrupt mode.
- Allows selection of with/without interrupt sampling for each bit.(Sampling frequency: T16KHZ, OSCLK/128(125kHz@OSCLK=16MHz), OSCLK/64(250kHz @ OSCLK=16MHz))
- The last status of comparator output (CMPnD) remains after the comparator is deactivated.
- Single mode is available.

26.1.2 Configuration

Figure 26-1 shows the configuration of the Comparator.



CMPnCON : Comparator control register n
CMPnMOD : Comparator mode register n
n = 0, 1

Figure 26-1 Configuration of Analog Comparator

26.1.3 List of Pins

Pin name	I/O	Description
P30/CMP0P	I	Analog comparator 0 non-inverted input pin
P31/CMP0M	I	Analog comparator 0 inverted input pin
P32/CMP1P	I	Analog comparator 1 non-inverted input pin
P33/CMP1M	I	Analog comparator 1 inverted input pin

26.2 Description of Registers

26.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F920	Comparator 0 control register	CMP0CON	–	R/W	8	00
0F922	Comparator 0 mode register	CMP0MODL	CMP0MOD	R/W	8/16	00
0F923		CMP0MODH		R/W	8	00
0F928	Comparator 1 control register	CMP1CON	–	R/W	8	00
0F92A	Comparator 1 mode register	CMP1MODL	CMP1MOD	R/W	8/16	00
0F92B		CMP1MODH		R/W	8	00

26.2.2 Comparator n Control Register (CMPnCON : n=0,1)

Address: 0F920H(CMP0CON), 0F928H(CMP1CON)
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
CMPnCON	–	–	–	–	–	CMPnRF	CMPnD	CMPnEN
R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W
Initial value	0	0	0	0	0	0	0	0

CMPnCON is a special function register (SFR) to control the Comparator.

Description of Bits

- **CMPnEN** (bit 0)
  The CMPnEN bit is used to control activation (ON) or deactivation (OFF) of the Comparator n.
  It is used to indicate Comparator active status.

CMPnEN	Description
0	Deactivates the Comparator n measurement is stopped(initial value)
1	Activates the Comparator n measurement is in progress

- **CMPnD** (bit 1)
  The CMPnD bit indicates the status of comparator n output (CMPnOUT shown in the Figure 26-1).
  It is set to "1" when the voltage at CMPnP pin is larger than the voltage at CMPnM pin (CMPnP > CMPnM), is set to "0" when the voltage at CMPnP pin is smaller than the voltage at CMnPM pin (CMPnP < CMPnM).
  The last status of this bit remains after the comparator is deactivated("0" is set to CMPnEN).

CMPnD	Description
0	CMPnP < CMPnM (initial value)
1	CMPnP > CMPnM

- **CMPnRF** (bit 2)
  The CMPnRF indicate the status of comparator n measurement setting.
  CMPnD is invalid until CMPnRF bit becomes 1 after starting measurement.

CMPnRF	Description
0	CMPnD is invalid (initial value)
1	CMPnD is valid

26.2.3 Comparator n mode Registers (CMPnMOD : n=0,1)

Address: 0F922H(CMP0MODL/CMP0MOD), 0F923H(CMP0MODH),
0F92AH(CMP1MODL/CMP1MOD), 0F92BH(CMP1MODH)
Access: R/W
Access size: 8/16 bits
Initial value: 0000H

	7	6	5	4	3	2	1	0
CMPnMODL	–	–	CMPnMD1	CMPnMD0	–	–	CMPnE1	CMPnE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
CMPnMODH	–	–	–	CMPnCK	–	–	CMPnSM1	CMPnSM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

CMPnMOD is special function registers (SFRs) to set the function mode of Comparator n.
CMPnMOD needs to be set during CMPnEN is "0".

Description of Bits

- **CMPnE1-0**(bits 1 to 0)
  The CMPnE1-0 are used to set comparator judge interrupt generation condition. Each function mode has different interrupt generation sources.

CMPnMD	CMPnE1	CMPnE0	Description
Single mode	0	*	Generate interrupt when CMPnD is "0"
	1	*	Generate interrupt when CMPnD is "1"
Single monitor mode	*	*	Setting is invalid (Generate interrupt once measurement is completed)
Supervisor mode	0	0	No interrupt（initial value）
	0	1	L interrupt : Generate interrupt when CMPnD is "0" CMPnD is "0" when starting measurement or CMPnD is changed from "1" to "0" during measurement.
	1	0	H interrupt : Generate interrupt when CMPnD is "1" CMPnD is "1" when starting measurement or CMPnD is changed from "0" to "1" during measurement.
	1	1	Both edge(L and H) interrupt CMPnD is "1" when starting measurement or CMPnD is changed from "0" to "1" or "1" to "0" during measurement.

[Note]
This setting affects CMPnTGO signal. Refer to 26.3.2 for details. Use the CMPnTGO signal in Supervisor mode.

- **CMPnMD1-0** (bit 5 to 4)
  Set function mode.

CMPnMD1	CMPnMD0	Description
0	0	Single mode After CMPnEN is set and complete the compare, if the interrupt condition is match, generate interrupt and stop automatically.
0	1	Single monitor mode After CMPnEN is set and complete the compare, generate interrupt and stop automatically.
1	*	Supervisor mode(initial value) Compare is started by setting CMPnEN

- **CMPnCK, CMPnSM1-0** (bit 12, 9 to 8)
  Set comparator control clock and sampling interval timing for filtering.
  Sampling is always disabled regardless of sampling setting during the STOP mode.

CMPnCK	CMPnSM1	CMPnSM0	Description	
			Operation clock	Sampling period
0	*	0	Low speed LSCLK	No sampling
	*	1	Low speed T16KHz(LTBC output: 1/2 of LSCLK)	61us
1	0	*	High speed 1/64 of OSCLK	No sampling
	1	0		4us
	1	1	High speed 1/128 of OSCLK	8us

* LSCLK = 32.768kHz, OSCLK=16MHz

[Note]
Keep OSCLK working at HALT mode when OSCLK is selected as control clock.
Depending on the operation mode, pay attention in the timing to set STOP mode.
Refer to the 26.3.1.1-3 for STOP mode switching timing of each operation mode.

26.3 Function description

26.3.1 Comparator function

The Comparator has following 3 modes.

1. Supervisor mode : Suitable for voltage monitor always.
2. Single mode : Suitable for voltage monitor regularly. Generate interrupts par specified.
3. Single monitor mode : Suitable for voltage monitor regularly. Software outputs compare result always.

26.3.2 Supervisor mode

This mode set comparator always on. And generate interrupt by variation of the compare result.
Without interrupt, compare result can be monitor by reading CMPnD bit from Software.

Setting instruction:

(1) Set Operating clock, filtering, interrupt option, and supervisor mode by CMPnMOD register.
The operation of the CMPnTGO signal changes by this setting..

CMPnE1-0	Description	
	Interrupt	CMPnTGO signal
00	No interrupt	Asserted when CMPnD is "1" when starting measurement or CMPnD is changed from "0" to "1" during measurement.
01	L interrupt : Generate interrupt when CMPnD is "0" CMPnD is "0" when starting measurement or CMPnD is changed from "1" to "0" during measurement.	Asserted when CMPnD is "0" when starting measurement or CMPnD is changed from "1" to "0" during measurement.
10	H interrupt : Generate interrupt when CMPnD is "1" CMPnD is "1" when starting measurement or CMPnD is changed from "0" to "1" during measurement.	Asserted when CMPnD is "1" when starting measurement or CMPnD is changed from "0" to "1" during measurement.
11	Both edge(L and H) interrupt CMPnD is "1" when starting measurement or CMPnD is changed from "0" to "1" or "1" to "0" during measurement.	

(2) Set CMPnEN
In case of interrupt, generate interrupt only when the condition set by CMPnE1-0 match.

(3)After Trdy progress, CMPnRF becomes "1", and then CMPnD becomes valid;
In case of reading CMPnD with no interrupt or before generating interrupt, please make sure CMPnRF is "1".
Because status is stable waiting during CMPnRF is "0" at operation, CMPnD value is invalid.
CMPnRF need to be "1" when switch to STOP mode.

The timing chart is as follows.

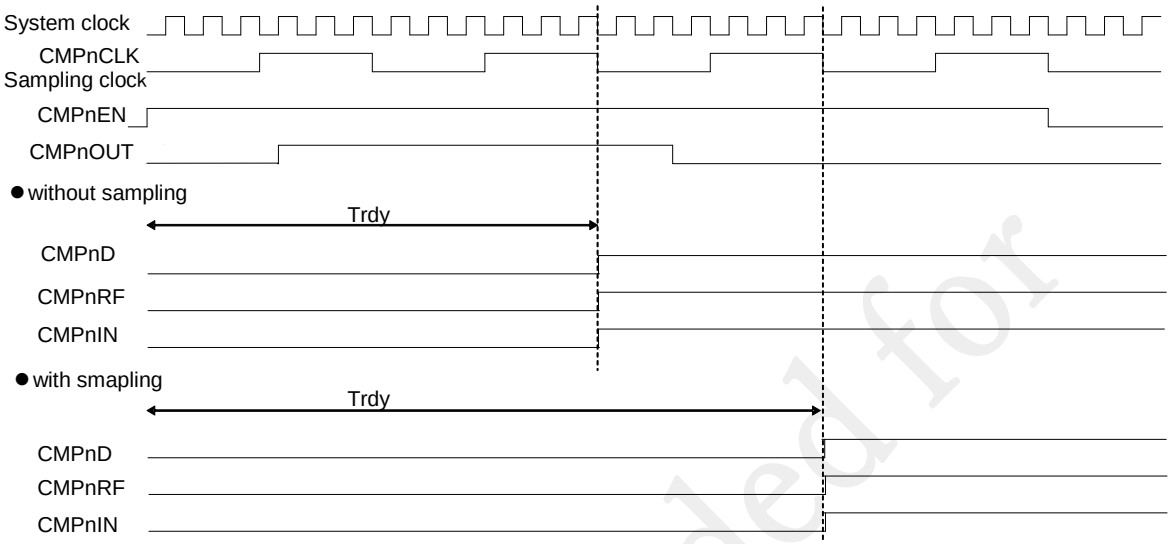


Figure 26-2 Timing in the supervisor mode

Time before CMPnD setting becoming valid is depending on operation/sampling clock setting.

CMPnCK	CMPnSM1	CMPnSM0	Operation clock	Sampling	T_{rdy}	
0	0	0	Low speed LSCLK	OFF	2φ	61.0 us
0	0	1	Low speed T16KHz(LTBC output: 1/2 of LSCLK)	ON	3φ	183.1 us
1	0	0	High speed 1/64 of OSCLK	OFF	3φ	12.0 us
1	1	0	High speed 1/64 of OSCLK	ON	4φ	16.0 us
1	1	1	High speed 1/128 of OSCLK	ON	3φ	24.0 us

* LSCLK = 32.768kHz, OSCLK=16MHz

26.3.3 Single mode

This mode activate comparator as specified and generate interrupt by compare result, and deactivate comparator automatically by hardware.

Setting instruction:

(1) Set Operating clock, filtering, interrupt option, and single mode by CMPnMOD register.

CMPnE1-0	Description
00	Generate interrupt when CMPnD is "0"
01	
10	Generate interrupt when CMPnD is "1"
11	

(2) Set CMPnEN

(3) After Trdy progress, CMPnRF is set to "1", and then data is set to CMPnD. At that time, if the condition that was set by CMPnE1-0 match, generate interrupt.

(4) After Tend progress, hardware set CMPnEN to "0". CMPnD compare result is kept until CMPnEN is set to "1".
Need interval (Trdy+Tend) of from CMPnEN setting to next MPnEN setting. It is recommended to confirm CMPnEN="0" before set CMPnEN.
It is prohibited to switch to STOP mode during operation. CMPnEN need to be set "0" when switch to STOP mode.

The timing chart is as follows

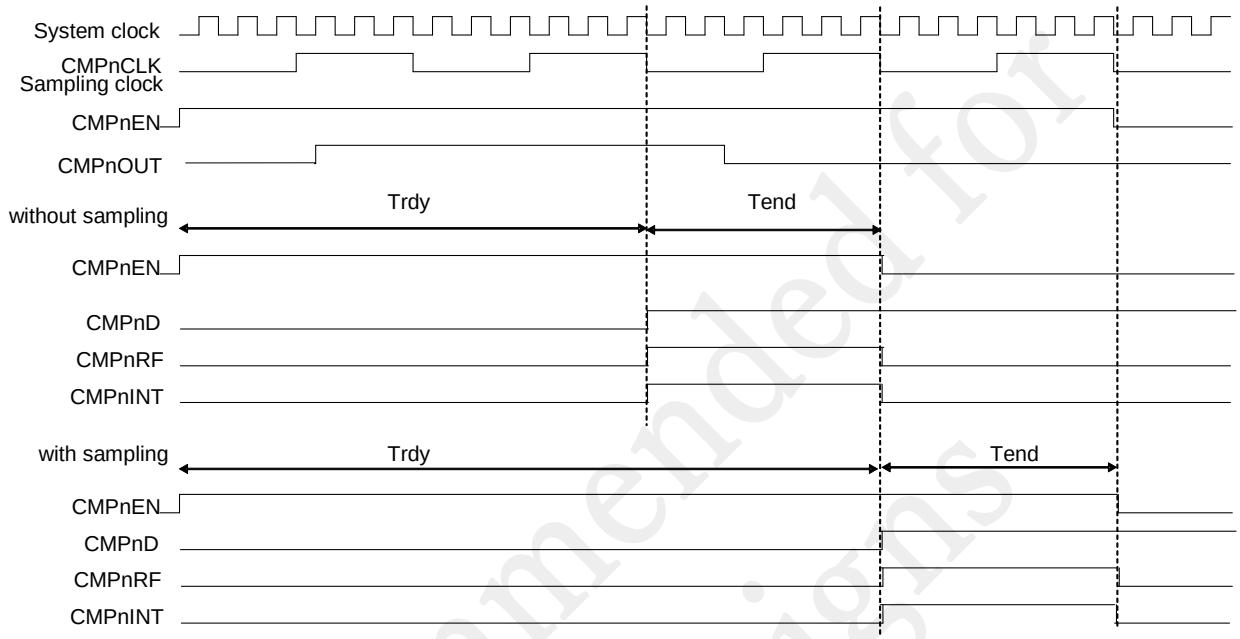


Figure 26-3 Timing in the single mode

Time before CMPnD setting becoming valid is depending on operation/sampling clock setting.

CMPnCK	CMPnSM1	CMPnSM0	Operation clock	Sampling	T_{rdy} (time to judge(interrupt))		$T_{rdy}+T_{end}$ (time to comparator off)	
0	0	0	Low speed LSCLK	OFF	2φ	61.0 us	3φ	91.6 us
0	0	1	Low speed T16KHz(LTBC output: 1/2 of LSCLK)	ON	3φ	183.1 us	4φ	244.2 us
1	0	0	High speed 1/64 of OSCLK	OFF	3φ	12.0 us	4φ	16.0 us
1	1	0	High speed 1/64 of OSCLK	ON	4φ	16.0 us	5φ	20.0 us
1	1	1	High speed 1/128 of OSCLK	ON	3φ	24.0 us	4φ	32.0 us

* LSCLK = 32.768kHz, OSCLK=16MHz

26.3.4 Single monitor mode

This mode activate comparator as specified and generate interrupt after measurement, and deactivate comparator automatically by hardware.

Setting instruction:
(1)Set operation clock, filtering, and single monitor mode by CMPnMOD register.
Interrupt setting is invalid. Only complete interrupt is generated. Also complete interrupt is generated in case of suspend of operation by software.

(2) Set CMPnEN

(3) After Tend progress, comparator is automatically off and generate complete interrupt. Read CMPnD(Compare result) from software. CMPnD (Compare result) is kept until "1" is set to CMPnEN.

It is prohibited switch to STOP mode during operation. CMPnEN need to be "0" when switch to STOP mode.

The timing chart is as follows

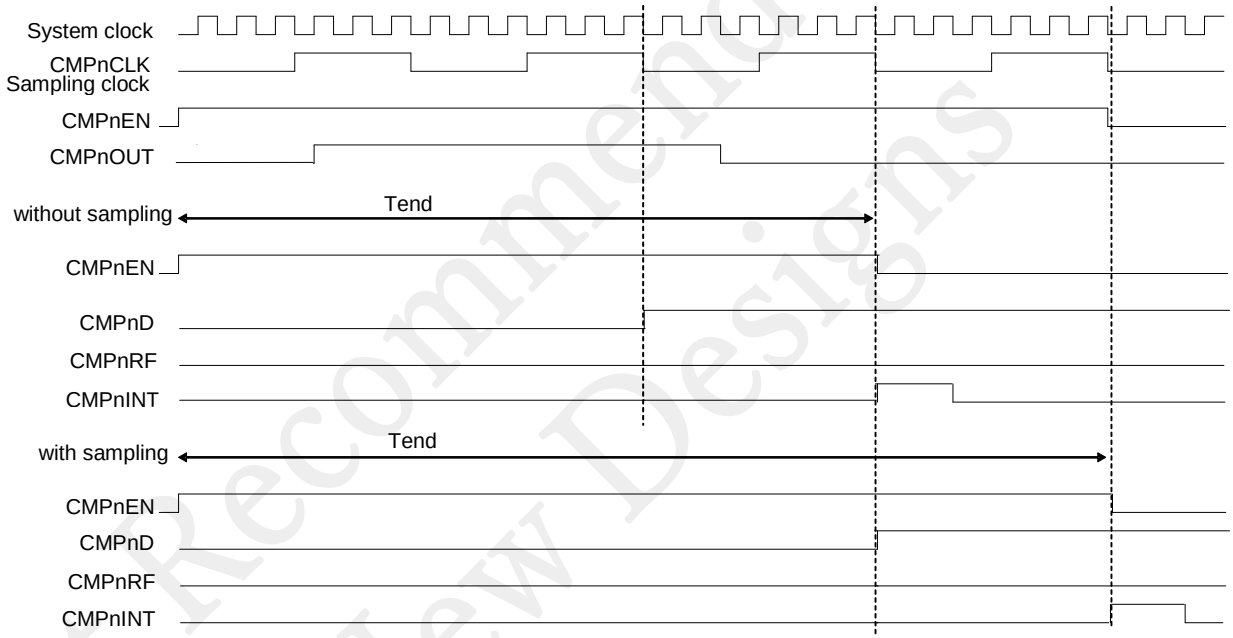


Figure 26-4 Timing in the single-monitor mode

Time before CMPnD setting becoming valid is depending on operation/sampling clock setting.

CMPnCK	CMPnSM1	CMPnSM0	Operation clock	Sampling	T_{end} (Time before turning off the comparator)	
0	0	0	Low speed LSCLK	OFF	3φ	91.6 us
0	0	1	Low speed T16KHz(LTBC output: 1/2 of LSCLK)	ON	4φ	244.2 us
1	0	0	High speed 1/64 of OSCLK	OFF	4φ	16.0 us
1	1	0	High speed 1/64 of OSCLK	ON	5φ	20.0 us
1	1	1	High speed 1/128 of OSCLK	ON	4φ	32.0 us

Chapter 27

Flash Memory Control

27 Flash Memory Control

27.1 General Description

The flash memory rewriting function includes rewriting function of the data flash using special function registers (SFRs), ISP (In System Programming) function used to rewrite the program memory by software, and remap function of the boot area.

For the rewriting conditions and specifications, refer to the section for flash memory specification in Appendix C "Electrical Characteristics".
For the program memory space and data flash area, refer to Chapter 2 "CPU and Memory Space".

27.1.1 Features

- Supports 1-word write function
- Supports two erase types, block erase (by 8 KB) and sector erase (by 1 KB)
- 10,000 times of rewrite for data flash (100 times for program memory)
- Avoids write errors by the write/erase command enable register (flash acceptor)
- Supports ISP function (boot area remap is possible by software and hardware)

27.2 Description of Registers

27.2.1 List of Registers

Address [H]	Name	Symbol (Word)	Symbol (Byte)	R/W	Size	Initial value [H]
0F0E0	Flash address register	FLASHAL	FLASHA	R/W	8/16	00
0F0E1		FLASHAH		R/W	8	00
0F0E2	Flash data register	FLASHDL	FLASHD	R/W	8/16	00
0F0E3		FLASHDH		R/W	8	00
0F0E4	Flash control register	FLASHCON	–	W	8	00
0F0E6	Flash acceptor	FLASHACP	–	W	8	00
0F0E8	Flash segment register	FLASHSEG	–	R/W	8	00
0F0EA	Flash self register	FLASHSLF	–	R/W	8	00
0F0EC	Remap address register	REMAPADD	–	R/W	8	00

27.2.2 Flash Address Register (FLASHA)

Address: 0F0E0H
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
FLASHAL	FA7	FA6	FA5	FA4	FA3	FA2	FA1	FA0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
FLASHAH	FA15	FA14	FA13	FA12	FA11	FA10	FA9	FA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHA is a special function register (SFR) used to set the flash memory rewrite addresses.

Description of Bits

- **FA15-0** (bits 15 to 0)
  The FA15 to FA0 bits are used to set the address for block erase, sector erase, or 1-word write. The bit 0 is fixed to 0, and write to bit 0 is ignored.
  At block erase, the block specified by FA15 to FA13 is erased.
  At sector erase, the sector specified by FA15 to FA10 is erased.

Table 27-1 and Table 27-2 show the address setting values for block erase and sector erase respectively.

[Note]
Specify the addresses before remap in this register even after software remap or hardware (external pin) remap. For remap function, refer to "27.3.4 Boot Area Remap Function by Software" and "27.3.5 Boot Area Remap Function by Hardware".

27.2.3 Flash Data Register (FLASHD)

Address: 0F0E2H
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
FLASHDL	FD7	FD6	FD5	FD4	FD3	FD2	FD1	FD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
FLASHDH	FD15	FD14	FD13	FD12	FD11	FD10	FD9	FD8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHD is a special function register (SFR) used to set the flash memory rewrite data.

Description of Bits

- **FD7-0** (bits 7 to 0)
  The FD7 to FD0 bits are used to set the lower data for 1-word write.

- **FD15-8** (bits 15 to 8)
  The FD15 to FD8 bits are used to set the upper data for 1-word write.
  Writing to the FD15 to FD8 bits starts the 1-word write.

[Note]
Clear the contents of the target addresses in advance. The content of an overwritten address is not guaranteed. For byte access, write data to FLASHDL and FLASHDH in this order, because writing to FLASHDH starts the 1-word write.

27.2.4 Flash Control Register (FLASHCON)

Address: 0F0E4H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHCON	–	–	–	–	–	–	FSERS	FERS
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

FLASHCON is a write-only special function register (SFR) to control the block erase and sector erase for the flash memory rewrite.

Description of Bits

- **FERS** (bit 0)
  The FERS bit is used to start the block erase.
  Setting the FERS bit to "1" erases the block specified by the FLASHSEG and FLASHAH registers. This bit is automatically set to "0" after completing the erase.

- **FSERS** (bit 1)
  FSERS is a bit to specify the start of the sector erase.
  Setting the FSERS bit to "1" erases the sector specified by the FLASHSEG and FLASHAH registers. This bit is automatically set to "0" after completing the erase.

FSERS	FERS	Description
0	0	Setting is invalid
0	1	Start block erase
1	0	Start sector erase
1	1	Start block erase

27.2.5 Flash Acceptor (FLASHACP)

Address: 0F0E6H
Access: W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHACP	fac7	fac6	fac5	fac4	fac3	fac2	fac1	fac0
R/W	W	W	W	W	W	W	W	W
Initial value	0	0	0	0	0	0	0	0

FLASHACP is a write-only special function register (SFR) to control the block erase for the flash memory rewrite or sector erase or enable/disable the 1-word write operation.

Description of Bits

- **fac7-0** (bits 7 to 0)
  The fac7 to fac0 bits are used to restrict the block erase or sector erase or 1-word write operation in order to prevent an unintended erase or an unintended write.
  Writing "0FAH" and "0F5H" to FLASHACP in this order enables a one-time block erase or sector erase or 1-word write.
  For subsequent block erase or sector erase or 1-word write, it is necessary to write "0FAH" and "0F5H" to FLASHACP each time.
  Even if another instruction is inserted between "0FAH" and "0F5H" written to FLASHACP, the block erase or sector erase or 1-word write is enabled. Note that, if data other than "0F5H" is written to FLASHACP after "0FAH" is written, the "0FAH" write processing becomes invalid. So, it is necessary to rewrite "0FAH" at first.

27.2.6 Flash Segment Register (FLASHSEG)

Address: 0F0E8H
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHSEG	–	–	–	–	–	FSEG2	FSEG1	FSEG0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHSEG is a special function register (SFR) used to set the flash memory rewrite segment address.

Description of Bits

- **FSEG2-0** (bits 2 to 0)
  The FSEG2 to FSEG0 bits are used to set the segment address of FLASH memory.

27.2.7 Flash Self Register (FLASHSLF)

Address: 0F0EAH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
FLASHSLF	–	–	–	–	–	–	–	FSELF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

FLASHSLF is a special function register (SFR) used to control the flash memory self-rewrite function.

Description of Bits

- **FSELF** (bit 0)
  To use the flash memory self-rewrite function, the FSELF bit needs to be set to "1".

FSELF	Description
0	Flash memory rewrite disabled (initial value)
1	Flash memory rewrite enabled

27.2.8 Remap Address Register (REMAPADD)

Address: 0F0ECH
Access: R/W
Access size: 8 bits
Initial value: 00H

	7	6	5	4	3	2	1	0
REMAPADD	RBTA	RES2	RES1	RES0	REA15	REA14	REA13	REA12
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value	0	0	0	0	0	0	0	0

REMAPADD is a special function register (SFR) used to specify the remap area.
In REMAPADD, the following two types of remapping can be specified.

1. Remap the addresses from 0000H to 0FFFH (4 KB) to an area of the same size (4 KB) starting from the address specified by the RES2 to RES0 bits and REA15 to REA12 bits.
2. Remap the addresses from 0000H to 03FFH (1 KB) to the ISP boot area (addresses from FC00H to FDFFH) by setting the RBTA bit.

When the software reset is executed by the BRK instruction (* only the CPU is reset), the CPU executes instructions from the beginning address of the remap area specified in REMAPADD. Note that the remap function remaps all of the vector table areas (reset vector area, hardware interrupt vector area, and software interrupt vector area).
* For the BRK instruction, refer to "nX-U16/100 Core Instruction Manual".

Description of Bits

- **REA15-12** (bits 3 to 0)
  The REA15 to REA12 bits are used to set the higher 4 bits (bits 15 to 12) of the start address of the area to remap.
  Example) When "0BH" is set in REA15 to 12 and the BRK instruction is executed, the area from B000H to BFFFH is mapped to 0000H to 0FFFH.

- **RES2-0** (bits 6 to 4)
  The RES2 to RES0 bits are used to set the segment of the area to remap.
  Since only segments 0 and 1 are used in this LSI, set these bits to 0 or 1.

- **RBTA** (bit 7)
  By setting RBTA to "1", bit[11:10] of head address which remapping is set to “11”b. The head address of remapping can be set to “FC00”H by setting REA15-12 as "F"h. And boot area can be remapping in ISP boot area (addresses from FC00H to FDFFH). It is also possible to use the external pin (TEST0) to boot from the ISP boot area (called "hardware remap"). For details of hardware remap, refer to "27.3. 5 Boot Area Remap Function by Hardware".

[Note]
To boot from the ISP boot area, it is necessary to write the boot program in advance in the addresses from FC00H to FDDFH of the ISP boot area (addresses FC00H to FDFFH) by using ICE, etc. Also, be sure to write "0FFH" in addresses from FDE0H to FDFFH.

27.3 Description of Operation

The following functions are executable by the flash memory control registers.

1) Data flash rewriting
2) Program code rewriting

When rewriting program code
If use of the self-rewrite function, it is necessary to prepare for the program in advance for self-rewrite on a program code area except the addresses targeted for block/sector erase or 1-word write.
The self-rewrite function includes the block erase function that erases by 4K words (8K bytes), the sector erase function that erases by 512 words (1K byte), and the 1-word write function that writes by 1 word (2 bytes).

The rewrite count of the flash memory depends on the address as shown in the table below.

Product name	Rewrite address	Rewrite count
ML620Q503H	0:0000h to 0:7FFFh*1	100
	7:0000h to 7:07FFh	10000
ML620Q504H	0:0000h to 0:FFFFh*2	100
	7:0000h to 7:07FFh	10000

Parameter	Specifications
Sector erase time	(Max.) 100ms
Block erase time	(Max.) 100ms
1-word (2 bytes) write	(Max.) 40μs

[Note]
*1: ML620Q503H : The test data area (0:7C00h to 0:7FFFh) is excluded.
*2: ML620Q504H : The test data area (0:FC00h to 0:FFFFh) is excluded.

It also includes the flash self register and flash rewrite acceptor function that restrict the self-rewrite operation, to prevent an improper rewriting of the flash memory. When "0FAH" and "0F5H" are written to the flash acceptor (FLASHACP) in this order after the self-rewrite function is enabled in the flash self register, the block/sector erase or 1-word write is enabled only once.

Notes:
• System clock for writing/erasing the flash
Flash write/erase cannot be performed at the low-speed system clock.
At the low-speed system clock, the write/erase command is disabled.
Make a selection the high-speed system clock as the CPU clock, and the frequency should be controlled in the range from 384kHz to 16MHz.

• Debugging of the flash rewrite program
When debugging the flash rewrite program by using uEASE, etc., do not use breaks or the step run in the flash rewrite sequence "from write to the flash acceptor to write to the flash data register". Otherwise, rewrite may fail.

27.3.1 Address Setting for Erase

Table 27-1 Address Setting Values for Block Erase

Area for block erase				FLASHSEG			FLASHAH							
Segment	Address			SEG 2	SEG 1	SEG 0	FA 15	FA 14	FA 13	FA 12	FA 11	FA 10	FA 9	FA 8
Segment 0	0:0000H	to	0:1FFFH	0	0	0	0	0	0	0	0	0	0	0
	0:2000H	to	0:3FFFH	0	0	0	0	0	1	0	0	0	0	0
	0:4000H	to	0:5FFFH	0	0	0	0	1	0	0	0	0	0	0
	0:6000H	to	0:7FFFH	0	0	0	0	1	1	0	0	0	0	0
	0:8000H	to	0:9FFFH	0	0	0	1	0	0	0	0	0	0	0
	0:A000H	to	0:BFFFH	0	0	0	1	0	1	0	0	0	0	0
	0:C000H	to	0:DFFFH	0	0	0	1	1	0	0	0	0	0	0
Segment 7	7:0000H	to	7:07FFH	1	1	1	0	0	0	0	0	0	0	0

Table 27-2 Address Setting Values for Sector Erase

Area for sector erase				FLASHSEG			FLASHAH							
Segment	Address			SEG 2	SEG 1	SEG 0	FA 15	FA 14	FA 13	FA 12	FA 11	FA 10	FA 9	FA 8
Segment 0	0:0000H	to	0:03FFH	0	0	0	0	0	0	0	0	0	0	0
	0:0400H	to	0:07FFH	0	0	0	0	0	0	0	0	1	0	0
	0:0800H	to	0:0BFFH	0	0	0	0	0	0	0	1	0	0	0
	:													
	:													
	0:F000H	to	0:F3FFH	0	0	0	1	1	1	1	0	0	0	0
	0:F400H	to	0:F7FFH	0	0	0	1	1	1	1	0	1	0	0
	0:F800H	to	0:FBFFH	0	0	0	1	1	1	1	1	0	0	0
Segment 7	7:0000H	to	7:03FFH	1	1	1	0	0	0	0	0	0	0	0
	7:0400H	to	7:07FFH	1	1	1	0	0	0	0	0	1	0	0

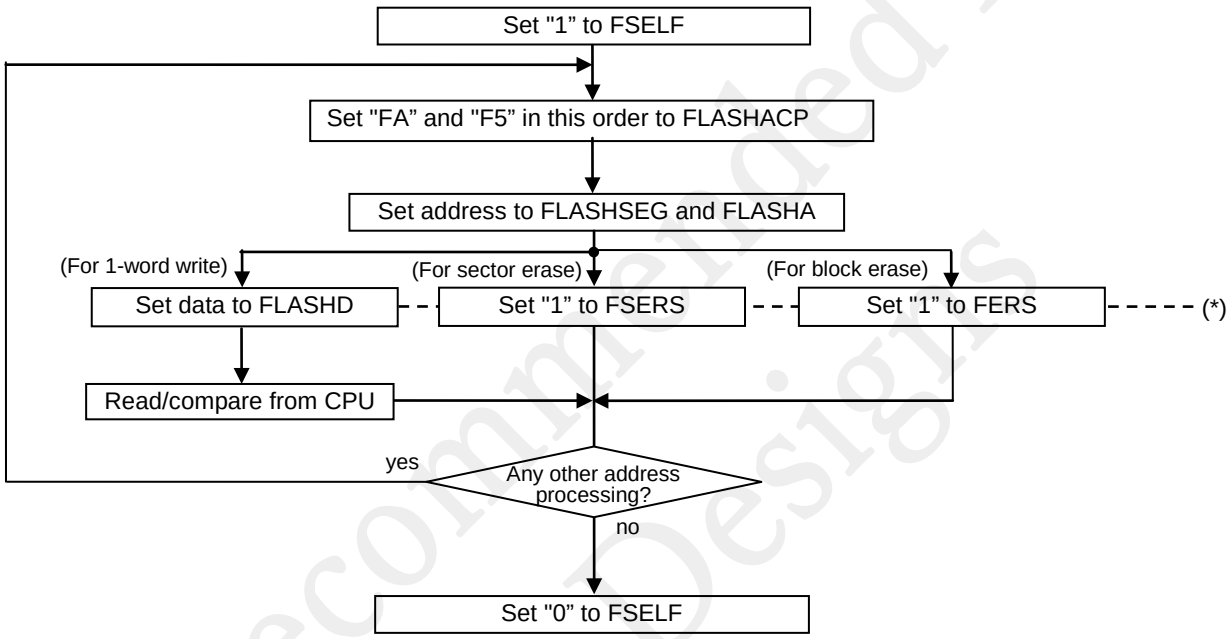
[Note]
ML620Q503H:
- For 0:6000H to 0:7BFFH, only the sector erase is available.
- 0:7E00H to 0:7FFFH cannot be erased.
- 0:8000H to 0:FFFFH cannot be used.

ML620Q504H:
- For 0:E000H to 0:FBFFH, only the sector erase is available.
- 0:FE00H to 0:FFFFH cannot be erased.

27.3.2 Data Flash Rewriting

The LSI is equipped with a data flash of 2 KB (2 sectors: 1 KB/sector). The rewrite count is 10,000.
Figure 27-1 shows the sequence of 1-word write/sector erase/block erase.

Writing is performed sequentially from the first sector. When writing to the second sector is saturated, the first sector is erased, and the next data is written to it. Thus, up to 1024 * 10,000 times of rewrite is realized when data is written by one word.
As the initial value after an erase is "FFFFH", the position matching the initial value is searched for as the write position.



*: The CPU stops during the write/erase processing. Perform the NOP processing twice after this processing.

Figure 27-1 Data Flash Rewrite Sequence

27.3.3 Program Memory Rewrite (ISP Function)

The program can be rewritten by software by using the ISP function. There are the following two ways to execute the ISP program:

1) Execute the program by remapping the boot area of the ISP program by software
2) Execute the program by remapping the ISP boot area by hardware at LSI startup

These methods boot the ISP program and rewrite the program memory in the same sequence as the data flash rewrite. These remap methods is as follows.

27.3.4 Boot Area Remap Function by Software

This function can remap the area from 0000H to 0FFFH (4 KB) to the area of the same size (4 KB) starting from the address set in the REMAPADD register.
The program can start from the remapped area by setting the start address of the area to remap in the REMAPADD register and performing the software reset (* only CPU is reset) by execution of the BRK instruction. For the BRK instruction, refer to "nX-U16/100 Core Instruction Manual".
The remap function also remaps the vector table areas (reset vector area, hardware interrupt vector area, and software interrupt vector area). It is feasible to manage interrupts independently by the program in the remap area. If the program size is 4 KB or less, it is feasible to develop the program independently of the main program. This is suitable for the cases that want to control interrupts such as the self-rewrite program separately from the normal interrupt.
Figure 27-2 shows a sample program for remap (when the start address of the remap area is F000H). Figure 27-3 shows the memory map before and after remapping.

```
MOV     R0,    #00FH      ;
ST      R0,    0F0ECH     ; Set the higher 4 bits of the start address of the area
                          ; to remap to the REMAPADD register (0F0ECH).
MOV     PSW, #02H         ; Set the interrupt level (ELEVEL) to 2.
BRK                       ; Execute the BRK instruction.
                          ; Execution starts with the code at the remapped F000H.
```

Figure 27-2 Sample Program for Remap

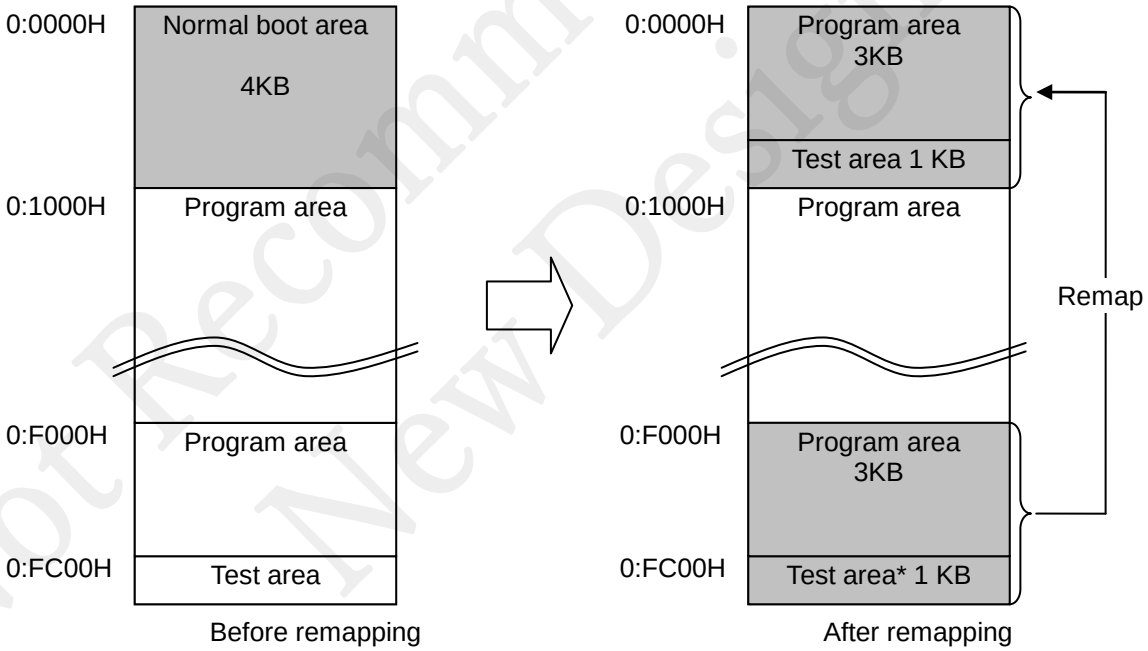


Figure 27-3 Memory Map before/after Remapping

[Note]
If the area 0:0000H to 0:1000H (4KB) before remapping need to be read after remapping, read it from 8th segment. If the area 0:0000H to 0:1000H (4KB) before remapping need to be written, set the address (0:0000H to 0:1000H) that was used before remapping to the flash address register (FLASHA). For FLASHA, refer to "27.2.2 Flash Address Register (FLASHA)".

27.3.5 Boot Area Remap Function by Hardware

When the power-on reset by power-on or the reset by the RESET_N pin is released under the condition that the external pin (TEST0) is set to High, 512 bytes of ISP boot area* and 512 bytes of test area (1 KB in total) are remapped to 0:0000H to 0:03FFH to allow the boot by the program in the ISP boot area. The ISP boot area is also remapped to 0:0400H to 0:0FFF repeatedly.
By writing the boot program in the ISP boot area in advance, the following functions can be achieved:

①When startup cannot be performed due to power down while rewriting the block 0 (area of 16 KB from 0000H) of FLASH, where the boot program is normally placed, startup (boot) from the ISP boot area can avoid a situation that recovery is not possible.

②The boot program can rewrite the internal program of the LSI by using UART which provides external communication. This can achieve a function equivalent to Flash Writer.

*: The ISP boot area differs among products. (0:FC00H to 0:FDFFH for ML620Q504H).

Figure 27-4 shows the memory map before and after remapping.

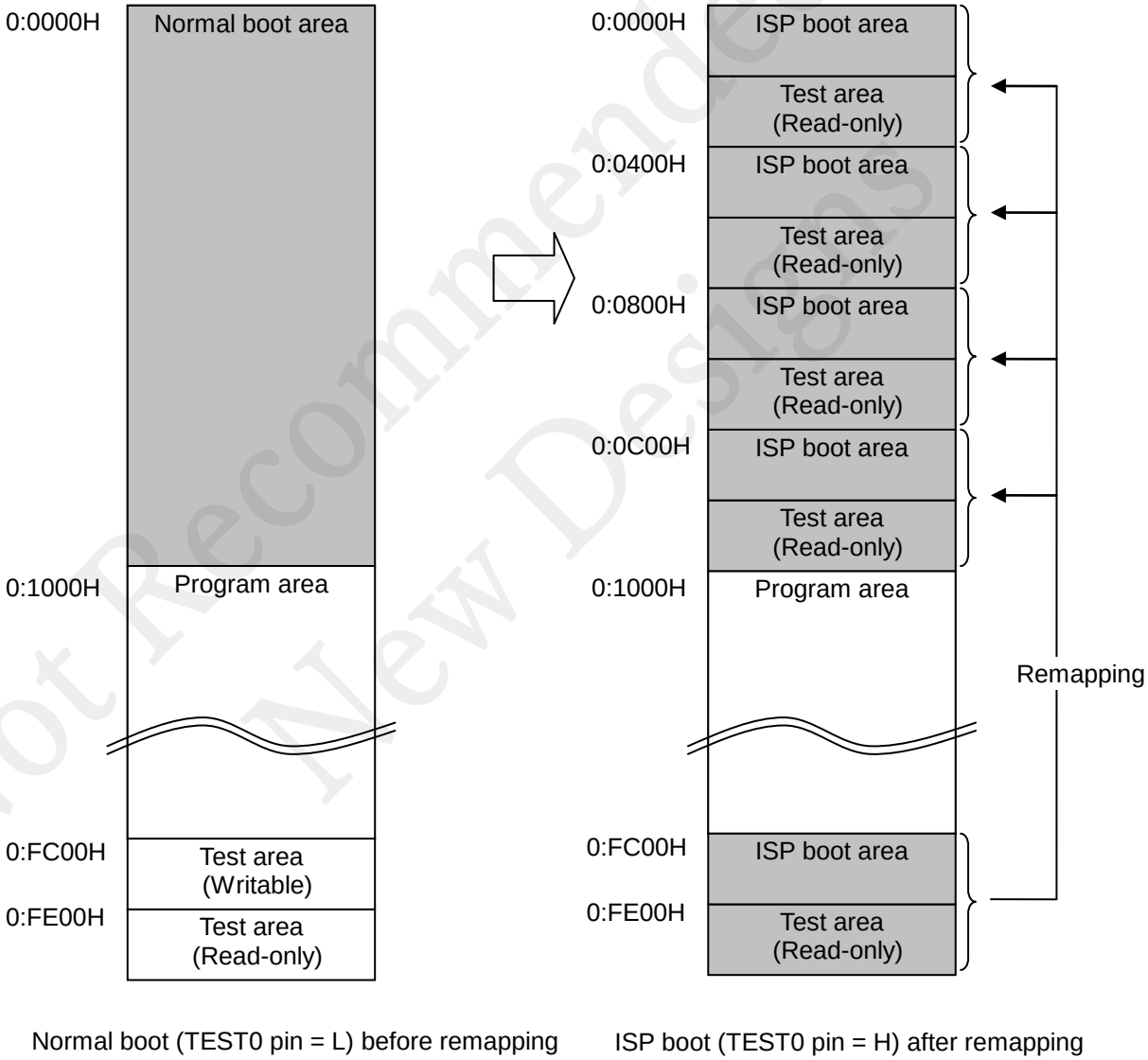


Figure 27-4 Boot Switch by Setting External Pin (TEST0)

[Note]
Write the boot program in the addresses from FC00H to FDDFH of the ISP boot area (addresses FC00H to FDFFH) in advance by using the on-chip ICE function. Please be sure to write "0FFH" in FDE0-FDFFH.
Do not set TEST0 pin to "0" during the program execution of hardware remapping.

27.3.6 Notes of the program after remapping

Load address 0000H of ROM by startup of program* executed after remapping at the head at which reset-vector points, and set it to stackpointer. Figure 27-5 shows an example of program.

```
$$start_up:
        L       ER0,    0000H
        MOV     SP,         ER0
        BAL     $begin
```

Figure 27-5 Example program of setting stackpointer

*:ISP program, loader program, user program will be targeted.
It is recommended to apply this setting even if the remap is not used.

[Note]
When the stackpointer is not set with software at the time of the software-remap from ISP program to user program, it is likely not to operate normally.

27.3.7 Sample Program

This section lists sample programs for block erase/sector erase/1-word write (assuming that the flash segment register is already set).

(1) Block erase/sector erase

```
        LEA     offset FLASHAH              ; EA←FLASHAH address
        MOV     R0,     #0FAH               ; Flash acceptor enable data
        MOV     R1,     #0F5H               ; Flash acceptor enable data
        MOV     R2,     #01H   (#02H)       ; Block (sector) erase setting data
        MOV     R4,     #(offset FLASHACP)&0FFH
        MOV     R5,     #(offset FLASHACP)>>8   ; ER4←FLASHACP address
        MOV     R6,     #(offset FLASHCON)&0FFH
        MOV     R7,     #(offset FLASHCON)>>8   ; ER6←FLASHCON address
        :
         (Set the erase start block address in R9)
MARK:
        SB      FSELF                       ; Enable flash write/erase
LOOP:

        ST      R0,     [ER4]               ; Enable flash acceptor
        ST      R1,     [ER4]               ; Enable flash acceptor
        ST      R9,     [EA]                ; Set block (sector) address
        ST      R2,     [ER6]               ; Start block (sector) erase
        NOP                                 ; *Always set
        NOP                                 ; *Always set

        RB      FSELF                       ; Disable flash write/erase
```

(2) 1-word write

```
        LEA     offset FLASHAH              ; EA←FLASHAH address
        MOV     R0,     #0FAH               ; Flash acceptor enable data
        MOV     R1,     #0F5H               ; Flash acceptor enable data
        MOV     R2,     #02H                ; Address increment data
        MOV     R3,     #00H
        MOV     R4,     #(offset FLASHACP)&0FFH
        MOV     R5,     #(offset FLASHACP)>>8   ; ER4←FLASHACP address
        :
         (Set the write start address in ER8)
         (Set the write end address in ER12)
MARK:
        SB      FSELF                       ; Enable flash write/erase

        ST      R0,     [ER4]               ; Enable flash acceptor
        ST      R1,     [ER4]               ; Enable flash acceptor
        ST      XR8,        [EA]            ; Set address and data, start 1-word write
        NOP                                 ; *Always set
        NOP                                 ; *Always set

        L       ER14,       [ER8]           ; Load data
        CMP     ER14,       ER10            ; Check data
        BNE     ERROR                       ; Go to error routine on error

        ADD     ER8,        ER2             ; Address increment
        CMP     ER8,        ER12
        BLE     MARK                        ; Compare addresses

        RB      FSELF                       ; Disable flash write/erase
```

Figure 27-6 Sample Programs for Write/Erase

[Note]
• Data erase/write during the program operation may cause the malfunction of program. Write to an address unrelated to the operation of the program.
• Be sure to set the NOP instruction twice or more, following the block erase start instruction or the write to FLASHD instruction.

Chapter 28

Voltage Level Supervisor (VLS)

28 Voltage Level Supervisor (VLS)

28.1 General Description

This LSI has one channel of built-in Voltage Level Supervisor (VLS).
This function can be used to judge whether the voltage level of V_{DD} is lower than the specified threshold voltage.

28.1.1 Features

- Accuracy: ±0.1V(Typ.)
- Threshold voltage: Selectable from 13 values (1.898V to 4.667V)
- Can be used as voltage level detection reset (VLS reset)
- Can be used as voltage level detection interrupt (VLS interrupt)

28.1.2 Configuration

The VLS consists of a comparator and a low level detection reset control circuit.
Figure 28-1 shows the configuration of the VLS.

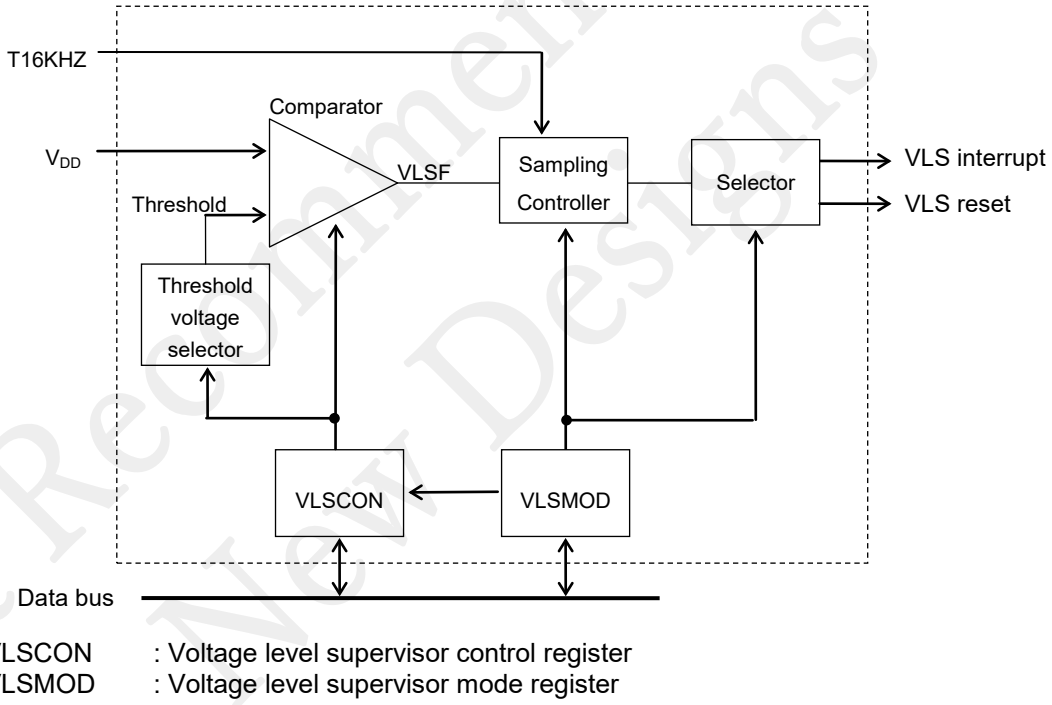


Figure 28-1 Configuration of Voltage Level Supervisor

28.2 Description of Registers

28.2.1 List of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F900	Voltage level supervisor control register	VLSCONL	VLSCON	R/W	8/16	00
0F901		VLSCONH		R/W	8	00
0F902	Voltage level supervisor mode register	VLSMODL	VLSMOD	R/W	8/16	00
0F903		VLSMODH		R/W	8	00

28.2.2 Voltage level supervisor control register (VLSCON)

Address: 0F900H
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
VLSCONL	–	–	–	–	VLSLV3	VLSLV2	VLSLV1	VLSLV0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value*	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
VLSCONH	–	–	–	–	–	VLSRF	VLSF	ENVLS
R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W
Initial value*	0	0	0	0	0	0	0	0

*: it is not reset when VLS reset is issued.

VLSCON is a special function register (SFR) used to control the voltage level detector.

Description of Bits

- **VLSLV3-0** (bits 3 to 0)
  The VLSLV3-0 bits are used to select the VLS threshold voltage of fall (V_{VLS}). The VLS has the hysteresis characteristics (H_{VLS}). The threshold voltage of rise is $V_{VLS} + H_{VLS}$. For detail, see VLS characteristic in Appendix C. They should be set when the VLS is in the OFF state (ENVLS="0").

VLSLV3	VLSLV2	VLSLV1	VLSLV0	Description
0	0	0	0	Use prohibit (initial value)
0	0	0	1	Use prohibit
0	0	1	0	Use prohibit
0	0	1	1	1.898±0.10V
0	1	0	0	2.000±0.10V
0	1	0	1	2.093±0.10V
0	1	1	0	2.196±0.10V
0	1	1	1	2.309±0.10V
1	0	0	0	2.409±0.10V
1	0	0	1	2.605±0.10V
1	0	1	0	2.800±0.10V
1	0	1	1	3.068±0.10V
1	1	0	0	3.394±0.10V
1	1	0	1	3.797±0.10V
1	1	1	0	4.226±0.10V
1	1	1	1	4.667±0.10V

- **ENVLS** (bit 8)
  The ENVLS bit is used to control ON/OFF of the VLS.
  VLS is turned on when ENVLS is set to "1", and off when "0".
  When the VLS reset is issued, the VLS keep the ON state.

ENVLS	Description
0	VLS: OFF (initial value)
1	VLS : ON

[Note]
Set VLSLV3 to VLSLV0 bits to any one of between"3"~"F"h, before setting ENVLS bit to "1".
Operation is not guaranteed in the case of the other setting.

- **VLSF** (bit 9)
  VLSF is the voltage level detection flag.
  It is "0" when the power supply voltage (V_{DD}) is higher than the threshold voltage (V_{VLS}), or "1" when the power supply voltage is lower than the threshold voltage. VLSF is initialized to 0 when VLS is set to on (ENVLS=1).

VLSF	Description
0	Higher than the threshold voltage (initial value)
1	Lower than the threshold voltage

- **VLSRF** (bit 10)
  The VLSRF flag is used to indicate whether the voltage level detection result is valid.
  When the threshold voltage value becomes valid (readable from CPU), this becomes "1".

VLSRF	Description
0	VLS is OFF or VLS is being judged (initial value)
1	VLS judgment result is valid

[Note]
Make sure that the VLSRF bit is set to "1" before enabling the STOP mode.

28.2.3 Voltage level supervisor mode register (VLSMOD)

Address: 0F902H
Access: R/W
Access size: 8/16 bit
Initial value: 0000H

	7	6	5	4	3	2	1	0
VLSMODL	–	–	–	–	–	–	VLSSEL1	VLSSEL0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value*	0	0	0	0	0	0	0	0

	15	14	13	12	11	10	9	8
VLSMODH	–	–	–	–	–	VLSAMD1	VLSAMD0	VLSSM0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Initial value*	0	0	0	0	0	0	0	0

*: it is not reset when VLS reset is issued.

VLSMOD is a special function register (SFR) used to control the voltage level detection function.
It is necessary to set this register during the VLS is in the OFF state (ENVLS="0").

Description of Bits

- **VLSSEL1-0** (bits 1 to 0)
  The VLSSEL1-0 bits are used to control enable/disable of the VLS reset/VLS interrupt request functions when the voltage is lower than the threshold voltage.

VLSSEL1	VLSSEL0	Description
0	0	Reset function: disable, Interrupt request function: disable (initial value)
0	1	Reset function: enable, Interrupt request function: disable
1	0	Reset function: disable, Interrupt request function: enable
1	1	Reset function: enable, Interrupt request function: disable

- **VLSSM0** (bit 8)
  The VLSSM0 bit is used to select whether or not to use sampling for the VLS detection.

VLSSM0	Description
0	Detects without sampling (initial value)
1	Detects with sampling (T16KHZ 2ϕ)

[Note]
In the STOP mode, no sampling is performed regardless of the value set in VLSSM0 since the sampling clock stops. The sampling depends on the frequency of LSCLK.

- **VLSAMD1-0 (bits 10 to 9)**
  The VLSAMD1-0 bits are used to set the VLS running mode.

VLSAMD1	VLSAMD0	Description
0	0	Use prohibit (initial value)
0	1	Use prohibit
1	0	Supervisor mode
1	1	Supervisor mode

[Note]
VLSAMD1 - 0 bits set to ”2” or ”3”h, before setting ENVLS bit to “1”.Operation is not guaranteed in the case of the other setting.

28.3 Description of Operation

The VLS can judge whether V_{DD} on the CPU is lower or higher than the specified threshold voltage by reading SFR, and also it can issue a VLS interrupt or VLS reset when V_{DD} becomes lower than the specified threshold voltage.
The VLS has a hysteresis characteristics (H_{VLS}), The threshold voltage of rise is $V_{VLS} + H_{VLS}$. For detail, see VLS characteristic in Appendix C.

The following operation mode are provided:

Supervisor mode:

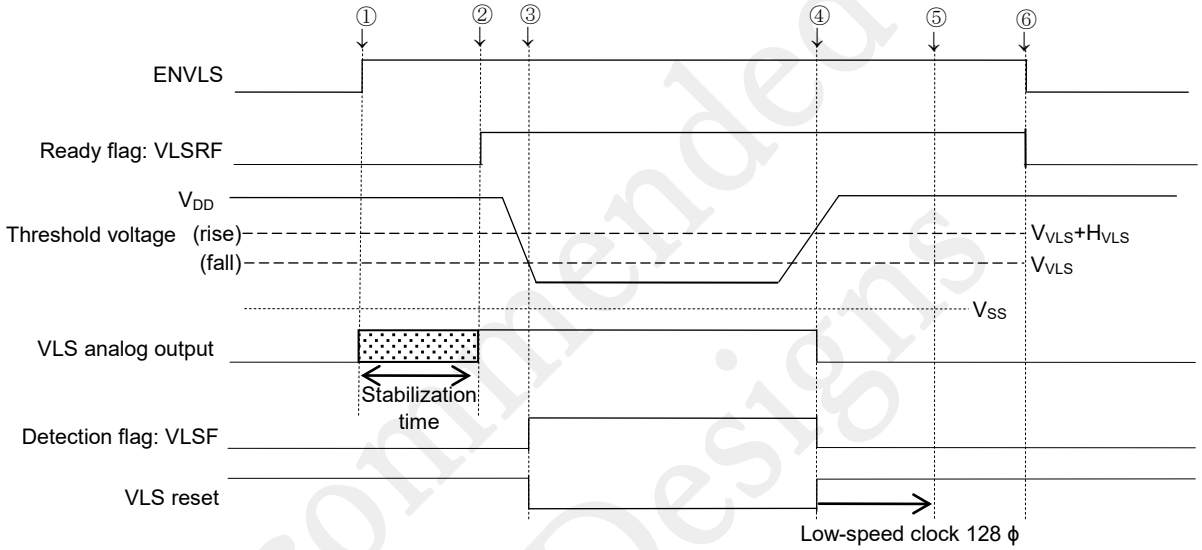
Set ENVLS to ”1” to turn on VLS for voltage judgment. When the judgment result becomes valid, it is notified by using the VLSRF flag. The judgment still continues.

VLS interrupt or VLS reset can be set to constantly monitor the power supply voltage and issue an interrupt or reset when it becomes lower than the threshold voltage.

28.3.1 Supervisor mode

When setting ENVLS with VLSAMD1-0 set to ”10” or ”11”, the supervisor mode is activated.
The supervisor mode is useful for using the low voltage detection interrupt/reset with always-ON. The detection flag(VLSF)/reset is masked until the ready flag is asserted.
If VLS interrupt is used, set the VLS interrupt before setting ENVLS.
VLSRF (ready flag) is asserted when T16KHZ 4ϕ (+2 ϕ when the sampling is enabled) passes after setting ENVLS. The software should read the VLSF value after VLSRF=”1”.
Even if the VLS interrupt or VLS reset is allowed, the issue is allowed after VLSRF is asserted.
When V_{DD} becomes lower than the specified threshold voltage, a VLS interrupt or VLS reset is issued.
To turn off the VLS function, set ENVLS to ”0” from the software.

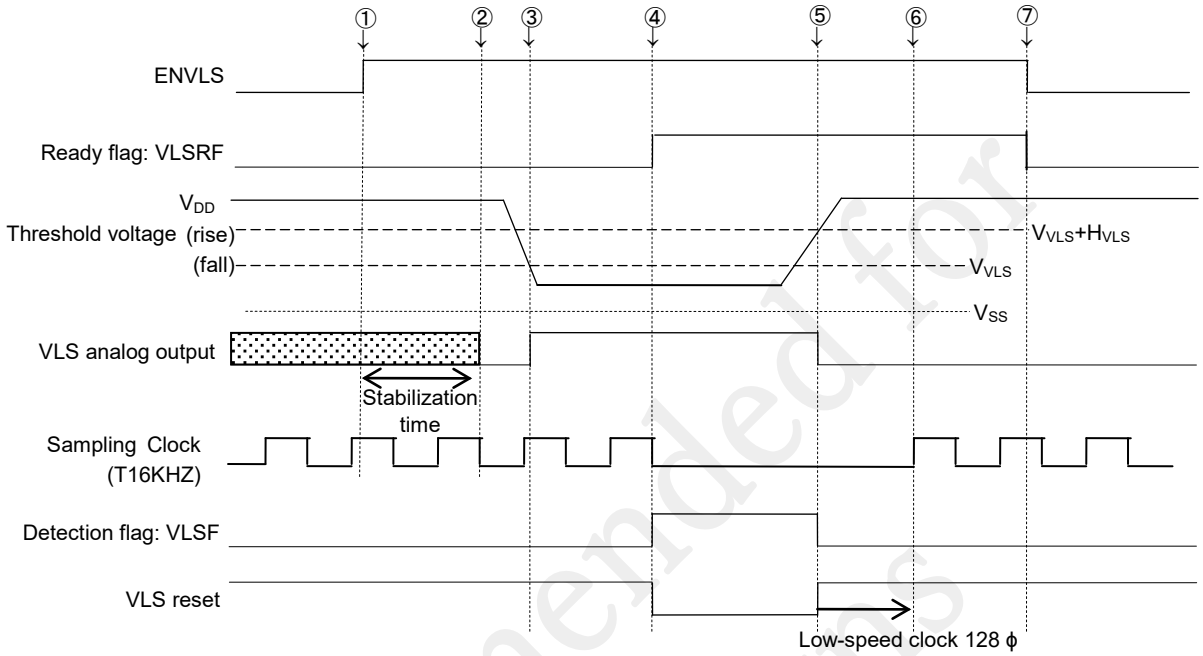
Figure 28-2 shows an example of the operation timing diagram when detecting without sampling and setting the VLS reset issue.



① Set ENVLS to “1” from the CPU to turn on the VLS.
② When the VLS analog output is stabilized, the ready flag (VLSRF) is set to ”1”.
③ The voltage level detection flag (VLSF) is set to “1” to issue a VLS reset because V_{DD} becomes lower than the specified threshold voltage (V_{VLS}).
④ The voltage level detection flag (VLSF) is set to “0” to release the VLS reset because V_{DD} becomes higher than the specified threshold voltage (V_{VLS}+H_{VLS}).
⑤ The CPU starts operation after 128ϕ of low-speed clock.
⑥ Set ENVLS to “0” from the CPU to turn off the VLS.

Figure 28-2 Operation Timing Diagram When Detecting without Sampling and Setting VLS Reset Issue

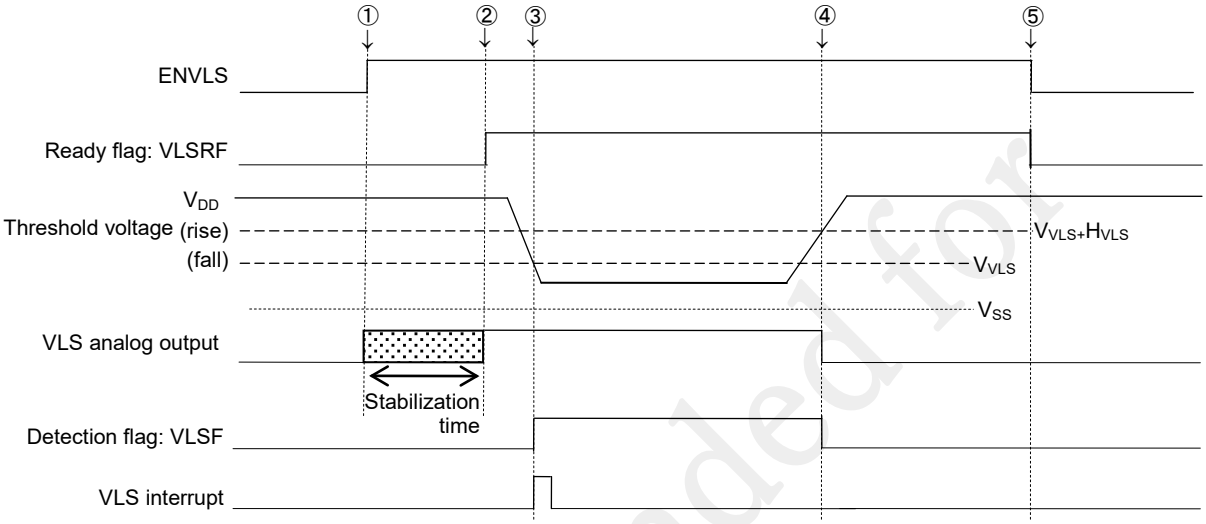
Figure 28-3 shows an example of the operation timing diagram when detecting with sampling and setting the VLS reset issue.



① Set ENVLS to “1” from the CPU to turn on the VLS.
② The VLS analog output is stabilized.
③ V_{DD} becomes lower than the specified threshold voltage (V_{VLS}).
④ The ready flag (VLSRF) is set to “1” after T16KHZ 2 ϕ. At the same time, the voltage level detection flag (VLSF) is set to “1” to issue a VLS reset because the V_{DD} is lower than the threshold voltage (V_{VLS}).
⑤ The voltage level detection flag (VLSF) is set to “0” to release the VLS reset because the V_{DD} returns to higher than the threshold voltage of rise ($V_{VLS}+H_{VLS}$).
⑥ The CPU starts after 128 ϕ of low-speed clock. Then the VLS does not operate while T16KHZ stops.
⑦ Set ENVLS to “0” from the CPU to turn off the VLS.

Figure 28-3 Operation Timing Diagram When Detecting with Sampling and Setting VLS Reset Issue

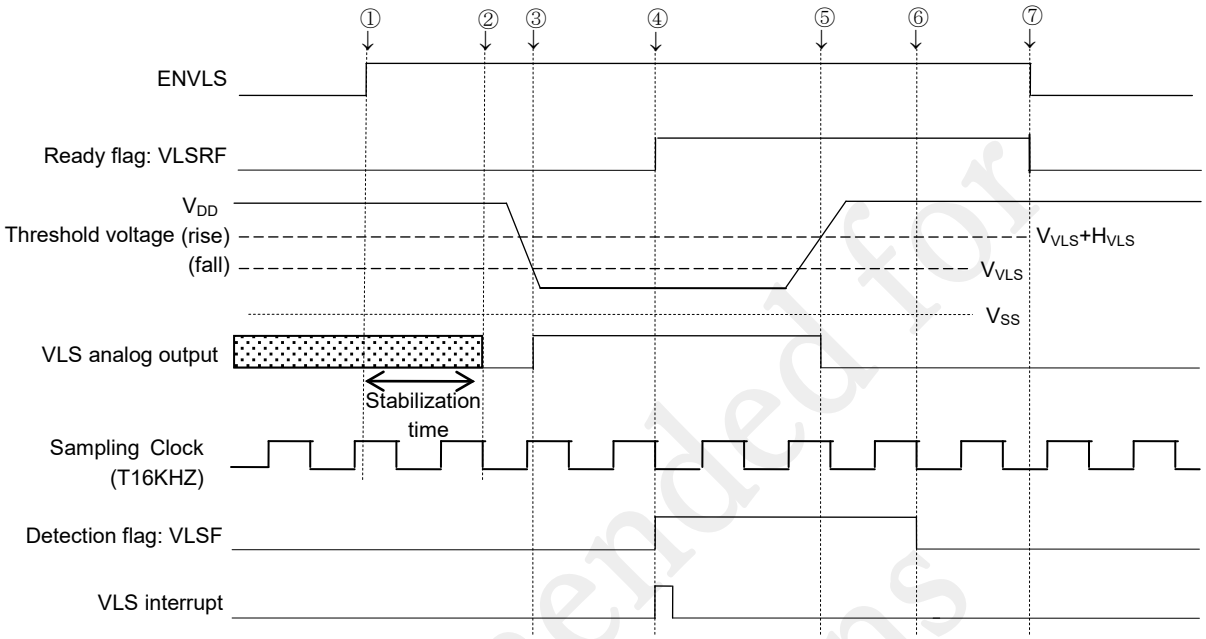
Figure 28-4 shows an example of the operation timing diagram when detecting without sampling and setting the VLS interrupt issue.



① Set ENVLS to “1” from the CPU to turn on the VLS.
② When the VLS analog output is stabilized, the ready flag (VLSRF) is set to ”1”.
③ The voltage level detection flag (VLSF) is set to “1” to issue a VLS interrupt because V_{DD} becomes lower than the specified threshold voltage (V_{VLS}).
④ The voltage level detection flag (VLSF) is set to “0” because V_{DD} becomes higher than the threshold voltage of rise ($V_{VLS}+H_{VLS}$).
⑤ Set ENVLS to “0” from the CPU to turn off the VLS.

Figure 28-4 Operation Timing Diagram When Detecting without Sampling and Setting VLS Interrupt Issue

Figure 28-5 shows an example of the operation timing diagram when detecting with sampling and setting the VLS interrupt issue.



① Set ENVLS to “1” from the CPU to turn on the VLS.
② The VLS analog output is stabilized.
③ V_{DD} becomes lower than the specified threshold voltage (V_{VLS}).
④ The ready flag (VLSRF) is set to ”1” after T16KHZ2ϕ. At the same time, the voltage level detection flag (VLSF) is set to “1” to issue a VLS interrupt because the VLS analog voltage is lower than the threshold voltage (V_{VLS}).
⑤ V_{DD} returns to higher than the threshold voltage of rise ($V_{VLS}+H_{VLS}$).
⑥ Because it is judged that a VLS analog voltage sampled at T16KHZ is higher than the threshold voltage ($V_{VLS}+H_{VLS}$),
the voltage level detection flag (VLSF) is set to “0”.
⑦ Set ENVLS to “0” from the CPU to turn off the VLS.

Figure 28-5 Operation Timing Diagram When Detecting with Sampling and Setting VLS interrupt issue

Chapter 29

LLD circuit

29 LLD circuit

29.1 General Description

LLD circuit monitors Power supply Voltage level. When Power supply Voltage falls than the threshold voltage, LLD reset this LSI.

29.1.1 Features

- Judgment Voltage : 1.8V±0.2V
- generate LSI reset
- Selectable LLD enable/disable

29.2 Description of resister

Control LLD validation by resister setting.
LLD is invalidated initially.
LLD can be validated by setting block control resister 45(BLKCON45) DLLD bit to "0".

29.3 Description of operation

LLD circuit is controlled by DLLD bit of block control register 45(BLKCON45).
This circuit compares the power supply voltage with the threshold voltage. If the power supply voltage is below the threshold voltage, LLD generate reset.
See DC characteristics(LLD) of Appendix C Electrical Characteristics for details about the threshold voltage.

Chapter 30

On-Chip Debug Function

30 On –Chip Debug Function

30.1 Overview

This LSI has an on-chip debug function allowing Flash memory rewriting.
The on-chip debug emulator is connected to this LSI to perform the on-chip debug function.
See manual of the debugger as necessary.

30.2 Method of Connecting to On-Chip Debug Emulator

Figure 30-1 shows connection to the on-chip debug emulator.

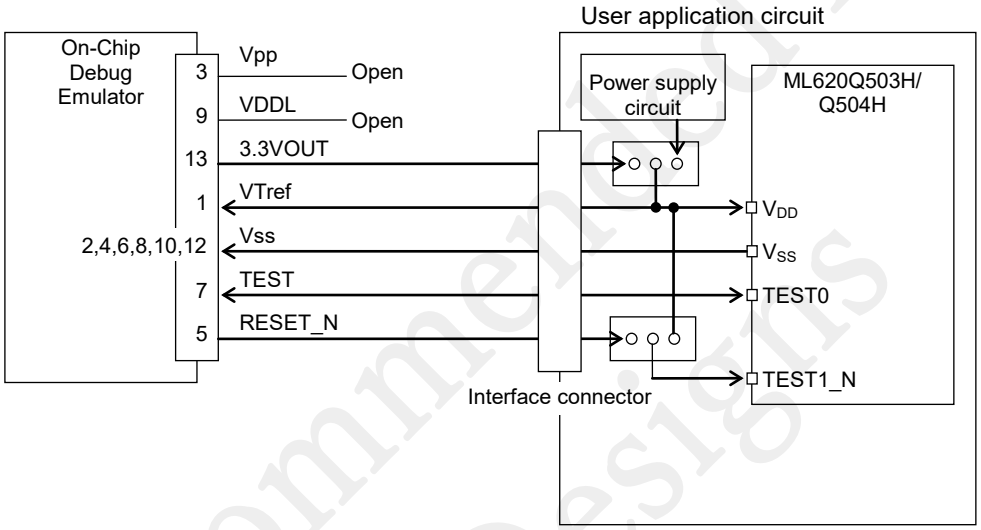


Figure 30-1 Connection to On-chip Debug Emulator

Note:
- Please do not apply LSIs used for debugging to mass production.
- When using the on-chip debug function or the flash rewrite function after mounting of the board, design the board so that the 4 pins (V_{DD}, V_{SS}, TEST1_N, TEST0) required for connection to the on-chip debug emulator can be connected.

30.3 Flash Memory Rewrite Function

Flash memory erase/write can be performed with the the memory mounted on board by using the commands from the on-chip debug emulator.
Table 30-1 shows the Flash memory rewrite functions.

Table 30-1 Flash Memory Rewrite Functions

Function	Condition	Outline
Chip erase	ML620Q503H	Erase 16K word（All area）
	ML620Q504H	Erase 32K word（All area）
Block erase	-	Erase 4K word(8K bytes)
1-word write	-	Write 1 word(2 bytes)
Random read	-	Read data from input address

Appendixes

Appendix A Registers

Contents of Registers

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F000	Data segment register	DSR	–	R/W	8	00
0F002	Frequency control register 01	FCON0	FCON01	R/W	8/16	73
0F003		FCON1		R/W	8	03
0F004	Frequency control register 23	FCON2	FCON23	R/W	8/16	02
0F005		FCON3		R/W	8	00
0F008	Stop code acceptor	STPACP	–	W	8	–
0F009	Standby control register	SBYCON	–	W	8	00
0F00A	Frequency status register	FSTAT	–	R	8	06
0F00C	Reset Status register	RSTAT	–	R/W	8	–
0F00E	Watchdog timer control register	WDTCON	–	R/W	8	00
0F00F	Watchdog timer mode register	WDTMOD	–	R/W	8	82
0F010	Interrupt enable register 01	IE0	IE01	R/W	8/16	00
0F011		IE1		R/W	8	00
0F012	Interrupt enable register 23	IE2	IE23	R/W	8/16	00
0F013		IE3		R/W	8	00
0F014	Interrupt enable register 45	IE4	IE45	R/W	8/16	00
0F015		IE5		R/W	8	00
0F016	Interrupt enable register 67	IE6	IE67	R/W	8/16	00
0F017		IE7		R/W	8	00
0F018	Interrupt request register 01	IRQ0	IRQ01	R/W	8/16	00
0F019		IRQ1		R/W	8	00
0F01A	Interrupt request register 23	IRQ2	IRQ23	R/W	8/16	00
0F01B		IRQ3		R/W	8	00
0F01C	Interrupt request register 45	IRQ4	IRQ45	R/W	8/16	00
0F01D		IRQ5		R/W	8	00
0F01E	Interrupt request register 67	IRQ6	IRQ67	R/W	8/16	00
0F01F		IRQ7		R/W	8	00
0F020	Interrupt level control enable register	ILENL	ILEN	R/W	8/16	00
0F021		ILENH		R/W	8	00
0F022	Interrupt Current request level register	CILL	CIL	R/W	8/16	00
0F023		CILH		R/W	8	00
0F024	Interrupt level control register 1	ILC1L	ILC1	R/W	8/16	00
0F025		ILC1H		R/W	8	00
0F026	Interrupt lever control register 2	ILC2L	ILC2	R/W	8/16	00
0F027		ILC2H		R/W	8	00
0F028	Interrupt lever control register 3	ILC3L	ILC3	R/W	8/16	00
0F029		ILC3H		R/W	8	00
0F02A	Interrupt lever control register 4	ILC4L	ILC4	R/W	8/16	00
0F02B		ILC4H		R/W	8	00
0F02C	Interrupt lever control register 5	ILC5L	ILC5	R/W	8/16	00
0F02D		ILC5H		R/W	8	00

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F02E	Interrupt lever control register 6	ILC6L	ILC6	R/W	8/16	00
0F02F		ILC6H		R/W	8	00
0F030	Interrupt lever control register 7	ILC7L	ILC7	R/W	8/16	00
0F031		ILC7H		R/W	8	00
0F040	External interrupt control register 01	EXICON0	EXICON01	R/W	8/16	00
0F041		EXICON1		R/W	8	00
0F042	External interrupt control register 23	EXICON2	EXICON23	R/W	8/16	00
0F043		EXICON3		R/W	8	00
0F048	External interrupt selection register 01	EXI0SEL	EXI01SEL	R/W	8/16	00
0F049		EXI1SEL		R/W	8	00
0F04A	External interrupt selection register 23	EXI2SEL	EXI23SEL	R/W	8/16	00
0F04B		EXI3SEL		R/W	8	00
0F04C	External interrupt selection register 45	EXI4SEL	EXI45SEL	R/W	8/16	00
0F04D		EXI5SEL		R/W	8	00
0F04E	External interrupt selection register 67	EXI6SEL	EXI67SEL	R/W	8/16	00
0F04F		EXI7SEL		R/W	8	00
0F060	Low-speed time base counter register	LTBR	–	R/W	8	00
0F062	Low-speed time base counter frequency adjustment register	LTBADJL	LTBADJ	R/W	8/16	00
0F063		LTBADJH		R/W	8	00
0F064	Low-speed time base counter interrupt select register	LTBINTL	LTBINT	R/W	8/16	30
0F065		LTBINTH		R/W	8	06
0F068	Block control register 01	BLKCON0	BLKCON01	R/W	8/16	00
0F069		BLKCON1		R/W	8	00
0F06A	Block control register 23	BLKCON2	BLKCON23	R/W	8/16	00
0F06B		BLKCON3		R/W	8	00
0F06C	Block control register 45	BLKCON4	BLKCON45	R/W	8/16	00
0F06D		BLKCON5		R/W	8	04
0F0E0	Flash address register	FLASHAL	FLASHA	R/W	8/16	00
0F0E1		FLASHAH		R/W	8	00
0F0E2	Flash data register	FLASHDL	FLASHD	R/W	8/16	00
0F0E3		FLASHDH		R/W	8	00
0F0E4	Flash control register	FLASHCON	–	W	8	00
0F0E6	Flash acceptor	FLASHACP	–	W	8	00
0F0E8	Flash segment register	FLASHSEG	–	R/W	8	00
0F0EA	Flash self register	FLASHSLF	–	R/W	8	00
0F0EC	Remap address register	REMAPADD	–	R/W	8	00
0F208	Port XT data register	PXTD	–	R	8	–
0F209	Port XT direction register	PXTDIR	–	R/W	8	00
0F210	Port 0 data register	P0D	–	R/W	8	00
0F211	Port 0 direction register	P0DIR	–	R/W	8	00
0F212	Port 0 control register	P0CON0	P0CON	R/W	8/16	00
0F213		P0CON1		R/W	8	00
0F214	Port 0 mode register	P0MOD0	P0MOD	R/W	8/16	00
0F215		P0MOD1		R/W	8	00
0F218	Port 1 data register	P1D	–	R/W	8	00

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F219	Port 1 direction register	P1DIR	–	R/W	8	00
0F21A	Port 1 control register	P1CON0	P1CON	R/W	8/16	00
0F21B		P1CON1		R/W	8	00
0F220	Port 2 data register	P2D	–	R/W	8	00
0F221	Port 2 direction register	P2DIR	–	R/W	8	00
0F222	Port 2 control register	P2CON0	P2CON	R/W	8/16	00
0F223		P2CON1		R/W	8	00
0F224	Port 2 mode register	P2MOD0	P2MOD	R/W	8/16	00
0F225		P2MOD1		R/W	8	00
0F228	Port 3 data register	P3D	–	R/W	8	00
0F229	Port 3 direction register	P3DIR	–	R/W	8	00
0F22A	Port 3 control register	P3CON0	P3CON	R/W	8/16	00
0F22B		P3CON1		R/W	8	00
0F22C	Port 3 mode register	P3MOD0	P3MOD	R/W	8/16	00
0F22D		P3MOD1		R/W	8	00
0F230	Port 4 data register	P4D	–	R/W	8	00
0F231	Port 4 direction register	P4DIR	–	R/W	8	00
0F232	Port 4 control register	P4CON0	P4CON	R/W	8/16	00
0F233		P4CON1		R/W	8	00
0F234	Port 4 mode register	P4MOD0	P4MOD	R/W	8/16	00
0F235		P4MOD1		R/W	8	00
0F238	Port 5 data register	P5D	–	R/W	8	00
0F239	Port 5 direction register	P5DIR	–	R/W	8	00
0F23A	Port 5 control register	P5CON0	P5CON	R/W	8/16	00
0F23B		P5CON1		R/W	8	00
0F23C	Port 5 mode register	P5MOD0	P5MOD	R/W	8/16	00
0F23D		P5MOD1		R/W	8	00
0F300	Timer 01 data register	TM0D	TM01D	R/W	8/16	FF
0F301		TM1D		R/W	8	FF
0F302	Timer 23 data register	TM2D	TM23D	R/W	8/16	FF
0F303		TM3D		R/W	8	FF
0F304	Timer 45 data register	TM4D	TM45D	R/W	8/16	FF
0F305		TM5D		R/W	8	FF
0F306	Timer 67 data register	TM6D	TM67D	R/W	8/16	FF
0F307		TM7D		R/W	8	FF
0F310	Timer 01 counter register	TM0C	TM01C	R/W	8/16	00
0F311		TM1C		R/W	8	00
0F312	Timer 23 counter register	TM2C	TM23C	R/W	8/16	00
0F313		TM3C		R/W	8	00
0F314	Timer 45 counter register	TM4C	TM45C	R/W	8/16	00
0F315		TM5C		R/W	8	00
0F316	Timer 67 counter register	TM6C	TM67C	R/W	8/16	00
0F317		TM7C		R/W	8	00
0F320	Timer 01 control register	TM0CON	TM01CON	R/W	8/16	00
0F321		TM1CON		R/W	8	00

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F322	Timer 23 control register	TM2CON	TM23CON	R/W	8/16	00
0F323		TM3CON		R/W	8	00
0F324	Timer 45 control register	TM4CON	TM45CON	R/W	8/16	00
0F325		TM5CON		R/W	8	00
0F326	Timer 67 control register	TM6CON	TM67CON	R/W	8/16	00
0F327		TM7CON		R/W	8	00
0F330	Timer start register 0	TMSTR0	–	W	8	00
0F332	Timer stop register 0	TMSTP0	–	W	8	00
0F334	Timer status register 0	TMSTAT0	–	R	8	00
0F400	FTM0 period register	–	FT0P	R/W	16	FFFF
0F402	FTM0 event A register	–	FT0EA	R/W	16	0000
0F404	FTM0 event B register	–	FT0EB	R/W	16	0000
0F406	FTM0 dead time register	–	FT0DT	R/W	16	0000
0F408	FTM0 counter register	–	FT0C	R/W	16	0000
0F40A	FTM0 control register 0	FT0CON0	–	R/W	8	00
0F40B	FTM0 control register 1	FT0CON1		R/W	8	00
0F40C	FTM0 mode register	FT0MODL	FT0MOD	R/W	8/16	00
0F40D		FT0MODH		R/W	8	00
0F40E	FTM0 clock register	FT0CLKL	FT0CLK	R/W	8/16	00
0F40F		FT0CLKH		R/W	8	00
0F410	FTM0 trigger register 0	FT0TRG0L	FT0TRG0	R/W	8/16	00
0F411		FT0TRG0H		R/W	8	00
0F412	FTM0 trigger register 1	FT0TRG1L	FT0TRG1	R/W	8/16	00
0F413		FT0TRG1H		R/W	8	00
0F418	FTM0 interrupt enable register	FT0INTEL	FT0INTE	R/W	8/16	00
0F419		FT0INTEH		R/W	8	00
0F41A	FTM0 interrupt status register	FT0INTSL	FT0INTS	R	8/16	00
0F41B		FT0INTSH		R	8	00
0F41C	FTM0 interrupt clear register	FT0INTCL	FT0INTC	W	8/16	00
0F41D		FT0INTCH		W	8	00
0F420	FTM1 period register	–	FT1P	R/W	16	FFFF
0F422	FTM1 event A register	–	FT1EA	R/W	16	0000
0F424	FTM1 event B register	–	FT1EB	R/W	16	0000
0F426	FTM1 dead time register	–	FT1DT	R/W	16	0000
0F428	FTM1 counter register	–	FT1C	R/W	16	0000
0F42A	FTM1 control register 0	FT1CON0	–	R/W	8	00
0F42B	FTM1 control register 1	FT1CON1		R/W	8	00
0F42C	FTM1 mode register	FT1MODL	FT1MOD	R/W	8/16	00
0F42D		FT1MODH		R/W	8	00
0F42E	FTM1 clock register	FT1CLKL	FT1CLK	R/W	8/16	00
0F42F		FT1CLKH		R/W	8	00
0F430	FTM1 trigger register 0	FT1TRG0L	FT1TRG0	R/W	8/16	00
0F431		FT1TRG0H		R/W	8	00
0F432	FTM1 trigger register 1	FT1TRG1L	FT1TRG1	R/W	8/16	00
0F433		FT1TRG1H		R/W	8	00

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F438	FTM1 interrupt enable register	FT1INTEL	FT1INTE	R/W	8/16	00
0F439		FT1INTEH		R/W	8	00
0F43A	FTM1 interrupt status register	FT1INTSL	FT1INTS	R	8/16	00
0F43B		FT1INTSH		R	8	00
0F43C	FTM1 interrupt clear register	FT1INTCL	FT1INTC	W	8/16	00
0F43D		FT1INTCH		W	8	00
0F440	FTM2 period register	–	FT2P	R/W	16	FFFF
0F442	FTM2 event A register	–	FT2EA	R/W	16	0000
0F444	FTM2 event B register	–	FT2EB	R/W	16	0000
0F446	FTM2 dead time register	–	FT2DT	R/W	16	0000
0F448	FTM2 counter register	–	FT2C	R/W	16	0000
0F44A	FTM2 control register 0	FT2CON0	–	R/W	8	00
0F44B	FTM2 control register 1	FT2CON1		R/W	8	00
0F44C	FTM2 mode register	FT2MODL	FT2MOD	R/W	8/16	00
0F44D		FT2MODH		R/W	8	00
0F44E	FTM2 clock register	FT2CLKL	FT2CLK	R/W	8/16	00
0F44F		FT2CLKH		R/W	8	00
0F450	FTM2 trigger register 0	FT2TRG0L	FT2TRG0	R/W	8/16	00
0F451		FT2TRG0H		R/W	8	00
0F452	FTM2 trigger register 1	FT2TRG1L	FT2TRG1	R/W	8/16	00
0F453		FT2TRG1H		R/W	8	00
0F458	FTM2 interrupt enable register	FT2INTEL	FT2INTE	R/W	8/16	00
0F459		FT2INTEH		R/W	8	00
0F45A	FTM2 interrupt status register	FT2INTSL	FT2INTS	R	8/16	00
0F45B		FT2INTSH		R	8	00
0F45C	FTM2 interrupt clear register	FT2INTCL	FT2INTC	W	8/16	00
0F45D		FT2INTCH		W	8	00
0F460	FTM3 period register	–	FT3P	R/W	16	FFFF
0F462	FTM3 event A register	–	FT3EA	R/W	16	0000
0F464	FTM3 event B register	–	FT3EB	R/W	16	0000
0F466	FTM3 dead time register	–	FT3DT	R/W	16	0000
0F468	FTM3 counter register	–	FT3C	R/W	16	0000
0F46A	FTM3 control register 0	FT3CON0	–	R/W	8	00
0F46B	FTM3 control register 1	FT3CON1		R/W	8	00
0F46C	FTM3 mode register	FT3MODL	FT3MOD	R/W	8/16	00
0F46D		FT3MODH		R/W	8	00
0F46E	FTM3 clock register	FT3CLKL	FT3CLK	R/W	8/16	00
0F46F		FT3CLKH		R/W	8	00
0F470	FTM3 trigger register 0	FT3TRG0L	FT3TRG0	R/W	8/16	00
0F471		FT3TRG0H		R/W	8	00
0F472	FTM3 trigger register 1	FT3TRG1L	FT3TRG1	R/W	8/16	00
0F473		FT3TRG1H		R/W	8	00
0F478	FTM3 interrupt enable register	FT3INTEL	FT3INTE	R/W	8/16	00
0F479		FT3INTEH		R/W	8	00

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F47A	FTM3 interrupt status register	FT3INTSL	FT3INTS	R	8/16	00
0F47B		FT3INTSH		R	8	00
0F47C	FTM3 interrupt clear register	FT3INTCL	FT3INTC	W	8/16	00
0F47D		FT3INTCH		W	8	00
0F480	FTM output 01 select register	FTO0SL	FTO01SL	R/W	8/16	00
0F481		FTO1SL		R/W	8	00
0F482	FTM output 23 select register	FTO2SL	FTO23SL	R/W	8/16	00
0F483		FTO3SL		R/W	8	00
0F484	FTM output 45 select register	FTO4SL	FTO45SL	R/W	8/16	00
0F485		FTO5SL		R/W	8	00
0F486	FTM output 67 select register	FTO6SL	FTO67SL	R/W	8/16	00
0F487		FTO7SL		R/W	8	00
0F488	FTM output 89 select register	FTO8SL	FTO89SL	R/W	8/16	00
0F489		FTO9SL		R/W	8	00
0F48A	FTM output AB select register	FTOASL	FTOABSL	R/W	8/16	00
0F48B		FTOBSL		R/W	8	00
0F48C	FTM output CD select register	FTOCSL	FTOCDSL	R/W	8/16	00
0F48D		FTODSL		R/W	8	00
0F48E	FTM output EF select register	FTOESL	FTOEFSL	R/W	8/16	00
0F48F		FTOFSL		R/W	8	00
0F700	Serial port 0 transmit/receive buffer	SIO0BUFL	SIO0BUF	R/W	8/16	00
0F701		SIO0BUFH		R/W	8	00
0F702	Serial port 0 control register	SIO0CON	–	R/W	8	00
0F704	Serial port 0 mode register	SIO0MOD0	SIO0MOD	R/W	8/16	00
0F705		SIO0MOD1		R/W	8	00
0F710	UART0 receive buffer	UA0BUF	–	R/W	8	00
0F711	UART0 control register	UA0CON	–	R/W	8	00
0F712	UART0 mode register	UA0MOD0	UA0MOD	R/W	8/16	00
0F713		UA0MOD1		R/W	8	00
0F714	UART0 baud rate register	UA0BRTL	UA0BRT	R/W	8/16	FF
0F715		UA0BRTH		R/W	8	0F
0F716	UART0 receive status register	UA0STAT	–	R/W	8	00
0F718	UART0 transmit buffer	UA1BUF	–	R/W	8	00
0F719	UART0 transmit monitor register	UA1CON	–	R/W	8	00
0F71E	UART0 transmit status register	UA1STAT	–	R/W	8	00
0F740	I^2C bus 0 receive data register	I2C0RD	–	R	8	00
0F742	I^2C bus 0 slave address register	I2C0SA	–	R/W	8	00
0F744	I^2C bus 0 transmit data register	I2C0TD	–	R/W	8	00
0F746	I^2C bus 0 control register	I2C0CON0	I2C0CON	R/W	8/16	00
0F747		I2C0CON1		R/W	8	00
0F748	I^2C bus 0 mode register	I2C0MODL	I2C0MOD	R/W	8/16	00
0F749		I2C0MODH		R/W	8	02
0F74A	I^2C bus 0 status register	I2C0STAL	I2C0STA	R	8/16	00
0F74B		I2C0STAH		R	8	00
0F750	I^2C bus 1 receive data register	I2C1RD	–	R	8	00
0F752	I^2C bus 1 slave address register	I2C1SA	–	R/W	8	00

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F754	I^2C bus 1 transmit data register	I2C1TD	–	R/W	8	00
0F756	I^2C bus 1 control register	I2C1CON0	I2C1CON	R/W	8/16	00
0F757		I2C1CON1		R/W	8	00
0F758	I^2C bus 1 mode register	I2C1MODL	I2C1MOD	R/W	8/16	00
0F759		I2C1MODH		R/W	8	02
0F75A	I^2C bus 1 status register	I2C1STAL	I2C1STA	R	8/16	00
0F75B		I2C1STAH		R	8	00
0F780	SIOF0 control register	SF0CTRLL	SF0CTRL	R/W	8/16	00
0F781		SF0CTRLH		R/W	8	00
0F782	SIOF0 interrupt control register	SF0INTCL	SF0INTC	R/W	8/16	00
0F783		SF0INTCH		R/W	8	00
0F784	SIOF0 transfer interval control register	–	SF0TRAC	R/W	16	0002
0F786	SIOF0 baud rate register	–	SF0BRR	R/W	16	5002
0F788	SIOF0 status register	SF0SRRL	SF0SRR	R	8/16	00
0F789		SF0SRRH		R	8	14
0F78A	SIOF0 status clear register	SF0SRCL	SF0SRC	W	8/16	00
0F78B		SF0SRCH		W	8	00
0F78C	SIOF0 FIF0 status register	SF0FSRL	SF0FSR	R	8/16	00
0F78D		SF0FSRH		R	8	00
0F78E	SIOF0 write data register	SF0DWRL	SF0DWR	R/W	8/16	00
0F78F		SF0DWRH		R/W	8	00
0F790	SIOF0 read data register	SF0DRRL	SF0DRR	R	8/16	00
0F791		SF0DRRH		R	8	00
0F7C0	UARTF0 transmit/receive buffer	UAF0BUFL	UAF0BUF	R/W	8/16	xx
0F7C1		UAF0BUFH		R/W	8	00
0F7C2	UARTF0 interrupt enable register	UAF0IERL	UAF0IER	R/W	8/16	00
0F7C3		UAF0IERH		R/W	8	00
0F7C4	UARTF0 interrupt status register	UAF0IIRL	UAF0IIR	R	8/16	01
0F7C5		UAF0IIRH		R	8	00
0F7C6	UARTF0 mode register	UAF0MODL	UAF0MOD	R/W	8/16	00
0F7C7		UAF0MODH		R/W	8	00
0F7C8	UARTF0 line status register	UAF0LSRL	UAF0LSR	R	8/16	60
0F7C9		UAF0LSRH		R	8	00
0F7CA	UARTF0 clock adjustment register	UAF0CAJL	UAF0CAJ	R/W	8/16	0D
0F7CB		UAF0CAJH		R/W	8	00
0F7CC	UARTF0 interrupt request register	UAF0IRQL	UAF0IRQ	W	8/16	00
0F7CD		UAF0IRQH		W	8	00
0F800	RC-ADC counter A register 0	RADCA0L	RADCA0	R/W	8/16	00
0F801		RADCA0H		R/W	8	00
0F802	RC-ADC counter A register 1	RADCA1L	RADCA1	R/W	8/16	00
0F803		RADCA1H		R/W	8	00
0F804	RC-ADC counter B register 0	RADCB0L	RADCB0	R/W	8/16	00
0F805		RADCB0H		R/W	8	00
0F806	RC-ADC counter B register 1	RADCB1L	RADCB1	R/W	8/16	00
0F807		RADCB1H		R/W	8	00

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F808	RC-ADC mode register	RADMODL	RADMOD	R/W	8/16	00
0F809		RADMODH		R/W	8	00
0F80A	RC-ADC control register	RADCONL	RADCON	R/W	8/16	00
0F80B		RADCONH		R/W	8	00
0F820	SA-ADC result register 0	SADR0L	SADR0	R	8/16	00
0F821		SADR0H		R	8	00
0F822	SA-ADC result register 1	SADR1L	SADR1	R	8/16	00
0F823		SADR1H		R	8	00
0F824	SA-ADC result register 2	SADR2L	SADR2	R	8/16	00
0F825		SADR2H		R	8	00
0F826	SA-ADC result register 3	SADR3L	SADR3	R	8/16	00
0F827		SADR3H		R	8	00
0F828	SA-ADC result register 4	SADR4L	SADR4	R	8/16	00
0F829		SADR4H		R	8	00
0F82A	SA-ADC result register 5	SADR5L	SADR5	R	8/16	00
0F82B		SADR5H		R	8	00
0F82C	SA-ADC result register 6	SADR6L	SADR6	R	8/16	00
0F82D		SADR6H		R	8	00
0F82E	SA-ADC result register 7	SADR7L	SADR7	R	8/16	00
0F82F		SADR7H		R	8	00
0F830	SA-ADC result register 8	SADR8L	SADR8	R	8/16	00
0F831		SADR8H		R	8	00
0F832	SA-ADC result register 9	SADR9L	SADR9	R	8/16	00
0F833		SADR9H		R	8	00
0F834	SA-ADC result register A	SADRAL	SADRA	R	8/16	00
0F835		SADRAH		R	8	00
0F836	SA-ADC result register B	SADRBL	SADRB	R	8/16	00
0F837		SADRBH		R	8	00
0F840	SA-ADC control register 0	SADCON0	–	R/W	8	22
0F841	SA-ADC control register 1	SADCON1		R/W	8	00
0F842	SA-ADC enable register	SADENL	SADEN	R/W	8/16	00
0F843		SADENH		R/W	8	00
0F844	SA-ADC touch sensor register	SADTCHL	SADTCH	R/W	8/16	00
0F845		SADTCHH		R/W	8	00
0F846	SA-ADC trigger register	SADTRGL	SADTRG	R/W	8/16	00
0F847		SADTRGH		R/W	8	00
0F848	SA-ADC accuracy control register	SADCVTL	SADCVT	R/W	8/16	FF
0F849		SADCVTH		R/W	8	FF
0F8C0	Melody 0 control register	MD0CON	–	R/W	8	00
0F8C1	Melody 0 tempo code register	MD0TMP	–	R/W	8	00
0F8C2	Melody 0 scale/tone length code register	MD0TON	MD0TL	R/W	8/16	00
0F8C3		MD0LEN		R/W	8	00
0F900	Voltage level supervisor control register	VLSCONL	VLSCON	R/W	8/16	00
0F901		VLSCONH		R/W	8	00
0F902	Voltage level supervisor mode register	VLSMODL	VLSMOD	R/W	8/16	00
0F903		VLSMODH		R/W	8	00

Address [H]	Name	Symbol (Byte)	Symbol (Word)	R/W	Size	Initial value [H]
0F920	Comparator 0 control register	CMP0CON	–	R/W	8	00
0F922	Comparator 0 mode register	CMP0MODL	CMP0MOD	R/W	8/16	00
0F923		CMP0MODH		R/W	8	00
0F928	Comparator 1 control register	CMP1CON	–	R/W	8	00
0F92A	Comparator 1 mode register	CMP1MODL	CMP1MOD	R/W	8/16	00
0F92B		CMP1MODH		R/W	8	00

Appendix B Package Dimensions

● ML620Q503H/Q504H

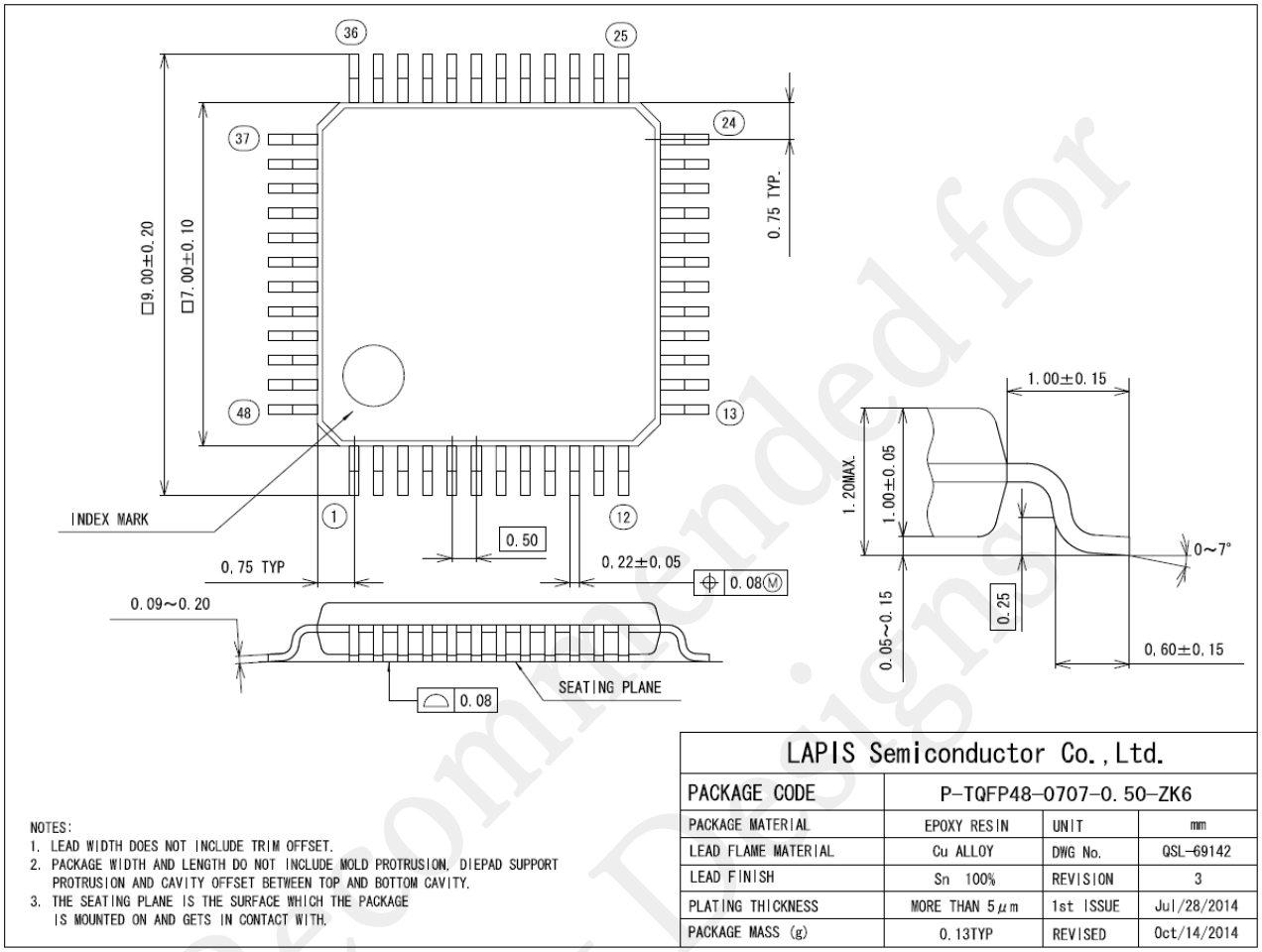


Figure B-1 TQFP48

Notes for Mounting the Surface Mount Type Package

The surface mount type packages are very susceptible to heat in reflow and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact a ROHM sales office for the product name, package name, pin number, package code and desired mounting conditions(reflow method, temperature and times).

Appendix C Electrical Characteristics

●Absolute Maximum Rating

(V_{SS}=0V)

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage 1	V_{DD}	Ta=25°C	-0.3 to +6.0	V
Power supply voltage 2	V_{DDL}	Ta=25°C	-0.3 to +2.0	V
Power supply voltage 3	V_{DDX}	Ta=25°C	-0.3 to +2.0	V
Input voltage	V_{IN}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Output voltage	V_{OUT}	Ta=25°C	-0.3 to V_{DD}+0.3	V
Output current 1	I_{OUT1}	Port 0~2 Ta=25°C	-12 to +11	mA
Output current 2	I_{OUT2}	Port 3~5 Ta=25°C	-12 to +20	mA
Power dissipation	PD	Ta=25°C	0.9	W
Storage temperature	T_{STG}	–	-55 to +150	°C

●Recommended Operating Conditions

(V_{SS}=0V)

Parameter	Symbol	Condition	Range	Unit
Operating temperature (Ambience)	T_{OP}	–	-40 to +85	°C
Operating voltage	V_{DD}	–	1.8 to 5.5	V
Reference voltage	V_{REF}	–	1.8 to V_{DD}	V
Operating frequency (CPU)	f_{OP}	–	30k to 16.8 M	Hz
Low-speed external clock input	f_{EXTL}	–	30k to 36k	Hz
High-speed external clock input	f_{EXTH}	–	2M to 16M	Hz
Low speed crystal oscillation frequency	f_{XTL}	–	32.768k	Hz
Low speed crystal oscillation external capacitor 1	C_{DL}	Using VT-200-FL(from SII)	6.8 to 12	pF
	C_{GL}		6.8 to 12	
Low speed crystal oscillation external capacitor 2	C_{DL}	Using DT-26(from Daishinku)	12 to 16	pF
	C_{GL}		12 to 16	
Low speed crystal *1 oscillation external capacitor 3	C_{DL}	Using VT-200-F(from SII)	12 to 22	pF
	C_{GL}		12 to 22	
High speed crystal/ Ceramic oscillation frequency	f_{XTH}	–	16M	Hz
High speed crystal oscillation external capacitor	C_{DH}	Using NX8045GB (from Nihon Denpa Kogyo)	12 to 20	pF
	C_{GH}		12 to 20	
Ceramic oscillation External capacitor	C_{DH}	Using FCSTCE16M0V53 (from Murata manufacturing) Build in CL type	0 to 5	pF
	C_{GH}		0 to 5	
V_{DDL} external capacitor *2	C_L	ESR ≦500mΩ	2.2 ± 30%	μF
V_{DDX} external capacitor	C_X	–	0.33 ± 30%	μF

*1 : Please use this crystal except DEEPHALT mode because this LSI may not be functioning at DEEPHALT mode with the crystal. Please evaluate the matching when other crystal oscillator/ceramic oscillator is used.

*2 : Please evaluate on user's conditions, put on C_{L0}(= 0.1uF) if necessary.

See the application note; "Precautions for MCU board design" for details, when designing MCU board.

●Operating Conditions of Flash Memory

(V_{SS}= 0V)

Parameter	Symbol	Condition		Range	Unit
Operating temperature (Ambience)	T_{OP}	Data area : write/erase		-40 to +85	°C
		Program area : write/erase		0 to +40	°C
Operating voltage Write time	V_{DD}	Write/erase		1.8 to 5.5	V
	C_{EPD}	Data area (1,024B x 2)		10,000	times
	C_{EPP}	Program area		100	times
Erase unit	–	Block erase	Program area	8	KB
			Data area	2	
		Sector erase		1	KB
Erase time(Maximum)	–	Block erase/Sector erase		100	ms
Write unit	–	–		1 word (2 byte)	–

●AC characteristics (Oscillation)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Low speed crystal oscillation start time	T_{XTL}	–	–	–	2	s	1
High speed crystal oscillation start time	T_{XTH}	–	–	–	20	ms	
Low speed built-in RC oscillation frequency*1*2	f_{LCR}	Ta=25°C	typ -1.5%	32.768	typ +1.5%	kHz	
		Ta=-40 to 85°C	typ -5%	32.768	typ +5%		
High speed build-in RC oscillation frequency*1*2	f_{HCR}	Ta=25°C	typ -1%	16	typ +1%	MHz	
		Ta=-40 to 85°C	typ -5%	16	typ +5%		

*1 : Mean value of 1024 cycle.
*2 : Guarantee value at the time of the shipment.

●DC Characteristics (IDD)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition		Rating Min.	Rating Typ. (3.0V)	Rating Max. (3.6V)	Rating Max. (5.5V)	Unit	Measuring circuit
Power consumption 1	IDD1	CPU is Stopped Low/High-speed oscillation is stopped	Ta=25°C	–	0.25	0.8	1.3	µA	1
			Ta=-40 to 85°C	–	–	15	18		
Power consumption 2	IDD2	DEEP-HALT mode *2*4 (LBTC function) Low-speed crystal oscillating (32.768kHz) High-speed oscillation is stopped.	Ta=25°C	–	0.45	1.3	1.6	µA	
			Ta=-40 to 85°C	–	–	15	18		
Power consumption 3	IDD3	HALT mode *2*4 (LTBC function) Low-speed crystal oscillating (32.768kHz) High speed oscillation is stopped.	Ta=25°C	–	2	2.7	3.0	µA	
			Ta=-40 to 85°C	–	–	18	19		
Power consumption 4	IDD4	CPU Low-speed *1*4 Low-speed built-in CR oscillating High speed oscillation is stopped.	Ta=25°C	–	10	12	13	µA	
			Ta=-40 to 85°C	–	–	25	28		
Power consumption 5	IDD5	CPU High-speed(16MHz) *1*4 High-speed Built-in CR oscillating	Ta=25°C	–	4	5.5	5.5	mA	
			Ta=-40 to 85°C	–	–	6	6		
Power consumption 6	IDD6	CPU High-speed(16MHz) *1*3*4 High speed crystal oscillating (16MHz)	Ta=25°C	–	6	7.5	9.4	mA	
			Ta=-40 to 85°C	–	–	8	9.9		

*1 : at CPU activity rate =100%（No HALT state）
*2 : using 32.768KHz crystal oscillator VT-200-FL (from SII)(C_{GL}/C_{DL}＝12pF)
using 32.768KHz crystal oscillator DT-26(from Daishinku)(C_{GL}/C_{DL}＝12pF）
*3 : using NX8045GB(from Nihon denpa kogyo) (C_{GH}/C_{DH}＝16pF)
*4 : BLKCON0~BLKCON5 valid bits are all "1".

●DC Characteristics (VLS)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating*1			Unit	Measuring circuit
			Min.	Typ.	Max.		
VLS judge voltage (V_{DD}=fall)	V_{VLS}	vlscon = 3H	1.798	1.898	1.998	V	1
		vlscon = 4H	1.900	2.000	2.100		
		vlscon = 5H	1.993	2.093	2.193		
		vlscon = 6H	2.096	2.196	2.296		
		vlscon = 7H	2.209	2.309	2.409		
		vlscon = 8H	2.309	2.409	2.509		
		vlscon = 9H	2.505	2.605	2.705		
		vlscon = AH	2.700	2.800	2.900		
		vlscon = BH	2.968	3.068	3.168		
		vlscon = CH	3.294	3.394	3.494		
		vlscon = DH	3.697	3.797	3.897		
		vlscon = EH	4.126	4.226	4.326		
		vlscon = FH	4.567	4.667	4.767		
V_{VLS} Hysteresis width (V_{DD}=rise)	H_{VLS}	–	V_{VLS} x 1.8%	V_{VLS} x 3.8%	V_{VLS} x 6.3%	V	

●DC characteristics (LLD)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
LLD judge Voltage	VLLR	–	1.60	1.80	2.00	V	1

●DC/AC characteristics (Analog comparator)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Common Input voltage range	V_{CMPIN}	–	0.2	–	V_{DD} -0.2	V	1
Input offset voltage	V_{CMPOF}	–	-30	–	30	mV	
Comparator judge time	T_{CMP}	CMPP- CMPM =40mV	–	–	2	µs	

●DC characteristics (VOHL, IOHL)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Output voltage 1 (P00-P05, P10-P11 P20-P23, P30-P37 P40-P47, P50-P57)	VOH1	3.6V < V_{DD} ≤ 5.5V IOH=-2.5mA	V_{DD} -0.6	–	–	V	2
		1.8V ≤ V_{DD} ≤ 3.6V IOH=-1.0mA	V_{DD} -0.5	–	–		
	VOL1	3.6V < V_{DD} ≤ 5.5V IOL=+5.0mA	–	–	0.6		
		1.8V ≤ V_{DD} ≤ 3.6V IOL=+0.5mA	–	–	0.4		
Output voltage 2 (P40,P41, P52, P53) (LED mode is selected)	VOL2	3.6V < V_{DD} ≤ 5.5V IOL=+5.0mA	–	–	0.4		
		2.7V ≤ V_{DD} ≤ 3.6V IOL=+5.0mA	–	–	0.6		
		1.8V ≤ V_{DD} < 2.7V IOL=+2.0mA	–	–	0.4		
Output voltage 3 (P30,P31, P34, P35, P40, P41, P44, P45, P50, P51, P54, P55) (I^2C mode is selected)	VOL3	IOL3= +3mA (I^2Cspec) (V_{DD} ≥ 2V)	–	–	0.4		
Output voltage 4 (P30, P31, P34, P35, P40, P41, P44, P45, P50, P51, P54, P55) (I^2C mode is selected)	VOL4	IOL3= +2mA(I^2Cspec) (V_{DD} < 2V)	–	–	V_{DD} ×0.2		
Output leak 1 (P00-P05,P20-P23, P30-P37, P40-P47, P50-P57)	IOOH1	VOH=V_{DD} (at high impedance)	–	–	+1	μA	3
	IOOL1	VOL=V_{SS} (at high impedance)	-1	–	–		
Output leak 2 (P10-P11)	IOOH2	VOH=V_{DD} (at high impedance)	–	–	+2		
	IOOL2	VOL=V_{SS} (at high impedance)	-2	–	–		

●DC characteristics (IIHL)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input current 1 (RESET_N, TEST1_N)	IIH1	VIH1=V_{DD}	–	–	1	μA	4
	IIL1	VIL1=V_{SS}	-900	-300	-20		
Input current 2 (TEST0)	IIH2	VIH2=V_{DD}	20	300	900		
	IIL2	VIL2=V_{SS}	-1	–	–		
Input current 3 (PXT0-PXT1, P00-P05, P20-P23, P30-P37, P40-P47, P50-P57)	IIH3	VIH3=V_{DD} (at pull down)	1	15	200		
	IIL3	VIL3=V_{SS} (at pull up)	-200	-15	-1		
	IIH3Z	VIH3=V_{DD} (at high impedance)	–	–	1		
	IIL3Z	VIL3=V_{SS} (at high impedance)	-1	–	–		
Input current 4 (P10-P11)	IIH4	VIH4=V_{DD} (at pull down)	1	15	200		
	IIL4	VIL4=V_{SS} (at pull up)	-200	-15	-1		
	IIH4Z	VIH4=V_{DD} (at high impedance)	–	–	2		
	IIL4Z	VIL4=V_{SS} (at high impedance)	-2	–	–		

*1 : typ.rating is Ta=25°C, V_{DD}=3.0V

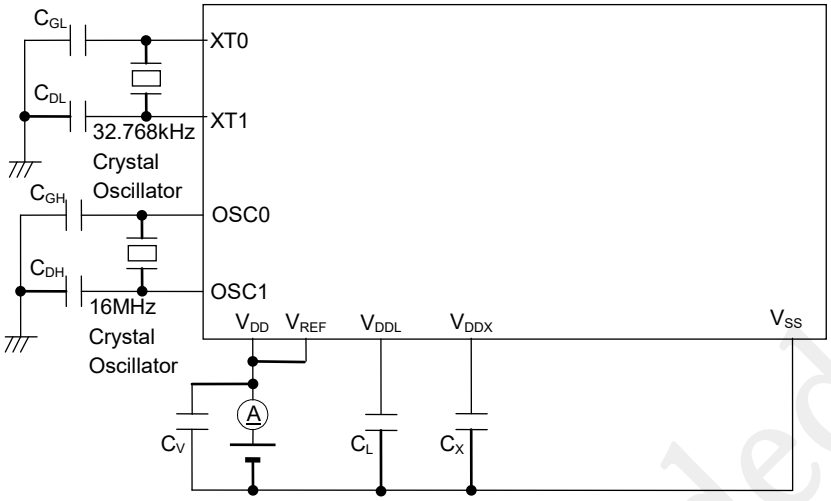
●DC characteristics (VIHL)

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Input voltage 1 (RESET_N, TEST0, TEST1_N, PXT0-PXT1, P00-P05, P10-P11, P20-P23, P30-P37, P40-P47, P50-P57)	VIH1	–	0.7 ×V_{DD}	–	V_{DD}	V	5
	VIL1	–	0	–	0.3 ×V_{DD}		
Input terminal capacitance (RESET_N, TEST0, TEST1_N, PXT0-PXT1, P00-P05, P10-P11, P20-P23, P30-P37, P40-P47, P50-P57)	CIN	f=10kHz V_{rms}=50mV Ta=25°C	–	–	10	pF	–

●Measuring circuit

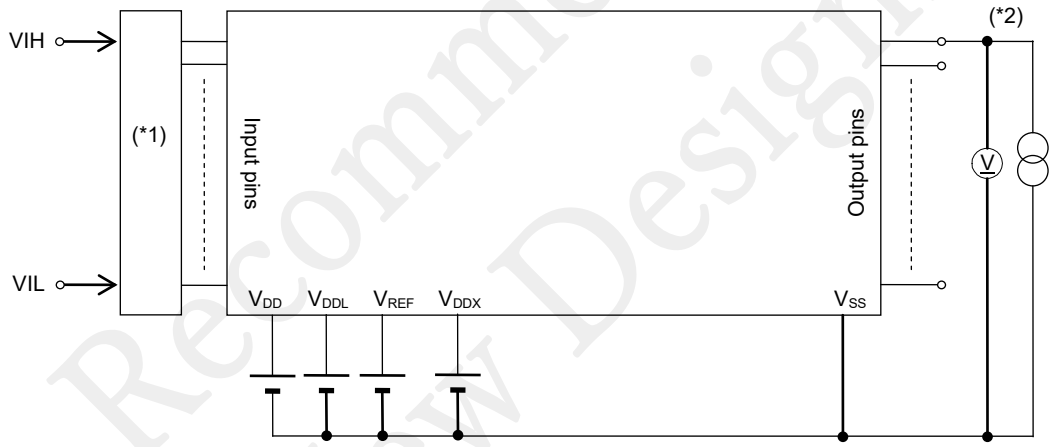
Measuring circuit 1



32.768kHz crystal oscillator : DT-26 (from Daishinku)
16MHz crystal oscillator : NX8045GB (from Nihon denpa kogyo)

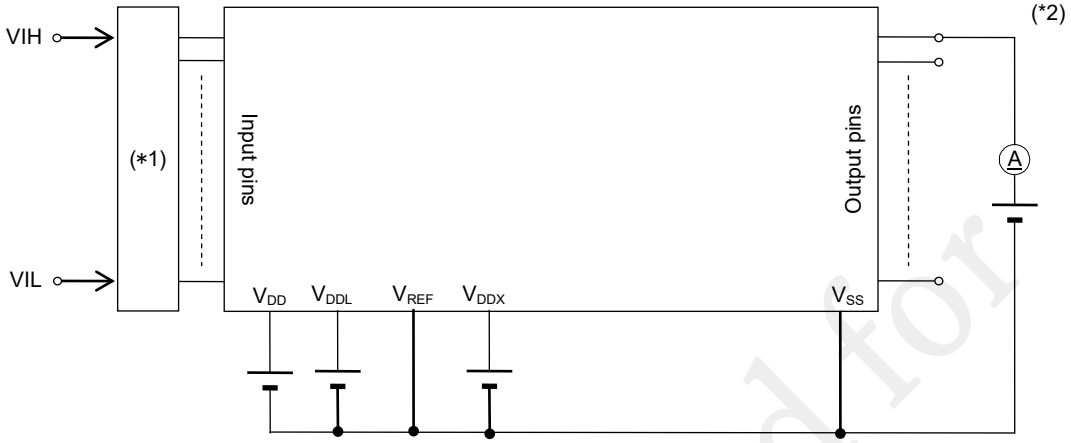
C_V	:	1.0μF
C_L	:	2.2μF
C_X	:	0.33μF
C_{GL}	:	12pF
C_{DL}	:	12pF
C_{GH}	:	16pF
C_{DH}	:	16pF

Measuring circuit 2



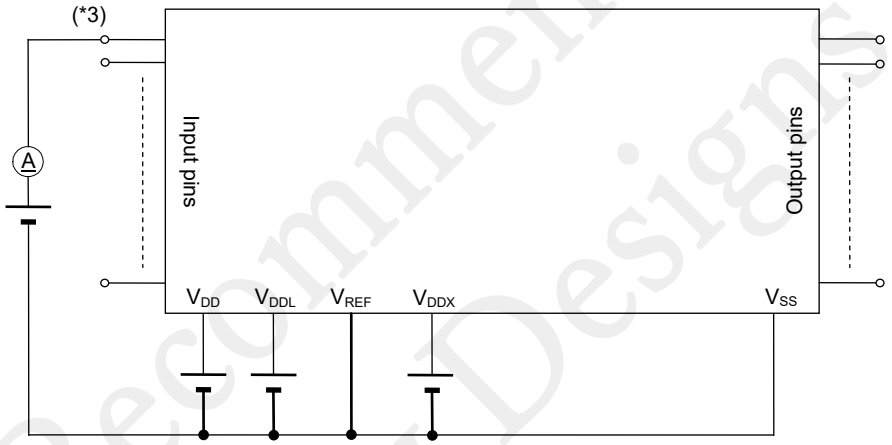
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring circuit 3



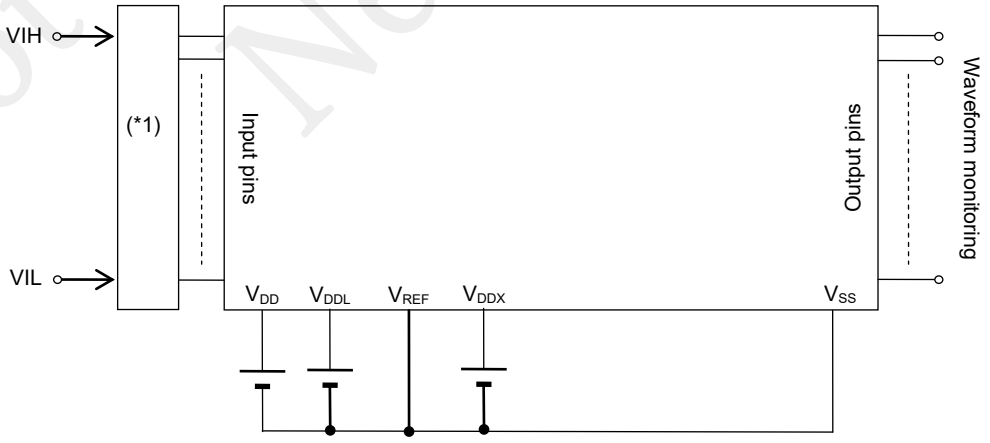
(*1) Input logic circuit to determine the specified measuring conditions.
(*2) Measured at the specified output pins.

Measuring circuit 4



(*3) Measured at the specified output pins.

Measuring circuit 5

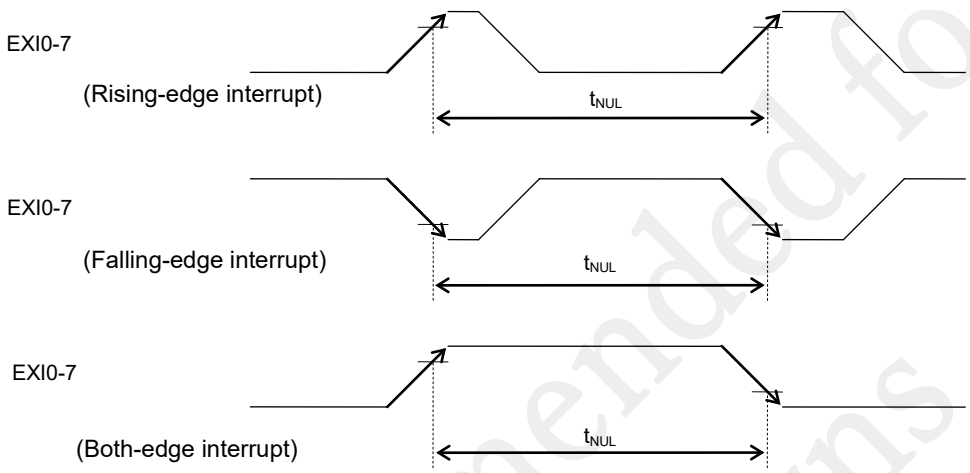


(*1) Input logic circuit to determine the specified measuring conditions.

●AC characteristics（external interrupt）

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
External interrupt disable period	t_{NUL}	Interrupt enable (MIE=1) CPU : NOP operation	2.5 x sysclk	–	3.5 x sysclk	φ



●AC characteristics (synchronous serial port)

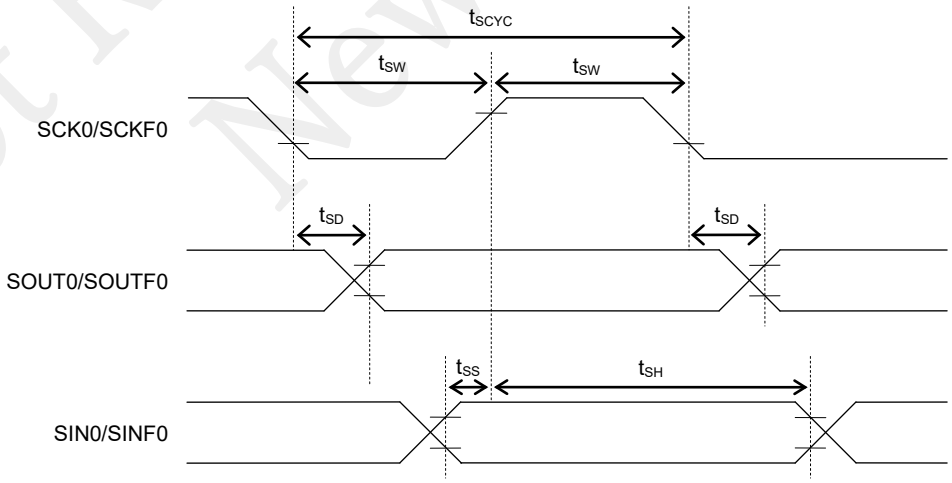
(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCK input cycle (slave mode)	t_{SCYC}	High-speed oscillation is not active	10	–	–	µs
		High-speed oscillation is active	500	–	–	ns
SCK output cycle (master mode)	t_{SCYC}	–	–	SCK*1	–	s
SCK input pulse width (slave mode)	t_{SW}	High-speed oscillation is not active	4	–	–	µs
		High-speed oscillation is active	200	–	–	ns
SCK output pulse width (master mode)	t_{SW}	–	t_{SCYC} ×0.4	t_{SCYC} ×0.5	t_{SCYC} ×0.6	s
SOUT output delay time (slave mode)	t_{SD}	–	–	–	180	ns
SOUT output delay time (master mode)	t_{SD}	–	–	–	80	ns
SIN input Setup time (slave mode)	t_{SS}	–	50	–	–	ns
SIN input Hold time	t_{SH}	–	50	–	–	ns

*1 : The clock period which is selected by the below registers(min:250ns@ regularly, min:500ns@P02, P22 is used)

In case of SSIO : S0CK2-0 of serial port 0 mode register(SIO0MOD).

In case of SSIOF : SF0BR9-0 of SIOF0 port register(SF0BRR)



●AC characteristics（I^2C Bus interface : Standard mode 100kHz）

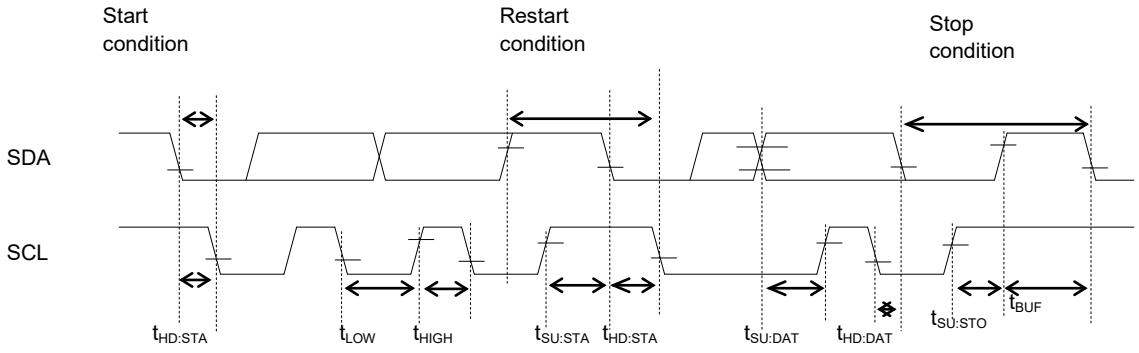
(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	–	0	–	100	kHz
SCL hold time (Start/restart condition)	$t_{HD:STA}$	–	4.0	–	–	µs
SCL"L" level time	t_{LOW}	–	4.7	–	–	µs
SCL"H" level time	t_{HIGH}	–	4.0	–	–	µs
SCL setup time (restart condition)	$t_{SU:STA}$	–	4.7	–	–	µs
SDA hold time	$t_{HD:DAT}$	–	0	–	3.45	µs
SDA setup time	$t_{SU:DAT}$	–	0.25	–	–	µs
SCL setup time (stop condition)	$t_{SU:STO}$	–	4.0	–	–	µs
Bus-free time	t_{BUF}	–	4.7	–	–	µs

●AC characteristics（I^2C bus interface : fast mode 400kHz）

(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rateing			Unit
			Min.	Typ.	Max.	
SCL clock frequency	f_{SCL}	–	0	–	400	kHz
SCL hold time (start/restart condition)	$t_{HD:STA}$	–	0.6	–	–	µs
SCL"L" level time	t_{LOW}	–	1.3	–	–	µs
SCL"H" level time	t_{HIGH}	–	0.6	–	–	µs
SCL setup time (restart condition)	$t_{SU:STA}$	–	0.6	–	–	µs
SDA hold time	$t_{HD:DAT}$	–	0	–	0.9	µs
SDA setup time	$t_{SU:DAT}$	–	0.1	–	–	µs
SCL setup time (stop condition)	$t_{SU:STO}$	–	0.6	–	–	µs
Bus-free time	t_{BUF}	–	1.3	–	–	µs



●AC characteristics (RC-ADC)

(V_{DD}=1.8~5.5V, V_{SS}=0V, Ta=-40~+85°C, unless otherwise specified)

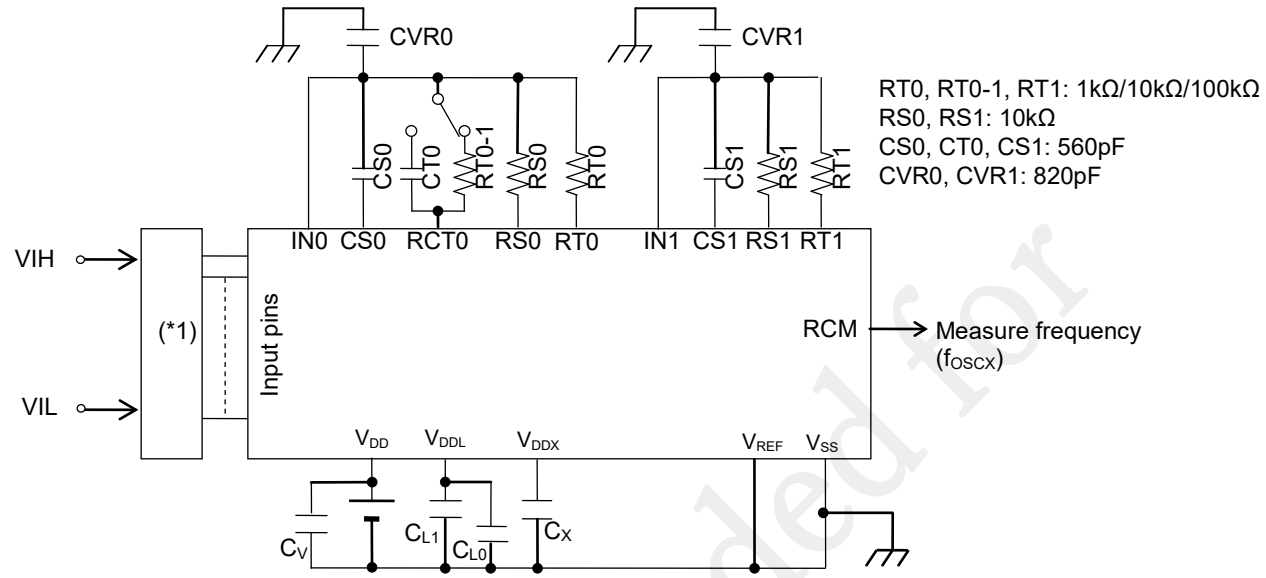
Parameter	Symbol	Condition	Rating			unit
			Min.	Typ.	Max.	
Resister for oscillation	RS0,RS1,RT0 ,RT0-1,RT1	–	1	–	400	kΩ
Oscillation frequency V_{DD} = 3.0V CVR=820pF CS=560pF RAMD0=0	f_{OSC1_0}	Resister for oscillation =1kΩ	–	528	–	kHz
	f_{OSC2_0}	Resister for oscillation =10kΩ	–	59	–	kHz
	f_{OSC3_0}	Resister for oscillation =100kΩ	–	5.9	–	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 3.0V CVR=820pF CS=560pF RAMD0=0	Kf1_0	RT0, RT0-1, RT1=1kΩ	8.225	8.94	9.655	–
	Kf2_0	RT0, RT0-1, RT1=10kΩ	0.99	1	1.01	–
	Kf3_0	RT0, RT0-1, RT1=100kΩ	0.093	0.101	0.109	–
Oscillation frequency V_{DD} = 5.0V CVR=820pF CS=560pF RAMD0=1	f_{OSC1_0}	Resister for oscillation =1kΩ	–	528	–	kHz
	f_{OSC2_0}	Resister for oscillation =10kΩ	–	59	–	kHz
	f_{OSC3_0}	Resister for oscillation =100kΩ	–	5.9	–	kHz
RS to RT oscillation frequency ratio *1 V_{DD} = 5.0V CVR=820pF CS=560pF RAMD0=1	Kf1_0	RT0, RT0-1, RT1=1kΩ	8.225	8.94	9.655	–
	Kf2_0	RT0, RT0-1, RT1=10kΩ	0.99	1	1.01	–
	Kf3_0	RT0, RT0-1, RT1=100kΩ	0.093	0.101	0.109	–

*1: Kfx is the ratio of the oscillation frequency by the sensor resistor to the oscillation frequency by the reference resistor on the same conditions.

$$Kfx = \frac{f_{OSCx}(\text{RT0-CS0 oscillation})}{f_{OSCx}(\text{RS0-CS0 oscillation})} \quad , \quad \frac{f_{OSCx}(\text{RT0-1-CS0 oscillation})}{f_{OSCx}(\text{RS0-CS0 oscillation})} \quad , \quad \frac{f_{OSCx}(\text{RT1-CS1 oscillation})}{f_{OSCx}(\text{RS1-CS1 oscillation})}$$

(x = 1, 2, 3)

Measuring circuit



(*1) Input logic circuit to determine the specified measuring conditions.

【Note】

・Please have the shortest layout for the common node (wiring patterns which are connected to the external capacitors, resistors and IN0/IN1 pin), including CVR0/CVR1. Especially, do not have long wire between IN0/IN1 and RS0/RS1. The coupling capacitance on the wires may occur incorrect A/D conversion. Also, please do not have signals which may be a source of noise around the node.

・When RT0/RT1 (Thermistor and etc.) requires long wiring due to the restricted placement, please shield the signal by V_{SS}(GND).

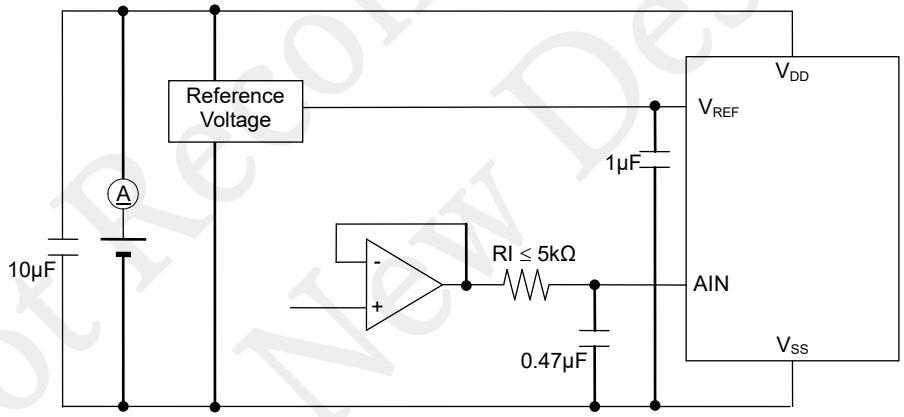
・Please make wiring to components (capacitor, resistor and etc.) necessary for objective measurement. Wiring to reserved components may affect to the A/D conversion operation by noise the components itself may have.

●Electrical Characteristics of SA-ADC

(V_{DD}=1.8~5.5V, V_{SS}=0V, Ta=-40~+85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Resolution	n	–	–	12	–	bit
Integral non-linearity error	INL	2.7V ≤ V_{REF} ≤ 5.5V	−4	–	+4	LSB
		2.2V ≤ V_{REF} < 2.7V	−6	–	+6	
		1.8V ≤ V_{REF} < 2.2V (using Low-speed clock)	−10	–	+10	
Differential non-linearity error	DNL	2.7V ≤ V_{REF} ≤ 5.5V	−3	–	+3	
		2.2V ≤ V_{REF} < 2.7V	−5	–	+5	
		1.8V ≤ V_{REF} < 2.2V (using Low-speed clock)	−9	–	+9	
Zero-scale error	V_{OFF}	2.2V ≤ V_{REF} ≤ 5.5V	−6	–	+6	
		1.8V ≤ V_{REF} < 2.2V (using Low-speed clock)	−10	–	+10	
Full-scale error	FSE	2.2V ≤ V_{REF} ≤ 5.5V	−6	–	+6	
		1.8V ≤ V_{REF} < 2.2V (using Low-speed clock)	−10	–	+10	
Input impedance	RI	–	–	–	5k	Ω
Reference voltage	V_{REF}	–	1.8	–	V_{DD}	V
Conversion time	t_{CONV}	Using High-speed clock(max. 4MHz)	–	170	–	clk
		Using Low-speed clock	–	16	–	

Measuring circuit

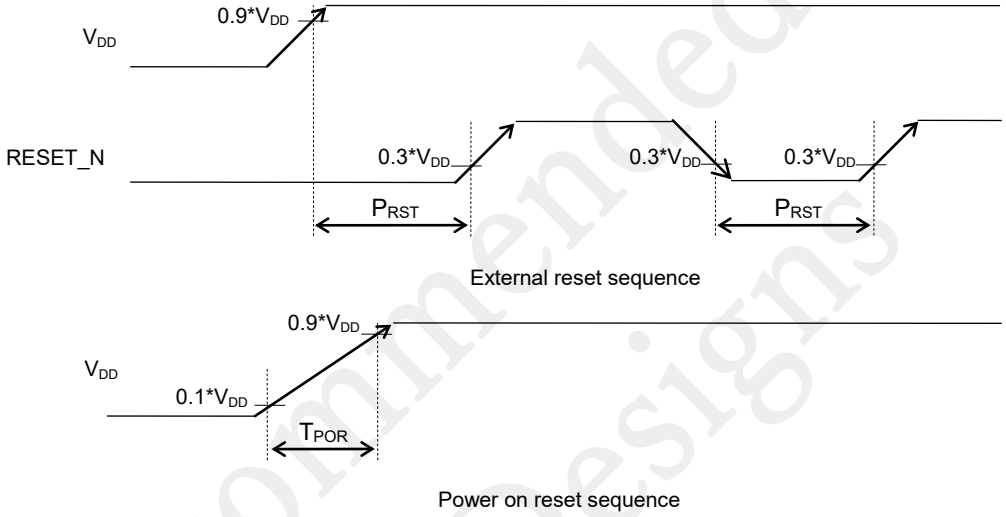


●Reset characteristics

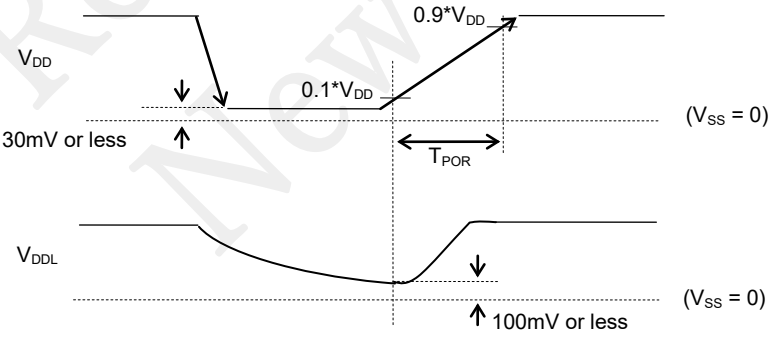
(V_{DD}=1.8 to 5.5V, V_{SS}=0V, Ta=-40 to +85°C, unless otherwise specified)

Parameter	Symbol	Condition	Rating			Unit	Measuring circuit
			Min.	Typ.	Max.		
Reset pulse width	P_{RST}	–	200	–	–	μs	1
Reset noise elimination pulse width	P_{NRST}	–	–	–	0.3	μs	
Power-on reset activation power rise time	T_{POR}	–	–	–	10	ms	

*1 : Mean value of 1024 cycle.
*2 : Guarantee value at the time of the shipment.

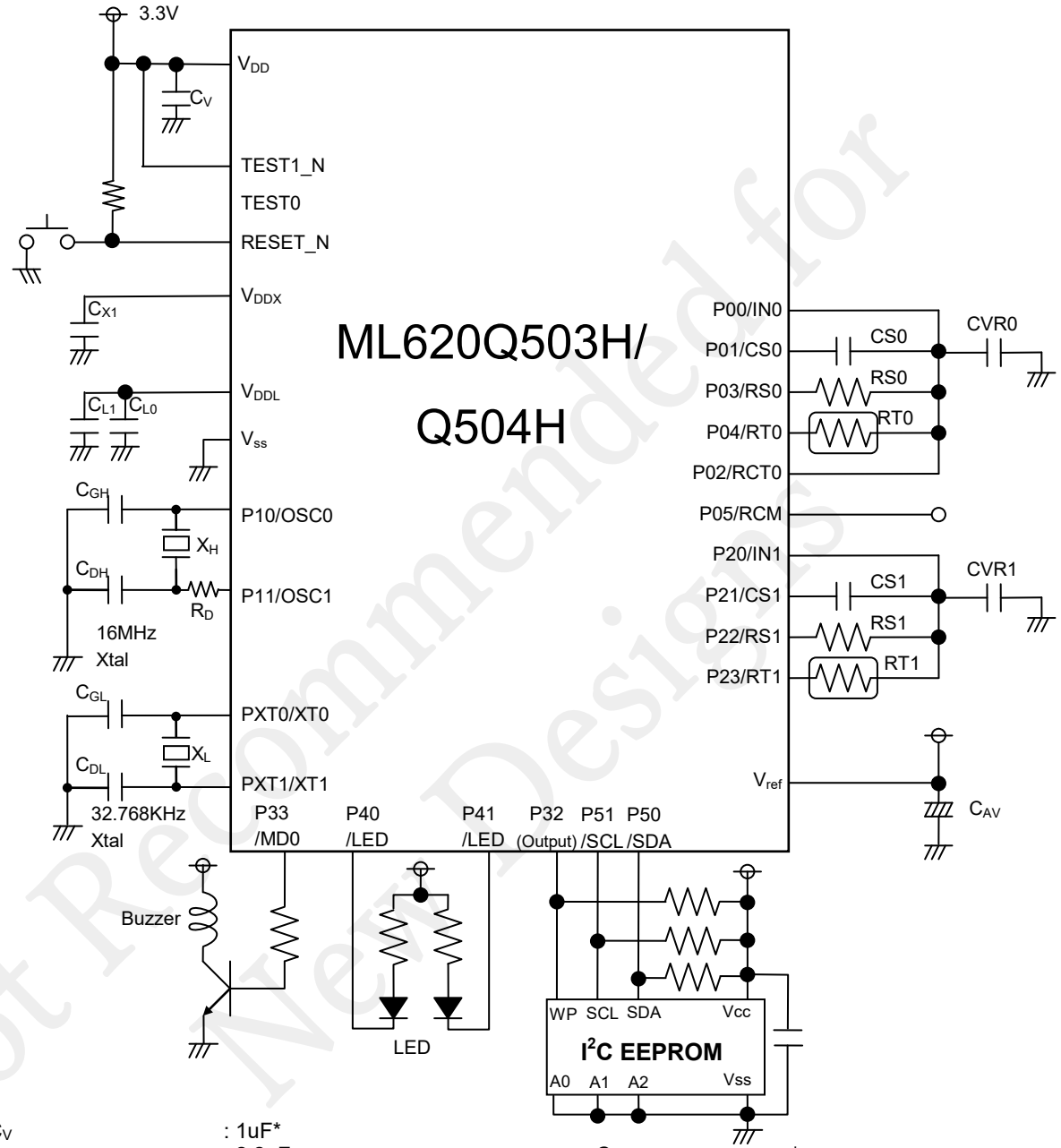


●Power-on and shutdown Procedures
In case of power-on or shutdown of V_{DD}, the procedures and constraints are shown as following.



【Note】
・If V_{DDL} level is 100mV or more over, reset the IC by RESET_N pin after power-on.
・T_{POR} is the value when V_{DD} slope is liner. If V_{DD} slope is not liner in your system, use RESET_N or contact us.

Appendix D Application Circuit Example



C_V	: 1uF*		
C_{L1}	: 2.2uF	C_{L0}	: open*
C_{X1}	: 0.33uF		
C_{GL}	: 12～16pF*	C_{DL}	: 12～16pF*
C_{GH}	: 12～20pF*	C_{DH}	: 12～20pF*
R_D	: 0Ω*		
C_{AV}	: 1uF*	RS0, RS1	: 10 KΩ
CS0, CS1	: 560 pF	CVR0, CVR1	: 820 pF
RT0, RT1	: Thermistor (103AT/Semitec)		
X_H	: NX8045GB/16.000MHz, Nihon Denpa Kogyo		
X_L	: DT-26, Daishinku		

*: Make a decision the parameters after evaluating on an user's conditions when designing circuits for mass production.

Revision History

Revision History

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
FEUL620Q504H-01	Aug. 31, 2015	–	–	Final edition 1.0
FEUL620Q504H-02	May. 20, 2020	2	2	Updated the relevant documents.
		1-4	1-4	[1.1] Updated Shipment
		1-13 D-1	1-13 D-1	[1.3.4] Updated about RESET_N, TEST1_N pins in table 1-1 and figure.
		2-2	2-2	[2.2] Corrected Fig.2-1(a) <published as errata>
		6-12	6-12	[6.3.1.2] Updated note.
		–	8-13	[8.3.4] Added new section <published as errata>
		9-9 9-23	9-9 9-23	[9.2.4][9.2.13] Corrected description of FTnIOB
		28-8 28-9	28-8 28-9	[28.3.1] Corrected exposition.
		30-1	30-1	[30.2] Updated the connection of TEST1_N pin in Fig.30-1
		B-1	B-1	Updated package dimensions
		C-2	C-2	Added comment in recommended operating conditions.
		C-18	C-18	Corrected "Power-on and shutdown Procedures" <published as errata>
		C-4	C-18	Changed placement of reset characteristics. Added note.