EVB-VSC8541-EDS Evaluation Board User's Guide

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ISBN: 978-1-6683-1647-4

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Preface

NOTICE TO CUSTOMERS

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Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the Microchip EVB-VSC8541-EDS Evaluation Board User's Guide. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Website
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document features the EVB-VSC8541-EDS Evaluation Board. The manual layout is as follows:

- **Chapter 1. "Overview"** – This section provides an overview of the evaluation board.
- **Chapter 2. "Getting Started"** – This section provides details on the board's power, clock, and reset circuit, and information on the use of the board with other EDS base boards.
- **Chapter 3. "Board Details and Configuration"** – This section shows the board features and configuration settings.
- **Appendix A. "Schematics"** – This section shows the EVB-VSC8541-EDS Evaluation Board schematic diagrams.
- **Appendix B. "Bill of Materials"** – This section shows the EVB-VSC8541-EDS Evaluation Board Bill of Materials.

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file.o`*`, where `*`file`*` can be any valid filename`
Square brackets [ ]	Optional arguments	`mcc18 [options] file [options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
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- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB® REAL ICE™ and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit™ 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows® Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are non-production development programmers such as PICSTART® Plus and PICkit™ 2 and 3.

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- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

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Technical support is available through the website at:
http://www.microchip.com/support

DOCUMENT REVISION HISTORY

Revisions	Section/Figure/Entry	Correction
DS50003414B (12-1-22)	Section 2.3 "Power Source"	Moved former Sections 2.1.1 and 2.1.2 to this section.
	Section 2.2 "Default Jumper Settings"	New section
	Section 2.6.2 "With EVB-LAN7801-EDS and EVB-LAN7431-EDS"	Expanded details in this section.
	Section 3.3 "Pin Strapping Configurations"	Rewrote this section and added Figure 3-2, Figure 3-3, and Figure 3-4.
	Section 3.5 "Connectors"	New section
	All	Made minor formatting changes
DS50003414A (09-28-22)	Initial release	

Chapter 1. Overview

1.1 INTRODUCTION

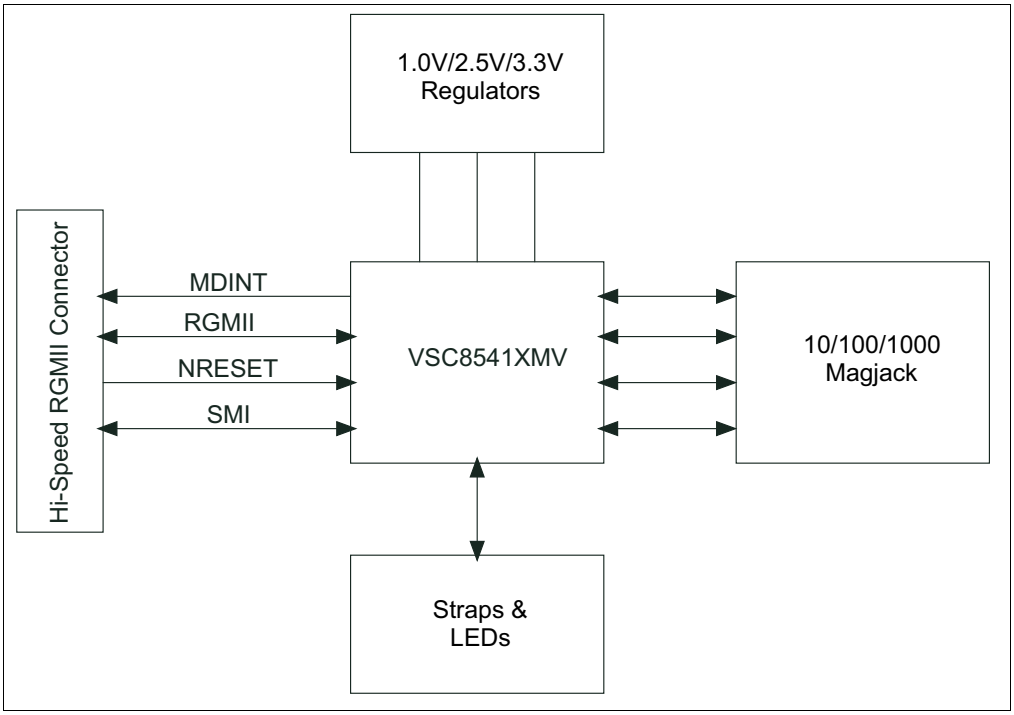
The EVB-VSC8541-EDS evaluation board is a plug-in daughter card that interfaces directly with a mating Microchip host processor or controller board, such as the SAMA5D3 Ethernet Development System (EDS) board, as well as a USB bridge board (EVB-LAN7801-EDS) and a PCIe® bridge board (EVB-LAN7431-EDS). It features the VSC8541, a highly integrated networking device that incorporates a 10/100/1000BASE-T physical layer transceiver (PHY). The board's PHY port is connected to an RJ45 Ethernet jack with integrated magnetics, and the PHY's RGMII connections are brought out to a high-speed (HS) multi-pin connector.

Together, the EVB-VSC8541-EDS and the EDS base board provide a highly flexible platform for evaluation of PHY features using their internal memory registers and the management interface.

This document describes the EVB-VSC8541-EDS setup and its user interface features. A simplified block diagram of the board is shown in Figure 1-1.

1.1.1 Block Diagram

FIGURE 1-1: EVB-VSC8541-EDS BLOCK DIAGRAM



1.1.2 References

Concepts and materials available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

- *VSC8541-02 and VSC8541-05 Data Sheet* (www.microchip.com/en-us/product/VSC8541)
- *VSC8541 Hardware Design Checklist*
- *EVB-VSC8541-EDS Schematics*
- *SAMA5D3 Ethernet Development System Schematics*
- *SAMA5D3 Ethernet Development System Board User's Guide*
- *EVB-LAN7801 Ethernet Development System Schematics*
- *EVB-LAN7801 Ethernet Development System User's Guide*
- *EVB-LAN7431 Ethernet Development System Schematics*
- *EVB-LAN7431 Ethernet Development System User's Guide*

1.1.3 Terms and Abbreviations

The following are the terms and abbreviations used in this document:

- EDS – Ethernet Development System
- HS – High speed
- MDC – Management Data Clock
- MDIO – Management Data Input/Output
- MII – Media Independent Interface
- PHY – Physical Layer Transceiver
- RGMII – Reduced Gigabit Media Independent Interface
- SMI – Serial Management Interface
- UTP – Unshielded Twisted Pair

Chapter 2. Getting Started

2.1 INTRODUCTION

The EVB-VSC8541-EDS evaluation board is designed as a plug-in card to interface directly with a mating Microchip host processor or controller board, such as the SAMA5D3 Ethernet Development System (EDS) board, as well as a USB bridge board (EVB-LAN7801-EDS) and a PCIe® bridge board (EVB-LAN7431-EDS). The base board supplies full power and provides full register access and configuration via MDIO/MDC bus management.

2.2 DEFAULT JUMPER SETTINGS

The EVB-VSC8541-EDS ships with the necessary jumpers installed for basic operation. These are:

- **J1**: shunt installed between pins [2-3]
- **J2**: shunt installed between pins [2-3]
- **J4**: shunt installed between pins [1-2]

See Figure 3-1 for an image of these default shunt installations.

See Section 3.5 "Connectors" for a full list of connector/header descriptions and directions for use.

2.3 POWER SOURCE

The EVB-VSC8541-EDS can be completely bus-powered from its mating Microchip host processor or control board. Alternatively, the EVB-VSC8541-EDS can be powered with an external 3.3V supply.

Refer to Figure 3-1 and the board schematics in Figure A-2 for details.

2.3.1 EDS-Powered Operation

For EDS-powered operation, **J1** needs a jumper on the pins [2-3], and **J2** needs a jumper on the VDDIO pins [2-3] as shown in Figure 3-1.

2.3.2 External-Powered Operation

For external-powered operation, **J1** needs a jumper on pins [1-2], while **J2** needs a jumper on either 2.5V pins [1-2] or VDDIO pins [2-3]. An external 3.3V power source should be connected to TP1.

2.4 CLOCK

The EVB-VSC8541-EDS utilizes a 25 MHz crystal to generate input reference clock for the VSC8541 device. Refer to Figure A-3 for details.

Note:	The EVB-VSC8541-EDS does not include options for supplying an external single-ended clock.

2.5 RESET CIRCUIT

2.5.1 Power-On Reset—EDS Reset

The SAMA5D3-EDS can provide the VSC8541 Reset when a jumper is placed on EVB-VSC8541-EDS, **J4** pins [1-2] (EDS Reset).

2.5.2 Power-On Reset—Reset Circuit

A discrete component MIC826TYMT provides power-on Reset to the VSC8541 device when a jumper is placed on EVB-VSC8541-EDS, **J4** pins [2-3] (Reset).

2.5.3 Manual Reset

The EVB-VSC8541-EDS SW3 can be pressed and released to provide VSC8541 Reset after device power-up. The EVB-VSC8541-EDS **J4** must have a jumper between pins [2-3] (Reset) to utilize this manual Reset.

2.6 USING THE EVB-VSC8541-EDS

2.6.1 With EVB-SAMA5D3-EDS

The EVB-VSC8541-EDS directly plugs into a mating Microchip host controller or processor board, such as the SAMA5D3-EDS, that can deliver full power and provide full register access and configuration via MDIO/MDC bus management.

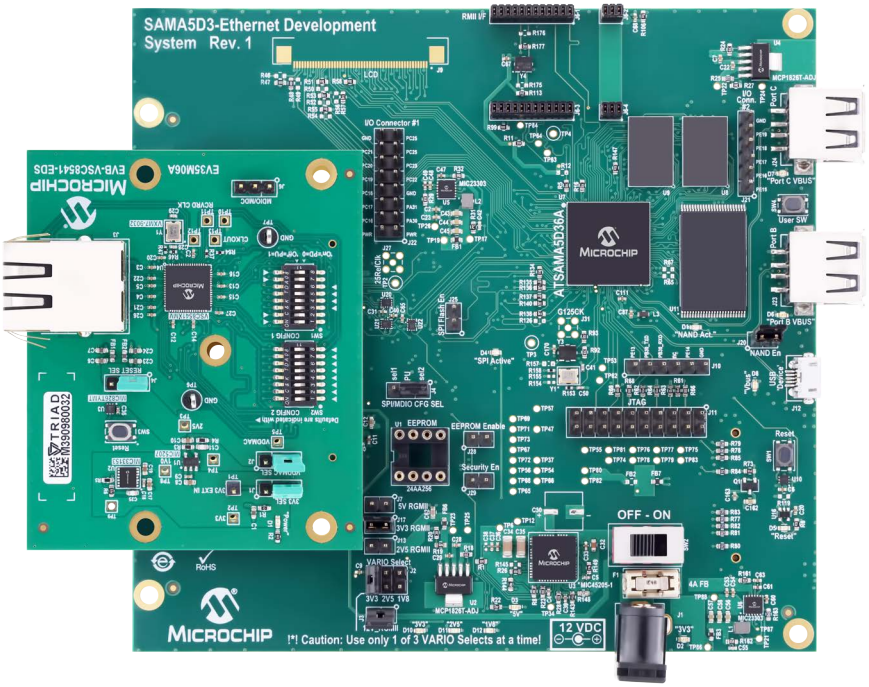
Together, the EVB-VSC8541-EDS and the SAMA5D3-EDS enable 10/100/1000 Mbps Ethernet traffic through RGMII and the PHY port of the VSC8541 device, with the RGMII port connecting to the SAMA5D3 processor and the PHY port connecting via copper Ethernet cable (CAT-5 UTP or better) to external Ethernet devices.

All VSC8541 registers are accessible via MDIO/MDC bus management from the SAMA5D3-EDS Board, enabling full evaluation and firmware for all VSC8541 features. MDIO/MDC pins are also available for external control at header **J6**.

> **Note:** Refer to the SAMA5D3 Ethernet Development System Board User's Guide on its usage.

Figure 2-1 shows the EVB-VSC8541-EDS connected to the SAMA5D3-EDS board.

FIGURE 2-1: EVB-VSC8541-EDS AND SAMA5D3-EDS BOARD (TOP VIEW)



Note: A document that describes the detailed source build and installation instructions for the VSC8541 PHY using the SAMA5D3 MPU is available on the EVB-VSC8541-EDS evaluation board product page.

2.6.2 With EVB-LAN7801-EDS and EVB-LAN7431-EDS

To work with EVB-LAN7801-EDS and EVB-LAN7431-EDS with the default jumper and switch settings on EVB-VSC8541-EDS, a specific EEPROM image for LAN7801/LAN7431 should be programmed onto the EVB baseboard. This is necessary to ensure that RGMII TXC and RXC delays settings are appropriately configured, and the 125 MHz clock source is enabled internal to the LAN7801/LAN7431.

A `readme` file that describes the detailed configuration and the binary files used to program the EEPROM on the bridge boards are available on the EVB-VSC8541-EDS evaluation board product page.

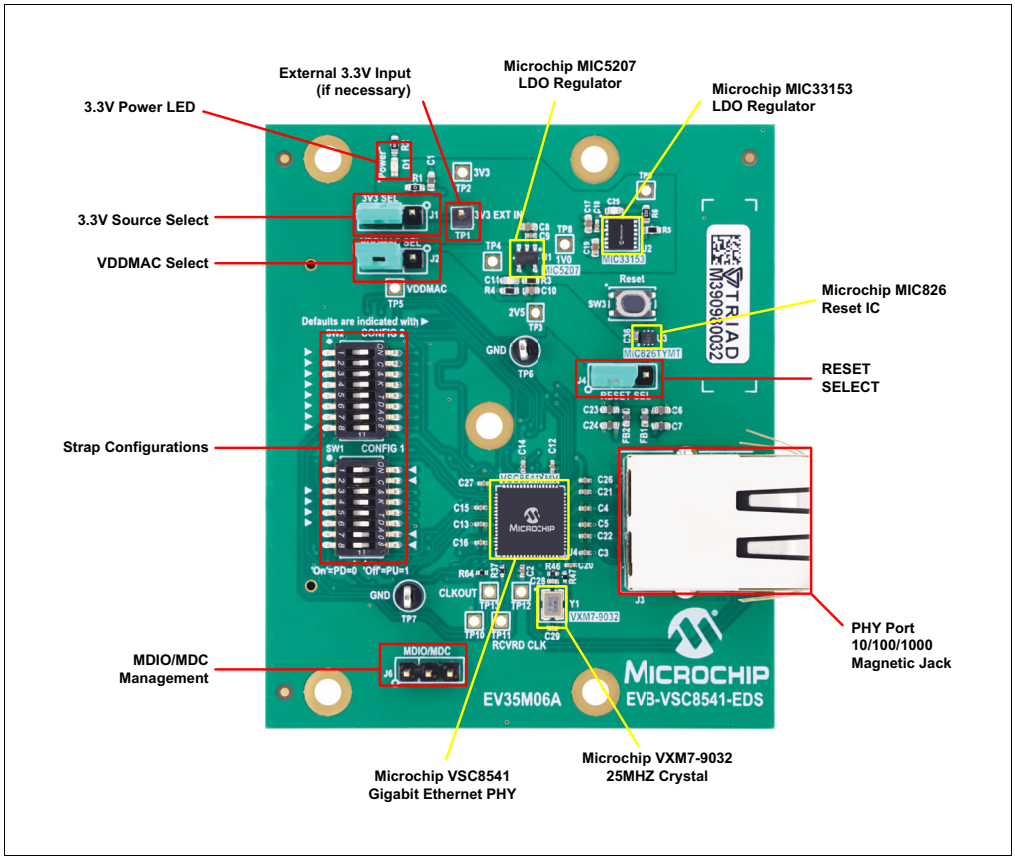
NOTES:

Chapter 3. Board Details and Configuration

3.1 INTRODUCTION

The following sections describe the board features and configuration settings. Figure 3-1 displays the top view of the EVB-VSC8541-EDS with key features, jumpers, straps, power, and headers highlighted in red. The Microchip components are highlighted in yellow.

FIGURE 3-1: EVB-VSC8541-EDS TOP VIEW WITH CALLOUTS



3.2 PHY PORT

PHY port (J3) supports 10BASE-T/100BASE-TX/1000BASE-T with both auto-negotiation enabled and Auto-MDI/MDI-X enabled as the power-up defaults.

3.3 PIN STRAPPING CONFIGURATIONS

As the power-up or Reset defaults, the VSC8541 device is configured via internal or external pull-up or pull-down resistors to the settings in Table 3-1 and Table 3-2 via **SW1** and **SW2**, respectively.

TABLE 3-1: SW1 PIN STRAPPING CONFIGURATION

SW1 Position	VSC8541 Pin Name	Options	Default Settings	
			SW1 Setting	Selection
1	RX_CLK_R	0 = Managed mode 1 = Unmanaged mode	OFF	Unmanaged mode
2	RX_D0_R	00 = 0.2 ns 01 = 2 ns 10 = 1.1 ns 11 = 2.6 ns	OFF	TX and RX to 2.0 ns delay
3	RX_D1_R		ON	
4	RX_D2_R	00 = Default mode 01 = 100BTX, HDX Forced mode, autoneg OFF 10 = 10/100 FDX/HDX, autoneg ON (disable 1000BT advertisements) 11 = 10BT, HDX Forced mode, autoneg OFF	ON	Default mode
5	RX_D3_R		ON	
6	RX_DV/ RX_CTL_R	0 = RGMII mode 1 = RMII mode	ON	RGMII mode
7	RX_D4_R	00 = PHY Address 0 01 = PHY Address 1 10 = PHY Address 2 11 = PHY Address 3	OFF	PHY Address 3
8	RX_D5_R		OFF	

TABLE 3-2: SW2 PIN STRAPPING CONFIGURATION

SW2 Position	VSC8541 Pin Name	Options	Default Settings	
			SW1 Setting	Selection
1	MII_TXCLK	0 = RGMII mode 1 = GMII/MII mode	ON	RGMII mode
2	RX_ER	0 = Normal Operation 1 = Enable Forced 1000BT mode	ON	Normal Operation
3	COL	Sampled only if RX_ER = 1 0 = Client mode 1 = Server mode	ON	Client mode
4	CRS	Sampled only if RX_ER = 1 0 = MDI mode 1 = MDI-X mode	ON	MDI mode
5	CLKOUT	0 = CLKOUT Output Disabled 1 = CLKOUT Output Enabled	ON	CLKOUT Output Disabled

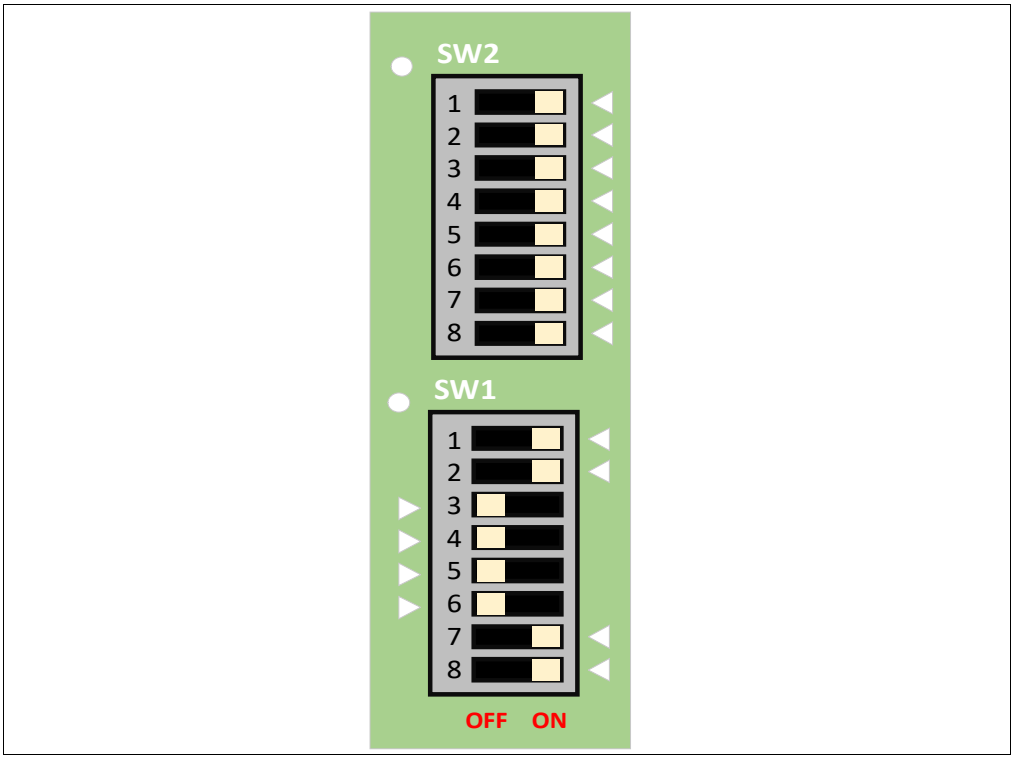
TABLE 3-2: SW2 PIN STRAPPING CONFIGURATION (CONTINUED)

SW2 Position	VSC8541 Pin Name	Options	Default Settings	
			SW1 Setting	Selection
6	RX_D6	00 = 25 MHz 01 = 50 MHz 10 = 125 MHz 11 = Reserved	ON	25 MHz (CLKOUT Output is disabled, so this setting is a 'don't care')
7	RX_D7		ON	
8	COMA_MODE	0 = PHY will be fully active once out of Reset. 1 = Keep the PHYs from becoming active until after initialization.	ON	PHY will be fully active once out of Reset.

Note: Traditionally, the communication protocol uses the terminologies, "master" and "slave." The equivalent Microchip terminologies used in this document are "client" and "server."

Figure 3-2 shows the default switch settings of SW1 and SW2.

FIGURE 3-2: DEFAULT SWITCH SETTINGS



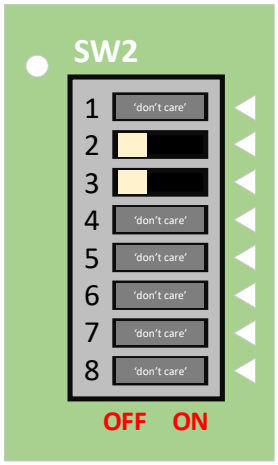
3.3.1 Alternate Strap Settings

3.3.1.1 DISABLING TXC AND RXC CLOCK DELAY

If TXC and RXC clock delays are being managed on the MAC side of the RGMII connection, then it may be necessary to disable TXC and RXC clock delay on the PHY. The TXC and RXC clock delays can be effectively disabled by selecting the 0.2 ns delay option through the following SW1 positions show in Figure 3-3:

- **SW2** position 2: OFF
- **SW2** position 3: OFF

FIGURE 3-3: DISABLING TXC/RXC CLOCK DELAY

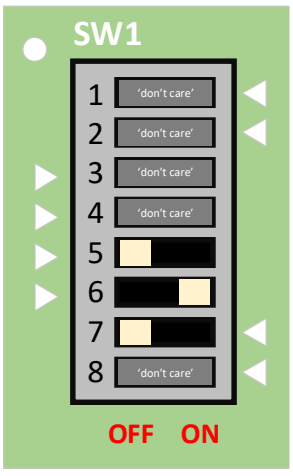


3.3.1.2 ENABLING 125 MHZ CLOCK OUTPUT

If the MAC requires an external 125 MHz clock, then this signal can be provided by the VSC8541 CLKOUT output. The clock output can be enabled by setting the following **SW2** positions shown in Figure 3-4:

- **SW2** position 5: OFF
- **SW2** position 6: ON
- **SW2** position 7: OFF

FIGURE 3-4: ENABLING 125 MHZ CLOCK OUTPUT



3.4 TEST POINTS

Table 3-3 lists the test points on the EVB-VSC8541-EDS:

TABLE 3-3: TEST POINTS

Test Point	Description
TP1	External 3V3 Input
TP2	3V3
TP3	2V5
TP4	GND
TP5	VDDMAC
TP6	GND
TP7	GND
TP8	1V0
TP9	GND
TP10	FASTLINK_FAIL
TP11	RCVRD_CLK
TP12	CLK_SQUELCH_IN
TP13	CLKOUT

3.5 CONNECTORS

Table 3-4 lists the connectors on the EVB-VSC8541-EDS:

TABLE 3-4: CONNECTORS

Connector Reference Designator	Function	Options
J1	3.3V Source Selection	Shunt pins [1-2]: 3.3V power is supplied via an off-board bench supply connected to **TP1**. Shunt pins [2-3]: 3.3V power is supplied from the attached baseboard (default).
J2	2.5V Source Selection	Shunt pins [1-2]: 2.5V power is supplied via an on-board regulator (U1 - MIC5207). Shunt pins [2-3]: 2.5V power is supplied from the attached baseboard (default).
J3	Ethernet RJ45 Connector	N/A
J4	Reset Source Selection	Shunt pins [1-2]: Reset signal is controlled off-board via the attached baseboard (default). Shunt pins [2-3]: PHY Reset signal is controlled from the on-board Reset supervisor (U3 - MIC826TYMT) and button (SW3).
J5	Board to Board Connector	N/A
J6	MDIO Probe Header Pin 1: MDC Pin 2: MDIO Pin 3: MDIO	For probe only. Do not connect shunt across any pins on **J6**.

NOTES:

Appendix A. Schematics

A.1 INTRODUCTION

This appendix shows the EVB-VSC8541-EDS Evaluation Board schematics.

FIGURE A-1: EVB-VSC8541-EDS BLOCK DIAGRAM

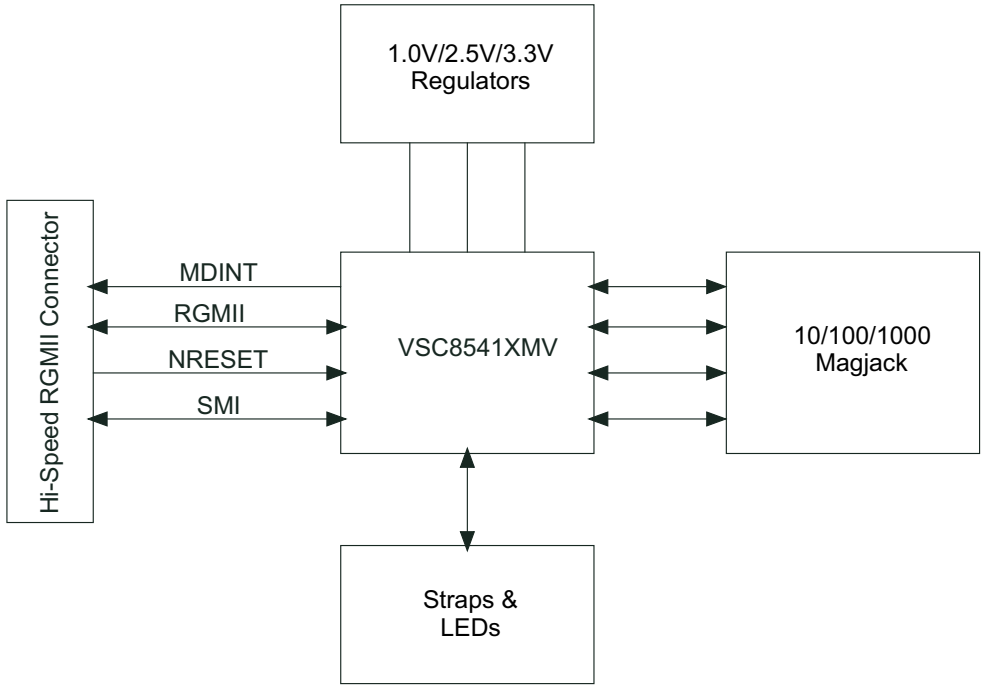
EVB-VSC8541-EDS Plug-In Evaluation Board

Table of Contents

Sheet	Description
1	Title Page
2	VSC8541 Power
3	VSC8541 PHY
4	VSC8541 Samtec Interface

Revision History

Revision	Date	Revision Summary	Author
A	02/11/2022	Initial release	Rahul Kommineni



Project Owner: Rahul Kommineni
PCB Layout Contact: Carl Johnson
PartNumber: EV35M06A
Project Title: EVB-VSC8541-EDS
Variant: [No Variations]
Sheet Title: Title Page
Size: B | SCH #: 03-00462 | Rev: 1 | Date: 9/6/2022
PCB #: 04-11568 | Rev: 1 | Sheet 1 of 4
File: VSC8541 TitlePage.SchDoc

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FIGURE A-2: EVB-VSC8541-EDS POWER

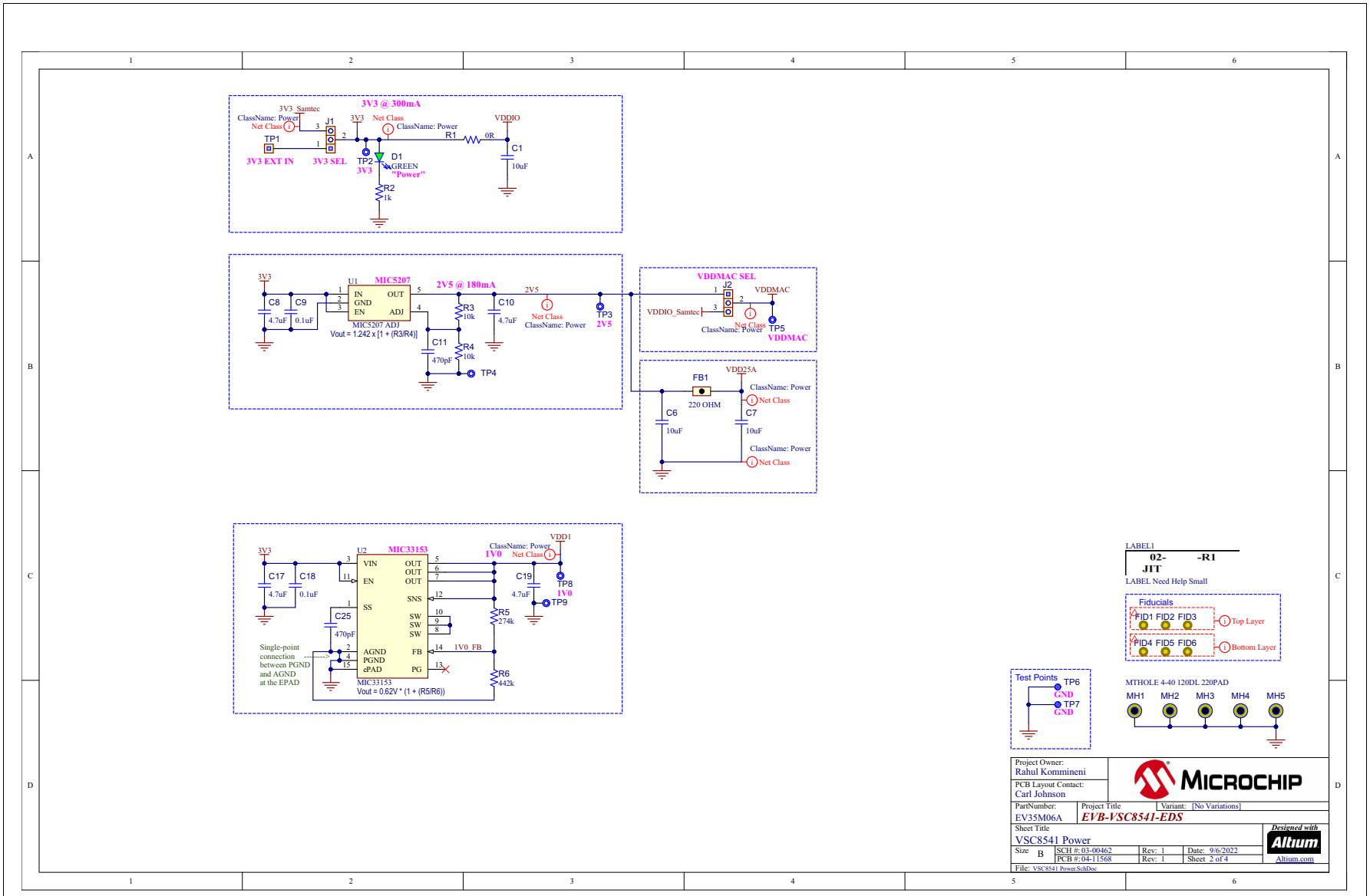


FIGURE A-3: EVB-VSC8541-EDS PHY

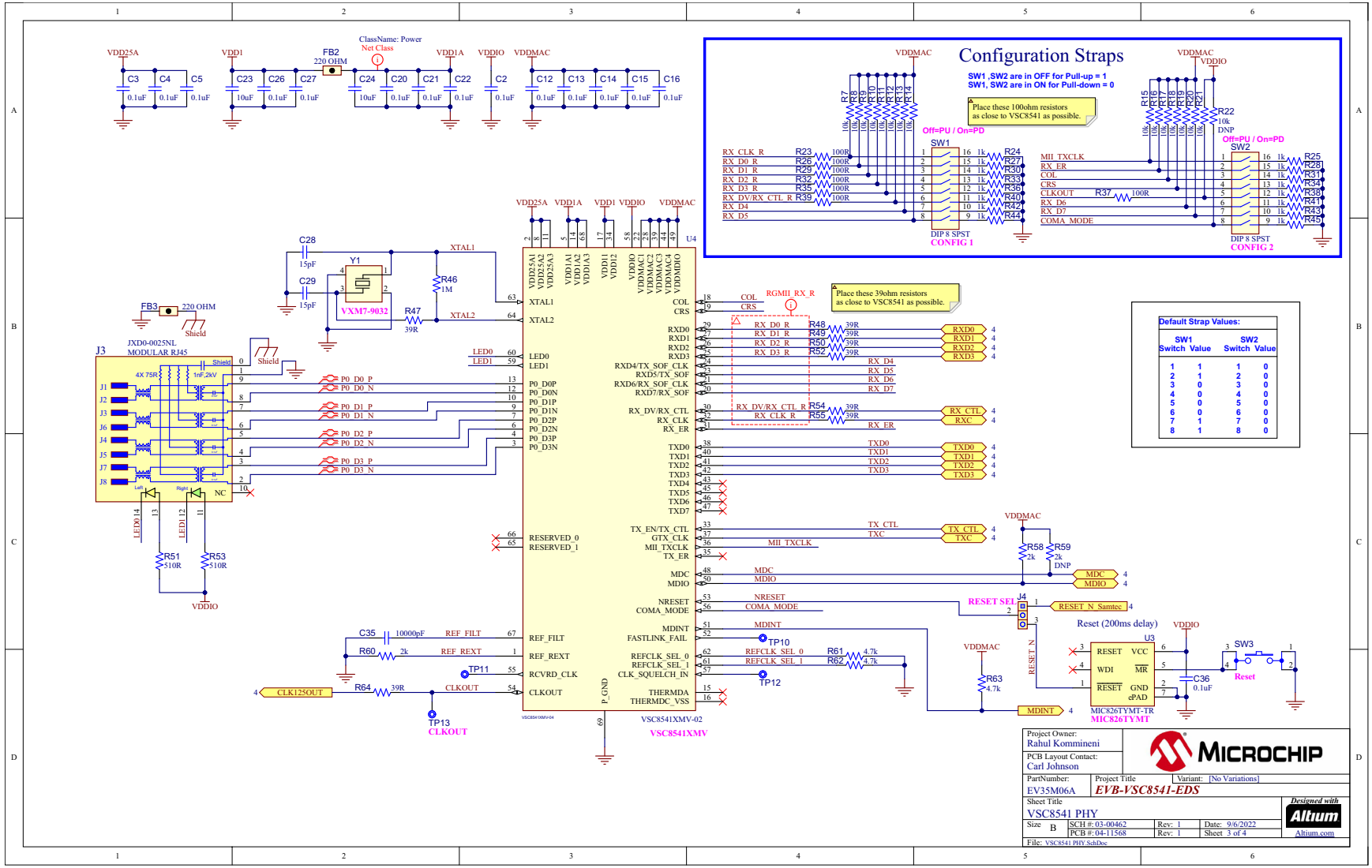
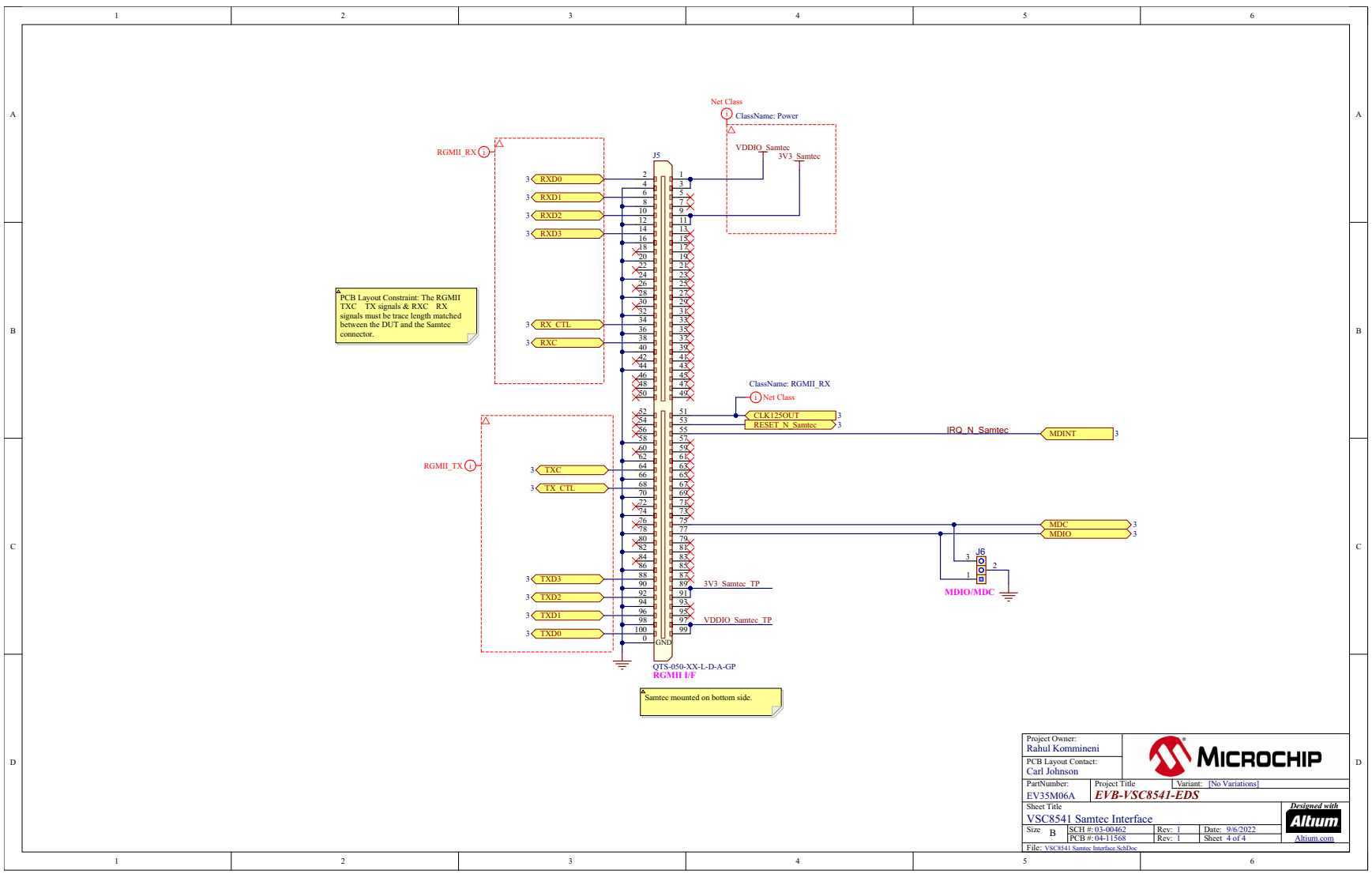


FIGURE A-4: EVB-VSC8541-EDS SAMTEC INTERFACE



NOTES:

Appendix B. Bill of Materials

B.1 INTRODUCTION

This appendix shows the EVB-VSC8541-EDS Evaluation Board Bill of Materials.

TABLE B-1: EVB-VSC8541-EDS BILL OF MATERIALS

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
1	5	C1, C6, C7, C23, C24	CAP CER 10 µF 6.3V 20% X5R SMD 0603	Yes	AVX	06036D106MAT2A
2	17	C2, C3, C4, C5, C9, C12, C13, C14, C15, C16, C18, C20, C21, C22, C26, C27, C36	CAP CER 0.1 µF 50V 10% X7R SMD 0402	Yes	Taiyo Yuden	UMK105B7104KV-FR
3	4	C8, C10, C17, C19	CAP CER 4.7 µF 10V 10% X5R SMD 0603	Yes	KEMET	C0603C475K8PACTU
4	2	C11, C25	CAP CER 470 pF 25V 5% NP0 SMD 0603	Yes	AVX	06033A471JAT2A
5	2	C28, C29	CAP HiQ 15 pF 50V 5% NP0 2.32GHz SMD 0402	Yes	Johanson Technology Inc	500R07S150JV4T
6	1	C35	CAP CER 10000 pF 16V 10% X7R SMD 0402	Yes	KEMET	C0402C103K4RACTU
7	1	D1	DIO LED GREEN 2V 30 mA 35 mcd Clear SMD 0603	Yes	Lite-On Inc	LTST-C191KGKT
8	3	FB1, FB2, FB3	FERRITE 500 mA 220R SMD 0603	Yes	Murata Electronics North America	BLM18AG221SN1D
9	4	J1, J2, J4, J6	CON HDR-2.54 Male 1x3 Gold 5.84 MH TH VERT	Yes	FCI	68000-103HLF
10	1	J3	CON MODULAR JACK RJ45 1000 MAGNETICS 2xLEDs TH R/A TAB-DN	Yes	Pulse Electronics	JXD0-0025NL
11	1	J5	CON STRIP High Speed Stacker 5mm Male 2x50 SMD VERT	Yes	Samtec	QTS-050-01-L-D-A-GP
12	1	LABEL1	LABEL, ASSY W/REV LEVEL (SMALL MODULES) PER MTS-0002	MECH	—	—
13	1	R1	RES TKF 0R 1/10W SMD 0603	Yes	Panasonic	ERJ-3GEY0R00V
14	17	R2, R24, R25, R27, R28, R30, R31, R33, R34, R36, R38, R40, R41, R42, R43, R44, R45	RES TF 1k 1% 1/10W SMD 0603 AEC-Q200	Yes	Stackpole Electronics Inc	RMCF0603FT1K00
15	17	R3, R4, R7, R8, R9, R10, R11, R12, R13, R14, R15, R16, R17, R18, R19, R20, R21	RES TKF 10k 1% 1/10W SMD 0603	Yes	Panasonic	ERJ-3EKF1002V
16	1	R5	RES TKF 274K 1% 1/10W SMD 0603	Yes	Panasonic Electronic Components	ERJ-3EKF2743V
17	1	R6	RES TKF 442k 1% 1/10W SMD 0603 AEC-Q200	Yes	Stackpole Electronics Inc	RMCF0603FT442K
18	1	R22	RES TKF 10k 1% 1/10W SMD 0603	DNP	Panasonic	ERJ-3EKF1002V
19	7	R23, R26, R29, R32, R35, R37, R39	RES TKF 100R 1% 1/10W SMD 0402 AEC-Q200	Yes	Panasonic Electronic Components	ERJ-2RKF1000X
20	1	R46	RES TKF 1M 1% 1/10W SMD 0402	Yes	Panasonic	ERJ-2RKF1004X
21	8	R47, R48, R49, R50, R52, R54, R55, R64	RES TKF 39R 1% 1/16W SMD 0402	Yes	Yageo	RC0402FR-0739RL
22	2	R51, R53	RES TKF 510R 1% 1/10W SMD 0603	Yes	Vishay Dale	CRCW0603510RFKEA
23	2	R58, R60	RES TKF 2k 1% 1/10W SMD 0402	Yes	Panasonic Electronic Components	ERJ-2RKF2001X
24	1	R59	RES TKF 2k 1% 1/10W SMD 0402	DNP	Panasonic Electronic Components	ERJ-2RKF2001X

TABLE B-1: EVB-VSC8541-EDS BILL OF MATERIALS (CONTINUED)

Item	Qty	Reference	Description	Populated	Manufacturer	Manufacturer Part Number
25	3	R61, R62, R63	RES TKF 4.7k 1% 1/16W SMD 0402	Yes	Yageo	RC0402FR-074K7L
26	2	SW1, SW2	SWITCH DIP 8 SPST 24V 25mA TDA08H0SB1R	Yes	C&K Components	TDA08H0SB1R
27	1	SW3	SWITCH TACT SPST-NO 16V 0.05A PTS810 SMD	Yes	C&K Components	PTS810 SJM 250 SMTR LFS
28	1	TP1	CON HDR-2.54 Male 1x1 Gold 5.84 MH TH VERT	Yes	TE Connectivity	5-146280-1
29	2	TP6, TP7	CON TP LOOP Black TH	Yes	Keystone	5011
30	1	U1	MCHP ANALOG LDO ADJ MIC5207YM5 SOT-23-5	Yes	Microchip Technology	MIC5207YM5-TR
31	1	U2	MCHP ANALOG SWITCHER Buck 0.6V to 3.6V MIC33153YHJ-TR VFDFN-14	Yes	Microchip Technology	MIC33153YHJ-TR
32	1	U3	MCHP ANALOG SUPERVISOR 3.075V MIC826TYMT-TR TDFN-6	Yes	Microchip Technology	MIC826TYMT-TR
33	1	U4	MCHP INTERFACE ETHERNET VSC8541XMV-02 QFN-68	Yes	Microchip Technology	VSC8541XMV-02
34	1	Y1	MCHP CRYSTAL 25 MHz +/–20 ppm 10pF SMD L3.2W2.5H0.8	Yes	Microchip / Microsemi	VXM7-9032-25M000

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