EVB-LAN9352 Evaluation Board User's Guide

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Signed for and on behalf of Microchip Technology Inc. at Chandler, Arizona, USA

Derek Carlson
VP Development Tools

12-Sep-14
Date

NOTES:

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Preface

NOTICE TO CUSTOMERS

All documentation becomes dated, and this manual is no exception. Microchip tools and documentation are constantly evolving to meet customer needs, so some actual dialogs and/or tool descriptions may differ from those in this document. Please refer to our web site (www.microchip.com) to obtain the latest documentation available.

Documents are identified with a "DS" number. This number is located on the bottom of each page, in front of the page number. The numbering convention for the DS number is "DSXXXXXA", where "XXXXX" is the document number and "A" is the revision level of the document.

For the most up-to-date information on development tools, see the MPLAB® IDE online help. Select the Help menu, and then Topics to open a list of available online help files.

INTRODUCTION

This chapter contains general information that will be useful to know before using the EVB-LAN9352. Items discussed in this chapter include:

- Document Layout
- Conventions Used in this Guide
- The Microchip Web Site
- Development Systems Customer Change Notification Service
- Customer Support
- Document Revision History

DOCUMENT LAYOUT

This document describes how to use the EVB-LAN9352 Evaluation Board as a development tool for the LAN9352 evaluation board. The manual layout is as follows:

- **Chapter 1. "Overview"** – Shows a brief description of the EVB-LAN9352 Evaluation Board.
- **Chapter 2. "Board Details"** – Includes instructions on how to get started with the EVB-LAN9352 Evaluation Board.
- **Chapter 3. "Board Configuration"** – Provides information about the EVB-LAN9352 Evaluation Board battery charging features.
- **Appendix A. "EVB-LAN9352 Evaluation Board"** – This appendix shows the EVB-LAN9352 Evaluation Board.
- **Appendix B. "EVB-LAN9352 Evaluation Board Schematics"** – This appendix shows the EVB-LAN9352 Evaluation Board schematics.
- **Appendix C. "Bill of Materials (BOM)"** – This appendix includes the EVB-LAN9352 Evaluation Board Bill of Materials (BOM).

CONVENTIONS USED IN THIS GUIDE

This manual uses the following documentation conventions:

DOCUMENTATION CONVENTIONS

Description	Represents	Examples
Arial font:		
Italic characters	Referenced books	*MPLAB® IDE User's Guide*
	Emphasized text	...is the *only* compiler...
Initial caps	A window	the Output window
	A dialog	the Settings dialog
	A menu selection	select Enable Programmer
Quotes	A field name in a window or dialog	"Save project before build"
Underlined, italic text with right angle bracket	A menu path	*File>Save*
Bold characters	A dialog button	Click **OK**
	A tab	Click the **Power** tab
N'Rnnnn	A number in verilog format, where N is the total number of digits, R is the radix and n is a digit.	4'b0010, 2'hF1
Text in angle brackets < >	A key on the keyboard	Press <Enter>, <F1>
Courier New font:		
Plain Courier New	Sample source code	`#define START`
	Filenames	`autoexec.bat`
	File paths	`c:\mcc18\h`
	Keywords	`_asm, _endasm, static`
	Command-line options	`-Opa+, -Opa-`
	Bit values	`0, 1`
	Constants	`0xFF, 'A'`
Italic Courier New	A variable argument	*`file`*`.o`, where *`file`* can be any valid filename
Square brackets [ ]	Optional arguments	`mcc18 [options]` *`file`* `[options]`
Curly brackets and pipe character: { | }	Choice of mutually exclusive arguments; an OR selection	`errorlevel {0|1}`
Ellipses...	Replaces repeated text	`var_name [, var_name...]`
	Represents code supplied by user	`void main (void) { ... }`

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- **General Technical Support** – Frequently Asked Questions (FAQs), technical support requests, online discussion groups, Microchip consultant program member listing
- **Business of Microchip** – Product selector and ordering guides, latest Microchip press releases, listing of seminars and events, listings of Microchip sales offices, distributors and factory representatives

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- **Emulators** – The latest information on Microchip in-circuit emulators.This includes the MPLAB REAL ICE and MPLAB ICE 2000 in-circuit emulators.
- **In-Circuit Debuggers** – The latest information on the Microchip in-circuit debuggers. This includes MPLAB ICD 3 in-circuit debuggers and PICkit 3 debug express.
- **MPLAB IDE** – The latest information on Microchip MPLAB IDE, the Windows Integrated Development Environment for development systems tools. This list is focused on the MPLAB IDE, MPLAB IDE Project Manager, MPLAB Editor and MPLAB SIM simulator, as well as general editing and debugging features.
- **Programmers** – The latest information on Microchip programmers. These include production programmers such as MPLAB REAL ICE in-circuit emulator, MPLAB ICD 3 in-circuit debugger and MPLAB PM3 device programmers. Also included are nonproduction development programmers such as PICSTART Plus and PIC-kit 2 and 3.

CUSTOMER SUPPORT

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- Distributor or Representative
- Local Sales Office
- Field Application Engineer (FAE)
- Technical Support

Customers should contact their distributor, representative or field application engineer (FAE) for support. Local sales offices are also available to help customers. A listing of sales offices and locations is included in the back of this document.

Technical support is available through the web site at:
http://www.microchip.com/support

DOCUMENT REVISION HISTORY

Revision A (September 2015)

- Initial Release of this Document.

Chapter 1. Overview

1.1 INTRODUCTION

The LAN9352 is a full-featured, 2-port 10/100 managed Ethernet switch designed for embedded applications where performance, flexibility, ease of integration and system cost control are required. The LAN9352 combines all the functions of a 10/100 switch system, including the Switch Fabric, packet buffers, Buffer Manager, Media Access Controllers (MACs), PHY transceivers, and host bus interface. IEEE 1588v2 is supported via the integrated IEEE 1588v2 hardware time stamp unit, which supports end-to-end and peer-to-peer transparent clocks.

The LAN9352 complies with the IEEE 802.3 (full/half-duplex 10BASE-T and 100BASE-TX) Ethernet protocol, IEEE 802.3az Energy Efficient Ethernet (EEE) (100Mbps only), and 802.1D/802.1Q network management protocol specifications, enabling compatibility with industry standard Ethernet and Fast Ethernet applications. 100BASE-FX is supported via an external fiber transceiver.

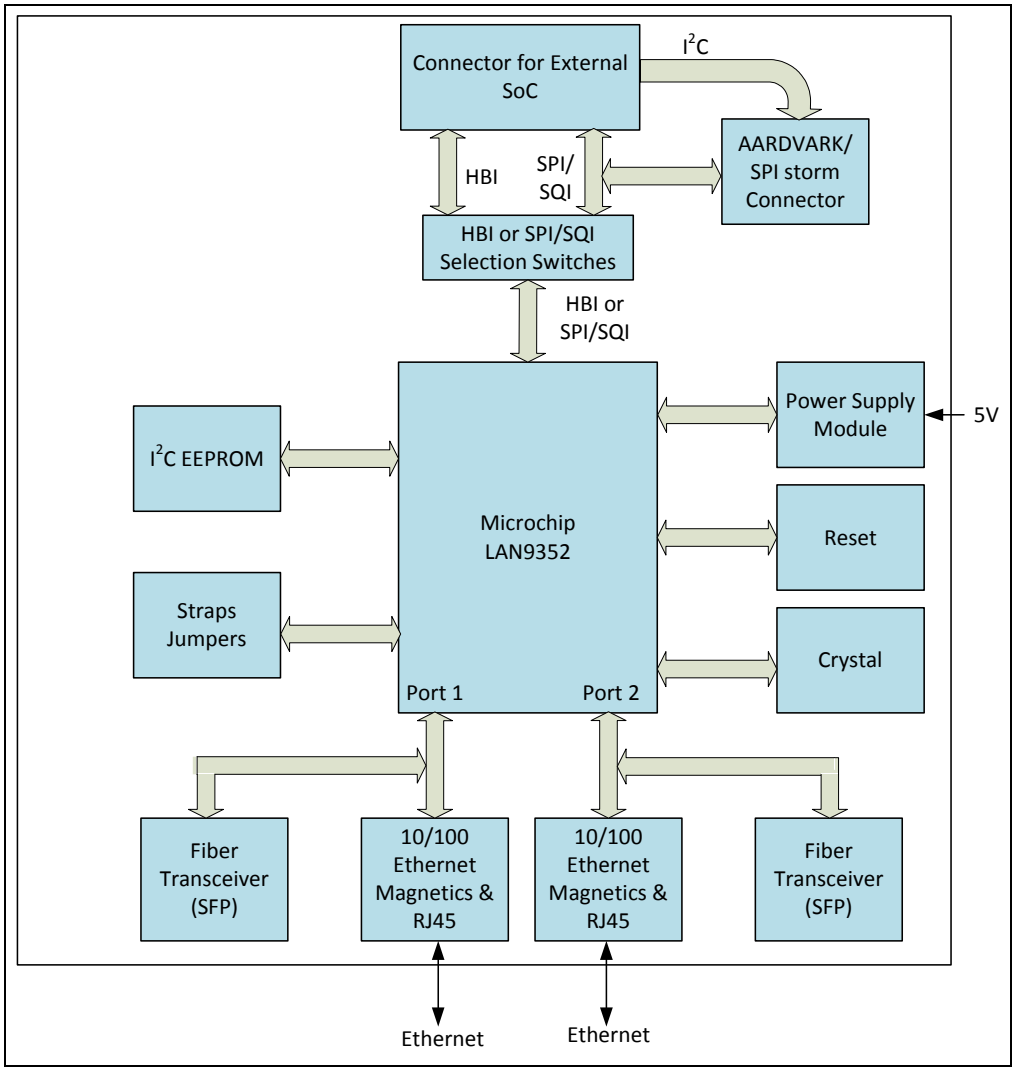
The Host MAC incorporates the essential protocol requirements for operating an Ethernet/IEEE 802.3-compliant node and provides an interface between the Host and the Switch Fabric (LAN9352). On the front end, the Host MAC interfaces to the Host via 2 sets of FIFOs.

On the back end, the Host MAC interfaces with the 10/100 Ethernet PHYs (Virtual PHY 0, PHY A, PHY B) via an internal SMI (Serial Management Interface) bus. This allows the Host MAC access to the PHY's internal registers.

This manual describes the EVB-LAN9352, designed to explore the various features of LAN9352.

Figure 1-1 displays the EVB-LAN9352 block diagram.

FIGURE 1-1: EVB-LAN9352 BLOCK DIAGRAM



1.2 REFERENCES

Concepts and material available in the following documents may be helpful when reading this document. Visit www.microchip.com for the latest documentation.

Document	Location
LAN9352 Datasheet	Visit www.microchip.com.
AN8-13 Suggested Magnetics	http://www.microchip.com/wwwAppNotes/AppNotes.aspx?appnote=en562793
EVB-LAN9352 Evaluation Board Schematic	Visit www.microchip.com.

1.3 TERMS AND ABBREVIATIONS

EVB - Evaluation Board

DNP - Do Not Populate

100BASE-TX - 100 Mbps Fast Ethernet, IEEE802.3u Compliant

GPIO - General Purpose I/O

HBI - Host Bus Interface

SPI - Serial Peripheral Interface

I^2C - Inter-Integrated Circuit

EEE - Energy-Efficient Ethernet

SFP - Small Form-factor Pluggable

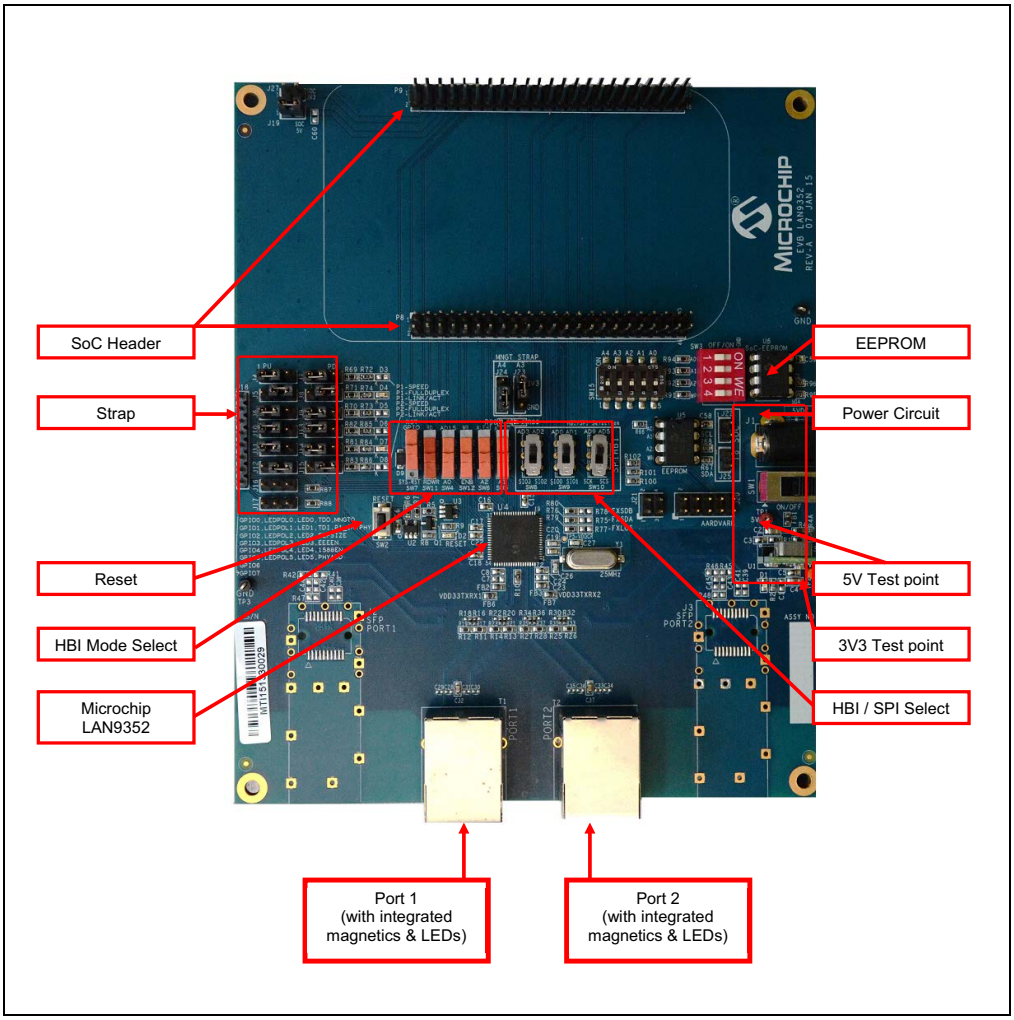
SoC - System on a Chip

NOTES:

Chapter 2. Board Details

The following sections describe the various board features, including jumpers, LEDs, test points, system connections, and switches. A top view of the EVB-LAN9352 is shown in Figure 2-1.

FIGURE 2-1: LAN9352 BOARD REV-A



2.1 POWER

DC 5V is applied through (J1) DC Socket, powered by a +5V external wall adapter. Switch (SW1) needs to be in the ON position for the 5V to reach the 3.3V regulator. Glowing of Green LED (D1) indicates successful generation of 3.3V o/p. This power is supplied to the LAN9352 and it has and internal 1.2 V regulator, which then supplies power to the internal core logic.

2.2 POWER-ON RESET

A power-on reset occurs whenever power is initially applied to the LAN9352 or if the power is removed and then reapplied to the LAN9352. This event resets all circuitry within the LAN9352. After initial power-on, the LAN9352 can be reset by pressing the reset switch (SW2). The reset LED D2 will assert (red) when the LAN9352 is in reset condition. For stability, a delay of approximately 180ms is added from the +3.3V o/p to reset release.

2.3 CLOCK

The LAN9352 requires a fixed-frequency 25MHz clock source for use by the internal clock oscillator and PLL. This is typically provided by attaching a 25MHz crystal to the OSCI and OSCO pins

Manufacturer: Cardinal Components Inc. and P/N: CSM1Z-A5B2C5-40-25.0D18-F

Chapter 3. Board Configuration

3.1 STRAP OPTIONS

The following tables describe the default settings and jumper descriptions for the EVB-LAN9352. These defaults are the recommended configurations for evaluation of the LAN9352. These settings may be changed as needed, however, any deviation from the defaults settings should be approached with care and knowledge of the schematics and datasheet. An incorrect jumper setting may disable the board.

3.1.1 GPIO Straps

The GPIO/LED Controller provides 8 configurable general purpose input/output pins, GPIO [7:0]. These pins can be individually configured to function as inputs, push-pull outputs or open drain outputs and each is capable of interrupt generation with configurable polarity. Alternatively, 6 GPIO pins can be configured as LED outputs, enabling these pins to drive Ethernet status LEDs for external indication of various attributes of the ports. All GPIOs also provide extended 1588 functionality.

Table 3-1 illustrates how the GPIO lines are multiplexed with other signals.

TABLE 3-1: GPIO STRAPS

GPIO Line	Multiplexed Signals
GPIO 0	LED0/MNGT0/TD0
GPIO 1	LED1/MNGT1/TD1
GPIO 2	LED2/E2PSIZE
GPIO 3	LED3/EEEN
GPIO 4	LED4/1588EN
GPIO 5	LED5/PHYADD

3.1.2 GPIO Header

The GPIO/LED Controller provides 8 configurable general purpose input/output pins, G

J18 is used GPIO Header for probing purpose. Table 3-2 illustrates how the GPIO lines are multiplexed with other signals.

TABLE 3-2: GPIO HEADER

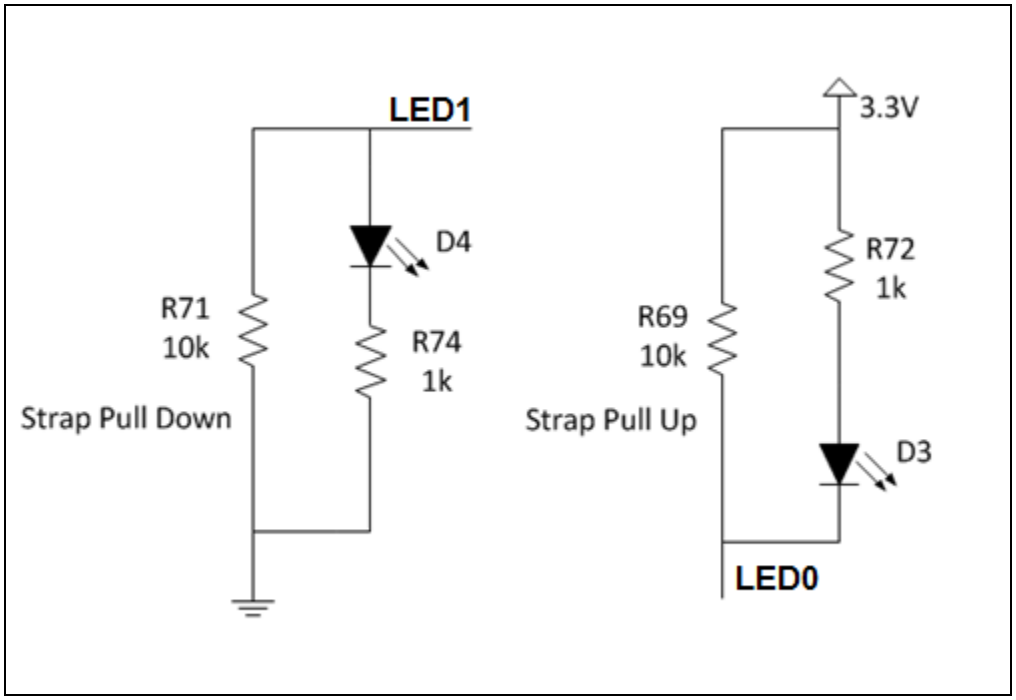
GPIO Line	Multiplexed Signals
GPIO 0	J18.1
GPIO 1	J18.2
GPIO 2	J18.3
GPIO 3	J18.4
GPIO 4	J18.5
GPIO 5	J18.6
GPIO 4	J18.7
GPIO 5	J18.8

In the context of using the GPIO signals as LED controller, the Jumpers J4-J15 (operated in pairs) are configured as below.

For example, J4 and J7 as a pair set as '0' or '1', decide whether LED0 (D3) is turned ON or OFF.

Likewise, J6 and J9 as a pair set as '0' or '1', decide whether LED1 (D4) is turned ON or OFF.

FIGURE 3-1: LED STRAP CIRCUIT



All strap values are read during power-up and on the rising edge of nRST signal. Once the strap value is set, the LAN9352 will drive the LEDs high or low for illumination according to the strap value.

3.1.2.1 GPIO/LED CONFIGURATIONS

GPIO/LED configuration straps are used to configure the LEDs and GPIOs through jumpers as shown below in Table 3-3.

TABLE 3-3: GPIO/LED CONFIGURATIONS

Header	Pin Settings	Signal Name	Strap Value	Description
J4 & J7	1-2(default)	GPIO0 /LED0	1	The LED (D3) is set as active LOW.
	2 -3		0	The LED (D3) is set as active HIGH.
J5 & J8	1-2(default)	GPIO1 /LED1	1	The LED (D4) is set as active LOW.
	2 -3		0	The LED (D4) is set as active HIGH.
J6 & J9	1-2(default)	GPIO2 /LED2	1	The LED (D5) is set as active LOW.
	2 -3		0	The LED (D5) is set as active HIGH.

TABLE 3-3: GPIO/LED CONFIGURATIONS (CONTINUED)

Header	Pin Settings	Signal Name	Strap Value	Description
J10 & J13	1-2(default)	GPIO3 /LED3	1	The LED (D6) is set as active LOW.
	2 -3		0	The LED (D6) is set as active HIGH.
J11 & J14	1-2(default)	GPIO4 /LED4	1	The LED (D7) is set as active LOW.
	2 -3		0	The LED (D7) is set as active HIGH.
J12 & J15	1-2(default)	GPIO5 /LED5	1	The LED (D8) is set as active LOW.
	2 -3		0	The LED (D8) is set as active HIGH.

3.1.2.2 HOST INTERFACE MODE STRAP SELECTION

MNGT0 strap along with MNGT1, MNGT2 and MNGT3 configures the host mode

MNGT0 and MNGT1 are multiplexed with GPIO0 and GPIO1 signals whereas MNGT3 and MNGT4 are multiplexed with address lines A3 and A4.

Table 3-4 illustrates the selection of Host mode based on the values of MNGT straps.

TABLE 3-4: MANAGEMENT STRAP SELECTION

MNGT1 J5 & J8	MNGT0 J4 & J7	MNGT3 J24	MNGT2 J23	Host Mode
0	0	X	X	SPI
0	1	0	0	HBI Multiplexed 1 Phase 8-bit
0	1	0	1	HBI Multiplexed 1 Phase 16-bit (Default)
0	1	1	0	HBI Multiplexed 2 Phase 8-bit
0	1	1	1	HBI Multiplexed 2 Phase 16-bit
1	0	X	X	HBI Indexed 8-bit
1	1	X	X	HBI Indexed 16-bit

3.1.2.3 EEPROM SIZE CONFIGURATION

The EEPROM size configuration strap (Multiplexed with GPIO2/LED2) [J6 & J9] determines the supported EEPROM size range. A low selects 1Kbits (128 x 8) through 16Kbits (2K x 8)_24C16. A high selects 32Kbits (4K x 8) through 512Kbits (64K x 8) or 4Mbits (512K x 8)_24C512 as shown below in Table 3-5.

TABLE 3-5: EEPROM SIZE CONFIGURATION

Header	Pin Settings	eeprom_size_strap Value	Description
J6 & J9	1-2 (default)	1	EEPROM size = 32K bits (4k x 8) through 512K bits (64K x 8)
	2 -3	0	EEPROM size = 1K bits (128 x 8) through 16K bits (2K x 8)

3.1.2.4 ENERGY EFFICIENT ETHERNET CONFIGURATION

EEEEN configuration strap (Multiplexed with GPIO3/LED3) is used to configure the default value of the EEE Enable 2-1 soft-straps (EEE_enable_strap_[2:1]) through jumpers as shown below in Table 3-6.

Note: "EEE_enable_strap_1" strap is used for the LAN9352 when in Port 1 internal PHY mode.

TABLE 3-6: EEEEN CONFIGURATION

Header	Pin Settings	EEE_enable_strap_[2:1] Value	Description
J10 & J13	1-2 (default)	1	EEE Enable
	2 -3	0	EEE Disable

3.1.2.5 1588 ENABLE CONFIGURATION

1588 Enable Strap (Multiplexed with GPIO4/LED4) is used to configure the default value of the 1588 Enable soft-strap (1588_enable_strap) through jumpers as shown below in Table 3-7.

TABLE 3-7: 1588 ENABLE CONFIGURATION

Header	Pin Settings	1588_enable_strap Value	Description
J11 & J14	1-2 (default)	1	1588 Enable
	2 -3	0	1588 Disable

3.1.2.6 PHY ADDRESS CONFIGURATION

PHY Address selection strap (Multiplexed with GPIO5/LED5) is used to configure the default value of the Switch PHY Address Select soft-strap (phy_addr_sel_strap) through jumpers as shown below in Table 3-8.

TABLE 3-8: PHY ADDRESSING

Header	Pin Settings	PHY_ADDR_SEL_STRAP Value	VIRTUAL PHY 0 and 1 Default Address Value	PHY A Default Address Value	PHY B Default Address Value
J12 & J15	1-2	1	1	2	3
	2-3 (default	0	0	1	2

3.1.3 GPIO 6 & GPIO 7 Input and Output Configurations

GPIO 6 & 7 configuration straps are used to configure the default input value of the GPIO 6 and 7 through jumpers as shown below in Table 3-9 and Table 3-10 respectively.

TABLE 3-9: INPUT CONFIGURATION

Header	Pin Settings	Input	Signal Name
J16	1 - 2	1	GPIO6
	2 - 3	0	
J17	1 - 2	1	GPIO7
	2 - 3	0	

TABLE 3-10: OUTPUT CONFIGURATION

Header	Pin Settings	Output	Signal Name
J16	2	Push Pull	GPIO6
J17	2	Push Pull	GPIO7

Note: By default, the jumpers settings for J16 & J17 will be OPEN.

3.1.4 External SoC

Purpose of External SoC is to provide HBI and SPI access to the LAN9352.

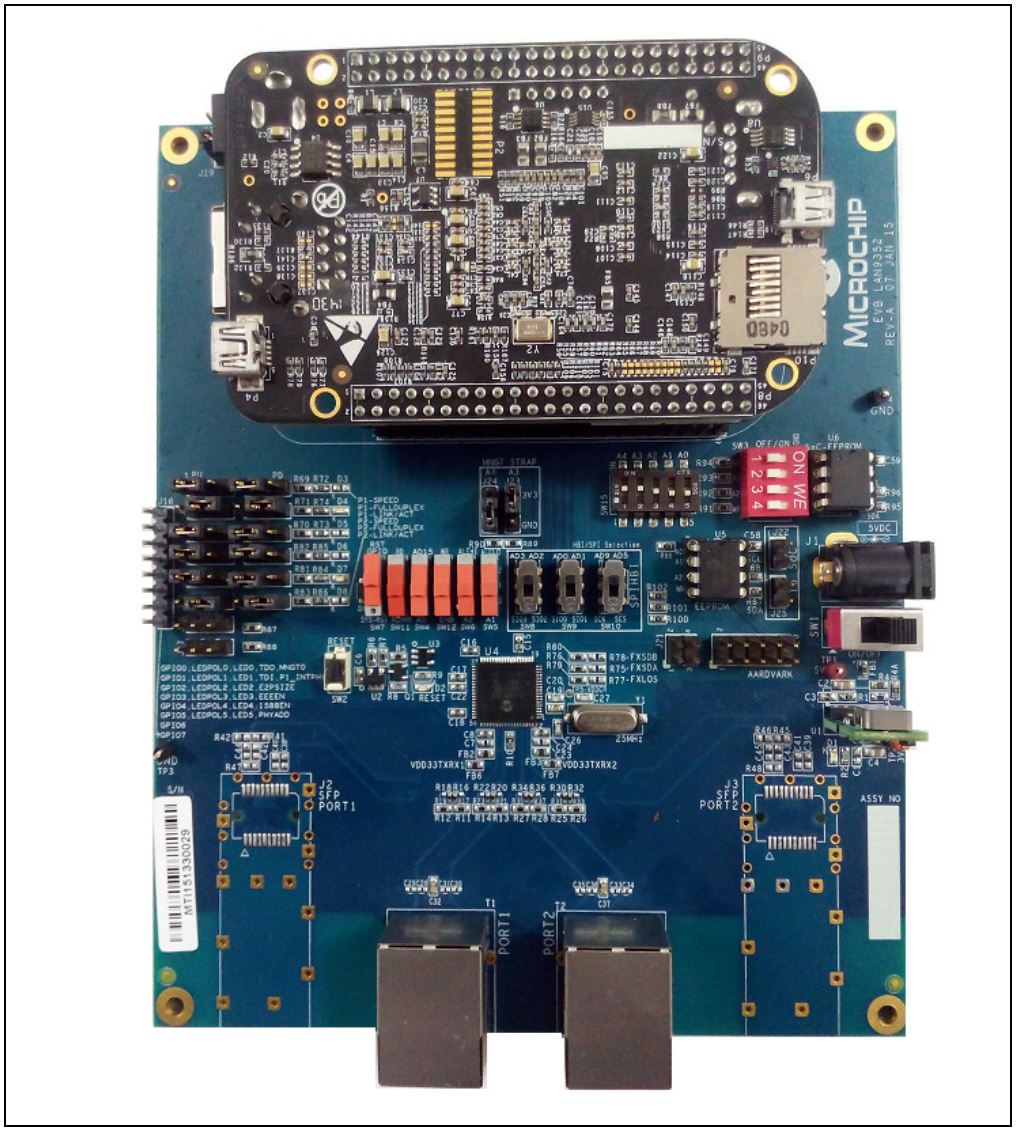
TABLE 3-11: EXTERNAL SOC SETTINGS

Header	Default Pin Settings	Signal Name
J19	1-2 (Short)	VDD_5V
J27	1-2 (Open)	VDD3V3EXP

Refer to this link for a detailed discussion on BeagleBone Black: http://www.newark.com/beagle-bone-accessories?rd=beaglebone&catalogId=15003&langId=-1&storeId=10194

Figure 3-2 shows how BeagleBone Black is mounted on EVB-LAN9352.

FIGURE 3-2: EVB-LAN9352 WITH BEAGLEBONE BLACK



3.1.5 HBI/SPI Selection

The EVB-LAN9352 supports two host interface modes of LAN9352:

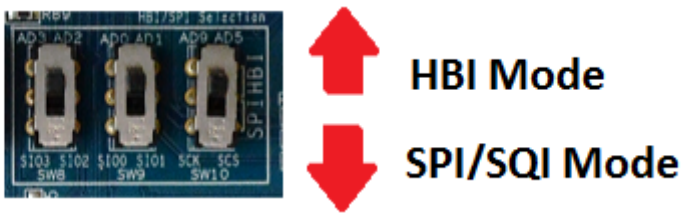
- HBI Mode (Default)
- SPI/SQI Mode

The HBI or SPI/SQI configuration is selected using the DPDT SW8 to SW10 switches.

TABLE 3-12: HBI AND SPI/SQI SWITCH CONFIGURATIONS

Switch	Description	Settings
SW8 to SW10	Up	HBI Mode (Default)
SW8 to SW10	Down	SPI/SQI Mode

FIGURE 3-3: SW8-SW10 HBI AND SPI/SQI MODE SELECTION



3.1.6 HBI Mode Selection

The LAN9352 supports various HBI modes. The HBI modes (Multiplexed Modes and Indexed Modes) can be selected using the SPST switches (P/N: 450301014042-Wurth Electronics) SW4 through SW6 and SW11 through SW12. The LAN9352 HBI signals are connected to the SoC through the switches.

3.1.6.1 MULTIPLEXED MODES

The following four HBI Multiplexed Modes are supported:

1. 8-bit Multiplexed single-phase mode
2. 16-bit Multiplexed single-phase mode
3. 8-bit Multiplexed dual-phase mode
4. 16-bit Multiplexed dual-phase mode

The BeagleBone Black will be configured by installing specific driver available from www.microchip.com. This is required to access LAN9352 through HBI Multiplexed mode.

The switch selection for Multiplexed Mode. All four Multiplexed Modes utilize the same switch positions.

FIGURE 3-4: MULTIPLEXED HBI MODE SELECTION

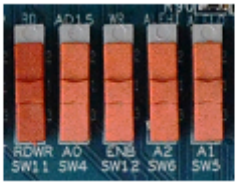


TABLE 3-13: SWITCH SELECTION FOR MULTIPLEXED MODE

Switch	Description
SW11	Down
SW4	Down
SW12	Down
SW6	Down
SW5	Down

Note: For Switches to short 1-2, knob position must be in the 1-3 position, and vice versa.

3.1.6.2 INDEXED MODE

Two Indexed modes are supported, namely 8-bit and 16-bit. The BeagleBone Black will be configured by installing specific driver available from www.microchip.com. This is required to access LAN9352 through HBI Indexed mode.

Note: In this mode. DIP switch SW15 to ON Position for PIC32 SoC and OFF Position for SoC.

FIGURE 3-5: 8-BIT INDEXED MODE SWITCH SELECTION

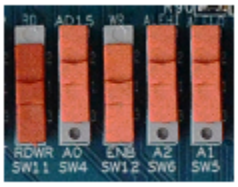


TABLE 3-14: SWITCH SELECTION FOR 8-BIT INDEXED MODE

Switch	Description
SW11	Down
SW4	Up
SW12	Down
SW6	Up
SW5	Up

Note: For Switches to short 1-2, knob position must be in the 1-3 position, and vice versa.

FIGURE 3-6: 16-BIT INDEXED MODE SWITCH SELECTION

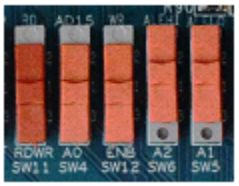


TABLE 3-15: SWITCH SELECTION FOR 16-BIT INDEXED MODE

Switch	Description
SW11	Down
SW4	Down
SW12	Down
SW6	Up
SW5	Up

Note: For Switches to short 1-2, knob position must be in the 1-3 position, and vice versa.

3.1.7 SPI/SQI Mode Selection

The LAN9352 supports SPI/SQI Mode. The SPI/SQI Mode will be selected using the DPDT SW8 to SW10 switches as shown in Figure 3-3.

3.1.8 I²C Aardvark® Header and SPI Storm Header

3.1.8.1 I²C AARDVARK HEADER

J20 connector is used for I²C Aardvark header. Respective pin details are given in Table 3-16.

TABLE 3-16: PIN NAMES FOR I²C AARDVARK HEADER

Signal Name	Pin Number
I2C2_SCL	J20.1
I2C2_SDA	J20.3
GND	J20.2 & J20.10

3.1.8.2 SPI STORM HEADER

J20+J21 connectors are used for SPI Storm header. Respective pin details are given in Table 3-17.

TABLE 3-17: PIN NAMES FOR SPI STORM HEADER

Signal Name	Pin Number
SIO1	J20.5
SCK	J20.7
SCS#	J20.9
SIO0	J20.8
SIO2	J21.3
SIO3	J21.4
GND	J20.2, J20.10, J21.1 & J21.2

3.1.9 Copper and Fiber Mode Selections

The LAN9352 supports 100BASE-TX (Copper) and 100BASE-FX (Fiber) modes. In 100BASE-FX operation, the presence of the receive signal is indicated by the external transceiver as either an open-drain, CMOS level, Loss of Signal (SFP) or a LVPECL Signal Detect (SFF).

This EVB supports 100BASE-TX (Copper) and 100BASE-FX (Fiber) in SFP mode. By default Copper Mode is active. Fiber Mode is supported as an assembly option. To select the Copper or Fiber Mode, the respective strap and signal routing resister assembly options must be configured.

Note: Vendor part number for SFP Transceiver: Finisar/FTLF1217P2

3.1.9.1 COPPER MODE

The EVB-LAN9352 is set to Copper Mode by default. Table 3-18 details the required strap resistors settings for Copper Mode operation.

TABLE 3-18: COPPER MODE STRAP RESISTORS

Resistors	Signal Names	Description
R79 (10K)	FXLOSEN	Copper twisted pair for ports A and B further determined by FXSDENA and FXSDENB
R76, R80 (10K)	FXSDA/FXSDB	Configures Port 0 and Port 1 to Copper Mode

Note: R75, R77, and R78 must not be populated (DNP).

Additionally, the signal routing resistors detailed in Table 3-19 must be assembled for Copper Mode operation.

TABLE 3-19: COPPER MODE SIGNAL ROUTING RESISTORS

Resistors	Description
R17, R19,R21, R23	Port 0 Copper mode is Enabled
R31, R33, R35, R37	Port 1 Copper mode is Enabled

Note: R16, R18, R20, R22, R30, R32, R34, and R36 (0402 package) must not be populated (DNP).

3.1.9.2 FIBER MODE

The LAN9352 supports SFP type 100BASE-FX mode. To enable Fiber Mode, the respective strap and signal routing resisters must be configured.

Note: Copper Mode related resistors must be DNP while Fiber Mode is active (refer to **Section 3.1.9.1 "Copper Mode"**).

Table 3-20 details the required strap resistor settings for Fiber Mode operation.

TABLE 3-20: FIBER MODE SIGNAL ROUTING RESISTORS

Resistors	Description
R16, R18, R20, R22	Port 0 Fiber mode is Enabled
R30, R32, R34, R36	Port 1 Fiber mode is Enabled

Note: R17, R19, R21, R23, R31, R33, R35, and R37 (0402 package) must not be populated (DNP).

3.1.9.3 FX-LOS FIBER MODE STRAP

FX-LOS strap details are shown in Table 3-21. These strap settings determine if the ports are to operate in FX-LOS Fiber Mode or FX-SD/Copper Mode.

TABLE 3-21: FX-LOS MODE STRAP SETTINGS

R77 (10K)	R79 (10K)	Reference Voltage (v)	Function
Populate	DNP	3.3	A level above 2V selects FX-LOS for Port 0 and Port 1
Populate	Populate	1.5	A level of 1.5V selects FX-LOS for Port 0 and FX-SD / Copper twisted pair for Port 1, further determined by FXSDB
DNP	Populate	0 (Default)	A level of 0V selects FX-SD / Copper twisted pair for Ports 0 and 1, further determined by FXSDA, FXSDB

Note: The above strap details describe the LAN9352 function. This EVB does not support SFF Fiber Mode. Therefore, FX-SD related straps are not applicable.

3.2 LEDS

LED details are shown in Table 3-22.

TABLE 3-22: LEDS

Reference	Color	Indication
D1	Green	3.3V Power active
D2	Red	LAN9352 is in reset condition

3.3 TEST POINTS

Test points are shown in Table 3-23.

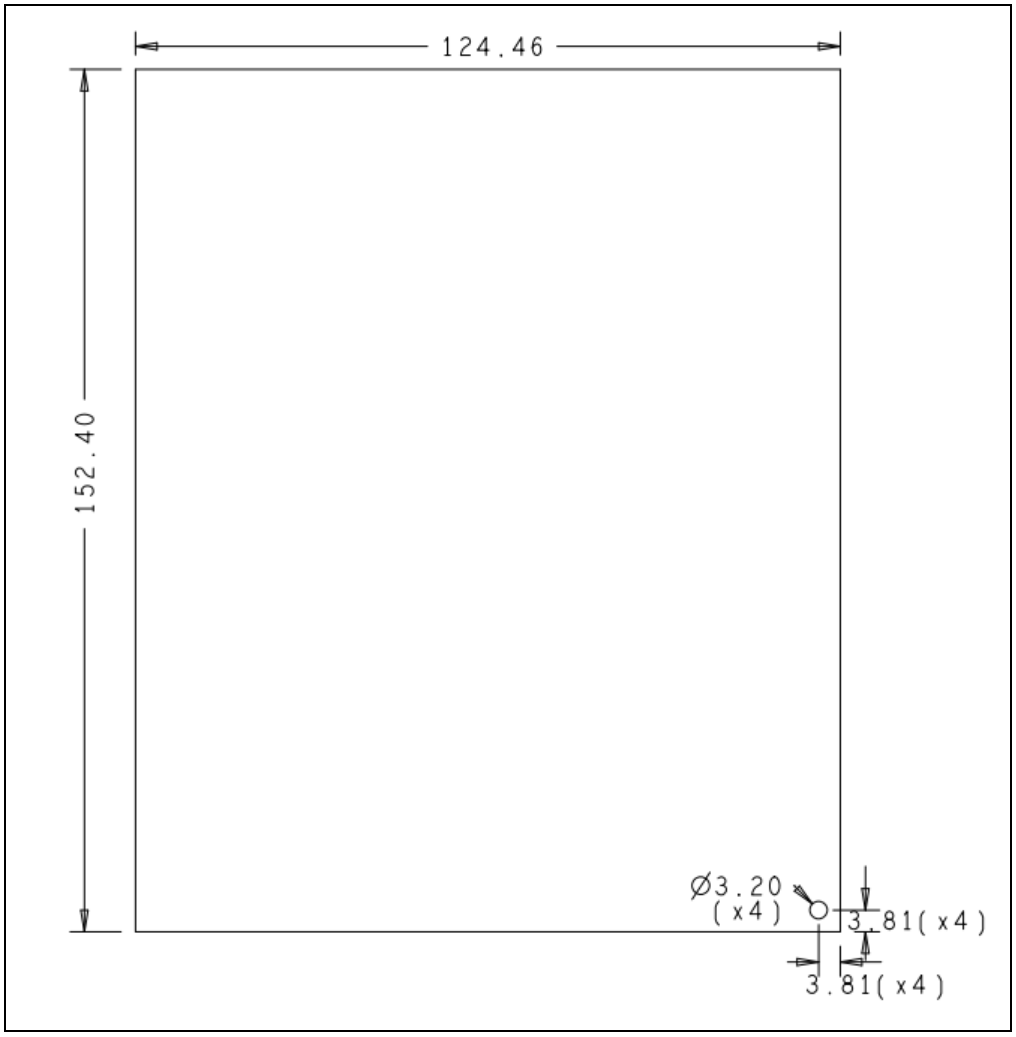
TABLE 3-23: TEST POINTS

Test Points	Description	Connection
TP1	Single pin populated 5V	5V_EXT
TP2	Single pin populated 3V3	3V3
TP3	Single pin populated GND	GND
TP4	Single pin populated GND	GND
TP5	Single pin unpopulated VDDCR	VDDCR/1.2V

3.4 MECHANICALS

Figure 3-7 details for EVB-LAN9352 mechanical dimensions. Dimensions are in mm.

FIGURE 3-7: EVB-LAN9352 MECHANICAL DIMENSIONS

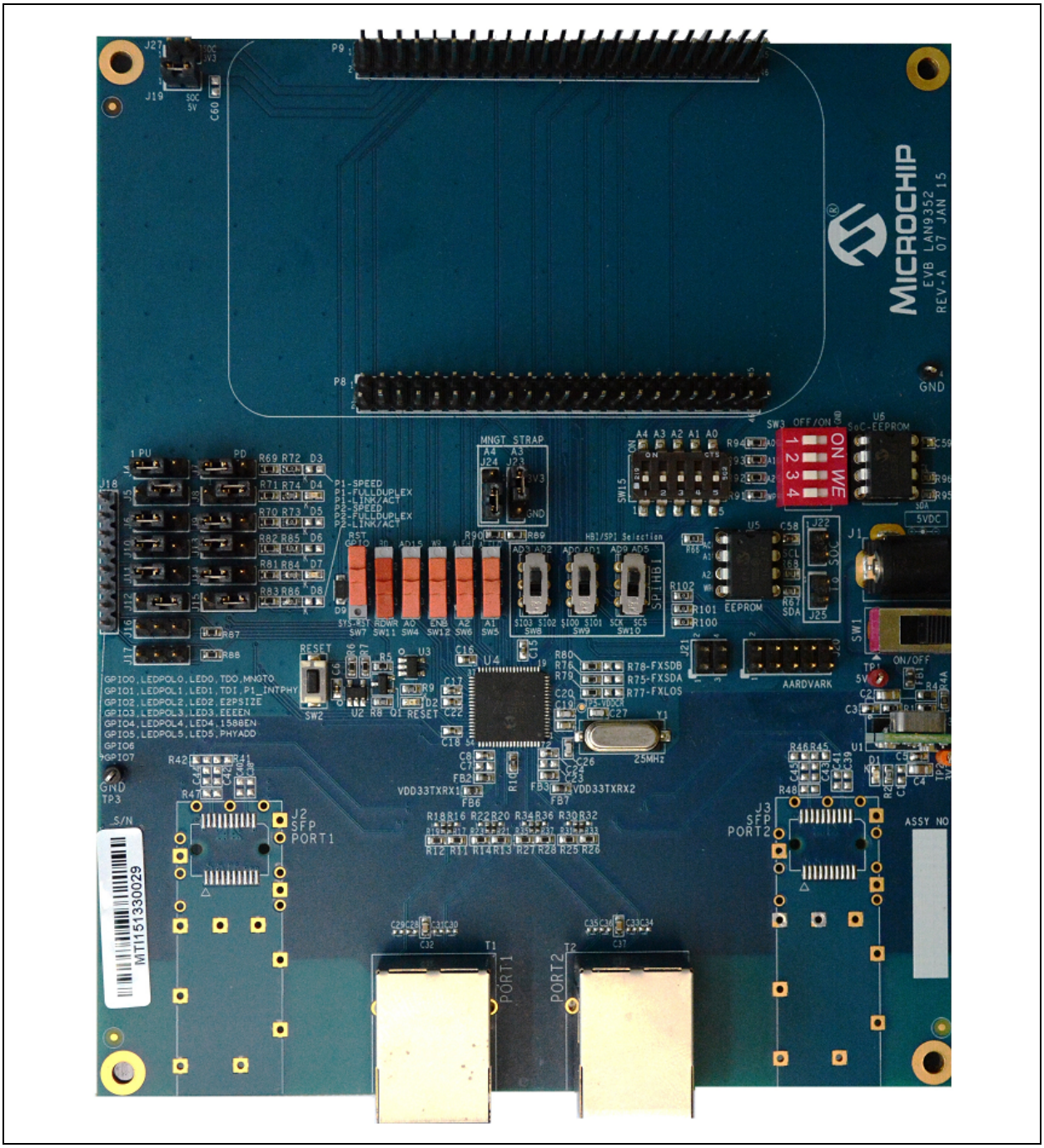


Appendix A. EVB-LAN9352 Evaluation Board

A.1 INTRODUCTION

This appendix shows the EVB-LAN9352 Evaluation Board.

FIGURE A-1: EVB-LAN9352 EVALUATION BOARD



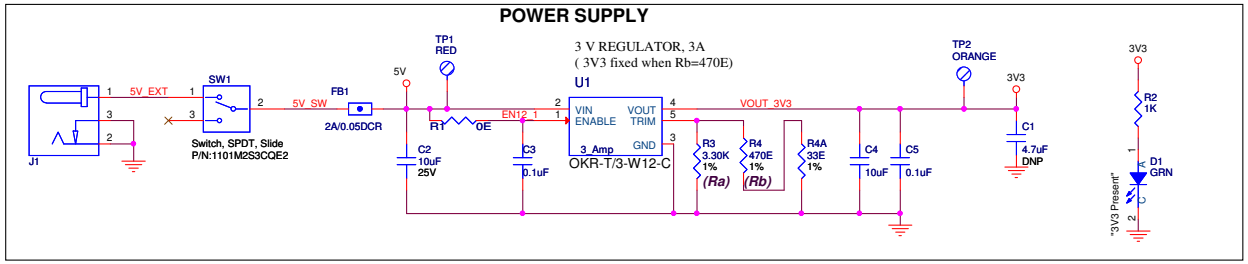
NOTES:

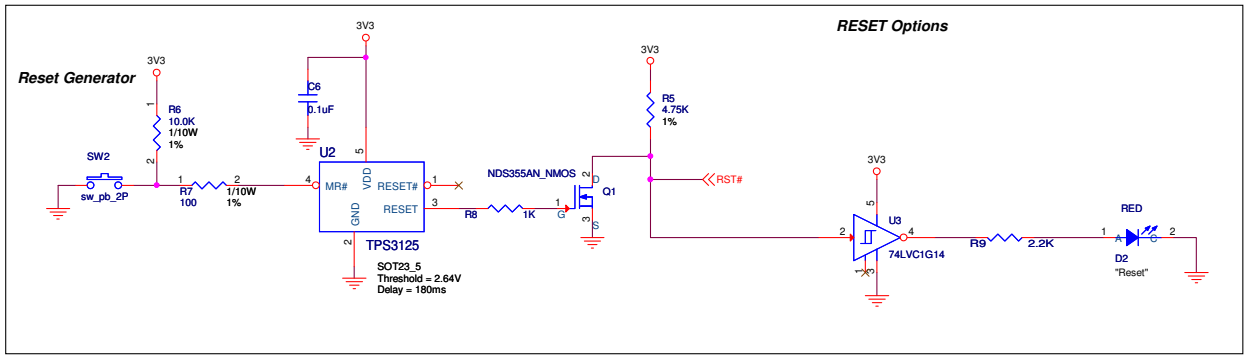
Appendix B. EVB-LAN9352 Evaluation Board Schematics

B.1 INTRODUCTION

This appendix shows the EVB-LAN9352 Evaluation Board Schematics.

FIGURE B-1: POWER SUPPLY & RST





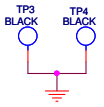


FIGURE B-2: LAN9352 (PART1)

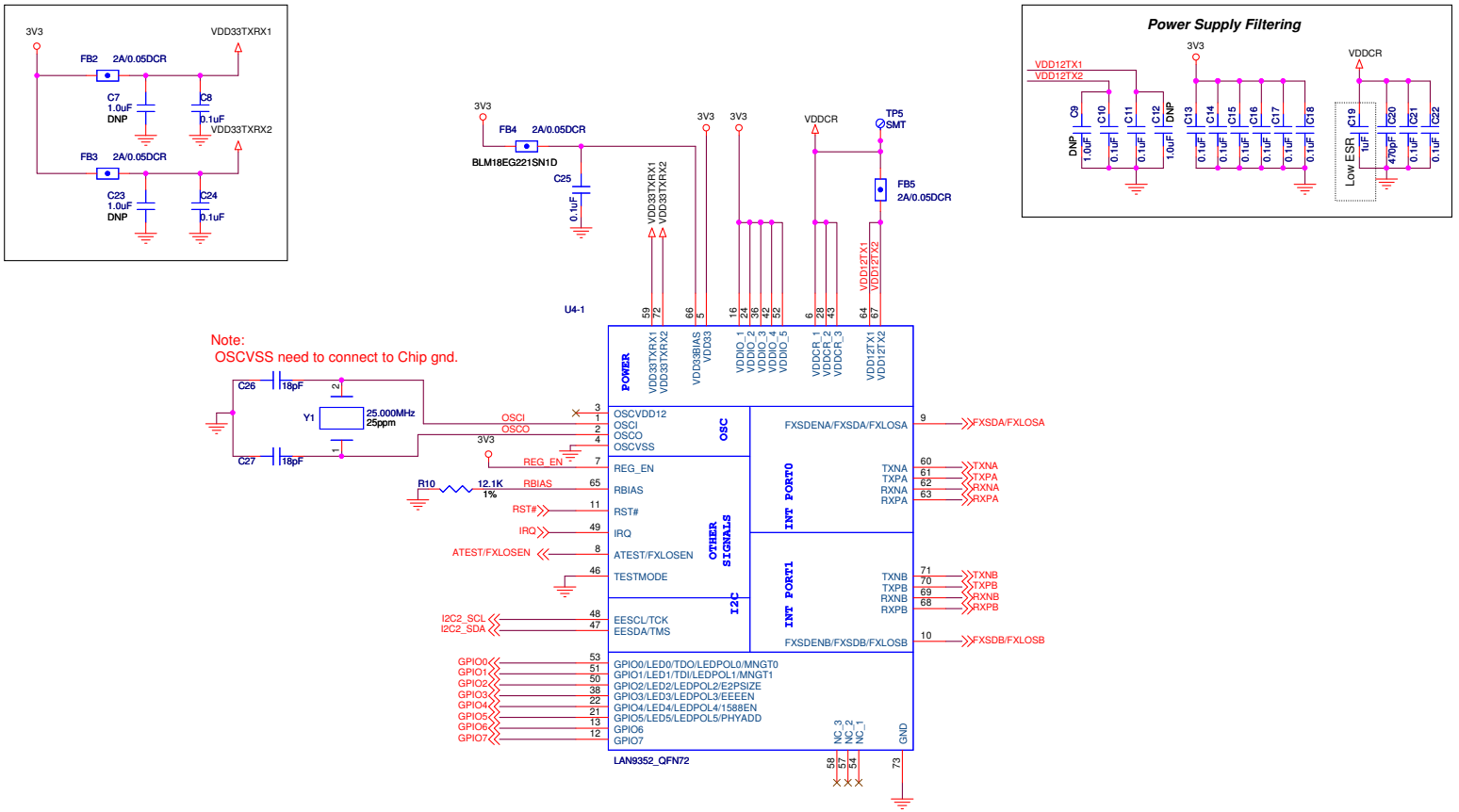


FIGURE B-3: COPPER MODE INTERFACE

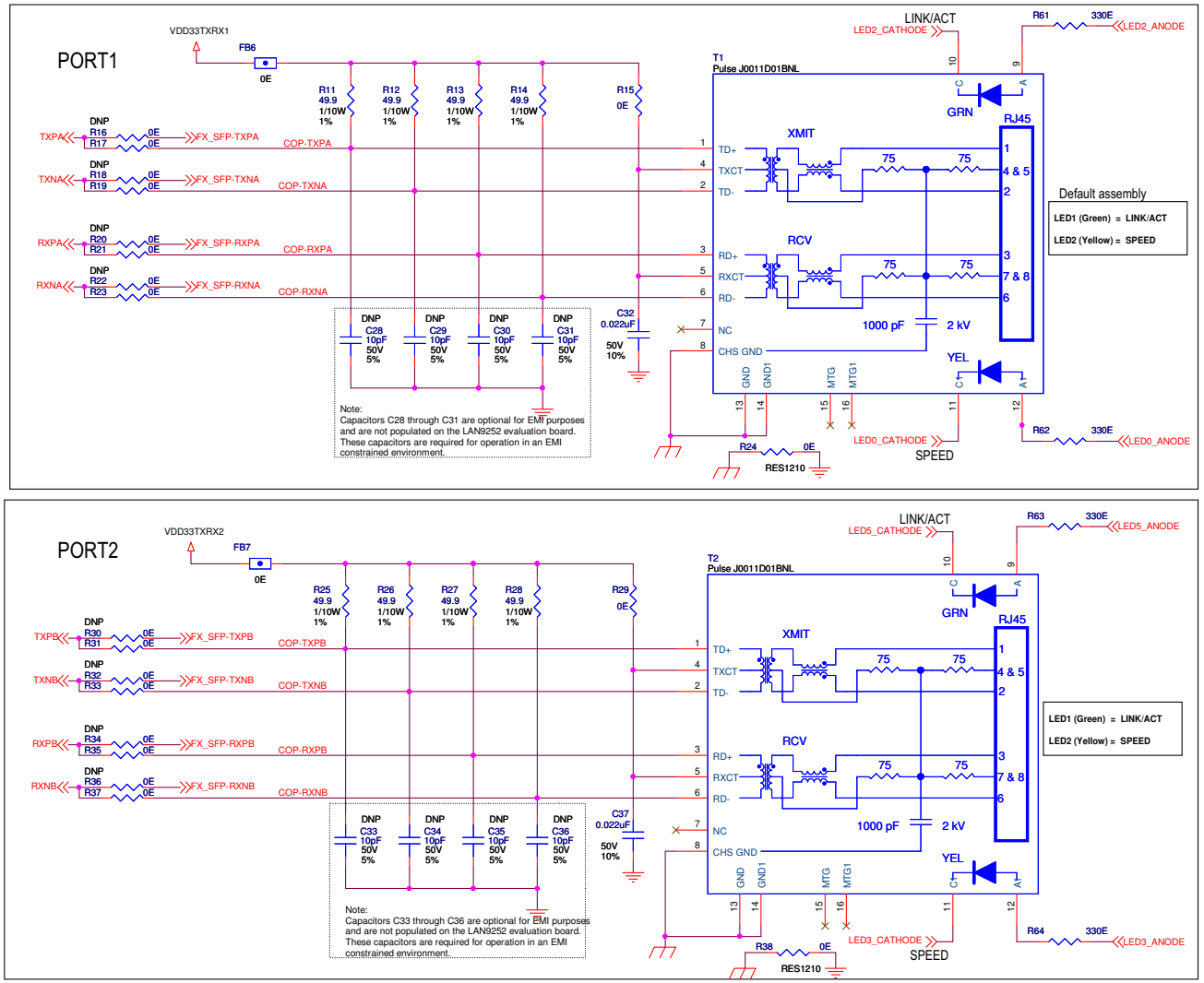


FIGURE B-4: SFP INTERFACE

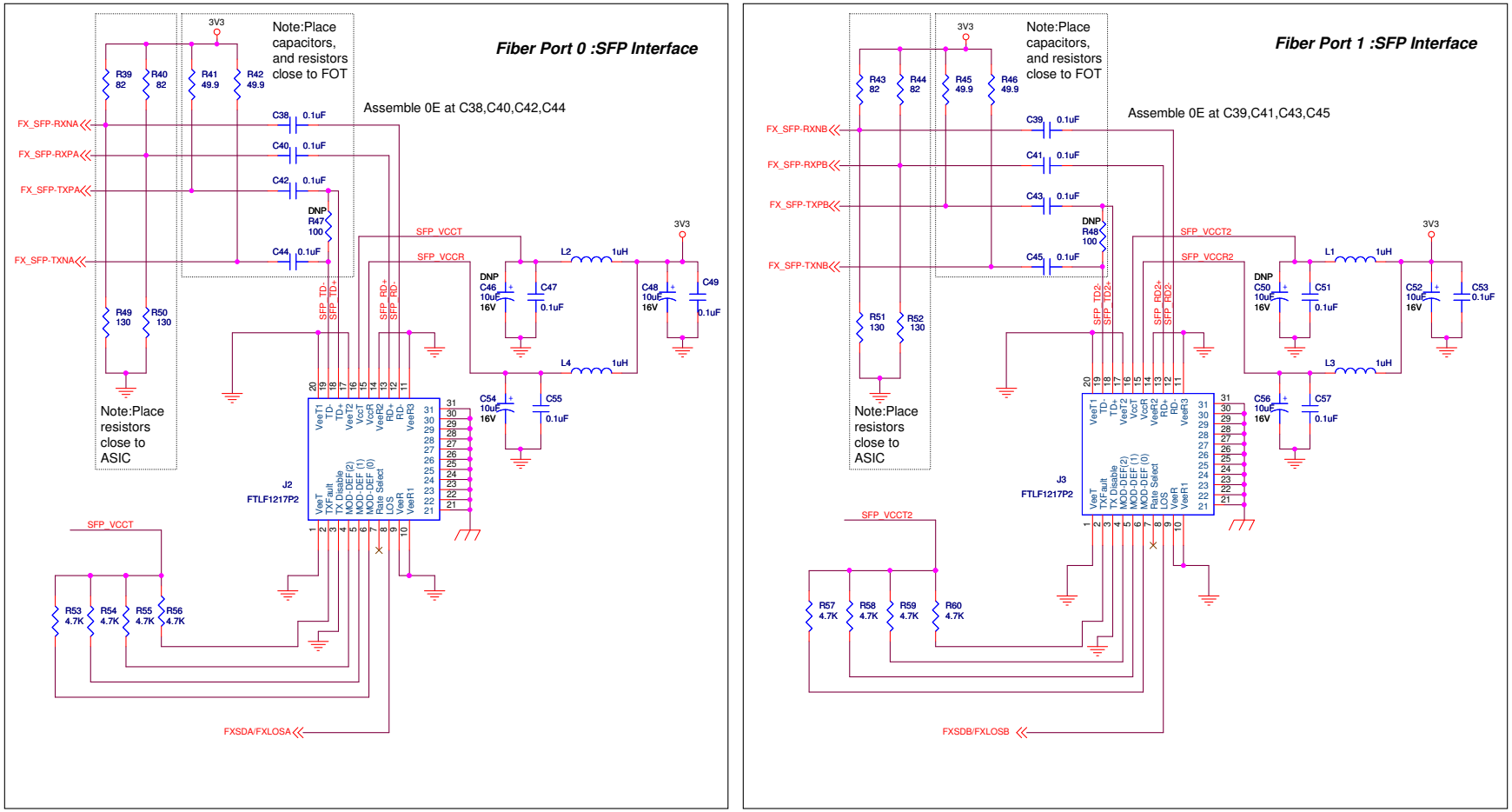
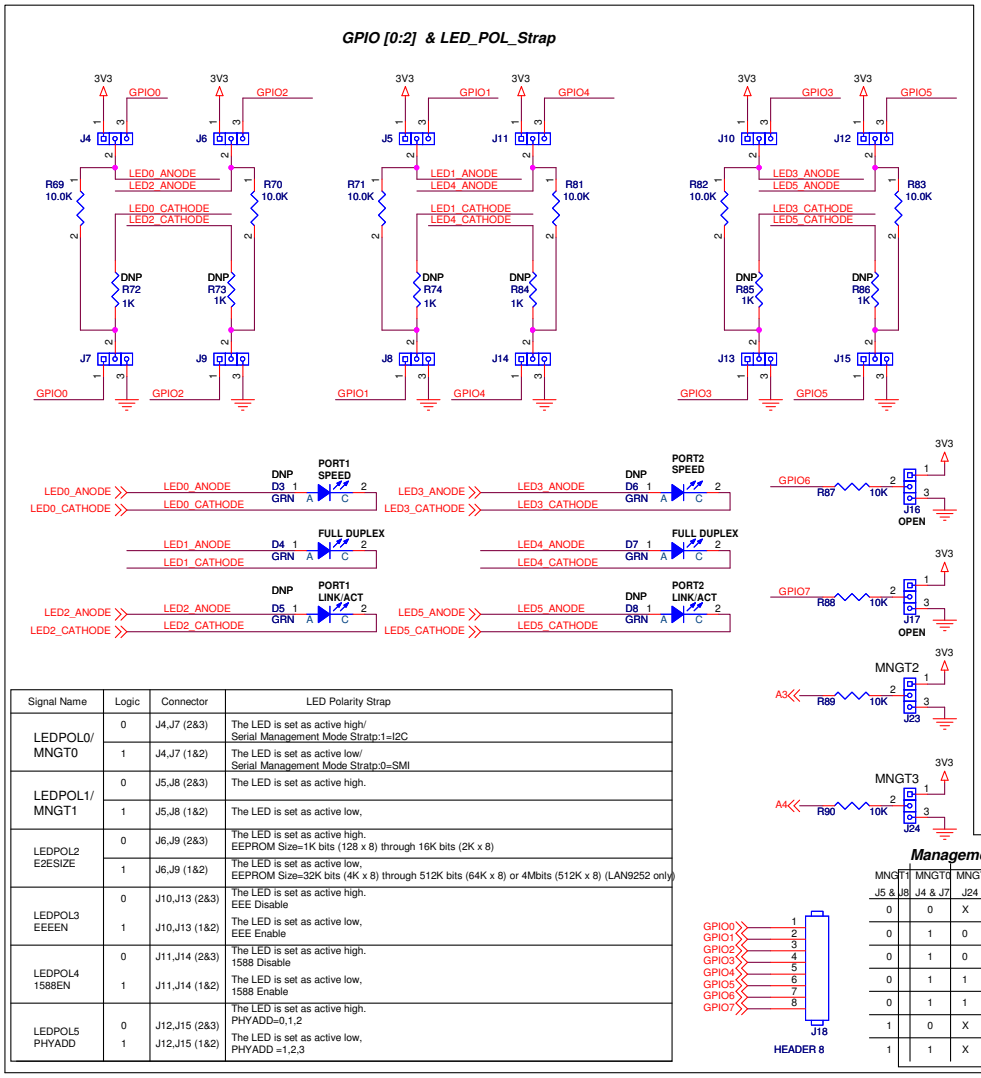
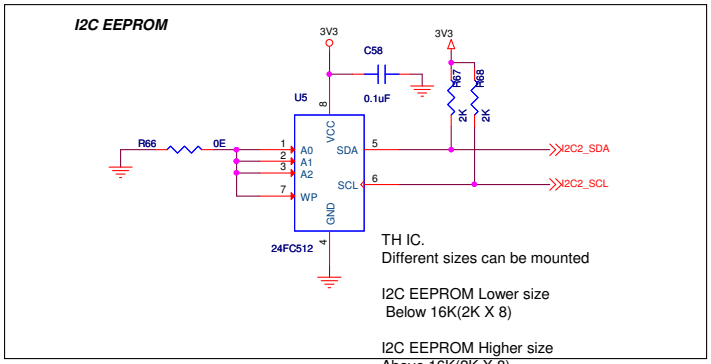
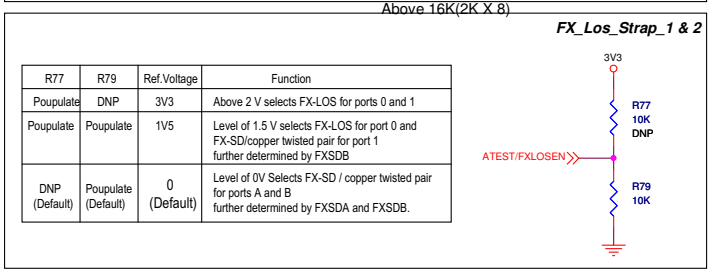


FIGURE B-5: STRAP, GPIO, I²C & FX-LOS

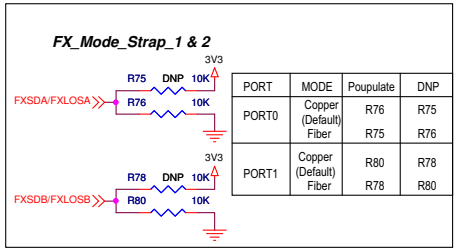


Signal Name	Logic	Connector	LED Polarity Strap
LEDPOL0/ MNGT0	0	J4,J7 (2&3)	The LED is set as active high/ Serial Management Mode Stratp:1=I2C
	1	J4,J7 (1&2)	The LED is set as active low/ Serial Management Mode Stratp:0=SMI
LEDPOL1/ MNGT1	0	J5,J8 (2&3)	The LED is set as active high.
	1	J5,J8 (1&2)	The LED is set as active low,
LEDPOL2 E2ESIZE	0	J6,J9 (2&3)	The LED is set as active high. EEPROM Size=1K bits (128 x 8) through 16K bits (2K x 8)
	1	J6,J9 (1&2)	The LED is set as active low, EEPROM Size=32K bits (4K x 8) through 512K bits (64K x 8) or 4Mbits (512K x 8) (LAN9252 only)
LEDPOL3 EEEEN	0	J10,J13 (2&3)	The LED is set as active high. EEE Disable
	1	J10,J13 (1&2)	The LED is set as active low, EEE Enable
LEDPOL4 1588EN	0	J11,J14 (2&3)	The LED is set as active high. 1588 Disable
	1	J11,J14 (1&2)	The LED is set as active low, 1588 Enable
LEDPOL5 PHYADD	0	J12,J15 (2&3)	The LED is set as active high. PHYADD=0,1,2
	1	J12,J15 (1&2)	The LED is set as active low, PHYADD =1,2,3





R77	R79	Ref.Voltage	Function
Poupulate	DNP	3V3	Above 2 V selects FX-LOS for ports 0 and 1
Poupulate	Poupulate	1V5	Level of 1.5 V selects FX-LOS for port 0 and FX-SD/copper twisted pair for port 1 further determined by FXSDB
DNP (Default)	Poupulate (Default)	0 (Default)	Level of 0V Selects FX-SD / copper twisted pair for ports A and B further determined by FXSDA and FXSDB.

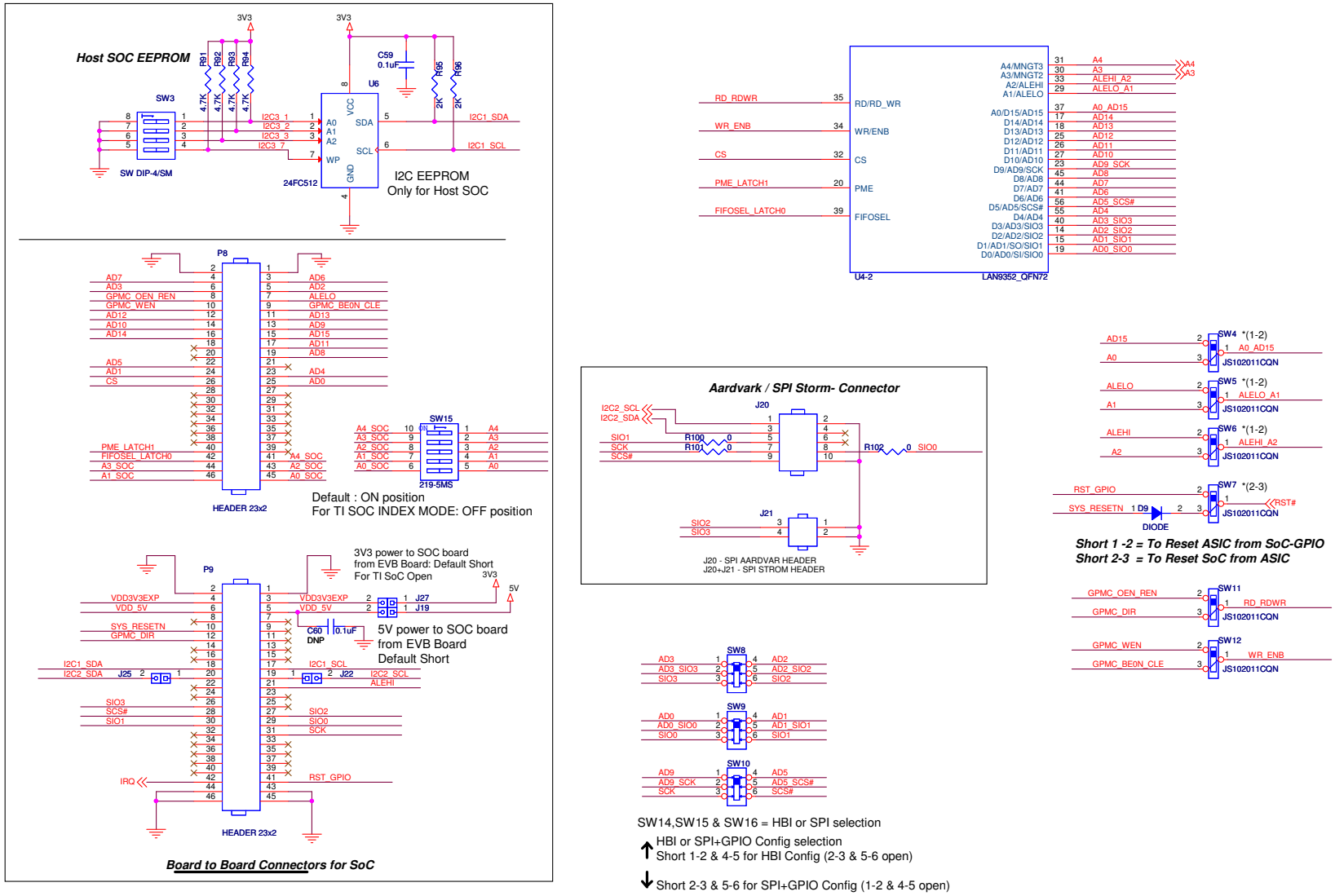


PORT	MODE	Poupulate	DNP
PORT0	Copper (Default)	R76	R75
	Fiber	R75	R76
PORT1	Copper (Default)	R80	R78
	Fiber	R78	R80

Management Strap Selection

MNGT1	MNGT0	MNGT3	MNGT2	HOST MODE
J5 & J8	J4 & J7	J24	J23	
0	0	X	X	SPI
0	1	0	0	HBI Multiplexed 1 Phase 8-bit
0	1	0	1	HBI Multiplexed 1 Phase 16-bit (Default)
0	1	1	0	HBI Multiplexed 2 Phase 8-bit
0	1	1	1	HBI Multiplexed 2 Phase 16-bit
1	0	X	X	HBI Indexed 8-bit
1	1	X	X	HBI Indexed 16-bit

FIGURE B-6: LAN9352 (PART2)



NOTES:

Appendix C. Bill of Materials (BOM)

C.1 INTRODUCTION

This appendix includes the EVB-LAN9352 Evaluation Board Bill of Materials (BOM).

TABLE C-1: EVB-LAN9352 EVALUATION BOARD BILL OF MATERIALS

Item	Qty	Reference	Part	PCB Footprint	DNP	Manufacturer	Manufacturer Part Number	Notes
2	2	C2,C4	10uF	CAP0805	No	Murata	GRM21BR61E106-KA73L	
3	18	C3,C5,C6,C8,C10,C11,C13,C14,C15,C16,C17,C18,C21, C22,C24,C25,C58,C59	0.1uF	CAP0603	No	Murata	GRM155R61E104-KA7D	
5	1	C19	1uF	CAP0603	No	Murata	GRM188R61C105-KA93D	
6	1	C20	470pF	CAP0603	No	Murata	GRM033R71E471-KA01D	
7	2	C26,C27	18pF	CAP0603	No	Murata	GRM1885C1H180-JA01D	
9	2	C32,C37	0.022uF	CAP0603	No	Kemet	C0603C223K5RACTU	
12	3	D1,D4,D7	GRN	LED0603	No	Wurth electronics	150 060 GS7 500 0	
13	1	D2	RED	LED0603	No	Wurth electronics	150 060 RS7 500 0	
15	1	D9	DIODE	SOD123	No	Micro Commercial Co	1N4148W-TP	
16	7	FB1,FB2,FB3,FB4,FB5	2A/0.05DCR	RES0603	No	Murata	BLM18EG221SN1D	
17	1	J1	SKT_P-WR_2R0mm_4A_THRU_RA	th_conn_pwr-jack_dc-210_rt	No	Cui Stack	PJ-002AH	
19	16	J4,J5,J6,J7,J8,J9,J10,J11,J12,J13,J14,J15,J16,J17,J23, J24	HDR_1x3	TH_CONN_1X3P	No	FCI	68000-103HLF	
20	1	J18	HEADER 8	TH_CONN_1X8P	No	FCI	68000-108HLF	
21	4	J19,J22,J25,J27	CONN_2P	th_conn_1x2p	No	FCI	68000-102HLF	
22	1	J20	HEADER 5X2	TH_CONN_2X5P	No	FCI	67997-210HLF	
23	1	J21	HEADER 2X2	TH_CONN_2X2P	No	FCI	67997-204HLF	
25	2	P8,P9	HEADER 23x2	TH_CON-N_2X23P_F	No	FCI	67996-8 46 150 030 LF	
26	1	Q1	NDS355AN_NMOS	sot23-NDS	No	Fairchild	NDS355AN	
27	9	R1,R15,R29,R66,R100,R101,R102,FB6,FB7	0E	RES0603	No	Panasonic	ERJ-3GEY0R00V	
28	2	R2,R8	1K	RES0603	No	Panasonic	ERJ-3GEYJ102V	
29	1	R3	3.30K	RES0603	No	Yageo America	9C06031A3301FKHFT	

TABLE C-1: EVB-LAN9352 EVALUATION BOARD BILL OF MATERIALS (CONTINUED)

Item	Qty	Reference	Part	PCB Footprint	DNP	Manufacturer	Manufacturer Part Number	Notes
30	1	R4A	33E	RES0603	No	BOURNS	CR0603-FX-33R0ELF	
31	1	R4	470E	RES0603	No	BOURNS	CR0603-FX-4700ELF	
32	1	R5	4.75K	RES0603	No	Panasonic	ERJ-3EKF4751V	
33	14	R6,R69,R70,R71,R81,R82,R83,R76,R79,R80,R87,R88,R89,R90	10.0K	RES0603	No	Panasonic	ERJ-3EKF1002V	
34	1	R7	100E	RES0603	No	Panasonic	ERJ-3EKF1000V	
35	1	R9	2.2K	RES0603	No	Panasonic	ERJ-3GEYJ222V	
36	1	R10	12.1K	RES0603	No	Rohm	MCR01MZPF1202	
37	8	R11,R12,R13,R14,R25,R26,R27,R28	49.9E	RES0603	No	Yageo America	9C06031A49R9FKHFT	
40	8	R17,R19,R21,R23,R31,R33,R35,R37	0E	RES0402	No	Panasonic	ERJ-2GE0R00X	
41	2	R24,R38	0E	RES1210	No	Vishay	CRCW12100000Z0EA	
47	4	R61,R62,R63,R64	330E	RES0603	No	Panasonic	ERJ-3GEYJ331V	
48	4	R67,R68,R95,R96	2K	RES0603	No	Panasonic	ERJ-3GEYJ202V	
53	4	R91,R92,R93,R94	4.7K	RES0603	No	Panasonic	ERJ-3EKF4701V	
55	1	SW1	SW-SPDT-SLIDE	sw_ck_1101m2s3cqe2	No	C&K	1101M2S3CQE2	
56	1	SW2	sw_pb_2P	sw_pb_2P	No	Panasonic	EVQ-PJU04K	
57	1	SW3	SW DIP-4/SM	TH_SW_DIP4	No	Wurth electronics	418117270904	
58	6	SW4,SW5,SW6,SW7,SW11,SW12	JS102011CQN	TH_SW_SP-ST_3P_10x2p5	No	Wurth electronics	450301014042	
59	3	SW8,SW9,SW10	JS202011CQN	TH_SW_DPDT_6P	No	C&K	JS202011CQN	
60	1	SW15	219-5MS	SW_DIP_5P-219-5MST	No	CTS Electrocompo-nents	219-5MST	
61	1	TP1	RED	TH_TP_60D40	No	Keystone	5000	
62	1	TP2	ORANGE	TH_TP_60D40	No	Keystone	5003	
63	2	TP3,TP4	BLACK	TH_TP_60D40	No	Keystone	5001	
65	2	T1,T2	Pulse - J0011D01BNL	th_conn_-pulse_rj45_j0026	No	Pulse Electronics	J0011D01BNL	
66	1	U1	3_Amp	TH_DC-DC_VERT_5PIN_P67	No	Murata	OKR-T/3-W12-C	
67	1	U2	TPS3125	SOT23_5	No	TI	TPS3125L30DBVR	

TABLE C-1: EVB-LAN9352 EVALUATION BOARD BILL OF MATERIALS (CONTINUED)

Item	Qty	Reference	Part	PCB Footprint	DNP	Manufacturer	Manufacturer Part Number	Notes
68	1	U3	74LVC1G14	SOT23_5	No	TI	SN74L VCIG14DBVR	
69	1	U4	LAN9352_QFN72	ic_qfn72	No	Microchip	LAN9352	
70	2	U5,U6	24FC512	IC_DIP8_300	No	Microchip	24FC512-I/P	
71	1	Y1	25.000MHz	XTAL_HCM49	No	Cardinal Components Inc.	CSM1Z-A5B2C5-40 -25.0D18-F	

TABLE C-2: MECHANICAL COMPONENTS

Item	Qty	Reference	Part	PCB Footprint	DNP	Manufacturer	Manufacturer Part Number	Notes
1	4	Footrest				3M	SJ61A1	Assembly instruction will be given
2	15	"Shunt (for jumpers)"				3M	969102-0000-DA	
3	1	Microchip Box				Microchip		
4	1	Product sticker (4.5X1.5 cm)				avalon		
5	1	ESD sticker				avalon		

TABLE C-3: DO NOT POPULATE (DNP) COMPONENTS

Item	Qty	Reference	Part	PCB Footprint	DNP	Manufacturer	Manufacturer Part Number	Notes
1	1	C1	4.7uF	CAP0603	DNP			
4	4	C7,C9,C12,C23	1.0uF	CAP0603	DNP			
8	8	C28,C29,C30,C31,C33,C34,C35,C36	10pF	CAP0402	DNP			
10	15	C38,C39,C40,C41,C42,C43,C44,C45,C47,C49,C51,C53 ,C55,C57,C60	0.1uF	CAP0603	DNP			
11	6	C46,C48,C50,C52,C54,C56	10uF	CAP_B_3528	DNP			
14	4	D3,D5,D6,D8	GRN	LED0603	DNP			
18	2	J2,J3	FTLF1217P2	CONN_FX_SF-P_FTLF1217P2	DNP			
24	4	L1,L2,L3,L4	1uH	L0805	DNP			
39	8	R16,R18,R20,R22,R30,R32,R34,R36	0E	RES0402	DNP			
42	4	R39,R40,R43,R44	82E	RES0603	DNP			
43	4	R41,R42,R45,R46	49.9E	RES0603	DNP			
44	2	R47,R48	100E	RES0603	DNP			
45	4	R49,R50,R51,R52	130E	RES0603	DNP			

TABLE C-3: DO NOT POPULATE (DNP) COMPONENTS (CONTINUED)

Item	Qty	Reference	Part	PCB Footprint	DNP	Manufacturer	Manufacturer Part Number	Notes
46	8	R53,R54,R55,R56,R57,R58,R59,R60	4.7K	RES0603	DNP			
51	3	R75,R77,R78	10K	RES0603	DNP			
64	1	TP5	SMT	tp-smd40	DNP			

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China - Xian
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China - Zhuhai
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India - Bangalore
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India - Pune
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Japan - Tokyo
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Korea - Daegu
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Fax: 82-53-744-4302

Korea - Seoul
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Fax: 82-2-558-5932 or
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Malaysia - Kuala Lumpur
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Fax: 60-3-6201-9859

Malaysia - Penang
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Philippines - Manila
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