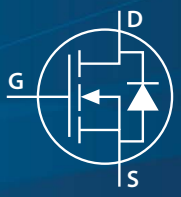
EPC8002 – Enhancement Mode Power Transistor

V_{DS}, 65 V
$R_{DS(on)}$, 480 mΩ
I_D, 2 A



EFFICIENT POWER CONVERSION

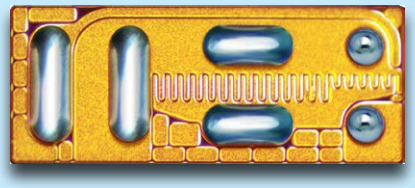
RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	65	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	78	
I_D	Continuous (T_A = 25°C, $R_{\theta JA}$ = 36°C/W)	2	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	2	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	–4	
T_J	Operating Temperature	–40 to 150	°C
T_{STG}	Storage Temperature	–40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	8.2	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	16	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	82	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details



EPC8002 eGaN FETs are supplied only in passivated die form with solder bars
Die Size: 2.1 x 0.85 mm

Applications

- Ultra High Speed DC-DC Conversion
- RF Envelope Tracking
- Wireless Power Transfer
- Game Console and Industrial Movement Sensing (Lidar)

Benefits

- Ultra High Efficiency
- Ultra Low $R_{DS(on)}$
- Ultra Low Q_G
- Ultra Small Footprint

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 125 µA	65			V
I_{DSS}	Drain-Source Leakage	V_{DS} = 52 V, V_{GS} = 0 V		20	100	µA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.1	1	mA
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		20	100	µA
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 0.1 mA	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 0.5 A		380	480	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.4 A, V_{GS} = 0 V		2.6		V

Specifications are with substrate connected to source where applicable.

Dynamic Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance	V_{DS} = 32.5 V, V_{GS} = 0 V		20	24	pF
C_{RSS}	Reverse Transfer Capacitance			0.12	0.18	
C_{OSS}	Output Capacitance			6.7	10	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 32.5 V, V_{GS} = 0 V		8.9		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			10		
R_G	Gate Resistance			0.3		Ω
Q_G	Total Gate Charge	V_{DS} = 32.5 V, V_{GS} = 5 V, I_D = 0.5 A		133	167	pC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 32.5 V, I_D = 0.5 A		57		
Q_{GD}	Gate-to-Drain Charge			15	26	
$Q_{G(TH)}$	Gate Charge at Threshold			46		
Q_{OSS}	Output Charge	V_{DS} = 32.5 V, V_{GS} = 0 V		334	500	
Q_{RR}	Source-Drain Recovery Charge			0		

Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BVDSS.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BVDSS.

Figure 1: Typical Output Characteristics at 25°C

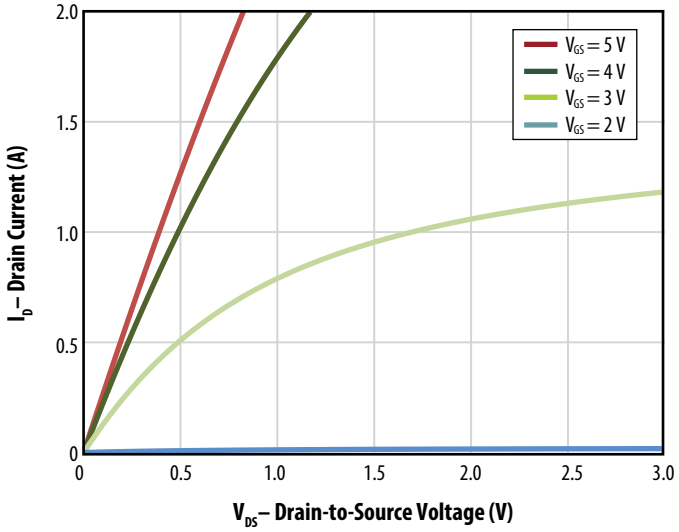


Figure 2: Transfer Characteristics

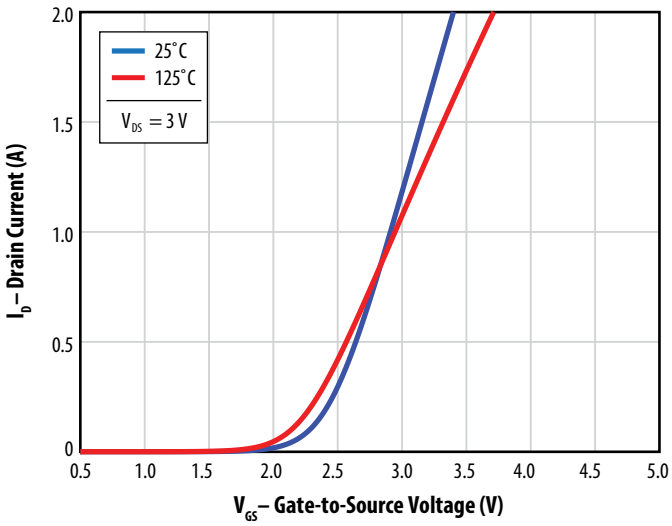


Figure 3: $R_{DS(on)}$ vs V_{GS} for Various Drain Currents

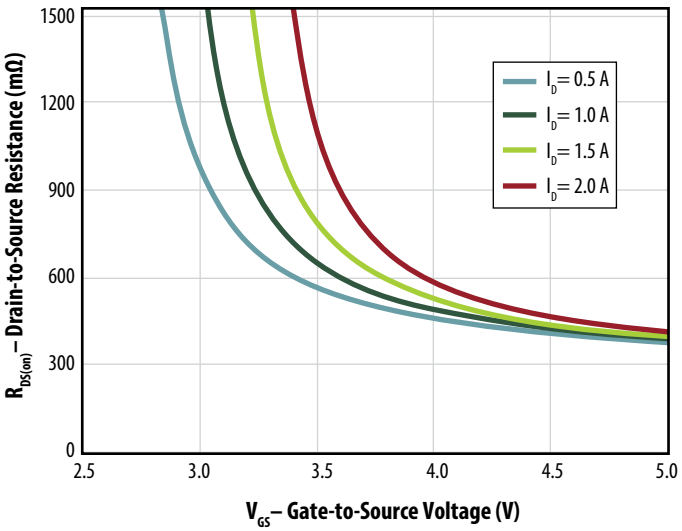


Figure 4: $R_{DS(on)}$ vs V_{GS} for Various Temperatures

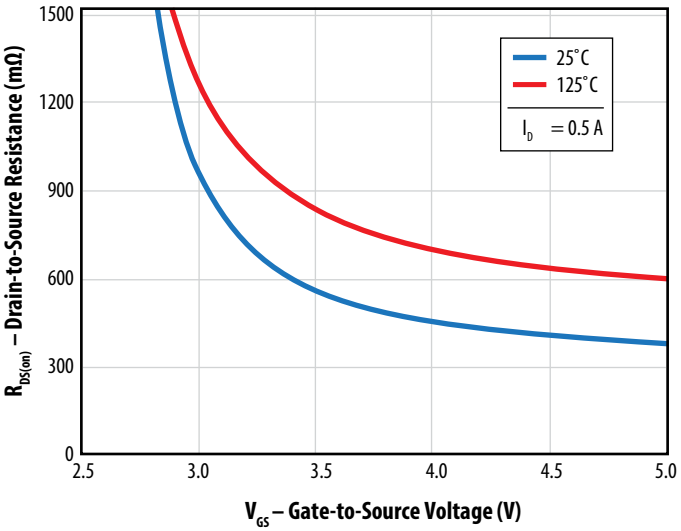


Figure 5: Capacitance (Linear Scale)

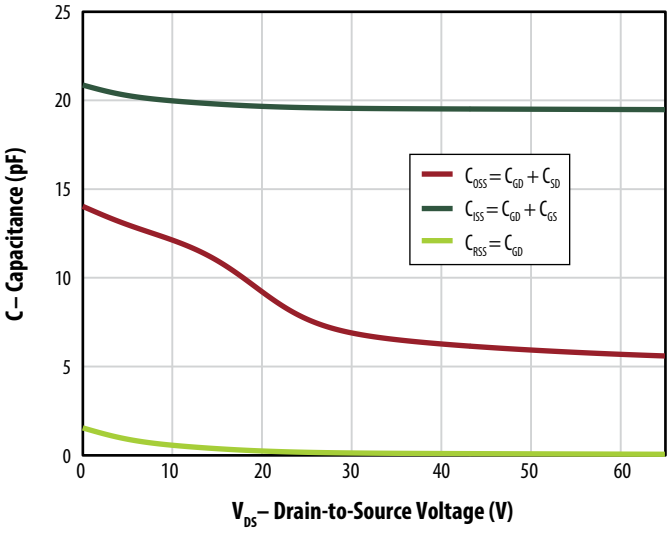


Figure 5A: Capacitance (Log Scale)

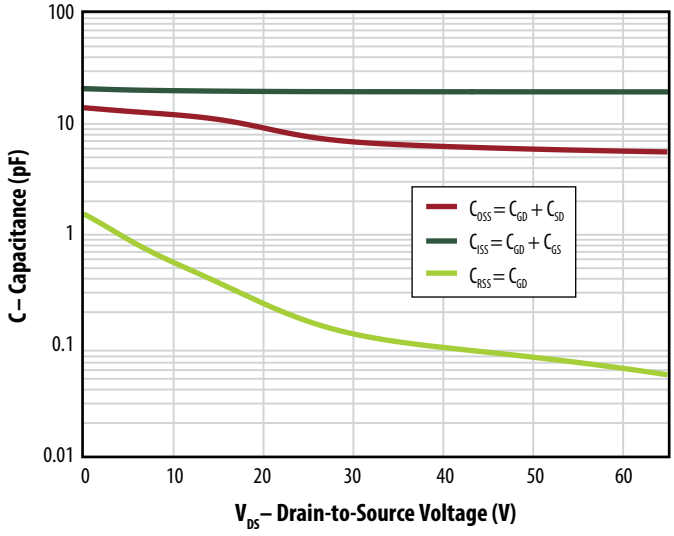


Figure 6: Gate Charge

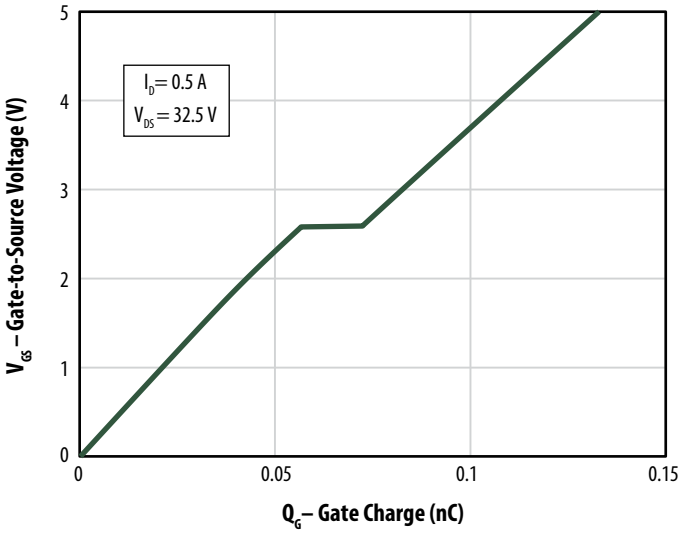


Figure 7: Reverse Drain-Source Characteristics

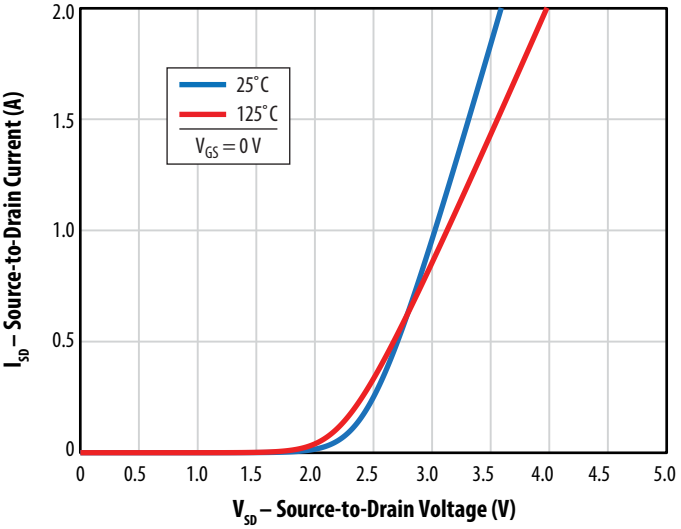


Figure 8: Normalized On-State Resistance vs Temperature

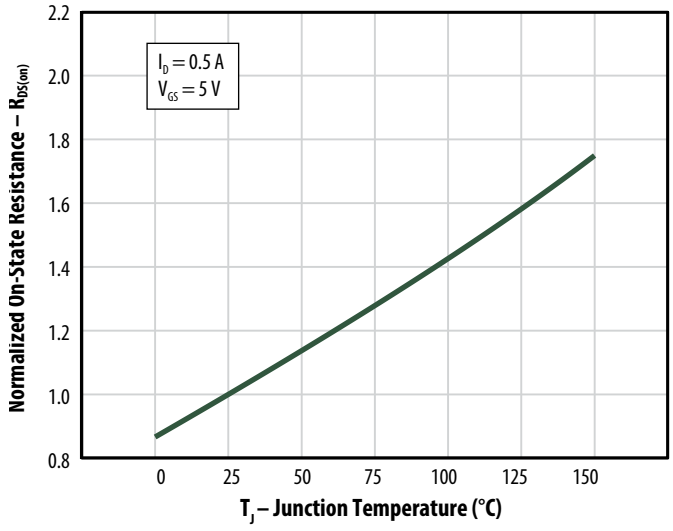


Figure 9: Normalized Threshold Voltage vs Temperature

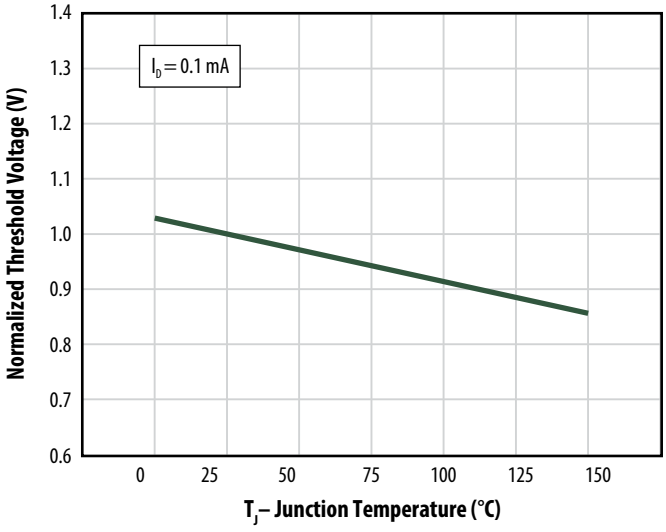
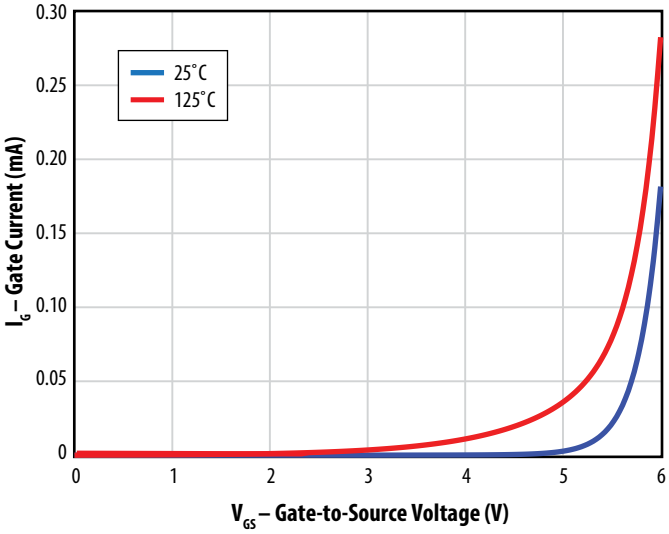


Figure 10: Gate Leakage Current



All measurements were done with substrate shortened to source.

Figure 11: Smith Chart

S-Parameter Characteristics
V_{GSQ} = 1.17 V, V_{DSQ} = 30 V, I_{DQ} = 0.2 A
Pulsed Measurement, Heat-Sink Installed, Z_0 = 50 Ω

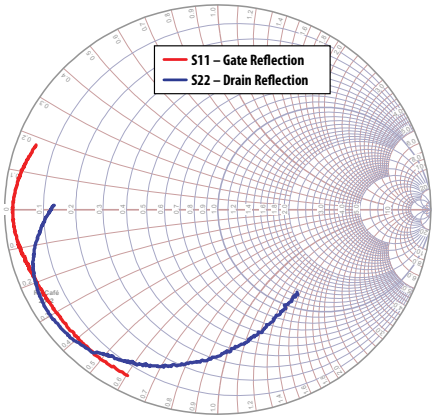
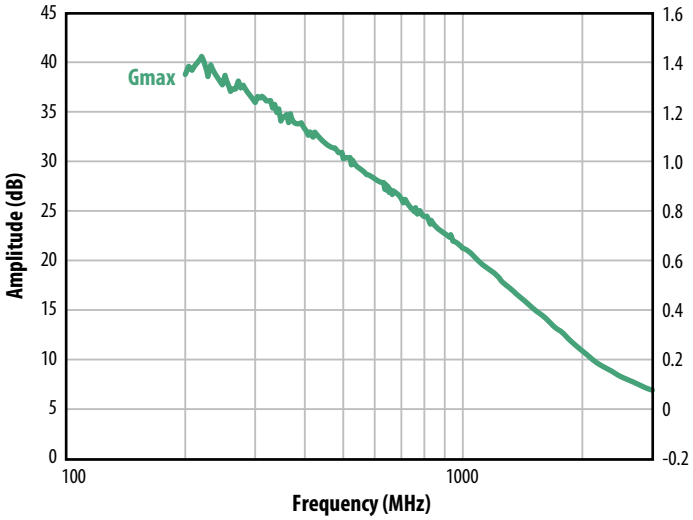


Figure 12: Gain Chart



Frequency	Gate (Z_{GS})	Drain (Z_{DS})
[MHz]	[Ω]	[Ω]
200	3.09 - j29.97	63.13 - j71.32
500	2.20 - j11.92	15.96 -j46.65
1000	1.14 - j4.46	3.35 - j23.47
1200	0.95 - j2.76	1.91 - j18.52
1500	0.87 - j0.55	1.66 - j12.66
2000	1.09 + j2.61	2.28 - j6.12
2400	1.44 + j4.87	4.35 - j2.80
3000	2.36 + j8.79	6.41 + j0.69

S-Parameter Table - Download S-parameter files at ***www.epc-co.com***

Figure 13: Device Reflection

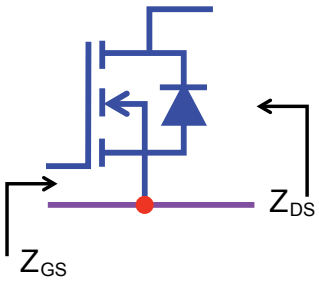


Figure 14: Taper and Reference Plane details – Device Connection

Micro-Strip design: 2-layer
½ oz (17.5 µm) thick copper
30 mil thick RO4350 substrate

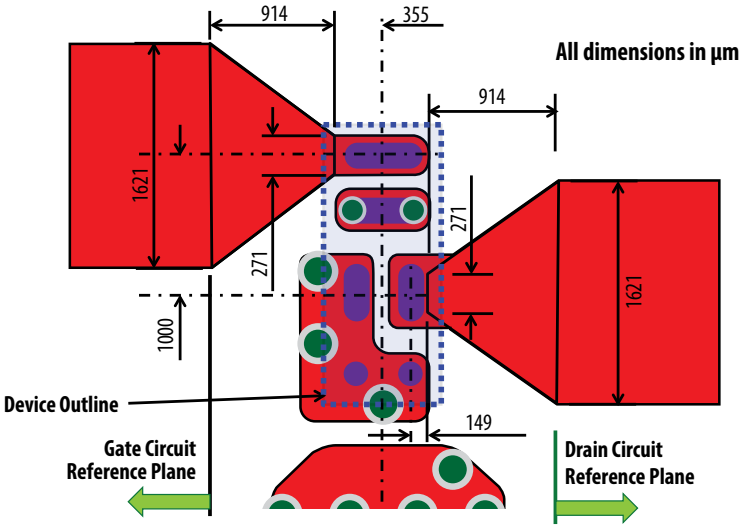


Figure 15: Transient Thermal Response Curves

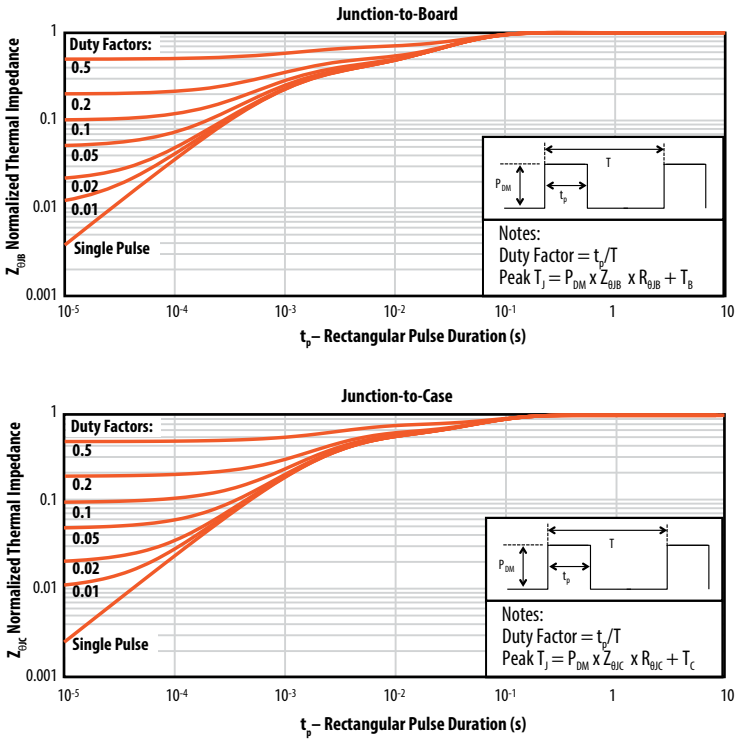
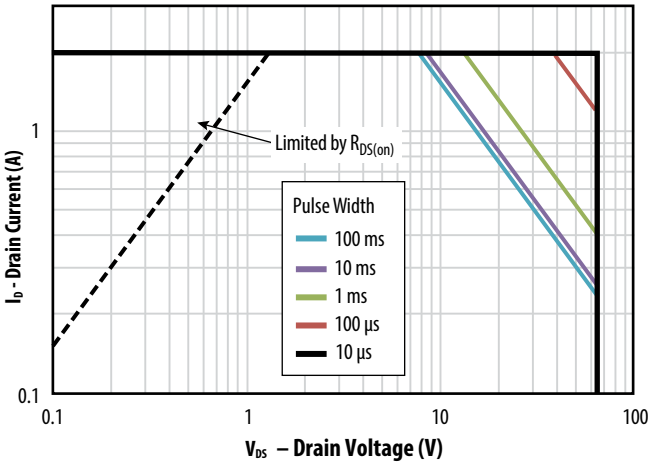
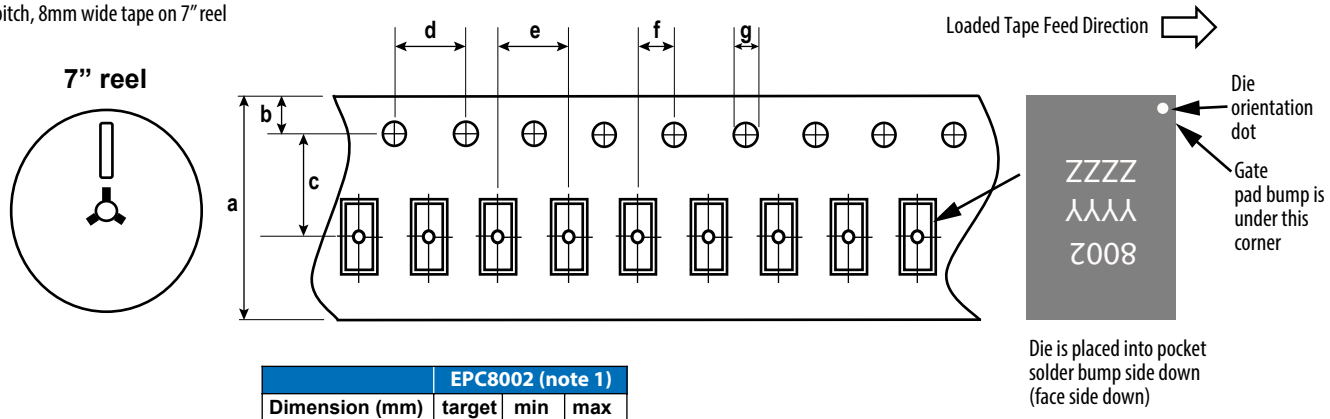


Figure 16: Safe Operating Area



TAPE AND REEL CONFIGURATION

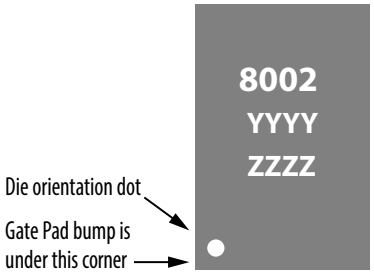
4mm pitch, 8mm wide tape on 7" reel



	EPC8002 (note 1)		
Dimension (mm)	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

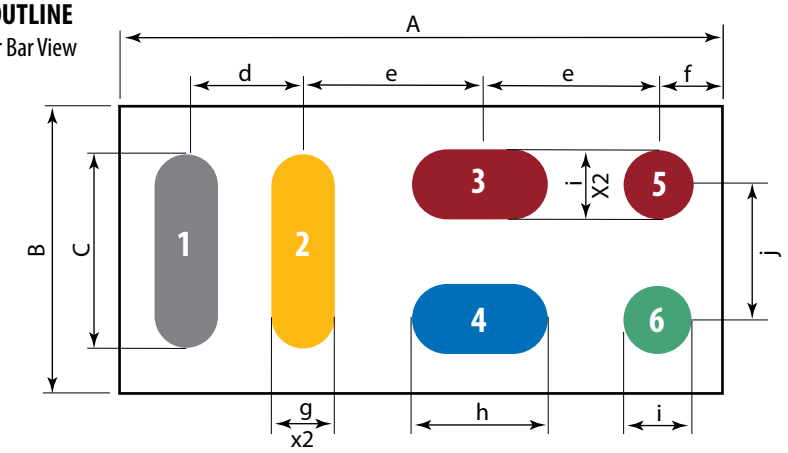
DIE MARKINGS



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking line 2	Lot_Date Code Marking Line 3
EPC8002	8002	YYYY	ZZZZ

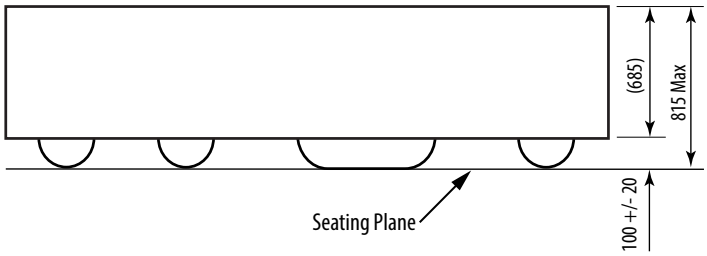
DIE OUTLINE

Solder Bar View



Dim	Micrometers		
	Min	Nominal	Max
A	2020	2050	2080
B	820	850	880
C	555	580	605
d	400	400	400
e	600	600	600
f	200	225	250
g	175	200	225
h	425	450	475
i	175	200	225
j	400	400	400

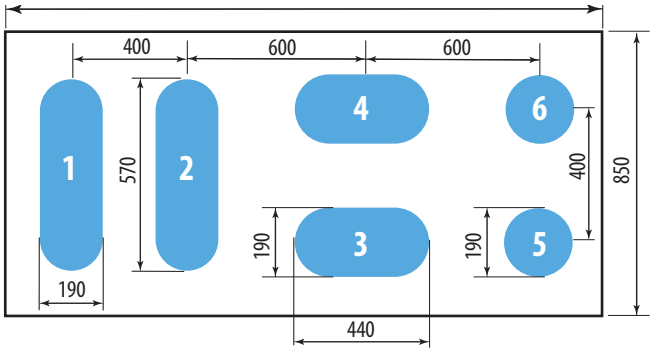
Side View



Pad no. 1 is Gate
Pad no. 2 is Source Return for Gate Driver
Pad no. 3 and 5 are Source
Pad no. 4 is Drain
Pad no. 6 is Substrate*

*Substrate pin should be connected to Source

RECOMMENDED LAND PATTERN *(measurements in µm)*

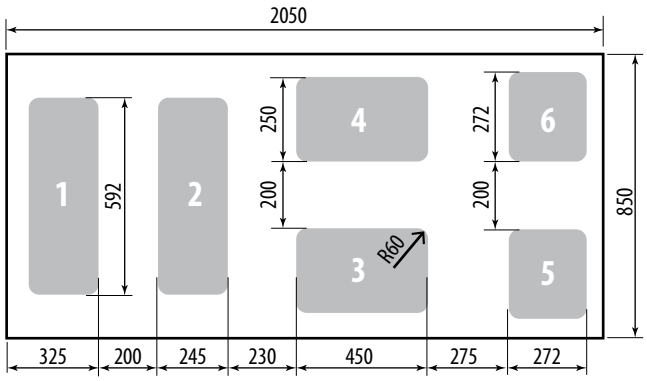


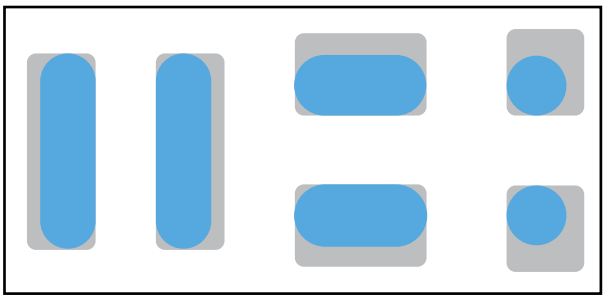
The land pattern is solder mask defined.
Solder mask opening is 5 µm smaller per side than bump.

Pad no. 1 is Gate
Pad no. 2 is Source Return for Gate Driver
Pad no. 3 and 5 are Source
Pad no. 4 is Drain
Pad no. 6 is Substrate*

*Substrate pin should be connected to Source

RECOMMENDED STENCIL DRAWING *(measurements in µm)*





Blue = bump, Gray = stencil

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing. Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Additional assembly resources available at: https://epc-co.com/epc/design-support/assemblybasics