EPC23103 – ePower™ Stage IC

V_{IN} , 100 V

I_{Load} , 25 A

PRELIMINARY

EFFICIENT POWER CONVERSION

RoHS Halogen-Free

The ePower™ Stage IC Product Family integrates input logic interface, level shifting, bootstrap charging and gate drive buffer circuits along with eGaN output FETs. Integration is implemented using EPC's proprietary GaN IC technology. The end result is a Power Stage IC that translates logic level input to high voltage and high current power output that is smaller in size, easier to manufacture, simpler to design and more efficient to operate.

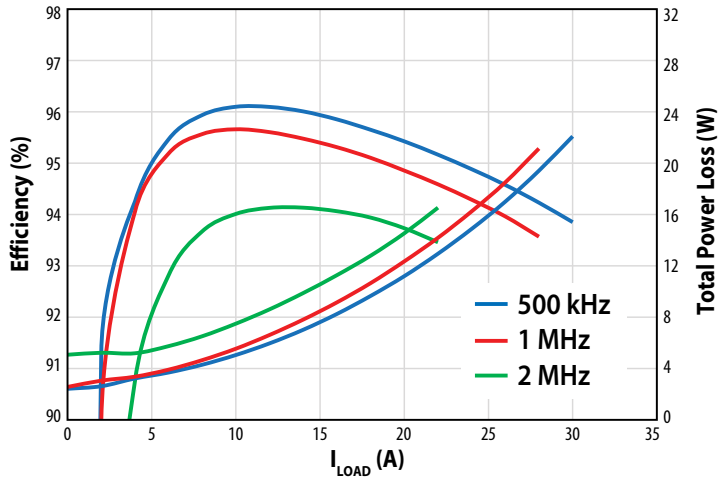
Key Parameters		
PARAMETER	**VALUE**	**UNIT**
Power Stage Load Current (1 MHz)	25	A
Pulsed current (25°C, T_{pulse} = 300 µs)	109	
Operating PWM Frequency (Minimum)	5	kHz
Operating PWM Frequency (Maximum)	3	MHz
Absolute Maximum Input Voltage	100	V
Operating Input Voltage Range	80	
Nominal Bias Supply Voltage	5	

Output Current and PWM Frequency Ratings are specified at ambient temperature of 25°C. See Application Information section for rating methodologies, test conditions, thermal management techniques and thermal derating curves.

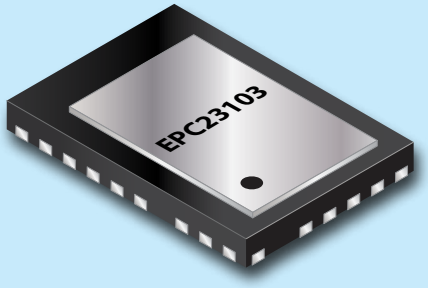
Device Information		
PART NUMBER	**Rated $R_{DS(on)}$ for HS and LS FETs at 25 °C**	**QFN Package Size (mm)**
EPC23103	7.6 mΩ + 7.6 mΩ	3.5 x 5

All exposed pads feature wettable flanks that allow side wall solder inspection. High voltage and low voltage pads are separated by 0.6mm spacing to meet IPC rules.

Figure 1: Performance Curves



Buck Converter, V_{IN} = 48 V, V_{OUT} = 12 V, Deadtime = 10 ns, L = 2.2 µH, DCR = 700 µΩ, Top Side Heatsink attached, Airflow = 400 LFM, T_A = 25°C, using **EPC90151 Evaluation Board**.



EPC23103 ePower™ Stage IC
Package size: 3.5 x 5 mm

Applications

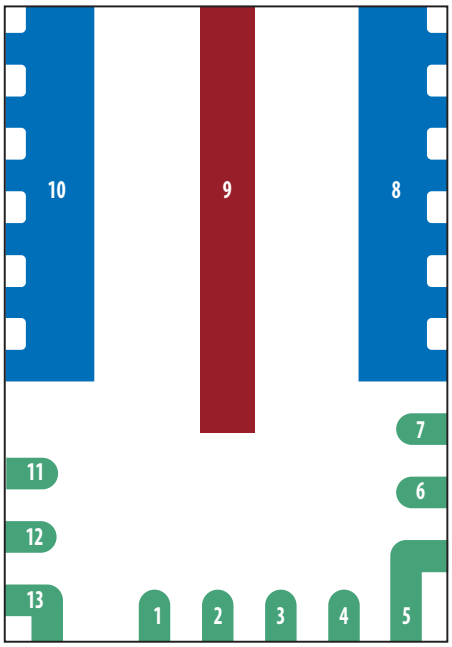
- Buck, Boost, Buck-Boost Converters
- Half-Bridge, Full Bridge LLC Converters
- Motor Drive Inverter
- Class D Audio Amplifier

Features

- Integrated high side and low side eGaN® FET with internal gate driver and level shifter
- 5 V external bias supply
- 3.3 V or 5 V CMOS input logic levels
- Independent high side and low side control inputs
- Logic lockout commands both FETs off when inputs are both high at same time
- External resistors to tune SW switching times and over-voltage spikes above rail and below ground
- Robust level shifter operating for hard and soft switching conditions
- False trigger immunity from fast switching transients
- Synchronous charging for high side bootstrap supply
- Disable input engages low quiescent current mode from V_{DRV} supply
- Power on reset for low side V_{DD} supply
- Power on reset for high side V_{Boot} supply
- Active gate pull-down for HS FET and LS FET with loss of V_{DRV} supply
- Thermally enhanced QFN package with exposed top for low thermal resistance from junction to top-side heatsink

https://l.ead.me/EPC23103

Figure 2: EPC23103 Quad Flat No-Lead (QFN) Package (Transparent Top View)



Transparent Top View

Pin	Description
1	HS_{IN}
2	LS_{IN}
3	SD
4	V_{DD}
5	V_{DRV}
6	R_{DRV}
7	AGND
8	PGND
9	SW
10	V_{IN}
11	V_{PHASE}
12	R_{BOOT}
13	V_{BOOT}

EPC23103 Pinout Description

Pin	Pin Name	Pin Type	Description
1	HS_{IN}	L	High side PWM logic input, level referenced to AGND. Internal pull-down resistor is connected between HS_{IN} and AGND.
2	LS_{IN}	L	Low side PWM logic input, level referenced to AGND. Internal pull-down resistor is connected between LS_{IN} and AGND.
3	SD	L	V_{DD} disable input, level referenced to AGND. Internal V_{DD} will be disabled when SD is pulled up to V_{DRV} or external 5 V source. Internal pull-down resistor is connected between SD and AGND, thereby V_{DD} will follow V_{DRV} with SD connected to AGND by default.
4	V_{DD}	S	Internal power supply referenced to AGND, connect a bypass capacitor from V_{DD} to AGND.
5	V_{DRV}	S	External 5 V nominal power supply referenced to AGND, connect a bypass capacitor from V_{DRV} to AGND.
6	R_{DRV}	G	Insert resistor between R_{DRV} to V_{DRV} to control the turn-on slew rate of the driven low side FET.
7	AGND	S	Logic ground. Connect bypass capacitors between operating bias supplies, V_{DRV} and V_{DD}, to AGND. Internal IC connection between AGND and PGND. Use star ground external connection with PGND to system ground.
8	PGND	P	Input power supply ground return. Connected to source terminal of internal low side FET. Connect power loop capacitors from V_{IN} to PGND.
9	SW	P	Output switching node. Connected to output of half-bridge power stage. SW pin connects together the source terminal of high side FET and the drain terminal of the low side FET.
10	V_{IN}	P	Power bus input. Connected to drain terminal of internal high side FET. Connect power loop capacitors from V_{IN} to PGND or power source terminals of low side FET.
11	V_{PHASE}	S	Kelvin connection to SW, the output switching node. The floating bootstrap power supply, V_{BOOT}, is also referenced to V_{PHASE}.
12	R_{BOOT}	G	Insert resistor between R_{BOOT} to V_{BOOT} to control the turn-on slew rate of the internal high side FET.
13	V_{BOOT}	S	Floating bootstrap power supply referenced to V_{PHASE} (=SW). Connect an external bypass capacitor from V_{BOOT} to V_{PHASE}.

Pin Type: P = Power, S = Bias Supplies, L = Logic Inputs/Outputs, G = Gate Drive Adjust

Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur and device reliability may be affected. All voltage parameters are absolute voltages referenced to PGND (=AGND) unless indicated otherwise.

Absolute Maximum Ratings				
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**
V_{IN}	Input Voltage (V_{IN} to PGND)		100	V
$SW_{(continuous)}$	Output Switching Node (SW to PGND), Continuous		100	
V_{DRV}	External Bias Supply (V_{DRV} to AGND)		6	
V_{DD}	Internal Low Side Supply Voltage (V_{DD} to AGND)		6	
$V_{BOOT} - V_{PHASE}$	Internal High Side Supply Voltage (V_{BOOT} to V_{PHASE}), V_{PHASE} = SW		6	
HS_{IN}, LS_{IN}	PWM Logic Inputs (HS_{IN} to AGND and LS_{IN} to AGND)		5.5	
SD	V_{DD} Disable Input (SD to AGND)		5.5	
T_J	Junction Temperature		150	°C
T_{STG}	Storage Temperature	-55	150	

ESD Ratings

ESD Ratings				
SYMBOL	**PARAMETER**	**MIN**	**MAX**	**UNITS**
HBM	Human-body model (JEDEC JS-001)	+/-1000		V
CDM	Charged-device model (JEDEC JESD22-C101)	+/-500		

Thermal Characteristics

$R_{\theta JA\_JEDEC}$ is measured using JESD51-2 standard setup with 1 cubic foot enclosure with no forced air cooling, heat dissipated only through natural convection. The test used JEDEC Standard 4-layers PCB with 2 oz top and bottom surface layers and 1oz buried layers. $R_{\theta JA\_EVB}$ is measured using EPC90151 EVB with no forced air cooling, this rating is more indicative of actual application environment.

Thermal Characteristics			
SYMBOL	**PARAMETER**	**TYP**	**UNITS**
$R_{\theta JC\_Top}$	Thermal Resistance, Junction-to-Case (Top surface of exposed die substrate)	0.45	°C/W
$R_{\theta JB\_Bottom}$	Thermal Resistance, Junction-to-Board (At solder joints of V_{IN}, SW and PGND pads)	2.7	
$R_{\theta JA\_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	46	
$R_{\theta JA\_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC90151 EVB)	26	

Recommended Operating Conditions

For proper operation the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to PGND (= AGND) unless indicated otherwise.

Recommended Operating Conditions					
SYMBOL	**PARAMETER**	**MIN**	**TYP**	**MAX**	**UNITS**
V_{IN}	Input Voltage (V_{IN} to PGND)	10		80	V
$SW_{(Q3\ Mode)}$	Output Switch Node, 3rd Quadrant Mode	-2.5		V_{IN} + 2.5	
$SW_{(pulse2ns)}$	Output Switch Node, Transient PW < 2 ns	-10		V_{IN} +10	
V_{DRV}	External Bias Supply (V_{DRV} to AGND)	4.75	5	5.5	
V_{DD}	Internal Low Side Supply Voltage (V_{DD} to AGND)	4.75	5	5.5	
$V_{BOOT} - V_{PHASE}$	Internal High Side Supply Voltage (V_{BOOT} to V_{PHASE}), V_{PHASE} = SW	4.75	5	5.5	
HS_{IN}, LS_{IN}	PWM Logic Inputs	0		5	
SD	V_{DD} Disable Input	0		5	
PW_min	Minimum Input On or Off Pulse Duration, 50% to 50% width	20			ns
PW_max	Maximum Input On or Off Pulse Duration, 50% to 50% width			200	µs
T_J	Operating Junction Temperature	-40		125	°C

Electrical Characteristics

Nominal V_{IN} = 48 V, V_{DRV} = V_{DD} = 5 V and (V_{BOOT} – V_{PHASE}) = 5 V. All typical ratings are specified at T_A = 25°C unless otherwise indicated. All voltage parameters are absolute voltages referenced to PGND (= AGND) unless indicated otherwise.

Electrical Characteristics						
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Low Side Power Supply						
I_{DRV_Q}	Off State Total Quiescent Current	HS_{IN}/LS_{IN}/SD = 0 V, V_{DRV} = V_{DD} = 5 V		10		mA
I_{DRV_100kHz}	Total Operating Current @100 kHz	PWM = 100 kHz, 50% On-Time		14		
I_{DRV_1MHz}	Total Operating Current @1 MHz	PWM = 1 MHz, 50% On-Time		22		
$I_{VIN\_disable}$	V_{IN} Quiescent Current at Disable Mode	SD = V_{DRV} = 5 V, V_{IN} = 48 V			600	µA
$I_{DRV\_disable}$	V_{DRV} Quiescent Current at Disable Mode	SD = V_{DRV} = 5 V, V_{IN} = 48 V			50	
Bootstrap Power Supply						
I_{BOOT_Q}	Off State Bootstrap Supply Current	HS_{IN} = 0 V, (V_{BOOT} – V_{PHASE}) = 5 V		6		mA
I_{BOOT_100kHz}	Bootstrap Supply Current @100 kHz	HS PWM = 100 kHz, 50% On-Time		7		
I_{BOOT_1MHz}	Bootstrap Supply Current @1 MHz	HS PWM = 1 MHz, 50% On-Time		14		
V_{SYNC_BOOT}	Sync Boot Generated (V_{BOOT} -V_{PHASE})	I_{SYNC_BOOT} = 20 mA		4.75		V
Power On Reset						
V_{DD_POR+}	POR Trip Level V_{DD} Rising	LS_{IN} = 5 V, V_{DD} Ramps Up		4		V
$V_{DD\_POR\_HYST}$	POR V_{DD} Falling Hysteresis	LS_{IN} = 5 V, V_{DD} Ramps Down		0.5		
V_{BOOT_POR+}	POR Trip Level (V_{BOOT} - V_{PHASE}) Rising	HS_{IN} = 5 V, V_{BOOT} Ramps Up		4		
$V_{BOOT\_POR\_HYST}$	POR (V_{BOOT} - V_{PHASE}) Falling Hysteresis	HS_{IN} = 5 V, V_{BOOT} Ramps Down		0.5		
Logic Input Pins						
V_{IH}	High-level Logic Threshold	HS_{IN}, LS_{IN} Rising	2.4			V
V_{IL}	Low-level Logic Threshold	HS_{IN}, LS_{IN} Falling			0.8	
V_{IHYST}	Logic Threshold Hysteresis	V_{IH} Rising – V_{IL} Falling		0.3		
R_{IN}	HS_{IN} and LS_{IN} Pull-Down Resistance	HS_{IN}, LS_{IN} = 5 V		6.5		kΩ
V_{DD} Disable Input						
V_{TH_EN}	SD Input Threshold	V_{DRV} = 5 V	3.3			V
R_{EN}	SD Pull-Down Resistance	SD = 5 V		150		kΩ
High Side Internal Power FET						
$R_{DS(on)\_HS}$	High Side FET $R_{DS(on)}$	I_{DS} = +/-10 A, HS_{IN} = 5 V, LS_{IN} = 0 V		6	7.6	mΩ
$V_{HS\_DS\_Clamp}$	High Side 3rd Quadrant Clamp	I_{DS} = - 10 A, HS_{IN} & LS_{IN} = 0 V		-1.5		V
I_{LEAK_VIN-SW}	Leakage Current (V_{IN} to SW)	HS_{IN} = 0 V, V_{IN} = 100 V, SW = 0 V			300	µA
C_{WELL}	HV-Well Capacitance (SW to PGND)	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 48 V		39		pF
C_{OSS_HSFET}	Output Capacitance (V_{IN} to SW)	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 0 V		264		
Q_{OSS_HSFET}	Output Charge (V_{IN} to SW)	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 0 V		21		nC
E_{QOSS_HSFET}	Output Capacitance Stored Energy	HS_{IN} = 0 V, V_{IN} = 48 V, SW = 0 V		0.38		µJ
$E_{ON\_HS\_0}$	Turn-On Switching Energy (HS_FET)	HS Turn-On, SW = 0 V to 48 V, R_{BOOT} = 0 Ω, I_{LOAD} = 10 A		2.1		
$E_{ON\_HS\_1}$		HS Turn-On, SW = 0 V to 48 V, R_{BOOT} = 2.2 Ω, I_{LOAD} = 10 A		3.8		
E_{OFF_HS}	Turn-Off Switching Energy (HS_FET)	HS Turn-Off, SW = 48 V to 0 V, I_{LOAD} = 10 A		0.13		
Low Side Internal Power FET						
$R_{DS(on)\_HS}$	Low Side FET $R_{DS(on)}$	I_{DS} = +/-10 A, LS_{IN} = 5 V, HS_{IN} = 0 V		6	7.6	mΩ
$V_{HS\_DS\_Clamp}$	Low Side 3rd Quadrant Clamp	I_{DS} = - 10 A, HS_{IN} & LS_{IN} = 0 V, SW = 0 V, SW = 0 V		-1.5		V
$I_{LEAK\_SW-PGND}$	Leakage Current (SW to PGND)	LS_{IN} = 0 V, V_{IN} = 100 V, SW = 100 V			100	µA
C_{OSS_LSFET}	Output Capacitance (SW to PGND)	LS_{IN} = 0 V, SW = 48 V, PGND = 0 V		264		pF
Q_{OSS_LSFET}	Output Charge (SW to PGND)	LS_{IN} = 0 V, SW = 48 V, PGND = 0 V		21		nC
E_{QOSS_LSFET}	Output Capacitance Stored Energy	LS_{IN} = 0 V, SW = 48 V, PGND = 0 V		0.38		µJ
$E_{ON\_LS\_0}$	Turn-On Switching Energy (LS_FET)	LS Turn-On, SW = 48 V to 0 V, R_{BOOT} = 0 Ω, I_{LOAD} = 10 A		2.1		
$E_{ON\_LS\_1}$		LS Turn-On, SW = 48 V to 0 V, R_{BOOT} = 2.2 Ω, I_{LOAD} = 10 A		3.8		
E_{OFF_LS}	Turn-Off Switching Energy (LS_FET)	LS Turn-Off, SW = 0 V to 48 V, I_{LOAD} = 10 A		0.13		

Electrical Characteristics *(continued)*

Electrical Characteristics (continued)						
SYMBOL	**PARAMETER**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNITS**
Dynamic Characteristics (Logic Input to Output Switching Node) See Figure 3a and 3b for Timing Diagram and Test Circuit)						
$t\_delay_{HS\_on}$	High-Side On Propagation Delay	SW = 0 V and HS FET Turn-On		20		ns
$t\_delay_{LS\_on}$	Low-Side On Propagation Delay	SW = 48 V and LS FET Turn-On		20		
$t\_delay_{HS\_off}$	High-Side Off Propagation Delay	SW = 48 V and HS FET Turn-Off		20		
$t\_delay_{LS\_off}$	Low-Side Off Propagation Delay	SW = 0 V and LS FET Turn-Off		20		
t_match_{on}	Delay Matching LS_{off} to HS_{on}	LS Turn-Off to HS Turn-On		0		
t_match_{off}	Delay Matching HS_{off} to LS_{on}	HS Turn-Off to LS Turn-On		0		
$t\_rise_{SW\_HS0}$	SW Rise Time at High Side FET Turn-On (Buck Mode, Hard Switching)	HS Turn-On Buck Mode, 0 V to 48 V, R_{BOOT} = 0 Ω, I_{Load} = 5 A		1.5		
$t\_rise_{SW\_HS1}$		HS Turn-On Buck Mode, 0 V to 48 V, R_{BOOT} = 2.2 Ω, I_{Load} = 5 A		3		
$t\_fall_{SW\_LS0}$	SW Fall Time at Low Side FET Turn-On (Boost Mode, Hard Switching)	LS Turn-On Boost Mode, 48 V to 0 V, R_{DRV} = 0 Ω, I_{Load} = 5 A		1.5		
$t\_fall_{SW\_LS1}$		LS Turn-On Boost Mode, 48 V to 0 V, R_{DRV}= 2.2 Ω , I_{Load} = 5 A		3		

Dynamic Characteristics Parameter Definition

Figure 3a: Test Circuit for Dynamic Characteristics

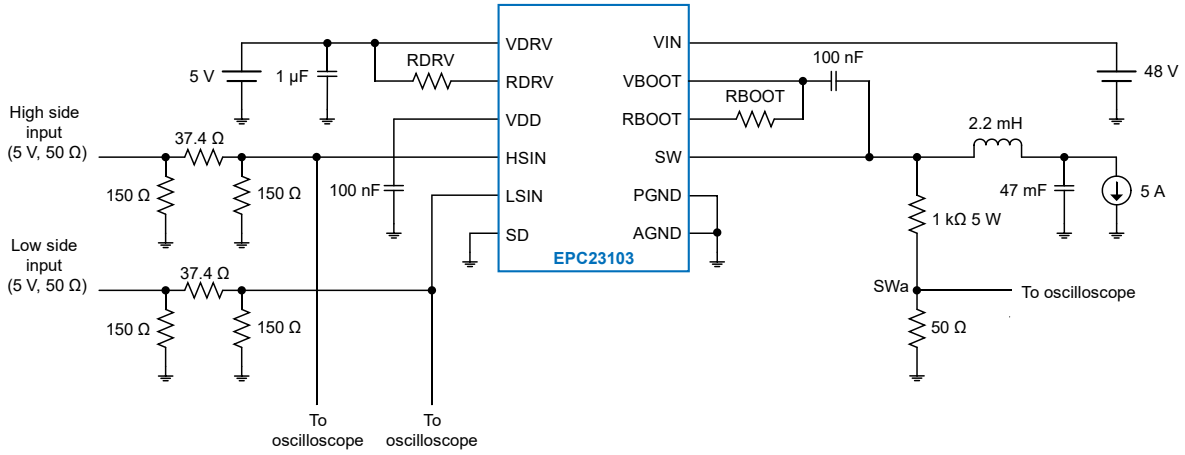
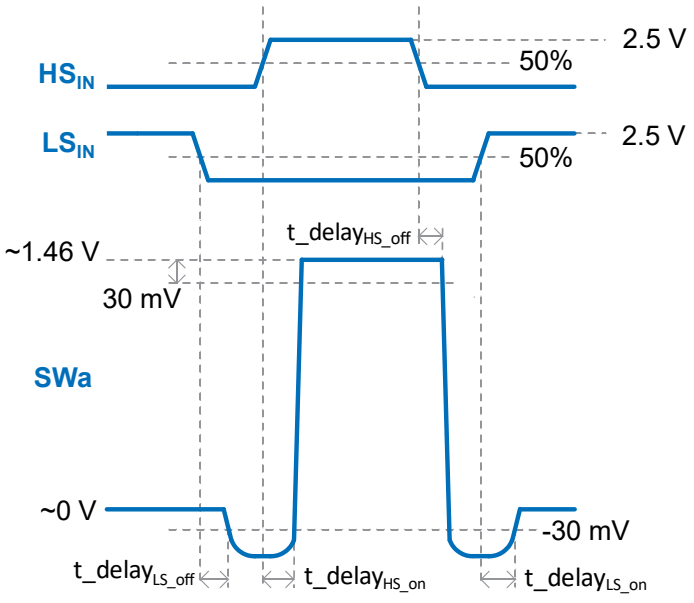


Figure 3b: Logic Input to Output Switching Node Timing Diagram



Truth Table

V_{DD}	$V_{BOOT} - V_{PHASE}$	HS_{IN}	LS_{IN}	HS FET	LS FET
$<V_{DD\_POR}$	–	–	–	OFF	OFF
$>V_{DD\_POR}$	$<V_{BOOT\_POR}$	–	0	OFF	OFF
		–	1	OFF	ON
$>V_{DD\_POR}$	$>V_{BOOT\_POR}$	0	0	OFF	OFF
		0	1	OFF	ON
		1	0	ON	OFF
		1	1	OFF	

Application Information

General Description

The EPC23103 ePower™ Stage IC integrates a half-bridge gate driver with internal high side and low side FETs. Integration is implemented using EPC's proprietary GaN IC technology. The monolithic chip integrates input logic interface, level shifting, bootstrap charging and gate drive buffer circuits controlling high side and low side eGaN output FETs configured as a half-bridge power stage. Robust level shifters from low side to high side channels are designed to operate correctly with soft and hard switching conditions even at large negative clamped voltage and to avoid false trigger from fast dv/dt transients including those driven by external sources or other phases. Internal circuits integrate the functions of charging and disabling of the logic and bootstrap power supplies. Protection features are added to protect the output FETs from unwanted turn-on at low or even complete loss of supply voltages.

The single chip is mounted inside a 3.5 x 5 mm Quad Flat No-lead (QFN) package using a flip chip on lead-frame technique. This packaging structure allows very low parasitic inductance from the power terminals to the underlying PCB solder pads. The exposed EPC23103 QFN pads are designed to have at least 0.6 mm spacing between high and low voltage pins to meet IPC voltage creepage rule for 100 V. Another enhancement exposes the backside of the Gan IC die on the top side of the package while completely encapsulating the rest of the GaN IC die. This allows a very low thermal resistance path from the die junction to an attached heatsink which in effect increase the allowable power dissipation and thus higher current handling capability.

Figure 4: Functional Block Diagram

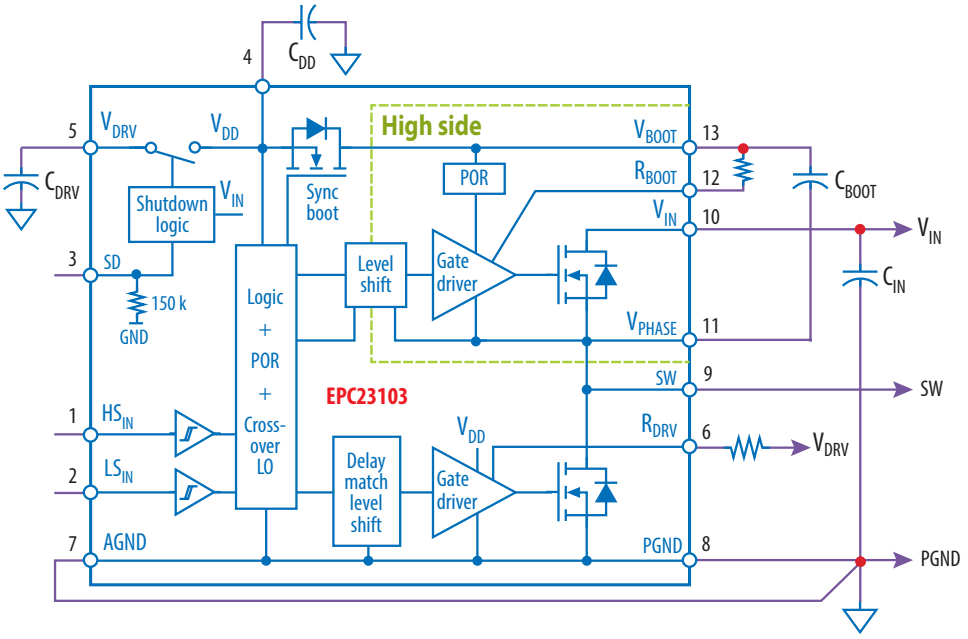
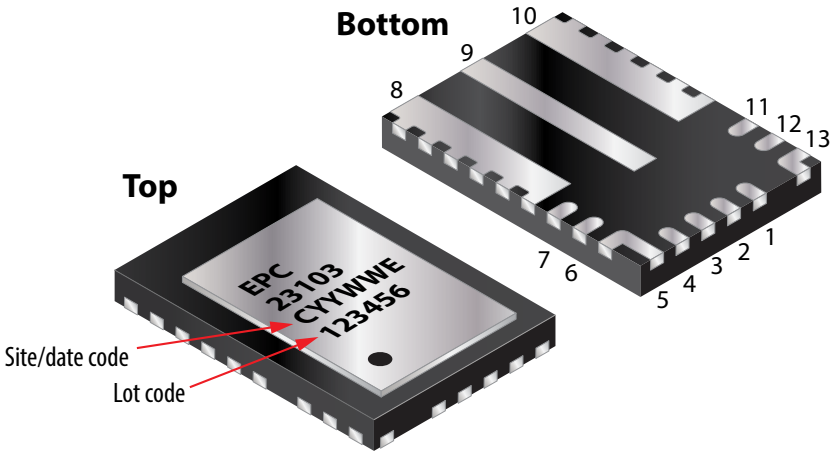


Figure 5: EPC23103 QFN package outline, pinouts and exposed backside of the GaN IC die



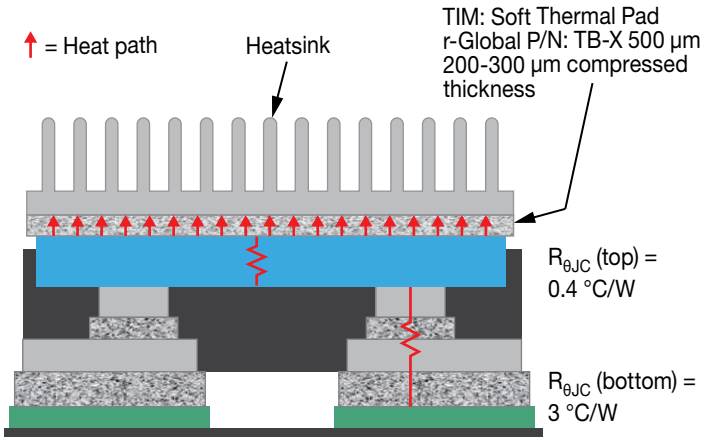
Output Current Rating

Power stage output current rating is best thought of as a figure of merit for specified output current level that accounts for the maximum amount of power dissipation allowed from the IC. Total power dissipation from a power stage IC is tied to the application circuit topologies, output current demand, switching frequencies, PCB construction, operating temperature range, thermal management technique and mechanical stress limit of the metallization imposed by electromigration. The rating is related to the respective maximum current capability of the two integrated output FETs in the half-bridge power stage but not measured the same way as individual discrete FET. For a power stage IC such as EPC23103, total power loss from the IC is the sum of the two output FETs conduction, switching and deadtime losses imposed by the application topologies at operating switching frequencies as well as power losses from the gate drive and logic circuit. The maximum power dissipation is defined by the following formula:

$$\text{Max } P_{Diss} = (\text{Max } T_J - T_A)/ R_{\theta JA}$$

where Max T_J is specified at 125 °C and the ambient temperature is specified at 25 °C. The big variable in achieving the theoretical maximum power dissipation is $R_{\theta JA}$, the thermal resistance from junction to ambient. The EPC23103 package construction allows two parallel path of heat dissipation where the bottom path goes from junction to metallization to lead-frame then the exposed pads at the bottom of the package. The three power bars (V_{IN}, SW and PGND) are designed to allow maximum contact area to the underlying PCB pads to achieve a $R_{\theta JB\_bottom}$ of 3 °C/W. The total thermal resistance to ambient in this path of $R_{\theta JA\_bottom}$ needs to add the heat dissipation from the PCB pads through the multi-layer PCB construction then radiating to the ambient which is highly dependent on the airflow and forced cooling method. (See Figure 6).

Figure 6: Parallel Thermal Resistance Paths of EPC23103 IC from junction to ambient



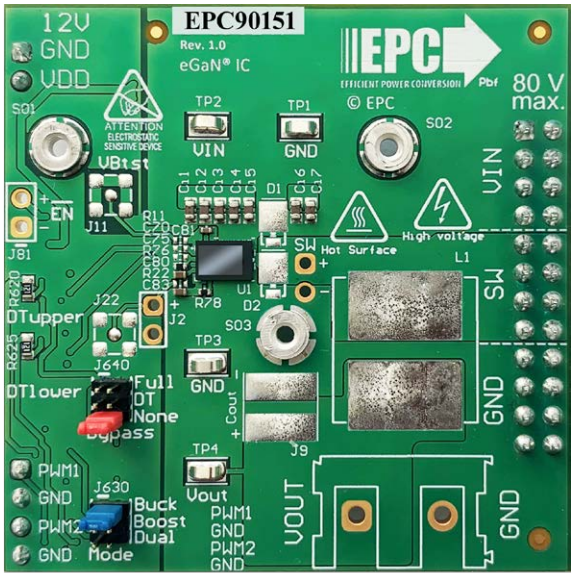
To achieve even lower effective thermal resistance, another path is provided from junction to the relatively lower thermal resistance Si substrate of the GaN IC structure to the exposed backside of the entire die at the top of the package to achieve a $R_{\theta JC\_top}$ of 0.4 °C/W. This lower thermal resistance path facilitates attachment of a topside heatsink through thermal interface material (TIM) to the exposed backside of the die. Note that the backside of the die is connected to the PGND (=AGND) pins which potentially provides added benefits of using electrically conductive TIM which has >2X higher thermal conductivity and lower cost than the insulating type. Typical parameters of electrically conducting vs. insulating TIMs are shown in the table below.

Typical parameters of electrically conducting vs. insulating TIMs		
Type of TIM	**Thermal Conductivity (W/m-K)**	**Relative Cost**
Electrically Conducting	40	1
Electrically Insulating	15	1.3

Another factor in specifying the output current rating is electromigration from a metallurgical standpoint. For EPC23103 this limit is a function of the metallization structure underlying the two output FETs plus their connection to the lead-frame and the three exposed power bars. A maximum of 39 A is allowed due to electromigration limit.

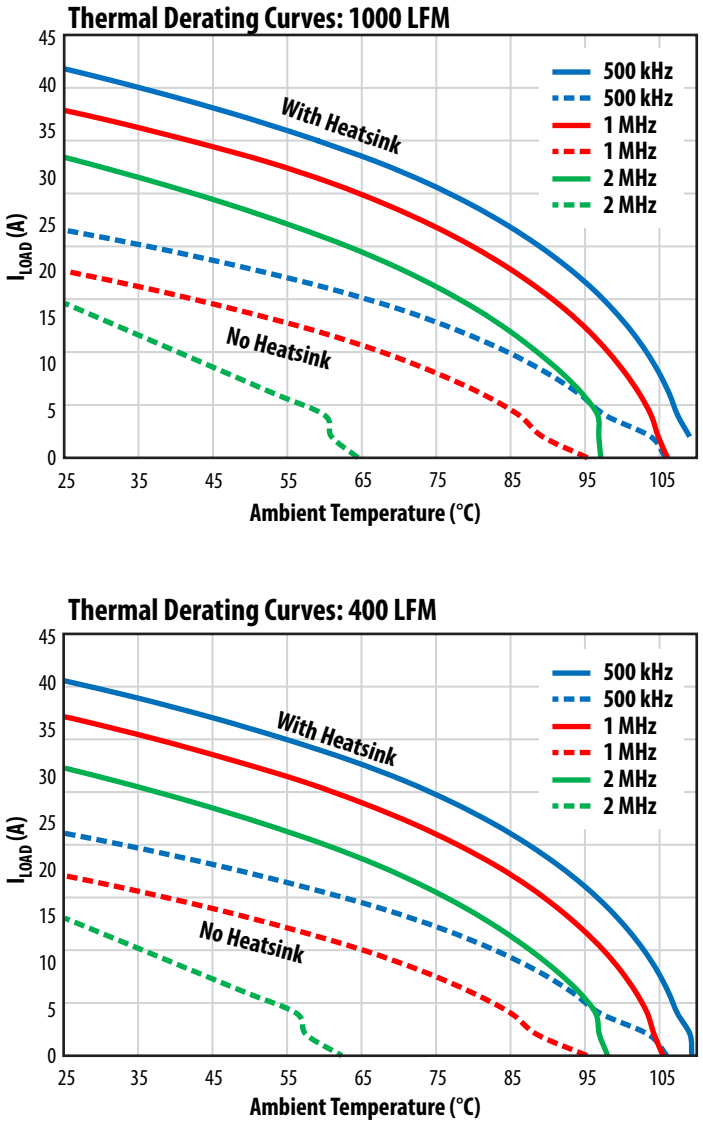
EPC uses a reference evaluation board, EPC90151 as shown in Figure 7, configured in a Buck Converter topology with the following test conditions: V_{IN} = 48 V, V_{OUT} = 12 V, PWM frequency = 0.5, 1, and 1.5 MHz, with and without top side heatsink, airflow = 500 and 1000 LFM, operating at ambient temperature starting at 25°C, maximum T_C not to exceed 110°C (derated from 125°C to avoid thermal runaway).

Figure 7: EPC90151 Evaluation Board (see EPC90151 Quick Start Guide for details)



Thermal derating curves in Figure 8 are derived from measurement data. At ambient temperature of 25°C using topside heatsink, the EPC23103 IC is specified with an output current handling capability greater than 35 A operating at 1 MHz switching frequency with airflow greater than 500 LFM. But without the benefit of topside heatsink, the same conditions at 1 MHz and 500 LFM, the current rating is reduced to 16 A at ambient temperature of 25°C showing the dramatic difference of using the lower $R_{\theta JC\_top}$ of the higher thermal conductive path.

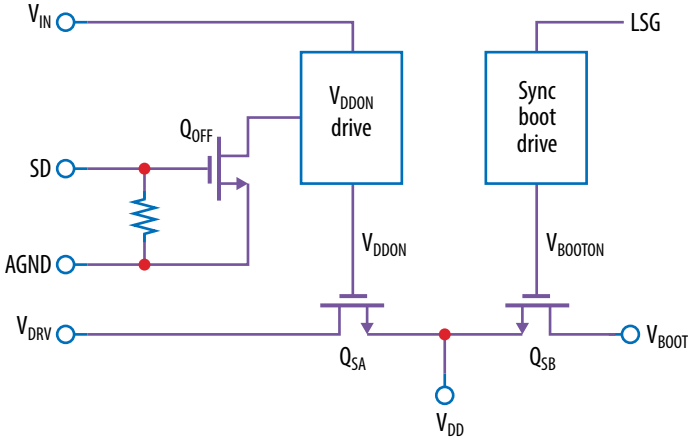
Figure 8: Thermal Derating Curves for Output Current Rating of EPC23103 IC using EPC90151 Evaluation Board



Power Supplies – V_{IN}, V_{DRV}, V_{DD}, and V_{BOOT}

The EPC23103 IC only requires an external 5 V V_{DRV} power supply. Internal low side and high side power supplies, V_{DD} and V_{BOOT}, are generated from the external supply via two series connected switches. Figure 9 shows the simplified circuit diagram of the different power supplies inside the IC and their interaction with each other.

Figure 9: Simplified circuit diagram of V_{IN}, V_{DRV}, V_{DD}, and V_{BOOT} Power Supplies



The internal supplies can be disabled to save quiescent power by turning off the series switch, Q_{SA} in Figure 9, with 5 V applied to the SD pin to engage chip shutdown mode. In this mode, minimum current is drawn from the external V_{DRV} supply while V_{DD} is open circuit. Whatever charges remain within the V_{DD} bypass capacitor will be discharged by the chip internal circuits at nominal rate of 10 mA/C_{DD}.

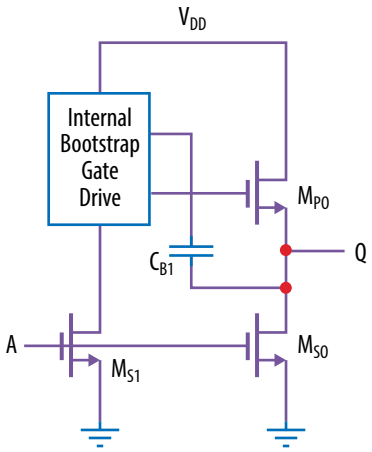
In the chip shutdown circuit, series switch (Q_{SA}) between V_{DRV} and V_{DD} is turned off by internal disable circuit which itself derived its power from V_{IN} such that the chip draws a maximum up to 600 µA at 48 V from V_{IN} when shutdown mode is engaged. The minimum input voltage (V_{INmin}) should be at least 10 V for the IC to be enabled. Below the minimum V_{IN} the pass-transistor between V_{DRV} and V_{DD} will be off. Same condition when V_{DD} disable pin, $\overline{EN}$, is connected to 5 V.

The series connected high voltage synchronous bootstrap FET, Q_{SB} in Figure 9, between V_{DD} and V_{BOOT} for the high side floating bootstrap supply is activated only after the LS FET (Q2) is turned on to avoid overcharging during deadtime. The use of GaN FET in the charging path eliminates reverse recovery and reduces power dissipation. Another advantage is the lower dropout voltage of 100 to 200 mV from the synchronous FET versus typical Si bootstrap diode voltage of 0.6 V. With synchronous charging V_{BOOT} is maintained closer to the V_{DD} voltage, allowing the HS FET gate drive circuit to have similar gate drive current and delay performance as the LS FET gate drive circuit.

Gate Driver

The EPC23103 IC integrates both HS and LS FET gate drivers with very low impedance (0.4 Ω) and high pulse current (5 A) push-pull NFET output stage. Figure 10 is the simplified circuit diagram of the gate driver output stage.

Figure 10: Simplified Circuit Diagram of Gate Driver Output Stage



The HS and LS gate drive voltage levels are derived from their respective internal low side (V_{DD}) and high side (V_{BOOT}) power supplies. To ensure that the gate drive level (Q) is sufficiently close to V_{DD} or V_{BOOT}, an internal bootstrap circuit is used to turn-on M_{PO}. Here the M_{PO} and M_{SO} pair works similarly to the half-bridge power stage Q1 and Q2 output FETs except all the circuits are internal to the IC. C_{B1} is an internal bootstrap capacitor. The PWM inputs, HS_{IN} and LS_{IN}, are used as the clocks for their respective high side and low side internal bootstrap gate drive circuit. As with any bootstrap circuit, the gate drive output cannot have 100% duty cycle to allow C_{B1} to be recharged. For the EPC23103 IC, the PWM input pulse width must not exceed a maximum of 200 µs on/off duration and a minimum pulse width on/off duration of 20 ns as specified in the recommended operating condition table. At initial startup of the HS_{IN} and LS_{IN} clocking cycle, C_{B1} needs to be charged from zero. A delay of nominally 6 switching cycles appears before the gate drive output will follow the PWM input pulses. Figure 11a and 11b illustrate the gate drive output switching behavior.

SW Node Switching Transients

The switching rate and transients at the output node, SW, is controlled by application topologies resulting in hard or soft switching transitions. The more stressful hard switching transition needs to be controlled by a combination of tuning gate drive turn-on and turn-off circuits for the HS FET (Q1) and LS FET (Q2) and minimizing the power loop parasitic inductances.

The on-chip gate drive buffers practically eliminate effects of common source inductance and gate drive loop inductance. Switching times are tuned by external resistors, R_{DRV} and R_{BOOT}, as shown in Figure 12 to achieve SW switching rate of 10 to 50 V/ns spanning zero to full load current. The choice of switching rates is dictated by efficiency versus EMI mitigation.

Figure 12: Simplified circuit diagram of external tuning resistor, internal gate drivers and output FETs

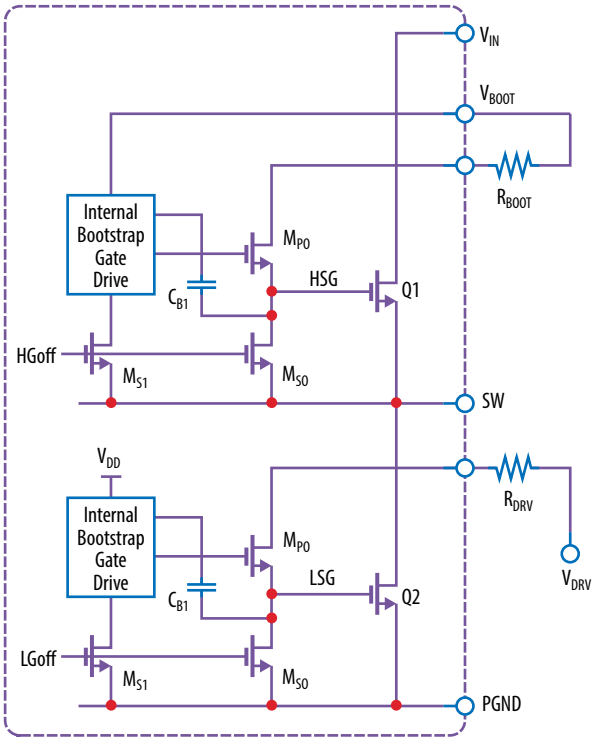


Figure 11a: Maximum and Minimum PWM Input Pulse Width On or Off duration to refresh internal gate drive bootstrap circuit

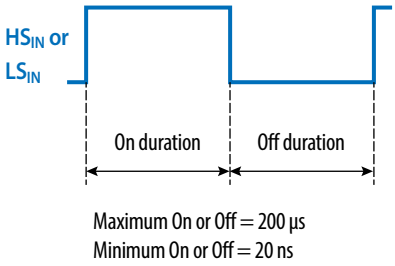
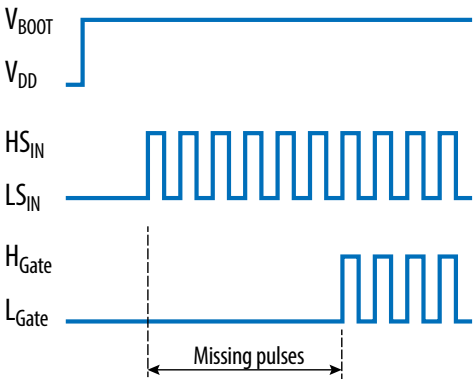


Figure 11b: Missing High Side and Low Side Gate pulses at startup due to initial charging of internal gate drive bootstrap circuit



During HS FET (Q1) or LS FET (Q2) turn-on transitions with hard switching conditions, the fast di/dt of the HS FET or LS FET coupled with the power loop inductance ($V_{peak} = L_{power\ loop} \cdot di/dt$) would cause a transient over-voltage spike above V_{IN} or below PGND. The EPC23103 pinouts for the three power bars (V_{IN}, SW, PGND) are coupled with the design of optimal layout techniques to achieve minimized power loop inductance. Together with SW switching rate tuning by R_{DRV} and R_{BOOT}, the over-voltage spikes can be controlled to less than +10 V above rail and -10 V below ground during hard switching transitions.

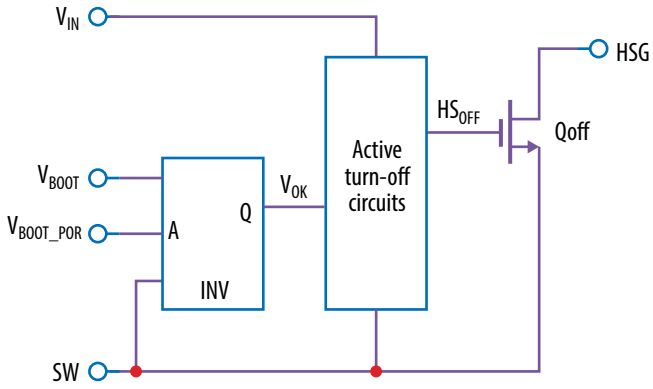
The EPC90151 Evaluation Board provides guidelines for PCB layout to use the EPC23103 in application circuits together with the Gerber files and Bill of Material. To control SW switching rate and transients, 2.2 Ω are used for both R_{DRV} and R_{BOOT} for high frequency DC-DC converter switching around 1 MHz and 4.7 Ω used for 100 kHz motor drive inverter applications.

Protection Circuits

EPC integrated eGaN FETs are very robust devices when operating within the recommended operating conditions, output current rating and thermal management techniques as described. Still there are inevitable power supplies sequencing at startup and brownout conditions where the power supplies would go out of the recommended range or even a complete loss of supply. A particular damaging condition could occur when V_{IN} supply is already fully charged but V_{DRV} is at the startup phase or discharged due to fault events. In these conditions the output FETs could be commanded on into high $R_{DS(on)}$ state with low gate drive voltage level. Or worse when V_{DRV} is completely lost, either the HS FET or LS FET or both can turn-on due to the output FET leakage current, especially at higher temperature. This could cause a short circuit across the C_{IN} capacitor.

The EPC23103 integrates protection circuits as shown in Figure 13 (below) and the Truth Table (page 6).

Figure 13: Simplified circuit diagram of the protection circuits against low voltage levels or complete loss of supplies



The Power On Reset (POR) circuit from the low side internal V_{DD} supply would turn off both HS and LS logic path when VDD voltage level is below the V_{DD_POR} threshold.

The Power On Reset (POR) circuit from the high side internal V_{BOOT} supply would turn on the HS logic path only when the V_{BOOT} bootstrap voltage rises above a starting threshold voltage level of 3.4 V (typical), and the output will become active. The output will become inactive after the V_{BOOT} bootstrap voltage falls 0.15 V below the starting threshold.

The IC features a sequencing protection that prevents the output FETs from turning on due to leakage when V_{DD} and V_{BOOT} are at a low voltage level and the input voltage is applied. When V_{BOOT} is low the active turn off circuit in Figure 13 will be powered by V_{IN} and will activate the Qoff switch to keep the high side FET (Q1) off. This protection allows user not to worry about sequencing..

Similar circuit is triggered by the low side loss of V_{DD} supply to turn on the Q_{OFF} switch for the LS FET (Q2). In this case the active turn off circuit is powered by the SW node voltage.

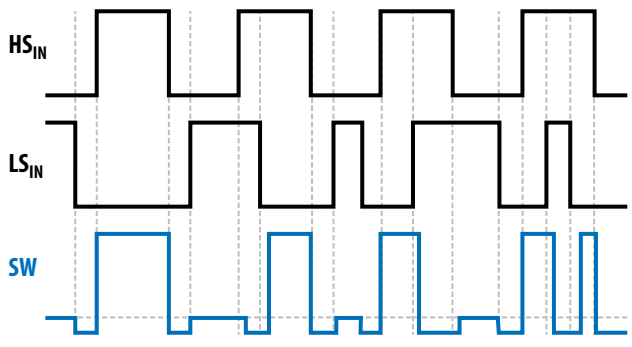
Logic Inputs

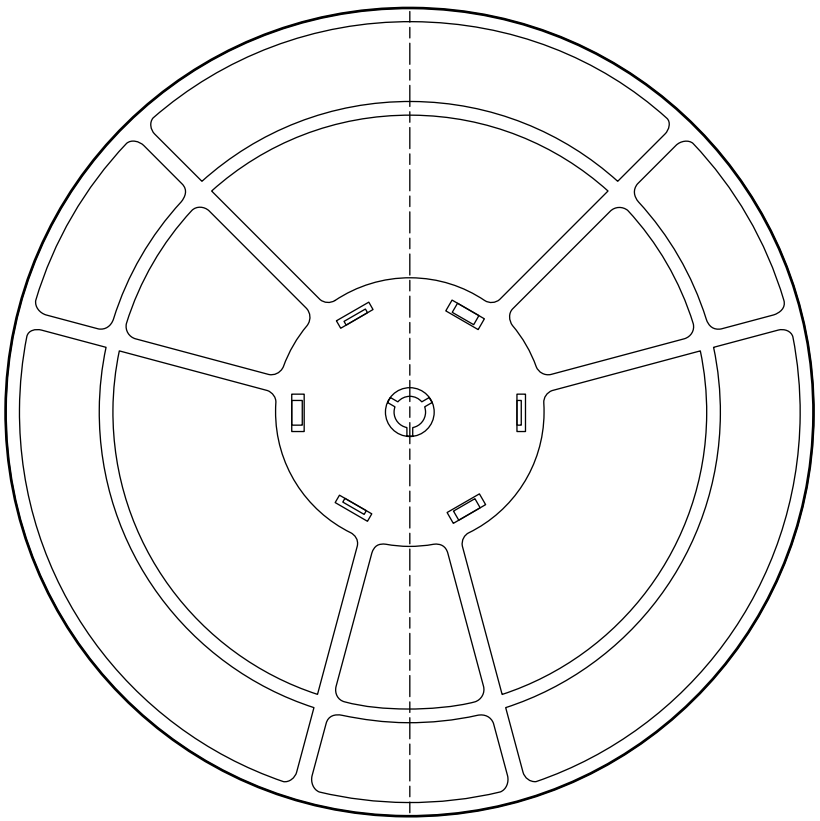
The EPC23103 IC is capable of interfacing to digital and analog controllers with 3.3 V or 5 V CMOS logic levels. The logic level translator at the frontend level- shifts the PWM signal, HS_{IN} and LS_{IN} respectively, to internal IC level to operate the logic, level shifting and gate drive circuits. Logic input thresholds are 2.4 V minimum to trigger a "high" state and 0.8 V maximum for a guaranteed "low" state. A hysteresis of 300 mV is built-in to increase noise margin.

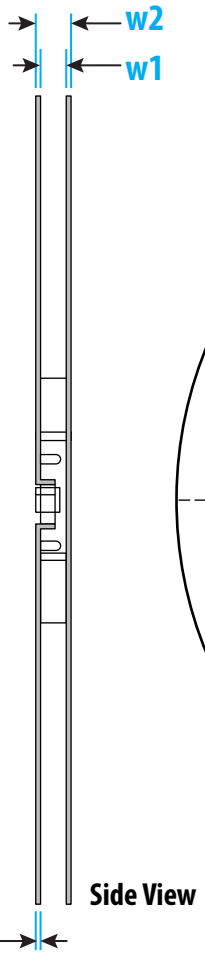
For interfacing with analog controller operating from V_{CC} = 12 V that outputs a 12 V PWM signal, a resistor network in series should be inserted to divide the voltage to acceptable V_{IH} level and limit the input current into the logic input pins HS_{IN} and LS_{IN} which is clamped to the V_{DD} supply by ESD protection network.

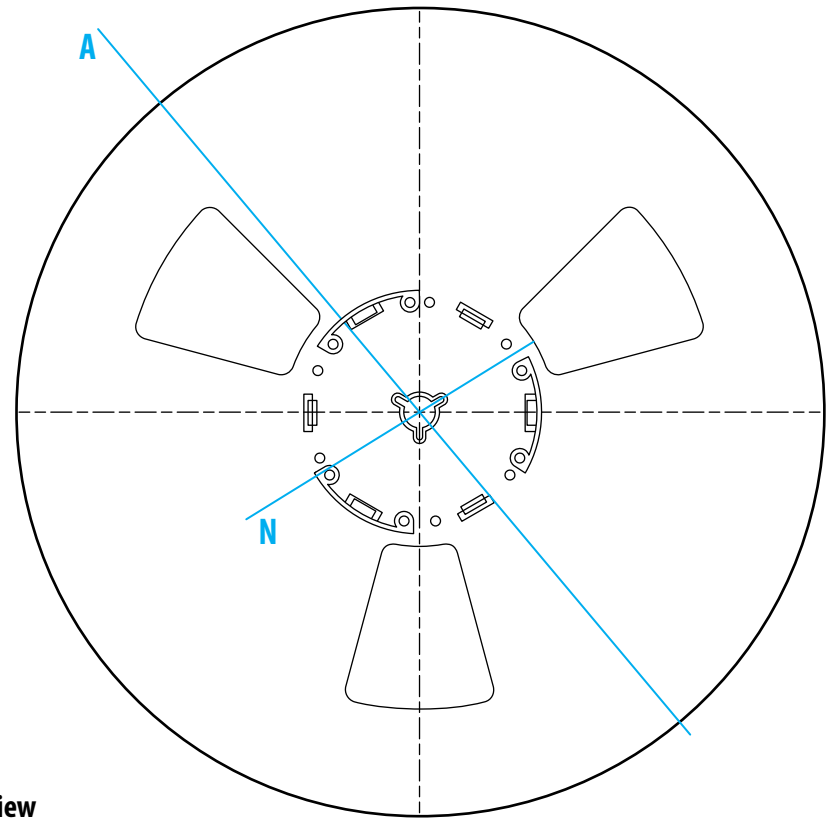
Separate and independent high side (HS_{IN}) and low side (LS_{IN}) logic control inputs allow external controllers to set fixed or adaptive deadtimes for optimal operating efficiency. Cross conduction lockout logic commands both FETs off when logic inputs are both high. Figure 14 shows how the logic inputs interact with each other. Here the timing diagram applies with the HS FET (Q1) and LS FET (Q2) in half-bridge configuration and current is in the positive direction going out of the half-bridge. When HS_{IN} and LS_{IN} are logic high at same time, both Q1 and Q2 will shut off. A built-in deadtime of 5 ns is added, after that current then commutates to Q2 in 3rd quadrant conduction and SW will be clamped at negative V_{SD} voltage of Q2.

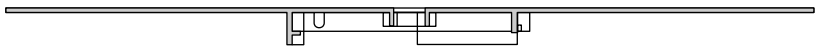
Figure 14: EPC23103 Input-to-Output Timing Diagram



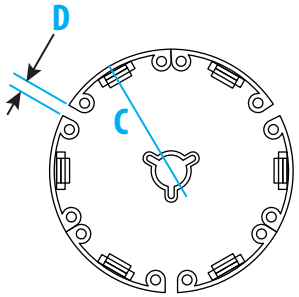




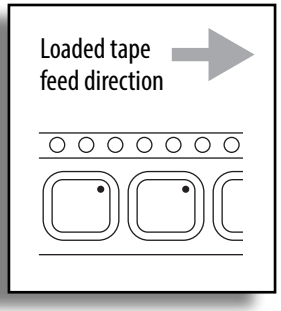




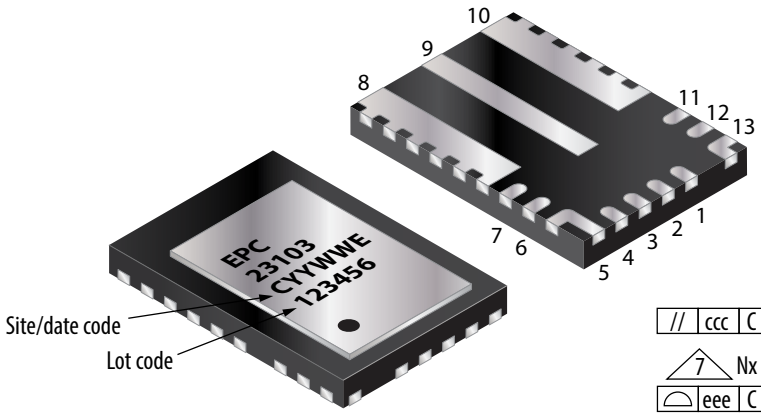
Top View Detail



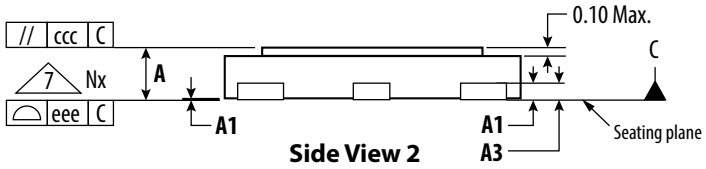
Bottom View Detail



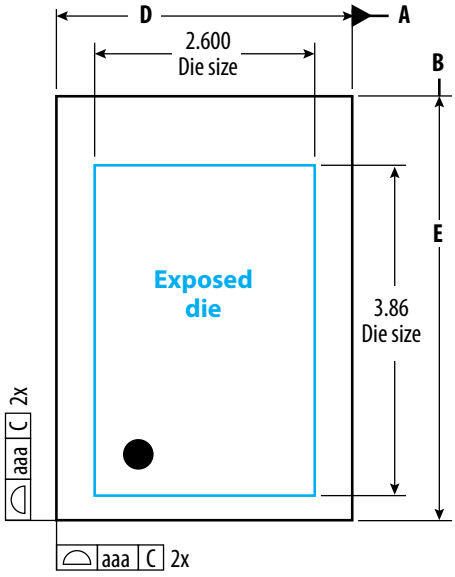
Type	A	N	C	D	w1	w2	T
8MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	8.4+1.5	14.4	2.1±0.5
12MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	12.4+1.5	18.4	2.1±0.5
16MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	16.4+1.5	22.4	2.1±0.5
24MM	Ø330±2	Ø100±2	Ø13.1±0.2	5.6±0.5	24.4+1.5	30,4	2.1±0.5



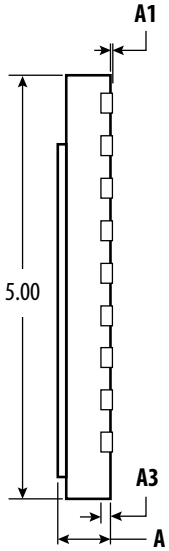
Pads 1-7, 11, 12 and 13 are IC pins;
Pad 9 is a SW pin ;
Pad 8 is a PGND pin and 10 is a V_{IN} pin



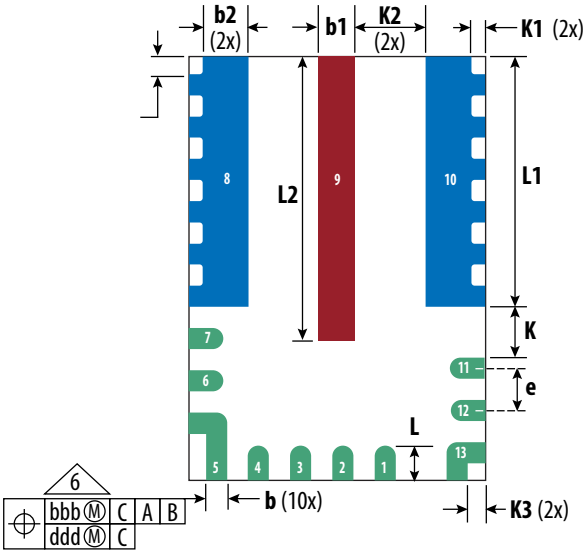
Side View 2



Top View



Side View 1



Bottom View

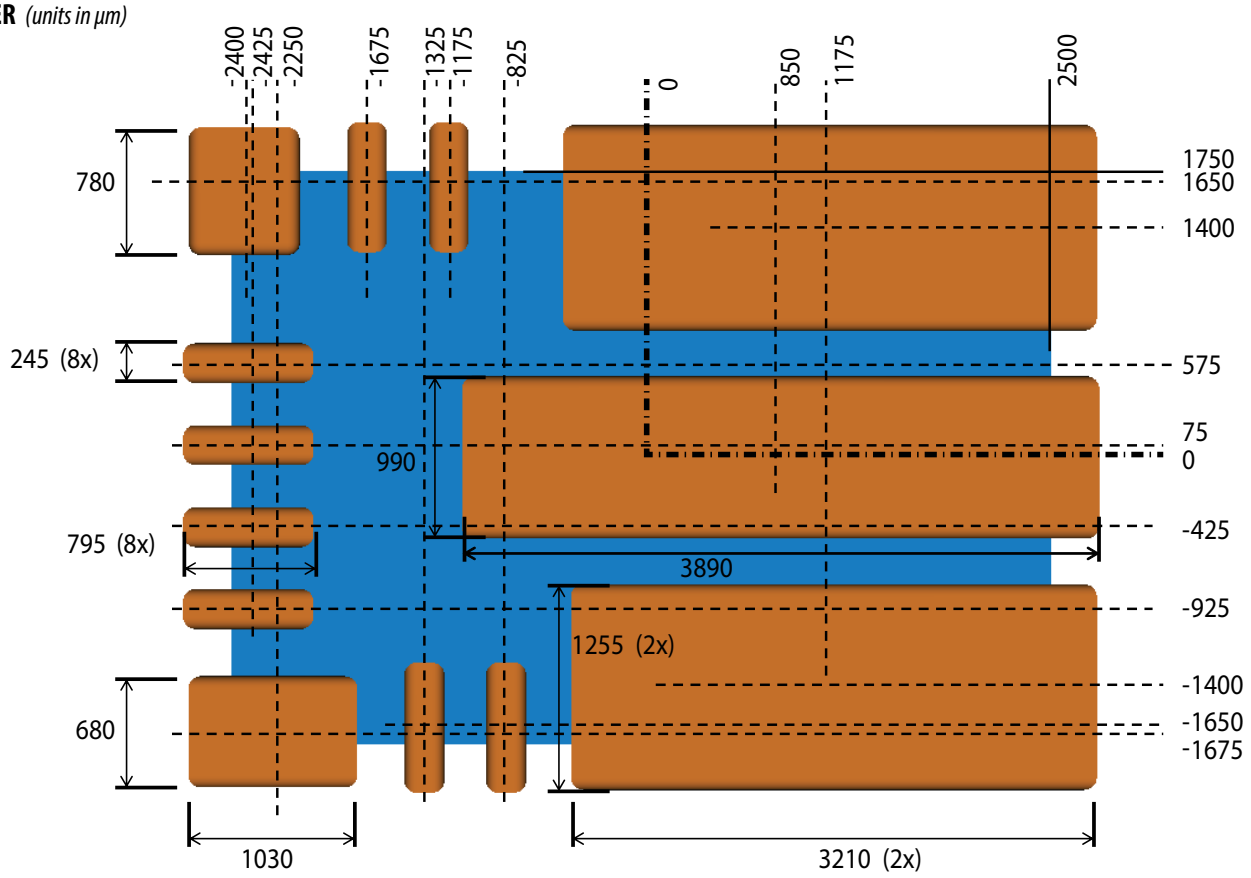
SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
A	0.60	0.65	0.70	
A1	0.00	0.02	0.05	
A3		0.20 Ref		
b	0.20	0.25	0.30	6
b1	0.38	0.43	0.48	6
b2	0.49	0.54	0.59	
D		3.50 BSC		
E		5.00 BSC		
e		0.50 BSC		
K	0.55	0.60	0.65	
K1	0.12	0.17	0.22	
K2	0.775	0.825	0.875	
K3	0.15	0.20	0.25	

SYMBOL	Dimension (mm)			
	MIN	Nominal	MAX	Note
L	0.30	0.40	0.50	
L1	2.85	2.95	3.05	
L2	3.25	3.35	3.45	
aaa		0.05		
bbb		0.10		
ccc		0.10		
ddd		0.05		
eee		0.08		
N		13		3
ND		6		5
NE		4		5
Notes		1, 2		

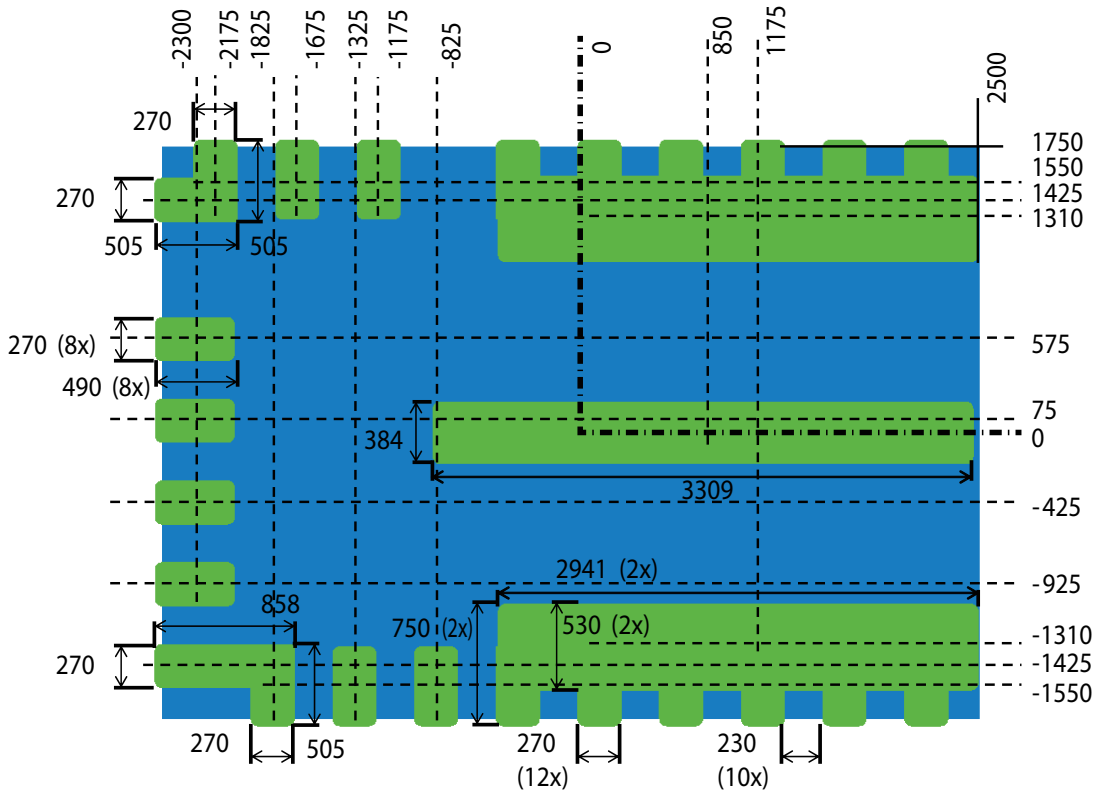
Notes:

1. Dimensioning and tolerancing conform to ASME Y14.5-2009
2. All dimensions are in millimeters
3. **N** is the total number of terminals
4. Dimension **b** applies to the metallized terminal. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area.
5. **ND** and **NE** refer to the number of terminals on each **D** and **E** side respectively.
6. Dimension **b** applies to the metallized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has a radius on the other end of it, dimension **b** should not be measured in that radius area.
7. Coplanarity applies to the terminals and all the other bottom surface metallization.

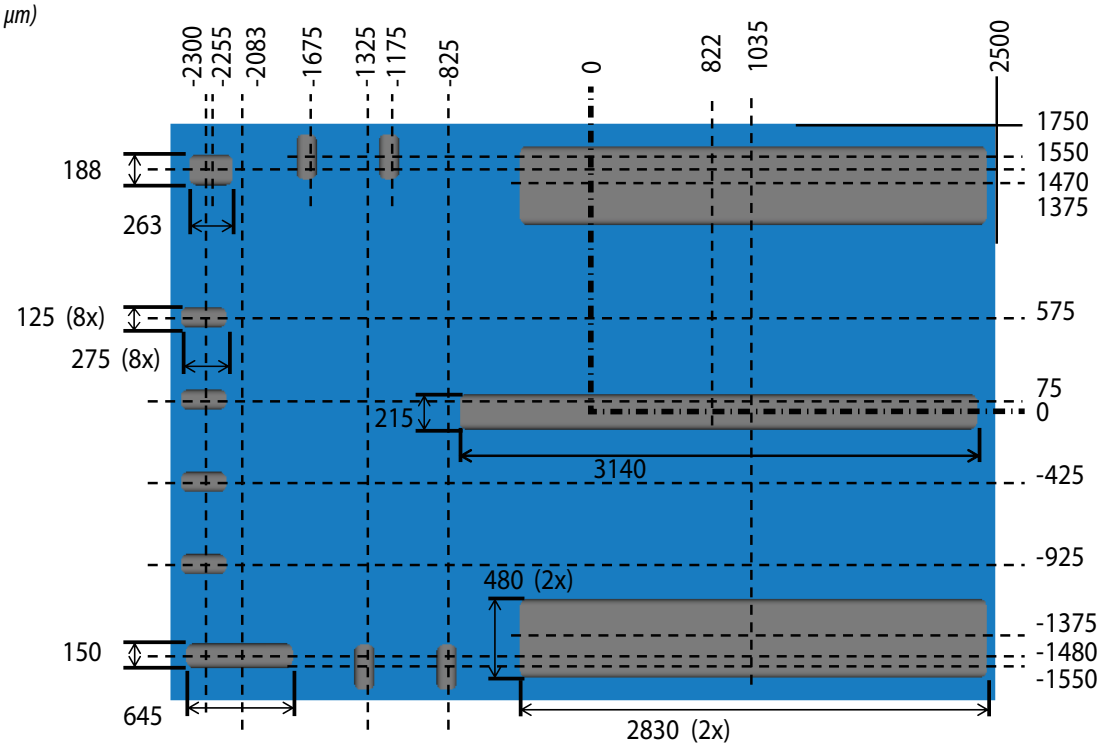
COPPER *(units in µm)*



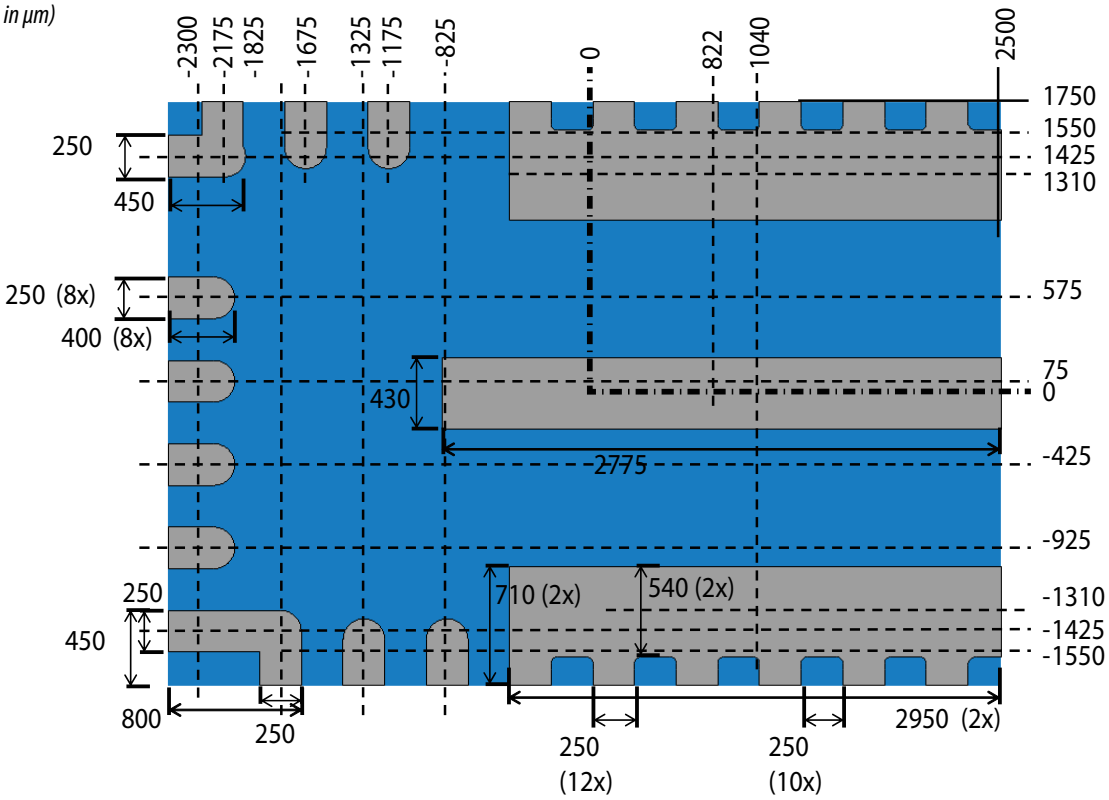
SOLDER MASK *(units in µm)*



PASTE *(units in µm)*



PACKAGE *(units in µm)*



Errata Sheet

STATUS	VERSION	DATE	REMARK
ENGRT	1.1	12/09/2022	The following features and parameters do not meet the datasheet description and specifications: 1) The maximum operating VIN voltage should not exceed 64 V 2) The maximum transient voltage at the output switch node SW, should not exceed 70 V. Recommend to use at least 4.7 Ω for R_{BOOT} and R_{DRV} to module the over-voltage spike above VIN rail and below PGND to less than 10 V.