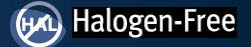


## EPC2069 – Enhancement Mode Power Transistor

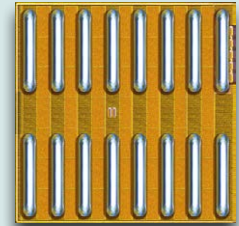
 $V_{DS}$ , 40 V $R_{DS(on)}$ , 2.25 m $\Omega$  $I_D$ , 80 A

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
PARAMETER		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage (Continuous)	40	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	48	
$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ )	80	A
	Pulsed ( $25^\circ\text{C}$ , $T_{PULSE} = 300 \mu\text{s}$ )	422	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
$T_J$	Operating Temperature	-40 to 150	$^\circ\text{C}$
$T_{STG}$	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.35	$^\circ\text{C}/\text{W}$
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	1.1	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	46	

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See [https://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details.



EPC2069 eGaN® FETs are supplied only in passivated die form with solder bars. Die Size: 3.25 x 3.25 mm

### Applications

- High frequency DC-DC Converters
- BLDC Motor Drives
- Sync Rectification for AC-DC and DC-DC

### Benefits

- High Power Density
- High Efficiency
- No Reverse Recovery
- Ultra Low  $Q_G$
- Small Footprint
- High Frequency Capability



Static Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0 \text{ V}$ , $I_D = 0.7 \text{ mA}$	40			V
$I_{DSS}$	Drain-Source Leakage	$V_{GS} = 0 \text{ V}$ , $V_{DS} = 32 \text{ V}$		0.01	0.7	mA
$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5 \text{ V}$		0.01	4	
	Gate-to-Source Forward Leakage <sup>#</sup>	$V_{GS} = 5 \text{ V}$ , $T_J = 125^\circ\text{C}$		0.05	9	
	Gate-to-Source Reverse Leakage	$V_{GS} = -4 \text{ V}$		0.01	0.8	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$ , $I_D = 14 \text{ mA}$	0.8	1.4	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5 \text{ V}$ , $I_D = 30 \text{ A}$		1.6	2.25	m $\Omega$
$V_{SD}$	Source-Drain Forward Voltage <sup>#</sup>	$I_S = 0.5 \text{ A}$ , $V_{GS} = 0 \text{ V}$		1.6		V

<sup>#</sup>Defined by design. Not subject to production test.

Dynamic Characteristics (T <sub>J</sub> = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C <sub>ISS</sub>	Input Capacitance	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V		1351	2027	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			32		
C <sub>OSS</sub>	Output Capacitance			1044	1566	
C <sub>OSS(ER)</sub>	Effective Output Capacitance, Energy Related (Note 2)	V <sub>DS</sub> = 0 to 20 V, V <sub>GS</sub> = 0 V		1465		pF
C <sub>OSS(TR)</sub>	Effective Output Capacitance, Time Related (Note 3)			1647		
R <sub>G</sub>	Gate Resistance			0.4		Ω
Q <sub>G</sub>	Total Gate Charge	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 5 V, I <sub>D</sub> = 30 A		12.5	16.2	nC
Q <sub>GS</sub>	Gate-to-Source Charge	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 30 A		3.9		
Q <sub>GD</sub>	Gate-to-Drain Charge			2.4		
Q <sub>G(TH)</sub>	Gate Charge at Threshold			2.9		
Q <sub>OSS</sub>	Output Charge	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V		32	48	
Q <sub>RR</sub>	Source-Drain Recovery Charge			0		

Note 2: C<sub>OSS(ER)</sub> is a fixed capacitance that gives the same stored energy as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 50% BV<sub>DSS</sub>.  
 Note 3: C<sub>OSS(TR)</sub> is a fixed capacitance that gives the same charging time as C<sub>OSS</sub> while V<sub>DS</sub> is rising from 0 to 50% BV<sub>DSS</sub>.

Figure 1: Typical Output Characteristics at 25°C

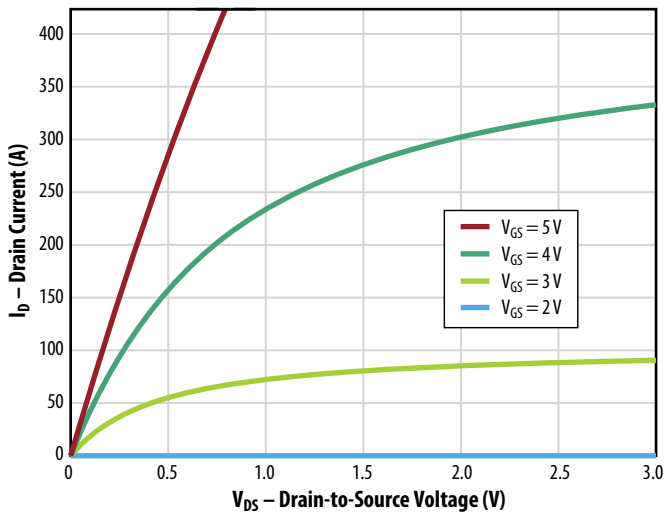


Figure 2: Typical Transfer Characteristics

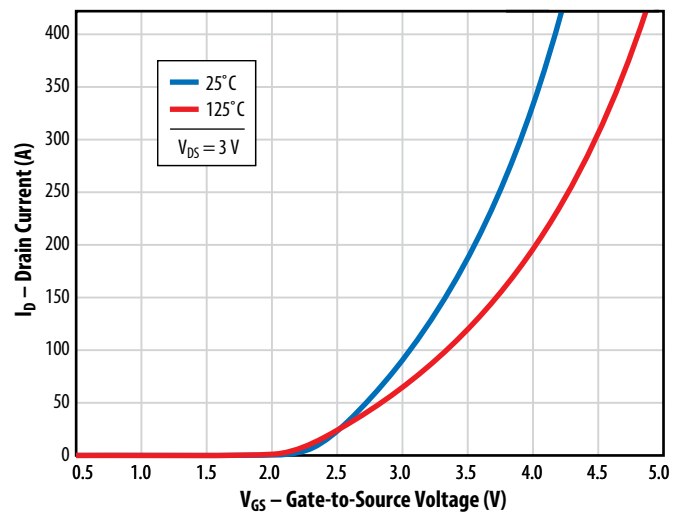


Figure 3: R<sub>DS(on)</sub> vs. V<sub>GS</sub> for Various Drain Currents

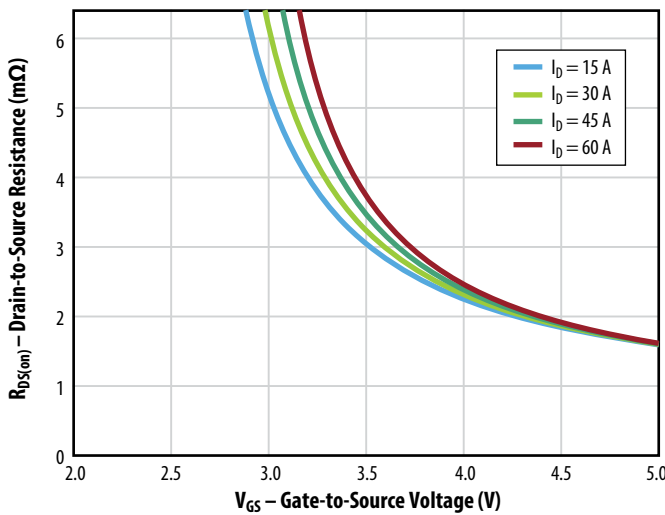


Figure 4: R<sub>DS(on)</sub> vs. V<sub>GS</sub> for Various Temperatures

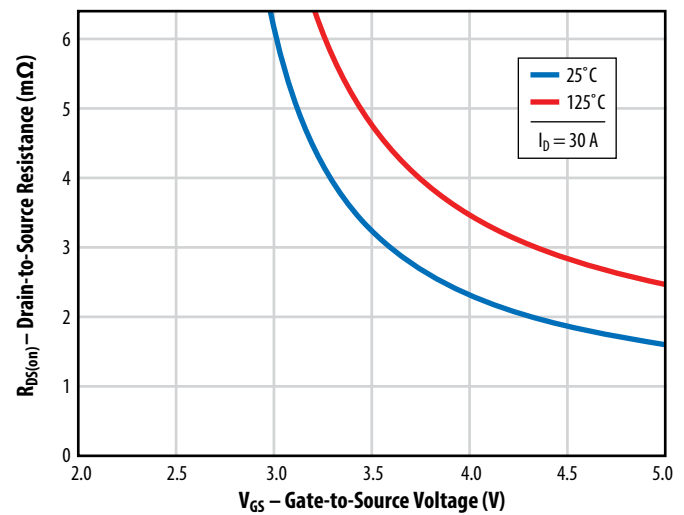


Figure 5a: Capacitance (Linear Scale)

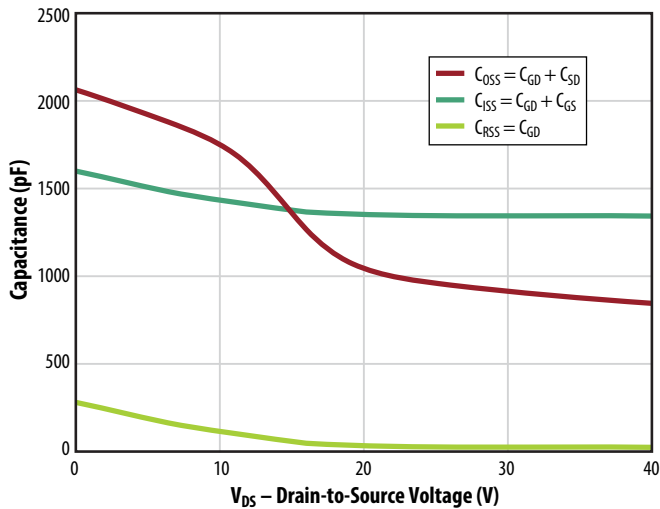


Figure 5b: Capacitance (Log Scale)

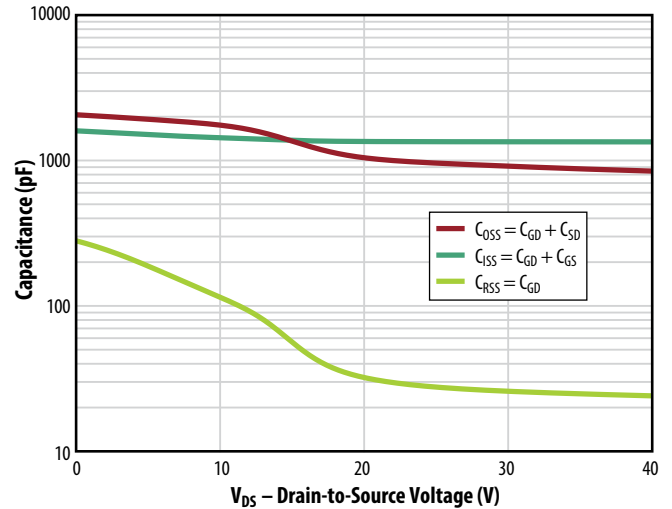


Figure 6: Output Charge and  $C_{OSS}$  Stored Energy

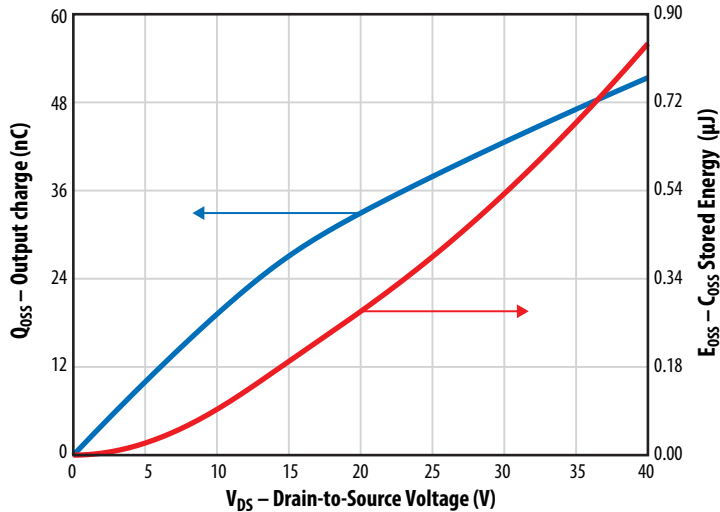


Figure 7: Gate Charge

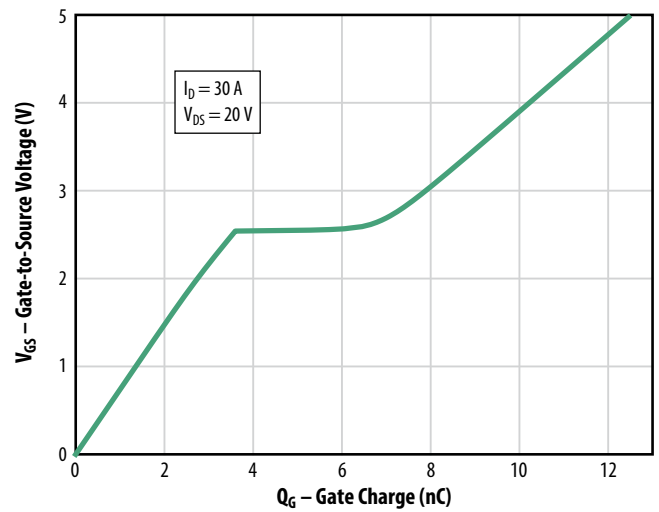


Figure 8: Reverse Drain-Source Characteristics

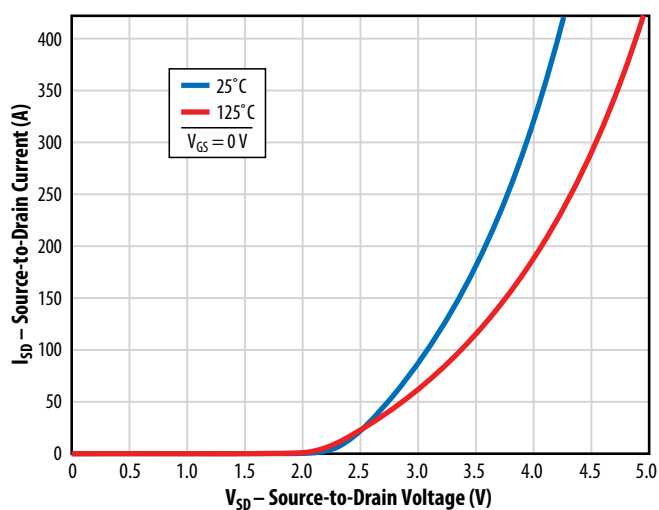


Figure 9: Normalized On-State Resistance vs. Temperature

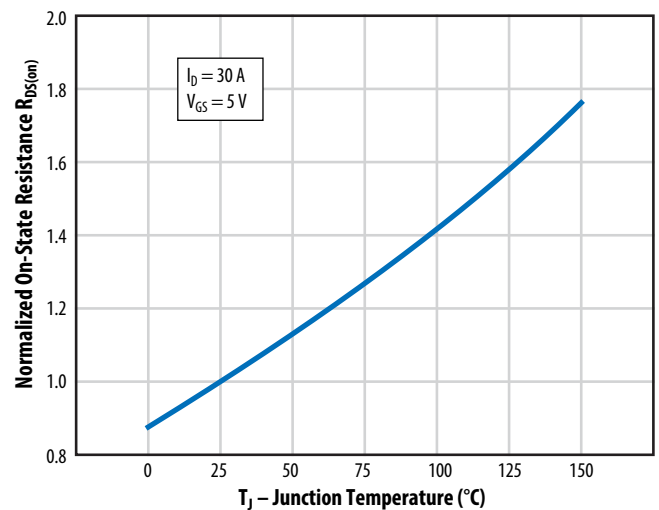


Figure 10: Normalized Threshold Voltage vs. Temperature

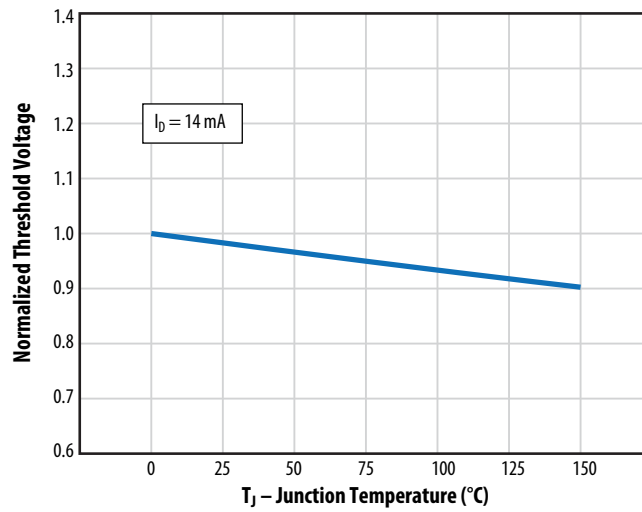


Figure 10: Transient Thermal Response Curves

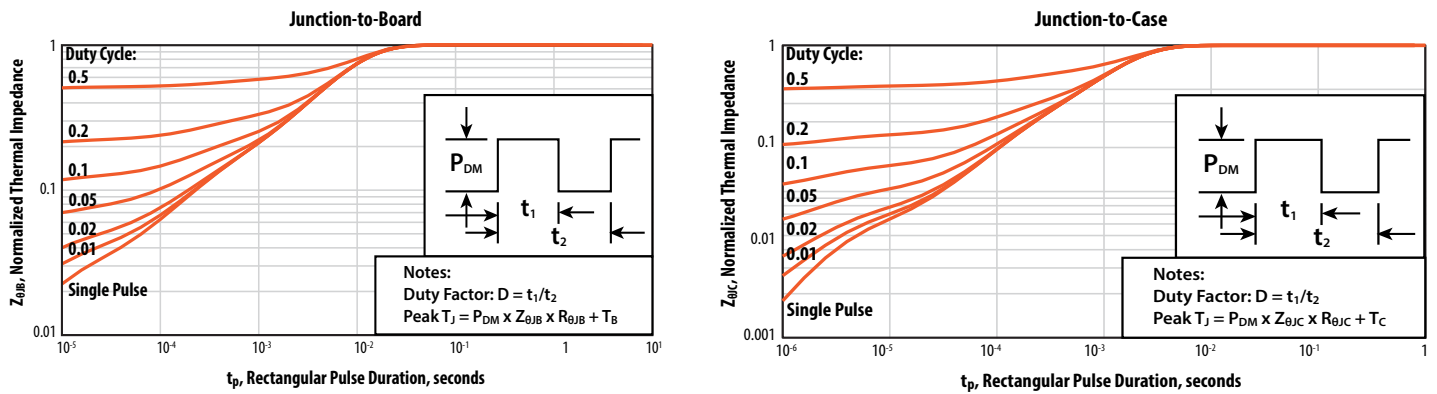
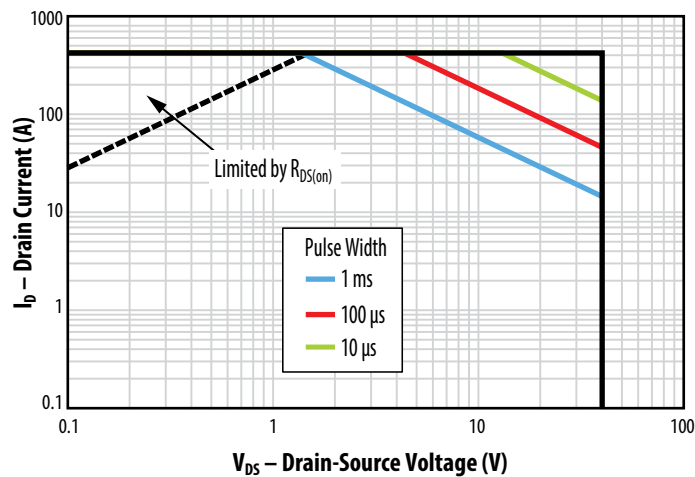
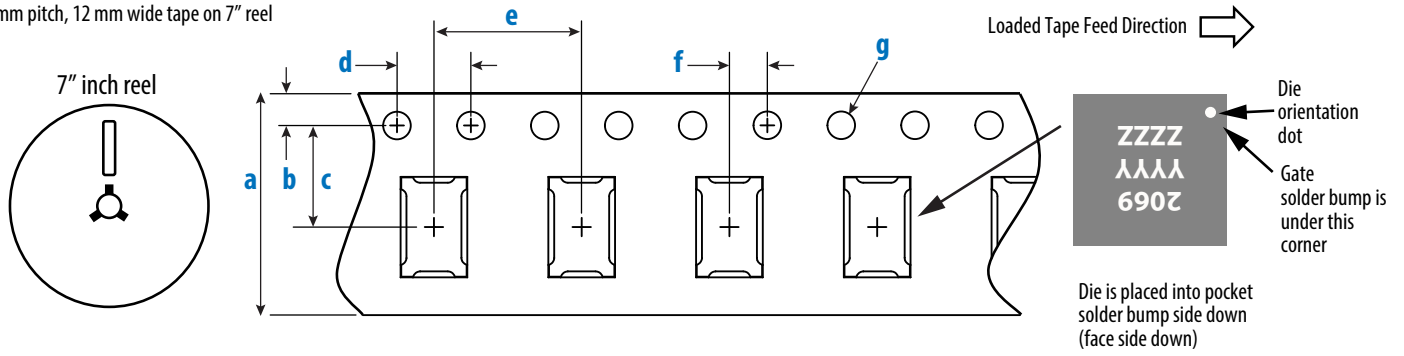


Figure 11: Safe Operating Area



**TAPE AND REEL CONFIGURATION**

8 mm pitch, 12 mm wide tape on 7" reel

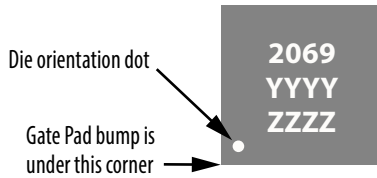


EPC2069 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
<b>a</b>	12.00	11.90	12.30
<b>b</b>	1.75	1.65	1.85
<b>c</b> (Note 2)	5.50	5.45	5.55
<b>d</b>	4.00	3.90	4.10
<b>e</b>	8.00	7.90	8.10
<b>f</b> (Note 2)	2.00	1.95	2.05
<b>g</b>	1.50	1.50	1.60

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

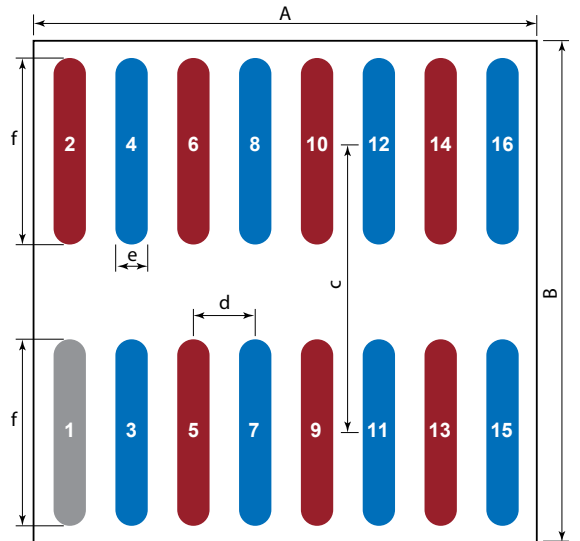
**DIE MARKINGS**



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2069	2069	YYYY	ZZZZ

**DIE OUTLINE**

Solder Bump View



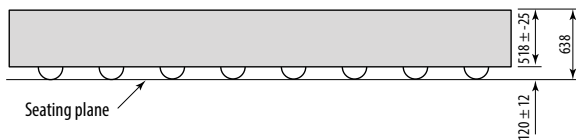
DIM	Micrometers		
	MIN	Nominal	MAX
<b>A</b>	3220	3250	3280
<b>B</b>	3220	3250	3280
<b>c</b>		1805	
<b>d</b>		400	
<b>e</b>	180	200	220
<b>f</b>	1175	1195	1215

Pad 1 is Gate;

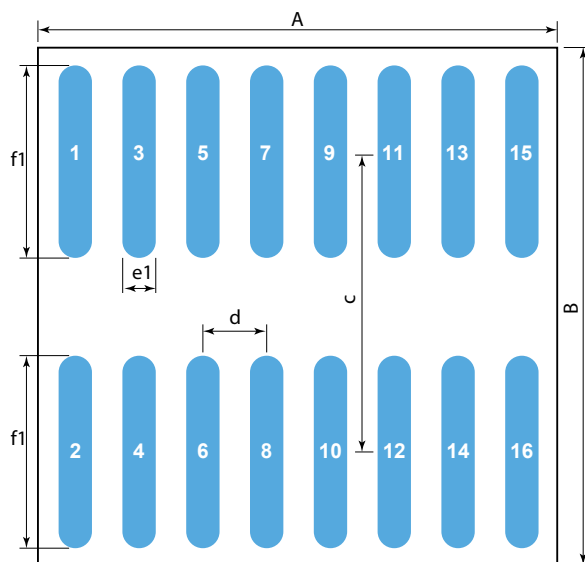
Pads 2,5,6,9,10,13,14 are Source;

Pads 3,4,7,8,11,12,15,16 are Drain

Side View



**RECOMMENDED LAND PATTERN**  
(units in  $\mu\text{m}$ )



Land pattern is solder mask defined  
Solder mask opening is  $10\ \mu\text{m}$

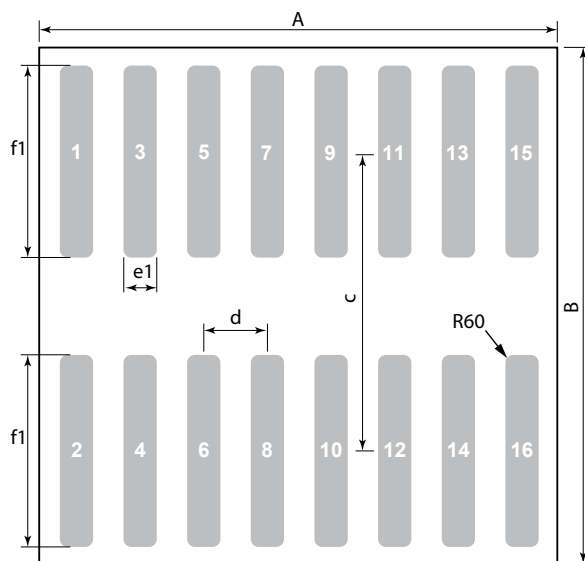
Pad 1 is Gate;

Pads 2,5,6,9,10,13, 14 are Source;

Pads 3,4,7,8,11,12, 15,16 are Drain

DIM	Micrometers
<b>A</b>	3250
<b>B</b>	3250
<b>c</b>	1805
<b>d</b>	400
<b>e1</b>	180
<b>f1</b>	1175

**RECOMMENDED STENCIL DRAWING**  
(units in  $\mu\text{m}$ )



DIM	Micrometers
<b>A</b>	3250
<b>B</b>	3250
<b>c</b>	1805
<b>d</b>	400
<b>e1</b>	180
<b>f1</b>	1175

Recommended stencil should be 4 mil ( $100\ \mu\text{m}$ ) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at <https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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Revised June 2022