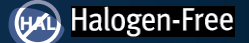


# EPC2066 – Enhancement Mode Power Transistor

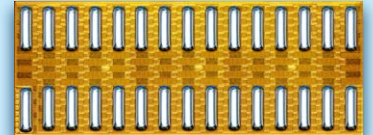
 $V_{DS}, 40\text{ V}$ 
 $R_{DS(on)}, 1.1\text{ m}\Omega\text{ max}$ 
 $I_D, 90\text{ A}$ 


Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

## Application Notes:

- Easy-to-use and reliable gate, Gate Drive ON = 5 V typical, OFF = 0 V (negative voltage not needed)
- Top of FET is electrically connected to source

## Questions:



6.05 x 2.3 mm

EPC2066 eGaN® FETs are supplied in passivated die form with solder bumps.

## Maximum Ratings

PARAMETER		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage (Continuous)	40	V
	Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	48	
$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ )	90	A
	Pulsed (25°C, $T_{PULSE} = 300\ \mu\text{s}$ )	639	
$V_{GS}$	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
$T_J$	Operating Temperature	-40 to 150	°C
$T_{STG}$	Storage Temperature	-40 to 150	

## Thermal Characteristics

PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Case TOP)	0.3	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board (Case BOTTOM)	1.0	
$R_{\theta JA\_JEDEC}$	Thermal Resistance, Junction-to-Ambient (using JEDEC 51-2 PCB)	51	
$R_{\theta JA\_EVB}$	Thermal Resistance, Junction-to-Ambient (using EPC90122 EVB)	29	

## Static Characteristics ( $T_J = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 1.2\text{ mA}$	40			V
$I_{DSS}$	Drain-Source Leakage	$V_{GS} = 0\text{ V}, V_{DS} = 32\text{ V}$		0.006	1.0	mA
$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.006	4.0	
	Gate-to-Source Forward Leakage <sup>#</sup>	$V_{GS} = 5\text{ V}, T_J = 125^\circ\text{C}$		0.2	9.0	
	Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		0.007	0.3	
$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 28\text{ mA}$	0.7	1.2	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}, I_D = 50\text{ A}$		0.8	1.1	mΩ
$V_{SD}$	Source-Drain Forward Voltage <sup>#</sup>	$I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}$		1.5		V

<sup>#</sup> Defined by design. Not subject to production test.

## Applications

- High Density DC-DC Conversion
- Motor Drive
- Industrial Automation
- Synchronous Rectification
- Inrush Protection
- Point-of-Load (POL) Converters

## Benefits

- Ultra High Efficiency
- Higher Switching Frequency
- Very Low  $R_{DS(on)}$ ,  $Q_G$ ,  $Q_{GD}$ ,  $Q_{OSS}$  and  $0\text{ }Q_{RR}$
- Small Footprint

Scan QR code or click link below for more information including reliability reports, device models, demo boards!



<https://l.ead.me/EPC2066>

Dynamic Characteristics# ( $T_J = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$C_{ISS}$	Input Capacitance	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}$		3539	4523	pF
$C_{RSS}$	Reverse Transfer Capacitance			30		
$C_{OSS}$	Output Capacitance			1670	1919	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 1)	$V_{DS} = 0\text{ to }20\text{ V}, V_{GS} = 0\text{ V}$		2431		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 2)			2970		
$R_G$	Gate Resistance			0.4		$\Omega$
$Q_G$	Total Gate Charge	$V_{DS} = 20\text{ V}, V_{GS} = 5\text{ V}, I_D = 50\text{ A}$		25	33	nC
$Q_{GS}$	Gate to Source Charge	$V_{DS} = 20\text{ V}, I_D = 50\text{ A}$		8.9		
$Q_{GD}$	Gate to Drain Charge			3.2		
$Q_{G(TH)}$	Gate Charge at Threshold			6.7		
$Q_{OSS}$	Output Charge	$V_{GS} = 0\text{ V}, V_{DS} = 20\text{ V}$		59	78	
$Q_{RR}$	Source-Drain Recovery Charge			0		

# Defined by design. Not subject to production test.

All measurements were done with substrate shorted to source.

Note 1:  $C_{OSS(ER)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

Note 2:  $C_{OSS(TR)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

Figure 1: Typical Output Characteristics at 25°C

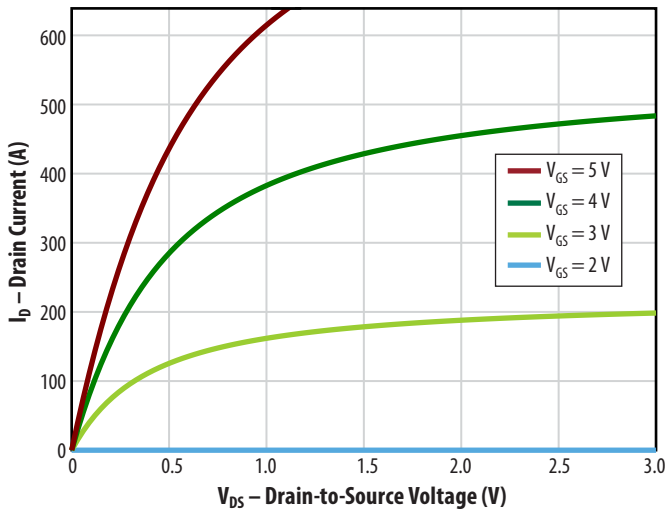


Figure 2: Typical Transfer Characteristics

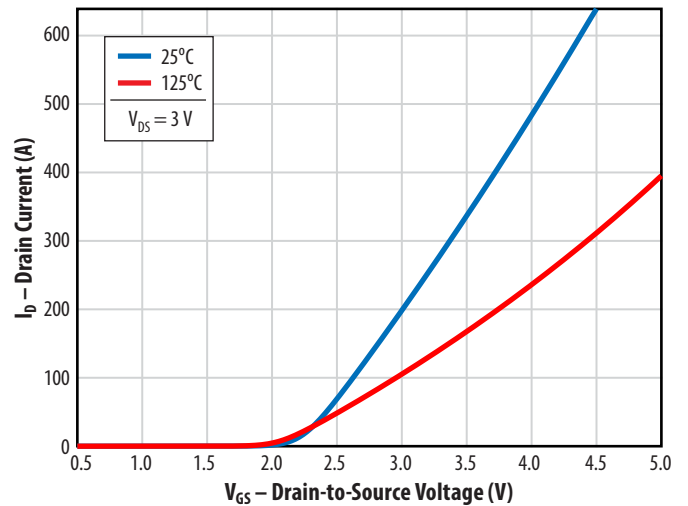


Figure 3:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Currents

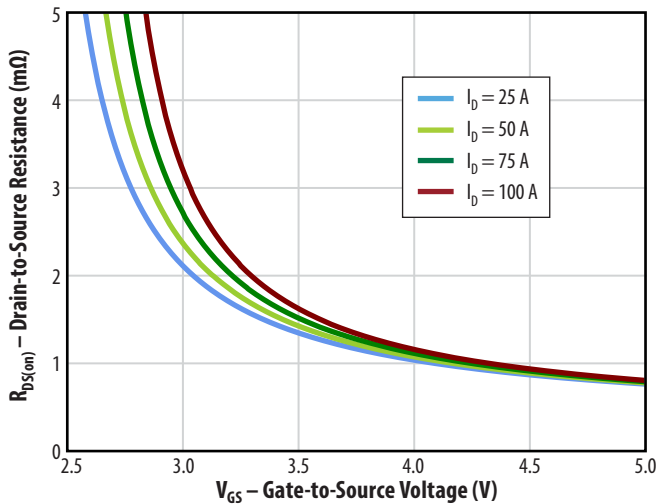


Figure 4:  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Temperatures

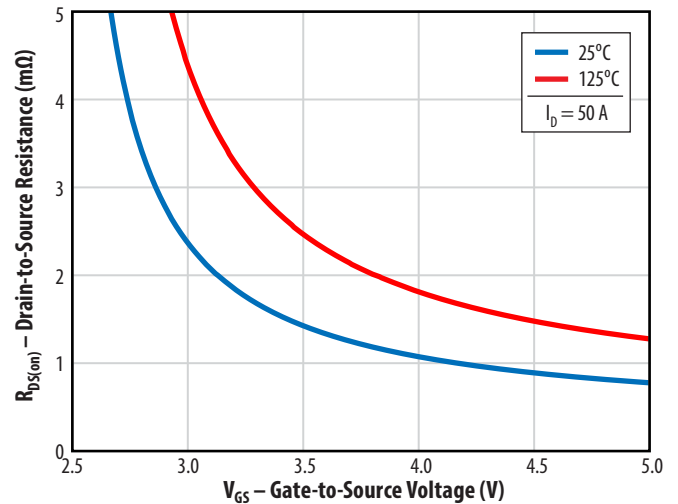


Figure 5a: Typical Capacitance (Linear Scale)

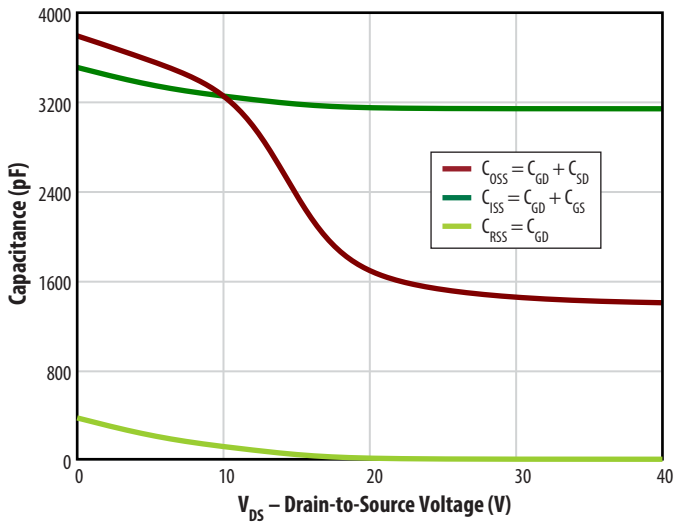


Figure 5b: Typical Capacitance (Log Scale)

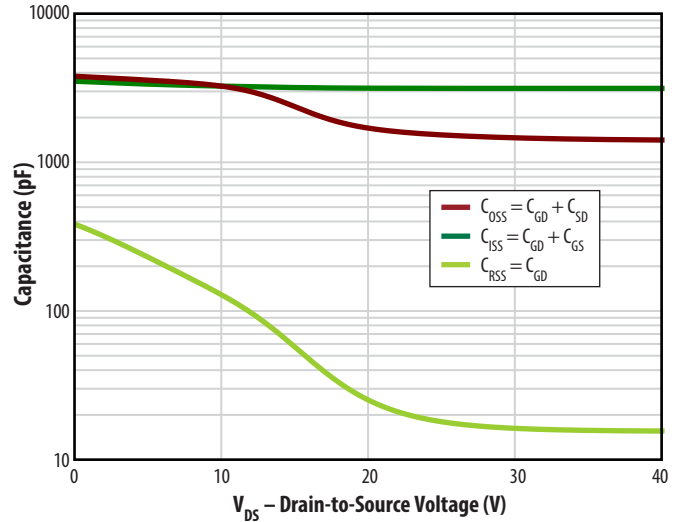


Figure 6: Typical Output Charge and  $C_{OSS}$  Stored Energy

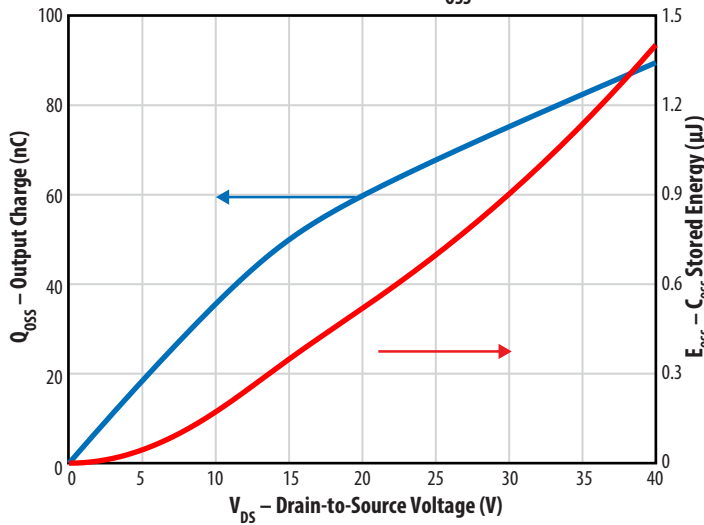


Figure 7: Typical Gate Charge

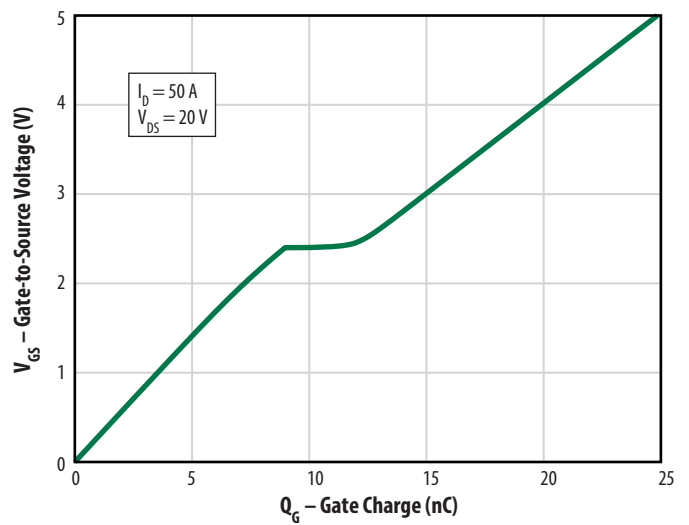


Figure 8: Reverse Drain-Source Characteristics

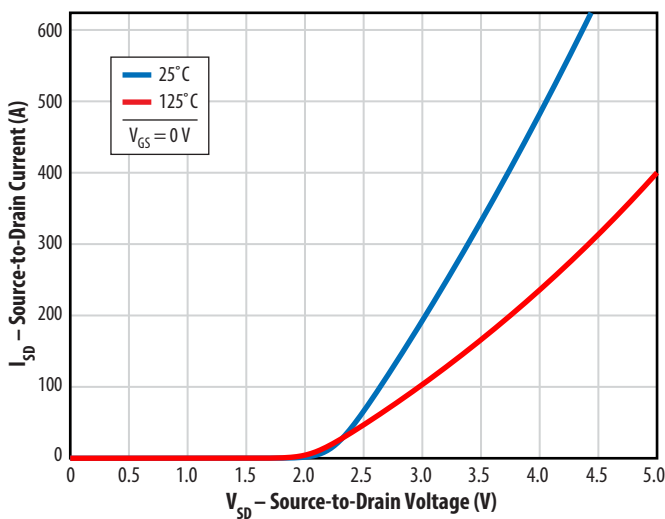
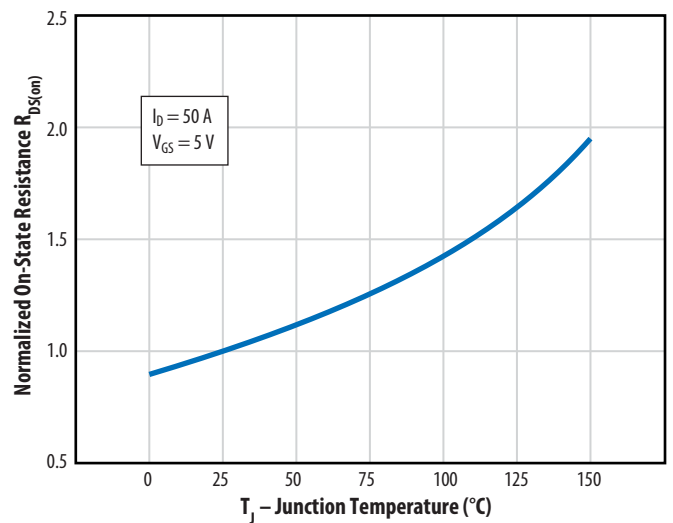


Figure 9: Normalized On-State Resistance vs. Temperature



Note: Negative gate drive voltage increases the reverse drain-source voltage.  
EPC recommends 0 V for OFF.

Figure 10: Normalized Threshold Voltage vs. Temperature

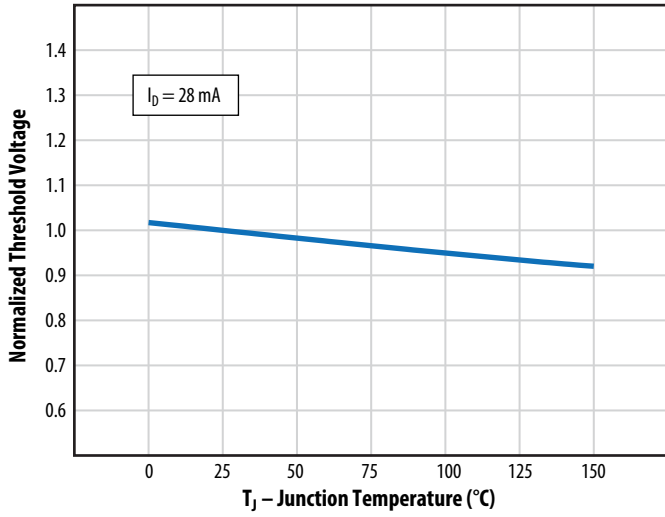


Figure 11: Safe Operating Area

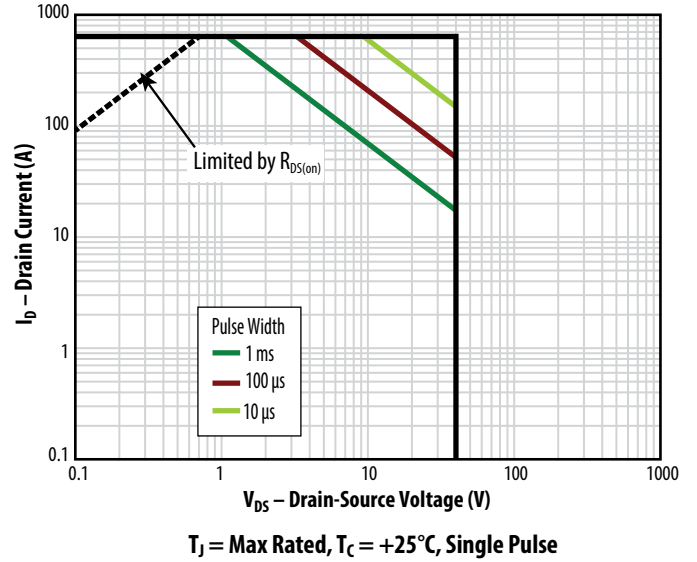
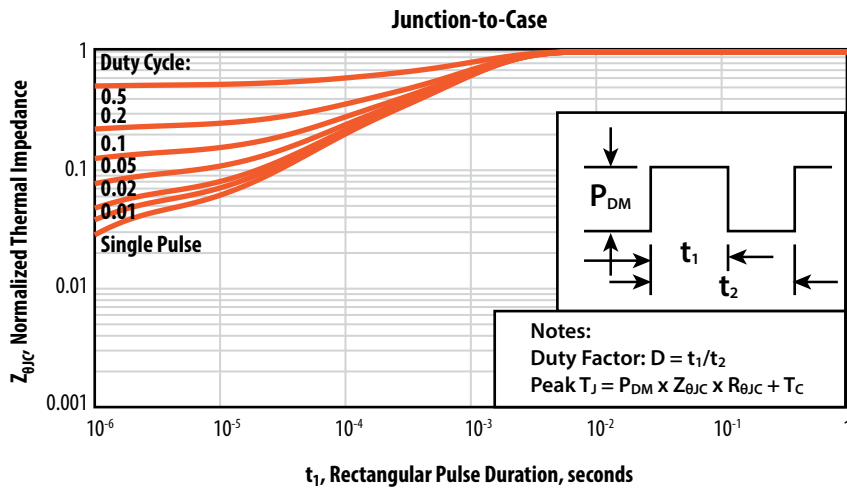
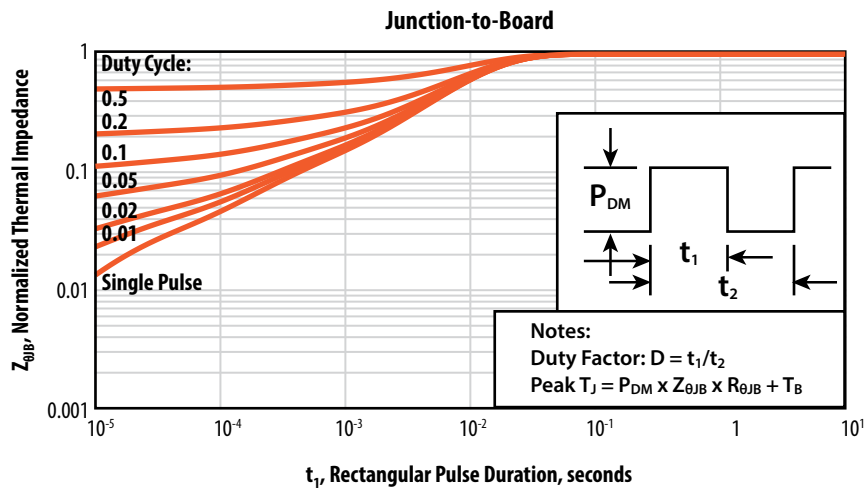
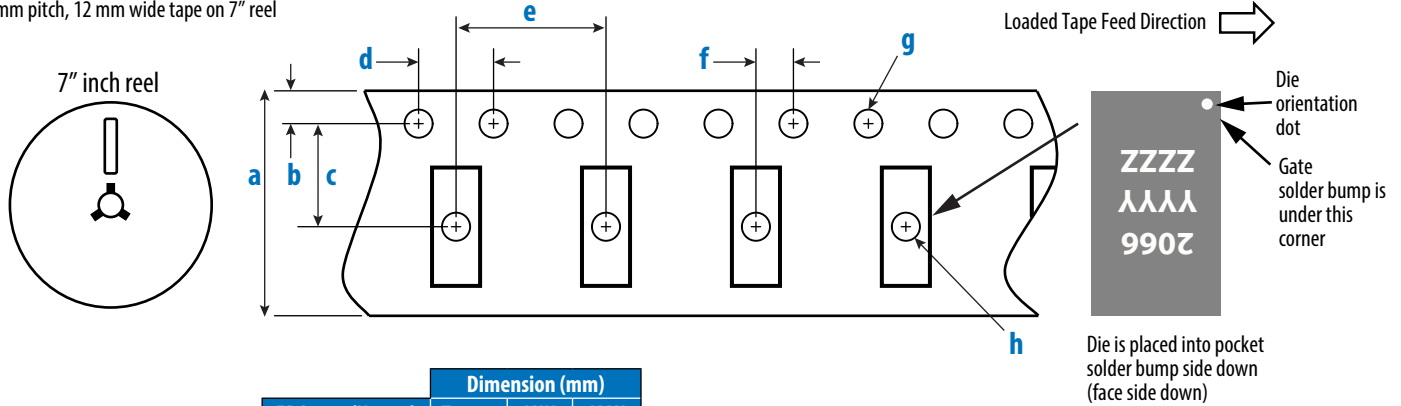


Figure 12: Transient Thermal Response Curves



**TAPE AND REEL CONFIGURATION**

8 mm pitch, 12 mm wide tape on 7" reel

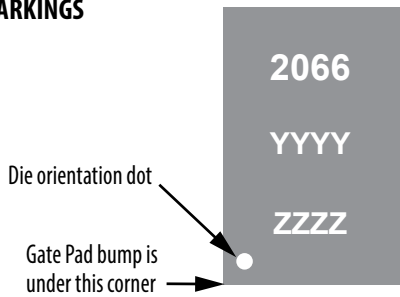


EPC2066 (Note 1)	Dimension (mm)		
	Target	MIN	MAX
a	12.00	11.90	12.30
b	1.75	1.65	1.85
c (Note 2)	5.50	5.45	5.55
d	4.00	3.90	4.10
e	8.00	7.90	8.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.50	1.50	1.75

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

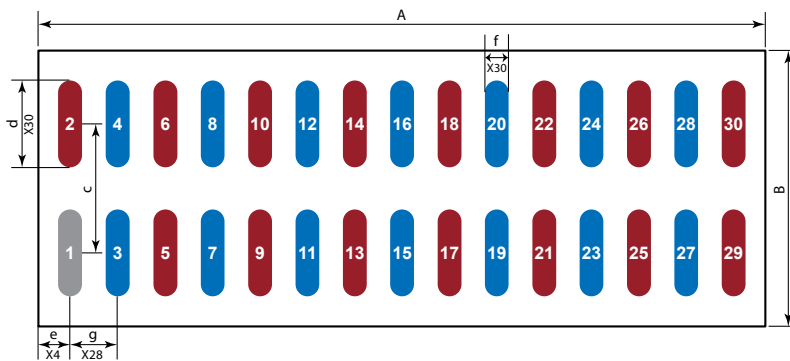
**DIE MARKINGS**



Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2066	2066	YYYY	ZZZZ

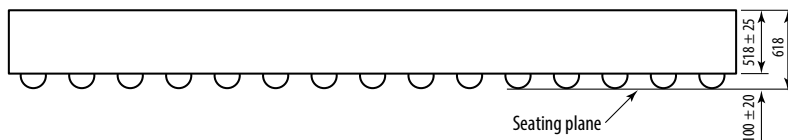
**DIE OUTLINE**

Solder Bump View



DIM	Micrometers		
	MIN	Nominal	MAX
A	6020	6050	6080
B	2270	2300	2330
c		1330	
d		720	
e		225	
f		200	
g		400	

Side View



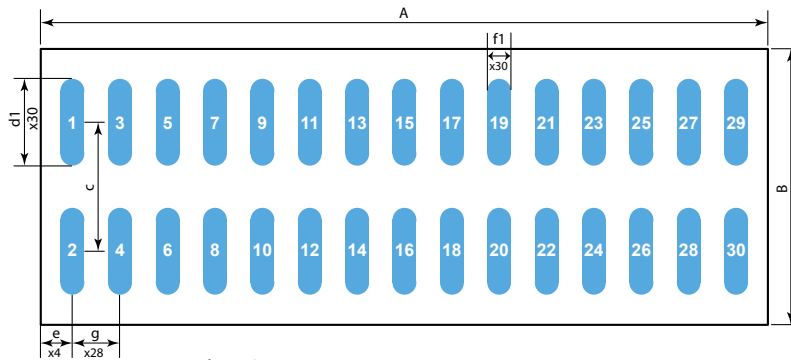
Pad 1 is Gate;

**Pads 2, 5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29, 30 are Source;**

**Pads 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28 are Drain**

Note: Substrate (top side) connected to source

**RECOMMENDED LAND PATTERN**  
(units in  $\mu\text{m}$ )

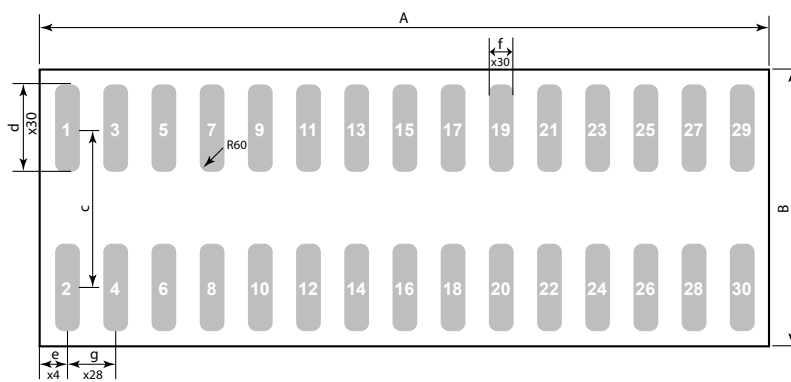


Pad 1 is Gate;  
 Pads 2, 5, 6, 9, 10, 13, 14, 17, 18, 21, 22, 25, 26, 29, 30 are Source;  
 Pads 3, 4, 7, 8, 11, 12, 15, 16, 19, 20, 23, 24, 27, 28 are Drain

Land pattern is solder mask defined.

DIM	Micrometers
A	6050
B	2300
c	1330
d1	700
e	225
f1	180
g	400

**RECOMMENDED STENCIL DRAWING**  
(units in  $\mu\text{m}$ )



Recommended stencil should be 4 mil (100  $\mu\text{m}$ ) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

DIM	Micrometers
A	6050
B	2300
c	1330
d	700
e	225
f	180
g	400

**Additional Resources Available**

- Assembly resources available at: <https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>
- Library of Altium footprints for production FETs and ICs: <https://epc-co.com/epc/documents/altium-files/EPC%20Altium%20Library.zip>  
(for preliminary device Altium footprints, contact EPC)

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