FMEMCU-UG-910070-17

FR60 FAMILY
SOCKET ADAPTER BOARD
EMA-MB91F467S-LS-176M07

USER GUIDE

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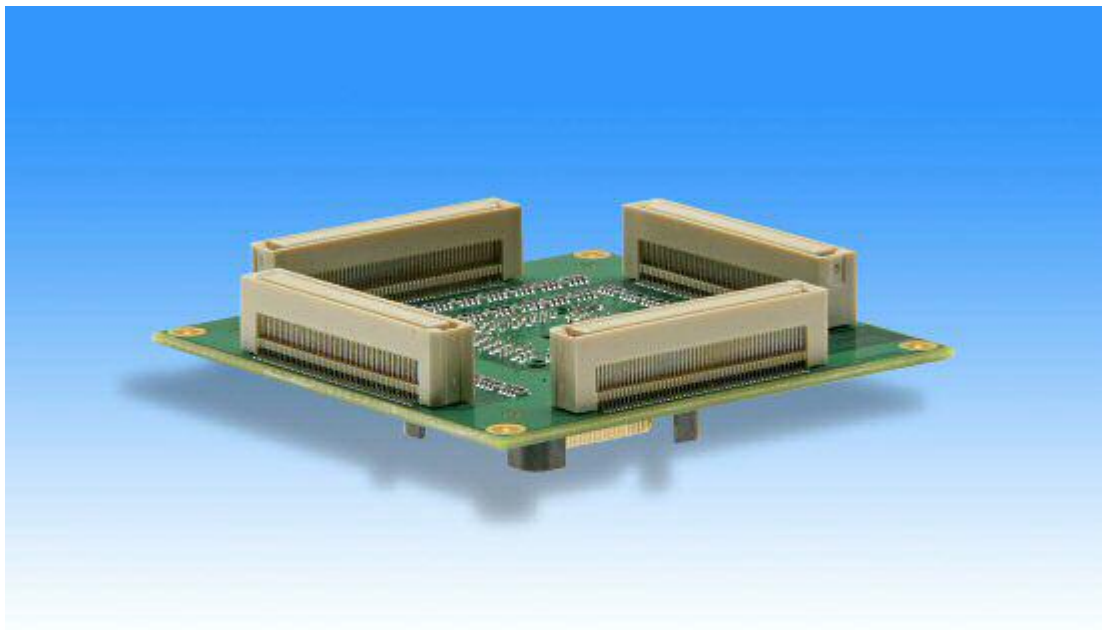
Revision History

Date	Issue
20.12.2007	V1.0, MB,AW,RH First creation
14.01.2008	V1.1, CPLD code and S401_4 default settings changed
14.01.2008	V1.2, CPLD code and default settings changed (SDRAM support)
15.01.2008	V1.3, Fig. 2.1 changed
07.04.2008	V1.4, China RoHS note added, CPLD code formatted, SDRAM removed
13.10.2008	V1.5, CEy Changed Figure 2.1, order of CS select switches interchanged, chapter 3.4 rewritten, some minor corrections and improved descriptions
16.01.2009	V1.6, CEy Description for EMA-MB91FV460B-001 and functional restrictions added
17.03.2009	V1.7, CEy Corrected numbering in chapter 1.3.2 and added hint regarding existing application note

Latest product revision: 1.1

Latest schematic revision: 1.1

Latest PCB revision: 1.0

Latest CPLD revision: 7S18

This document contains 26 pages.

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0 Contents

1 Overview

1.1 Abstract

The EMA-MB91F467S-LS-176M07 in combination with the EMA-MB91V460A-002B/-80/003 or EMA-MB91FV460B-001 is a development system for the Fujitsu FR60 MB91V460 Flash microcontroller.

The EMA-MB91F467S-LS-176M07 is an adapter board with level shifters to support the MB91V460A external bus interface at 3.3V levels.

The development system allows the designer immediately to start with the software development before MB91V460 based silicon samples are available.

This board must only be used for test applications in an evaluation laboratory environment.

Before using the EMA-MB91F467S-LS-176M07 adapter board, make sure that the following packed components have been delivered:

- o 1 pcs. EMA-MB91F467S-LS-176M07 socket adapter board
- o 1 pcs. YQPACK176SD
- o 5 pcs. Screw M2x12
- o 5 pcs. Washer M2, Nylon
- o 10 pcs. 2mm mini jumper
- o 1 pcs. User Guide

1.2 General Description

The EMA-MB91F467S-LS-176M07 in combination with the EMA-MB91V460A-002B/-80/003 or EMA-MB91FV460B-001 replaces a MB91F467S microcontroller. For further details of the EMA-MB91V460A-002B/-80/003 or EMA-MB91FV460B-001 board please refer to the User Guide of the EMA-MB91V460A-002B/-80/003 or EMA-MB91FV460B-001.

In case EMA-MB91V460A-002B/-80/003 is used, the EMA-MB91V460A-300 extension board is required for the emulation of the APIX functionality of MB91F467S. Please refer to the User Guide of the EMA-MB91V460A-300 for further details.

In case of EMA-MB91FV460B-001, it is recommended to use EMA-MB91F460S-176M07 as socket adapter board.

1.3 Functional Restrictions

1.3.1 Valid for EMA-MB91V460A-002B/-80/003

This probe cable can only be used for the following Microcontroller configuration:

1. VDD5 = 5V, VDD35 = 3.3V

The following Microcontroller configurations (2 & 3) are applicable with this probe cable, but it is recommended to use the appropriate MCU "NLS" probe cable!

2. VDD5 = 5V, VDD35 = 5V

3. VDD5 = 3.3V, VDD35 = 3.3V

While using this probe cable, the GPIO functionality on the external bus interface (VDD35 voltage domain) is restricted!

Unused external bus function pins (e.g. address lines) cannot be configured as general purpose in- or output randomly!

The following ports can be configured as permanent general purpose input OR output.

1. P07[0..7]

2. P06[0..7]

3. P05[0..7]

It is only possible to configure the whole port as input OR output!

Configuring each pin of these ports separately as input or output is not applicable!

For details on how to configure the port input and output direction please see chapter 3.2 Level-shifter direction control jumper!

The following pins can be configured as permanent general purpose input OR output separately.

4. P08[0..1], P08_4, P08_7, P09[0..3], P10[0..1], P10_3

It is possible to configure the pins each as input OR output! Configuring each pin of these ports separately as input or output is applicable by removing certain resistors and making appropriate DIP-Switch settings!

For details on how to configure the pins input and output direction please see chapter 3.3 Bus control jumpers and the corresponding schematics.

APIX functionality must be emulated via external bus access to extension board EMA-MB91V460A-300. Please refer also to chapter "Port 17 Jumpers (APIX AIC Link)" for further restrictions.

1.3.2 Valid for EMA-MB91FV460B-001

This probe cable can only be used for the following Microcontroller configuration:

1. VDD5 = 5V, VDD35 = 3.3V

The following Microcontroller configurations (2 & 3) are applicable with this probe cable, but it is recommended to use the appropriate MCU "NLS" probe cable!

2. VDD5 = 5V, VDD35 = 5V

3. VDD5 = 3.3V, VDD35 = 3.3V

While using this probe cable, the GPIO functionality on the external bus interface (VDD35 voltage domain) is restricted!

Unused external bus function pins (e.g. address lines) cannot be configured as general purpose in- or output randomly!

The following ports can be configured as permanent general purpose input OR output.

5. P07[0..7]

6. P06[0..7]

7. P05[0..7]

It is only possible to configure the whole port as input OR output!

Configuring each pin of these ports separately as input or output is not applicable!

For details on how to configure the port input and output direction please see chapter 3.2 Level-shifter direction control jumper!

The following pins can be configured as permanent general purpose input OR output separately.

8. P08[0..1], P08_4, P08_7, P09[0..3], P10[0..1], P10_3

It is possible to configure the pins each as input OR output! Configuring each pin of these ports separately as input or output is applicable by removing certain resistors and making appropriate DIP-Switch settings!

For details on how to configure the pins input and output direction please see chapter 3.3 Bus control jumpers and the corresponding schematics.

The routing of SDINM, SDINP, SDOUTM, SDOUTP to the target board is not possible, so you have to use the APIX interface on EMA-MB91FV460B-001.

The MCU socket pins 100-103 on your target board will be driven by EMA-MB91FV460B-001 with 5V and 1.8V respectively (please see schematic). Check if this is a problem for your target hardware.

Ensure that J200-J205 are set to position 2-3! Otherwise the related signals will be driven by EMA-MB91FV460B-001 with various voltages (please see schematic)

Set AVCC1 and AVRH1 jumpers on EMA-MB91FV460B-001 so that VDD5 is selected as source. Otherwise these inputs would be supplied by your target board VDD1.8

Please refer also to Application Note mcu-an-300100-e-vxx-ema_mb91f467s_ls_176-m07_with_ema_mb91fv460_001 for more information about the limitations and precautions when using EMA-MB91FV460B-001 together with EMA-MB91F467S-LS-176M07

2 Installation

Remove carefully the EMA-MB91F467S-LS-176M07 board from the shipping carton and check if there are any damages.

Please refer to the attached document "NQPACK/ YQPACK/ HQPACK Technical Information" for installation the socket adapter.
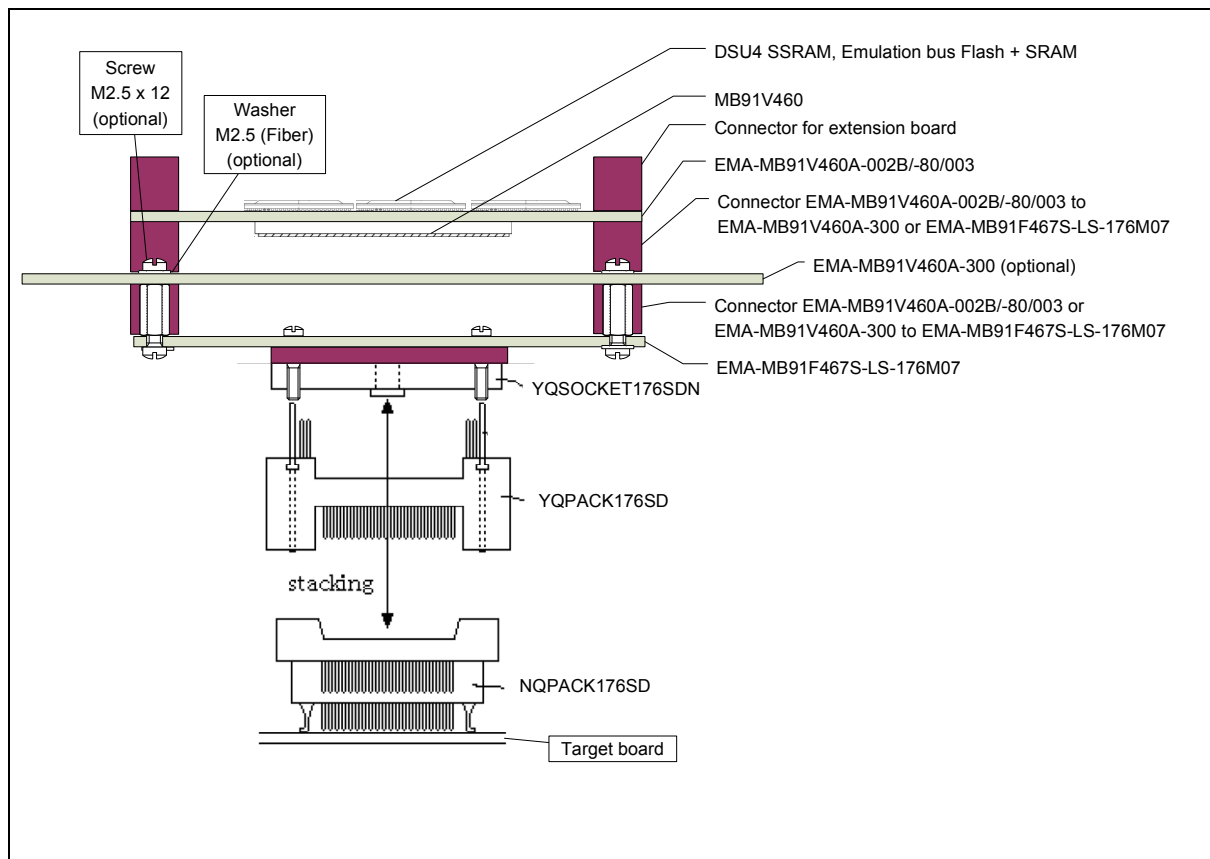

Figure 2-1: Installation

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3   Switches and Jumpers

This chapter describes all switches and jumpers that can be modified or accessed on the EMA-MB91F467S-LS-176M07 board. The default setting is shown with a grey shaded area.

3.1   Level Shifter Switches and Jumpers overview

Jumper	Description/ Function	Type	Default
S400-1	DIR_U406	DIP-Switch	OFF
S400-2	DIR_U407	DIP-Switch	OFF
S400-3	DIR_U408	DIP-Switch	OFF
S400-4	P09_0 ⇐ CS0#	DIP-Switch	OFF
S400-5	P09_1 ⇐ CS1#	DIP-Switch	OFF
S400-6	P09_2 ⇐ CS2#	DIP-Switch	OFF
S400-7	P09_3 ⇐ CS3#	DIP-Switch	OFF
S400-8	P10_0 ⇐ SYSCLK	DIP-Switch	OFF
S400-9	P10_1 ⇐ AS#	DIP-Switch	OFF
S400-10	P10_3 ⇐ WE#	DIP-Switch	OFF
S401-1	CS select	DIP-Switch	OFF
S401-2		DIP-Switch	OFF
S401-3		DIP-Switch	ON
S401-7	P08_7 ⇒ RDY	DIP-Switch	OFF
S401-8	P08_4 ⇐ RD#	DIP-Switch	OFF
S401-9	P08_1 ⇐ WR1	DIP-Switch	OFF
S400-10	P08_0 ⇐ WR0#	DIP-Switch	OFF
R400	P09_0 ⇒ CS0#	0603	Closed
R401	P09_1 ⇒ CS1#	0603	Closed
R402	P09_2 ⇒ CS2#	0603	Closed
R403	P09_3 ⇒ CS3#	0603	Closed
R404	P10_1 ⇒ AS#	0603	Closed
R405	P10_3 ⇒ WE#	0603	Closed
R406	P08_0 ⇒ WR0#	0603	Closed
R407	P08_1 ⇒ WR1#	0603	Closed
R408	P08_4 ⇒ RD#	0603	Closed
R410	P08_7 ⇐ RDY	0603	Closed
R413	P10_0 ⇒ SYSCLK	0603	Closed

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3.2 Level-shifter direction control jumper

Jumper	Setting	Description
S400-1 (Direction U406)	ON	Target board A[0..7] ⇨ MB91V460 A[0..7]
	OFF	Target board A[0..7] ⇦ MB91V460 A[0..7]
S400-2 (Direction U407)	ON	Target board A[8..15] ⇨ MB91V460 A[8..15]
	OFF	Target board A[8..15] ⇦ MB91V460 A[8..15]
S400-3 (Direction U408)	ON	Target board A[16..23] ⇨ MB91V460 A[16..23]
	OFF	Target board A[16..23] ⇦ MB91V460 A[16..23]

Default: S400-1, S400-2, S400-3: OFF

3.3 Bus control jumpers

3.3.1 WR0# (P08_0)

R406	S400-10	Description
Closed	OFF	MB91V460 P08_0 ⇨ Target board WR0#
Open	ON	MB91V460 P08_0 ⇦ Target board WR0#
Closed	ON	Prohibited

Default: R406: Closed, S400-10: OFF

3.3.2 WR1# (P08_1)

R407	S401-09	Description
Closed	OFF	MB91V460 P08_1 ⇨ Target board WR1#
Open	ON	MB91V460 P08_1 ⇦ Target board WR1#
Closed	ON	Prohibited

Default: R407: Closed, S401-09: OFF

3.3.3 RD# (P08_4)

R408	S401-8	Description
Closed	OFF	MB91V460 P08_4 ⇨ Target board RD#
Open	ON	MB91V460 P08_4 ⇦ Target board RD#
Closed	ON	Prohibited

Default: R408: Closed, S401-8: OFF

3.3.4 RDY (P08_7)

R410	S401-7	Description
Closed	OFF	MB91V460 P08_7 ⇦ Target board RDY
Open	ON	MB91V460 P08_7 ⇨ Target board RDY
Closed	ON	Prohibited

Default: R410: Closed, S401-7: OFF

3.3.5 CS0# (P09_0)

R400	S400-4	Description
Closed	OFF	MB91V460 P09_0 ⇨ Target board CS0#
Open	ON	MB91V460 P09_0 ⇦ Target board CS0#
Closed	ON	Prohibited

Default: R400: Closed, S400-4: OFF

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3.3.6 CS1# (P09_1)

R401	S400-5	Description
Closed	OFF	MB91V460 P09_1 ⇨ Target board CS1#
Open	ON	MB91V460 P09_1 ⇦ Target board CS1#
Closed	ON	Prohibited

Default: R401: Closed, S400-5: OFF

3.3.7 CS2# (P09_2)

R402	S400-6	Description
Closed	OFF	MB91V460 P09_2 ⇨ Target board CS2#
Open	ON	MB91V460 P09_2 ⇦ Target board CS2#
Closed	ON	Prohibited

Default: R402: Closed, S400-6: OFF

3.3.8 CS3# (P09_3)

R403	S400-7	Description
Closed	OFF	MB91V460 P09_3 ⇨ Target board CS3#
Open	ON	MB91V460 P09_3 ⇦ Target board CS3#
Closed	ON	Prohibited

Default: R403: Closed, S400-7: OFF

3.3.9 SYSCLK (P10_0)

R413	S400-8	Description
Closed	OFF	MB91V460 P10_0 ⇨ Target board SYSCLK
Open	ON	MB91V460 P10_0 ⇦ Target board SYSCLK
Closed	ON	Prohibited

Default: R413: Closed, S400-8: OFF

3.3.10 AS# (P10_1)

R404	S400-9	Description
Closed	OFF	MB91V460 P10_1 ⇨ Target board AS#
Open	ON	MB91V460 P10_1 ⇦ Target board AS#
Closed	ON	Prohibited

Default: R404: Closed, S400-9: OFF

3.3.11 WE# (P10_3)

R405	S400-10	Description
Closed	OFF	MB91V460 P10_3 ⇨ Target board WE#
Open	ON	MB91V460 P10_3 ⇦ Target board WE#
Closed	ON	Prohibited

Default: R405: Closed, S400-10: OFF

3.3.12 CS select (CPLD)

Chip select signals, selected by S401-1..3, will not be routed towards the target hardware! For applications with extension board EMA-MB91V460A-300 or equivalent extension boards, please select and set the corresponding chip select signal (CSx) used for the extension board! Please also refer to the user guide of the extension board and to the settings on the extension board itself.

E.g. EMA-MB91V460A-300 is configured to use chip select CS3, please set S401-1,2,3 on EMA-MB91F467S-LS-176M07 to CS3 (ON, ON, OFF)!

In default setting all chip select signals are routed to the target hardware.

S401-1	S401-2	S401-3	Description
OFF	OFF	OFF	CS0# is selected
ON	OFF	OFF	CS1# is selected
OFF	ON	OFF	CS2# is selected
ON	ON	OFF	CS3# is selected
Don't care		ON	None selected

Default: S401-1, S401-2: OFF, S401-3: ON

3.4 Port 17 Jumpers (APIX AIC Link)

If EMA-MB91FV460B-001 is used together with EMA-MB91F467S-LS-176M07 set J200-J205 to 2-3 and the following mentioned restrictions will not apply!

When using EMA-MB91V460A-002B/-80/003 with the EMA-MB91V460A-300 extension board for APIX emulation, it is possible to route the signals from the APIX Automotive Interconnection Link on EMA-MB91V460A-300 to the appropriate pins of the EMA-MB91F467S-LS-176M07.

Due to wrong pin connections (P17_7 is used as TCLKI on final MB91F467S instead of P17_4) only the Use Cases where one of the data bits acts as the clock signal are supported.

Please note: The APIX Automotive Interconnection Link 0 signals of EMA-MB91V460A-300 are routed to APIX Automotive Interconnection Link 1 of EMA-MB91F467S-LS-176M07

3.4.1 P17 / AIC Link function

Jumper	U100 pin	P 1-2 [AIC Link used]	P 2-3 [P17 function]	P 3-4 [AIC Link used]
J200	*87[1]*	*J801_66 (RCK1)*	*P17_0*	*P17_0 pulldown*
J201	86	J801_69 (RDA10)	P17_1	P17_1 pulldown
J202	85	J801_70 (RDA11)	P17_2	P17_2 pulldown
J203	*83[2]*	*J801_67 (TCKI1)*	*P17_4*	*P17_4 pulldown*
J204	82	J801_68 (TDA10)	P17_5	P17_5 pulldown
J205	81	J801_65 (TDA11)	P17_6	P17_6 pulldown

Default: all 2-3

[1] Signal available, but corresponding Use Case not supported due to wrong pin assignment of TCLKI1 signal
[2] TCLKI1 signal available on this pin (P17_4 instead of P17_7)

Please refer also to the User Guide of EMA-MB91V460A-300 for the necessary settings on that board.

3.5 Default Jumper Setting

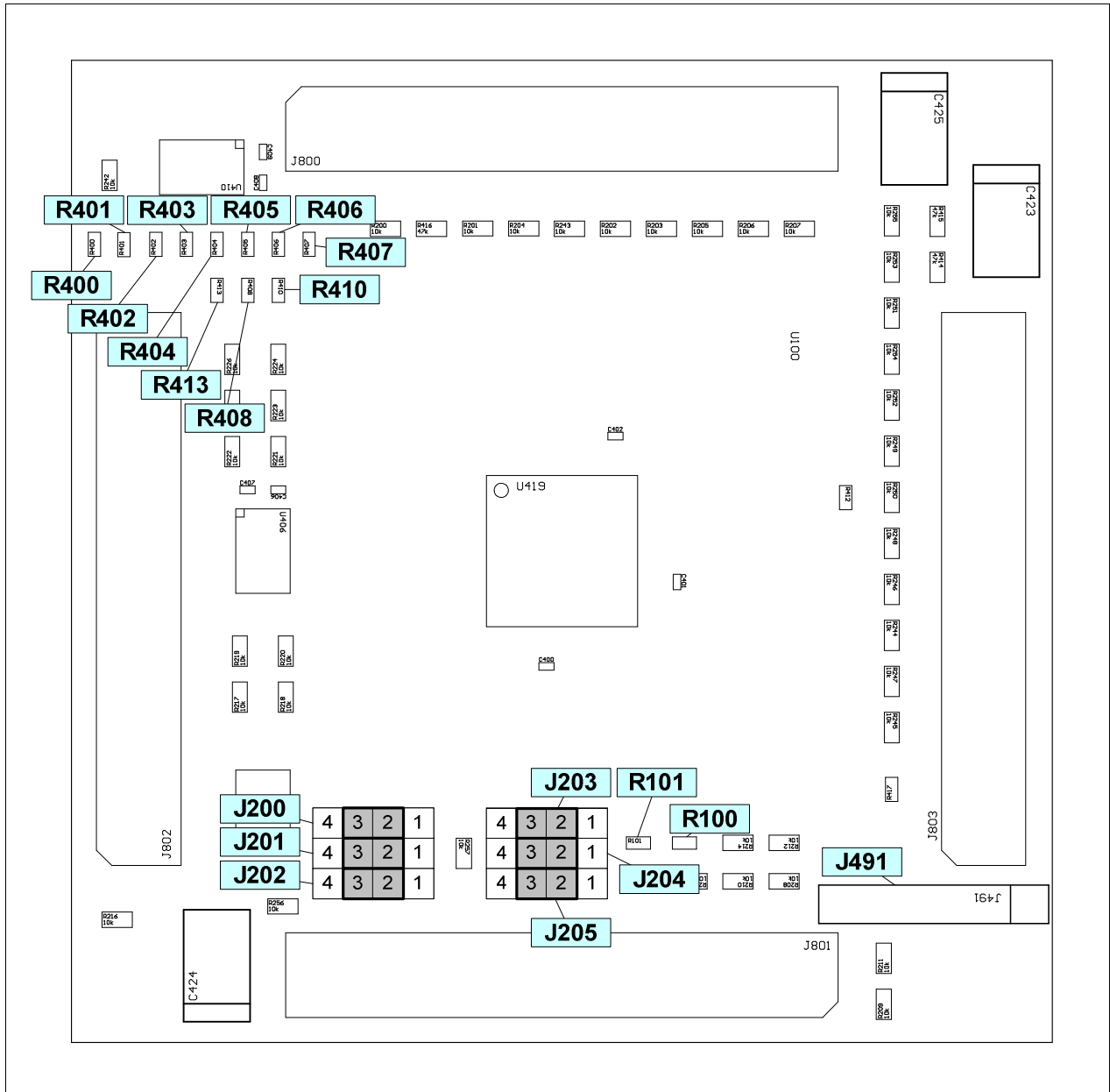The following jumper setting is the default setting.

Figure 3-1: Jumper default setting, top

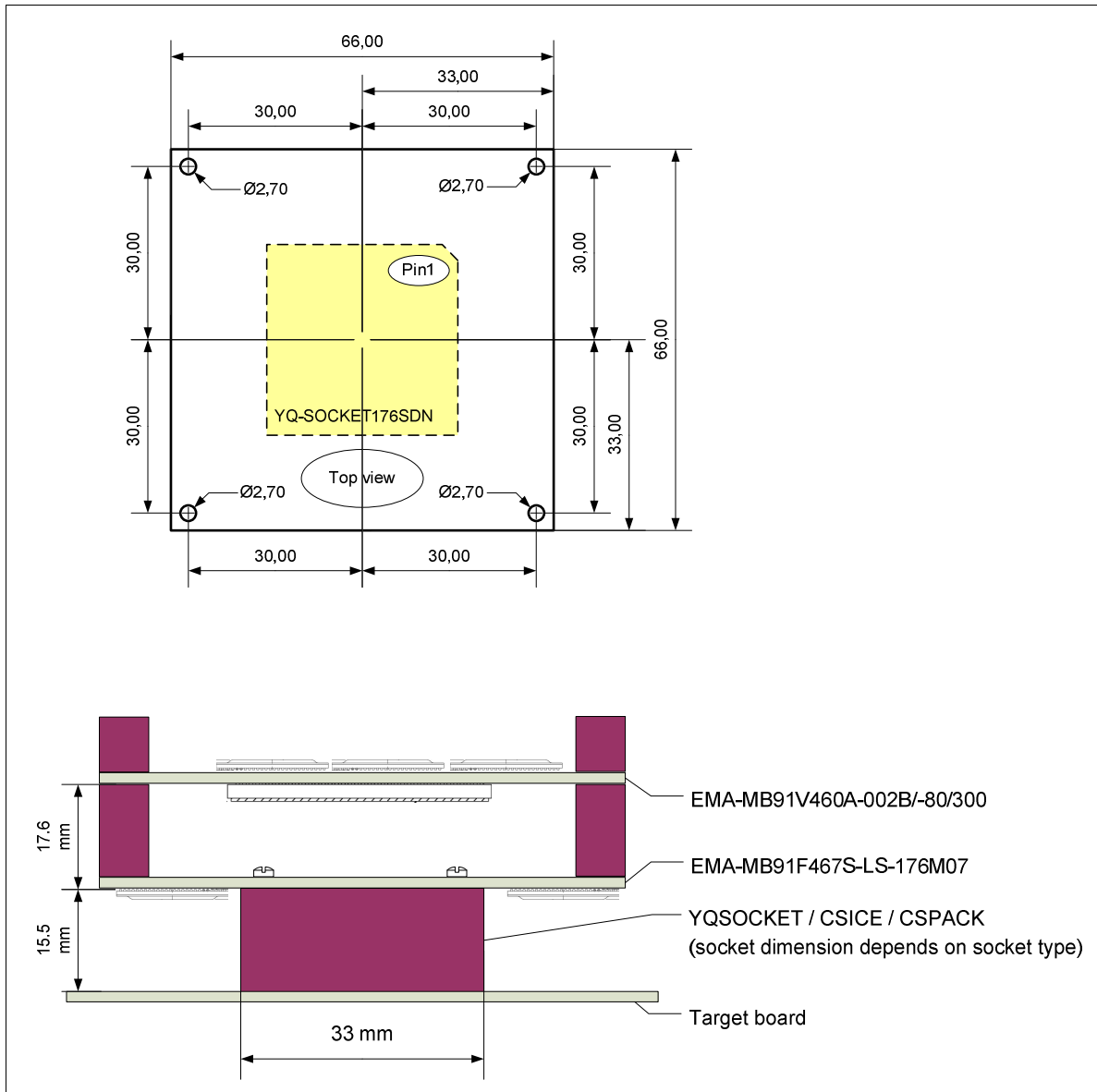Figure 3-2: Jumper location, bottom

4 Mechanical dimensions

Figure 4-1: Mechanical Dimensions

5 CPLD

The CPLD Xilinx XC9536XL-5VQL44C controls the direction of the data bus.

5.1 CPLD Verilog Code

```
`timescale 1ns / 1ps
//////////////////////////////////////////////////////////////////////////////
// Company:        Accemic GmbH & Co. KG
// Engineer:       RH / AW
//
// Create Date:    05/12/2007
// Design Name:    EMA-MB91F467S-LS-176M07
// Module Name:    F467S
// Project Name:
// Target Devices: XC9536XL-5VQ44
// Tool versions:  ISE 9.2
// Description:
//
// Dependencies:
//
// Revision:
// Revision              1.8
// Additional Comments:  none
//
// USERCODE:    7S18
//              ||||____ Subversion
//              |||_____ Version
//              ||_____ Target 467S
//                          **
//
//////////////////////////////////////////////////////////////////////////////

module EMA_MB91F467S_LS_176M07_V11_cpld_7S18(
ECSx,
CSx,               // P09_7..P09_0
WRx,               // P08_3..P08_0
RDx,               // P08_4
ASx,               // P10_1
BAAx,              // P10_2
WEx,               // P10_3
IORDx,             // P11_0
IOWRx,             // P11_1
S401,
DIR_U400,
DIR_U401,
DIR_U404,
DIR_U405,
OEx_U404,
OEx_U405);
```

```verilog
input ECSx;
input[7:0] CSx;
input[3:0] WRx;
input RDx;
input ASx;
input BAAx;
input WEx;
input IORDx;
input IOWRx;
input[7:1] S401;
output DIR_U400;
output DIR_U401;
output DIR_U404;
output DIR_U405;
output OEx_U404;
output OEx_U405;

reg OEx_U404, OEx_U405;
reg DIR_U400, DIR_U401, DIR_U404, DIR_U405;

always @*
begin
     case (S401[3:1])  // CS_MASK
          3'b111:      // CS0
               OEx_U404 =  !ECSx | (CSx[1] & CSx[2] & CSx[3]);
          3'b110:      // CS1
               OEx_U404 =  !ECSx | (CSx[0] & CSx[2] & CSx[3]);
          3'b101:      // CS2
               OEx_U404 =  !ECSx | (CSx[0] & CSx[1] & CSx[3]);
          3'b100:      // CS3
               OEx_U404 =  !ECSx | (CSx[0] & CSx[1] & CSx[2]);
          default:     // none masked
               OEx_U404 =  !ECSx | (CSx[0] & CSx[1] & CSx[2] & CSx[3]);
     endcase

     OEx_U405 = OEx_U404;

     // check schematic for DIR level (different on LS boards)
     DIR_U400 = 1;
     DIR_U401 = 1;
     DIR_U404 = !RDx;
     DIR_U405 = !RDx;
end

endmodule
```

5.2 CPLD Constraints

```
NET "ASx"  LOC = "P13"  ;
NET "BAAx"  LOC = "P14"  ;
NET "CSx<0>"  LOC = "P2"  ;
NET "CSx<1>"  LOC = "P1"  ;
NET "CSx<2>"  LOC = "P3"  ;
NET "CSx<3>"  LOC = "P5"  ;
NET "CSx<4>"  LOC = "P6"  ;
NET "CSx<5>"  LOC = "P7"  ;
NET "CSx<6>"  LOC = "P8"  ;
NET "CSx<7>"  LOC = "P12"  ;
NET "DIR_U400"  LOC = "P39" | SLEW = FAST ;
NET "DIR_U401"  LOC = "P38" | SLEW = FAST ;
NET "DIR_U404"  LOC = "P36" | SLEW = FAST ;
NET "DIR_U405"  LOC = "P37" | SLEW = FAST ;
NET "ECSx"  LOC = "P32"  ;
NET "IORDx"  LOC = "P18"  ;
NET "IOWRx"  LOC = "P19"  ;
NET "OEx_U404"  LOC = "P34" | SLEW = FAST ;
NET "OEx_U405"  LOC = "P33" | SLEW = FAST ;
NET "RDx"  LOC = "P44"  ;
NET "S401<1>"  LOC = "P31"  ;
NET "S401<2>"  LOC = "P30"  ;
NET "S401<3>"  LOC = "P29"  ;
NET "S401<4>"  LOC = "P28"  ;
NET "S401<5>"  LOC = "P27"  ;
NET "S401<6>"  LOC = "P23"  ;
NET "S401<7>"  LOC = "P22"  ;
NET "WEx"  LOC = "P16"  ;
NET "WRx<0>"  LOC = "P40"  ;
NET "WRx<1>"  LOC = "P41"  ;
NET "WRx<2>"  LOC = "P43"  ;
NET "WRx<3>"  LOC = "P42"  ;
```

5.3 CPLD programming jumper (J491)

The CPLD is re-configurable by programming via J491. Please refer to www.xilinx.com for details and tools for Xilinx CPLD configuration.

J491 pin	Name
1	GND
2	TDO
3	TCK
4	TMS
5	TDI
6	VREF

6 Information in the WWW

Information about FUJITSU MICROELECTRONICS Products
can be found on the following Internet pages:

Microcontrollers (8-, 16- and 32bit), Graphics Controllers
Datasheets and Hardware Manuals, Support Tools (Hard- and Software)

http://mcu.emea.fujitsu.com/mcu_portal.htm

Linear Products: Power Management, A/D and D/A Converters

http://www.fujitsu.com/emea/services/microelectronics

Media Products: SAW filters, acoustic resonators and VCOs

http://www.fujitsu.com/emea/services/microelectronics/saw

For more information about FUJITUS MICROELECTRONICS

http://www.fujitsu.com/emea/services/microelectronics

7 China-RoHS regulation

Evaluation Board 评估板

Emulation Board 仿真板

根据SJ/T11364-

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1．电子信息产品污染控制标志说明 Explanation of Pollution Control Label

该标志表明本产品含有超过中国标准SJ/T11363-

2006《电子信息产品中有毒有害物质的限量要求》中限量的有毒有害物质。标志中的数字为本产品的环保使用期，表明本产品在正常使用的条件下，有毒有害物质不会发生外泄或突变，用户使用本产品不会对环境造成严重污染或对其人身、财产造成严重损害的期限，单位为年。

为保证所申明的环保使用期限，应按产品手册中所规定的环境条件和方法进行正常使用，并严格遵守产品维修手册中规定的定期维修和保养要求。

产品中的消耗件和某些零部件可能有其单独的环保使用期限标志，并且其环保使用期限有可能比整个产品本身的环保使用期限短。应到期按产品维修程序更换那些消耗件和零部件，以保证所申明的整个产品的环保使用期限。

本产品在使用寿命结束时不可作为普通生活垃圾处理，应被单独收集妥善处理。

请注意：环保使用期限50年的指定不是与产品的耐久力，使用期限或任何担保要求等同的。

This symbol to be added to all EIO sold to China, indicates the product contains hazardous materials in excess of the limits established by the Chinese standard SJ/T11363-2006 *Requirements for Concentration Limits for Certain Hazardous Substances in Electronic Information Products*. The number in the symbol is the Environment-friendly Use Period (EFUP), which indicates the period, starting from the manufacturing date, during which the toxic or hazardous substances or elements contained in electronic information products will not leak or mutate under normal operating conditions so that the use of such electronic information products will not result in any severe environmental pollution, any bodily injury or damage to any assets, the unit of the period is "Year".

In order to maintain the declared EFUP, the product shall be operated normally according to the instructions and environmental conditions as defined in the product manual, and periodic maintenance schedules specified in Product Maintenance Procedures shall be followed strictly.

Consumables or certain parts may have their own label with an EFUP value less than the product. Periodic replacement of those consumables or parts to maintain the declared EFUP shall be done in accordance with the Product Maintenance Procedures.

This product must not be disposed of as unsorted municipal waste, and must be collected separately and handled properly after decommissioning.

Please note: The designation of 10 years EFUP is not to be equated with the durability, use-duration or any warranty-claims of the product.

产品中有毒有害物质或元素的名称及含量

Table of hazardous substances name and concentration

部件名称 EMA-MB91F467S-LS-176M07	有毒有害物质或元素 Hazardous substances name					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (Cr(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
	x	o	o	o	o	o

O: 表示该有毒有害物质在该部件所有均质材料中的含量均在SJ/T11363-2006 标准规定的限量要求以下

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出SJ/T11363-2006 标准规定的限量要求

•　此表所列数据为发布时所能获得的最佳信息

•　由于缺少经济上或技术上合理可行的替代物质或方案，此医疗设备运用以上一些有毒有害物质来实现设备的预期临床功能，或给人员或环境提供更好的保护效果。

O: Indicates that this toxic or hazardous substance contained in all of the homogeneous materials for this part is below the limit requirement in SJ/T11363-2006.

X: Indicates that this toxic or hazardous substance contained in at least one of the homogeneous materials used for this part is above the limit requirement in SJ/T11363-2006.

•　Data listed in the table represents best information available at the time of publication

8 Recycling

Gültig für EU-Länder:

Gemäß der Europäischen WEEE-Richtlinie und deren Umsetzung in landesspezifische Gesetze nehmen wir dieses Gerät wieder zurück.

Zur Entsorgung schicken Sie das Gerät bitte an die folgende Adresse:

Fujitsu Microelectronics Europe GmbH

Warehouse

Monzastraße 4a

63225 Langen

Valid for European Union Countries:

According to the European WEEE-Directive and its implementation into national laws we take this device back.

For disposal please send the device to the following address:

Fujitsu Microelectronics Europe GmbH

Warehouse

Monzastraße 4a

63225 Langen