

**NOT RECOMMENDED FOR NEW DESIGNS  
NO RECOMMENDED REPLACEMENT  
contact our Technical Support Center at  
1-888-INTERSIL or www.intersil.com/tsc**

EL5225

10-Channel TFT-LCD Reference Voltage Generator

FN7356  
Rev 0.00  
March 11, 2004

The EL5225 is designed to produce the reference voltages required in TFT-LCD applications. Each output is programmed to the required voltage with 10 bits of resolution. Reference pins determine the high and low voltages of the output range, which are capable of swinging to either supply rail. Programming of each output is performed using the 3-wire, SPI compatible interface.

A number of the EL5225 can be stacked for applications requiring more than 10 outputs. The reference inputs can be tied to the rails, enabling each part to output the full voltage range, or alternatively, they can be connected to external resistors to split the output range and enable finer resolutions of the outputs.

The EL5225 has 10 outputs, and is available in the 24-pin TSSOP package. They are specified for operation over the full -40°C to +85°C temperature range.

**Ordering Information**

| PART NUMBER (See Note) | PACKAGE (Pb-Free) | TAPE & REEL | PKG. DWG. # |
|------------------------|-------------------|-------------|-------------|
| EL5225IRZ              | 24-Pin TSSOP      | -           | MDP0044     |
| EL5225IRZ-T7           | 24-Pin TSSOP      | 7"          | MDP0044     |
| EL5225IRZ-T13          | 24-Pin TSSOP      | 13"         | MDP0044     |

NOTE: Intersil Pb-free products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020C.

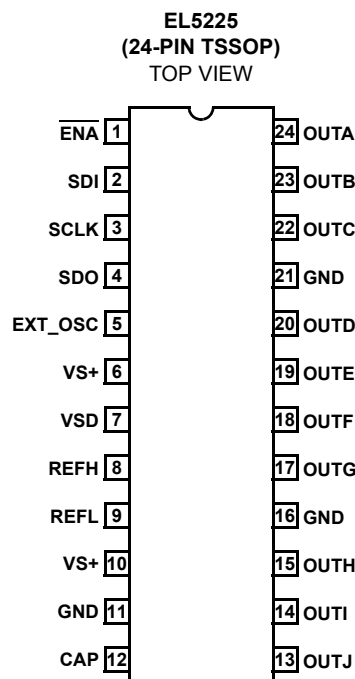
**Features**

- 10-channel reference outputs
- Accuracy of ±1%
- Supply voltage of 5V to 16.5V
- Digital supply 3.3V to 5V
- Low supply current of 9mA
- Rail-to-rail capability
- Pb-free available (RoHS compliant)

**Applications**

- TFT-LCD drive circuits
- Reference voltage generators

**Pinout**



**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$ )

Supply Voltage between  $V_S$  & GND . . . . . 4.5V (min) to 18V (max)  
 Supply Voltage between  $V_{SD}$  & GND . . . 3V (min) to  $V_S$  and 7V (max)  
 Maximum Continuous Output Current . . . . . 30mA  
 Power Dissipation . . . . . See Curves

Maximum Die Temperature . . . . .  $+125^\circ\text{C}$   
 Storage Temperature . . . . .  $-65^\circ\text{C}$  to  $+150^\circ\text{C}$   
 Ambient Operating Temperature . . . . .  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

*IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typ values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore:  $T_J = T_C = T_A$*

**Electrical Specifications**  $V_S = 15\text{V}$ ,  $V_{SD} = 5\text{V}$ ,  $V_{REFH} = 13\text{V}$ ,  $V_{REFL} = 2\text{V}$ ,  $R_L = 1.5\text{k}\Omega$  and  $C_L = 200\text{pF}$  to 0V,  $T_A = 25^\circ\text{C}$ , unless otherwise specified.

| PARAMETER        | DESCRIPTION                                | CONDITIONS  | MIN   | TYP   | MAX  | UNIT          |
|------------------|--|---|-------|-------|------|---------------|
| <b>SUPPLY</b>    |  |   |       |       |      |               |
| $I_S$            | Supply Current                             | No load   |       | 9     | 11.5 | mA            |
| $I_{SD}$         | Digital Supply Current                     |   |       | 0.17  | 0.35 | mA            |
| <b>ANALOG</b>    |  |   |       |       |      |               |
| $V_{OL}$         | Output Swing Low                           | Sinking 5mA ( $V_{REFH} = 15\text{V}$ , $V_{REFL} = 0$ )  |       | 50    | 150  | mV            |
| $V_{OH}$         | Output Swing High                          | Sourcing 5mA ( $V_{REFH} = 15\text{V}$ , $V_{REFL} = 0$ ) | 14.85 | 14.95 |      | V             |
| $I_{SC}$         | Short Circuit Current                      | $R_L = 10\Omega$  | 100   | 140   |      | mA            |
| PSRR             | Power Supply Rejection Ratio               | $V_{S+}$ is moved from 14V to 16V                         | 45    | 65    |      | dB            |
| $t_D$            | Program to Out Delay                       |   |       | 4     |      | ms            |
| $V_{AC}$         | Accuracy referred to the ideal value       | Code = 512  |       | 20    |      | mV            |
| $\Delta V_{MIS}$ | Channel to Channel Mismatch                | Code = 512  |       | 2     |      | mV            |
| $V_{DROOP}$      | Droop Voltage                              |   |       | 1     | 2    | mV/ms         |
| $R_{INH}$        | Input Resistance @ $V_{REFH}$ , $V_{REFL}$ |   |       | 32    |      | k $\Omega$    |
| REG              | Load Regulation                            | $I_{OUT} = 5\text{mA}$ step                               |       | 0.5   | 1.5  | mV/mA         |
| CAP              | Band Gap                                   | Bypass with 0.1 $\mu\text{F}$                             | 1     | 1.3   | 1.6  | V             |
| <b>DIGITAL</b>   |  |   |       |       |      |               |
| $V_{IH}$         | Logic 1 Input Voltage                      | $V_{SD} = 5\text{V}$                                      | 4     |       |      | V             |
|                  |  | $V_{SD} = 3.3\text{V}$                                    | 2     |       |      | V             |
| $F_{CLK}$        | Clock Frequency                            |   |       |       | 5    | MHz           |
| $V_{IL}$         | Logic 0 Input Voltage                      | $V_{SD} = 3.3\text{V}/5\text{V}$                          |       |       | 1    | V             |
| $t_S$            | Setup Time                                 |   |       | 20    |      | ns            |
| $t_H$            | Hold Time                                  |   |       | 20    |      | ns            |
| $t_{LC}$         | Load to Clock Time                         |   |       | 20    |      | ns            |
| $t_{CE}$         | Clock to Load Line                         |   |       | 20    |      | ns            |
| $t_{DCO}$        | Clock to Out Delay Time                    | Negative edge of SCLK                                     |       | 10    |      | ns            |
| $R_{SDIN}$       | $SD_{IN}$ Input Resistance                 |   |       | 1     |      | G $\Omega$    |
| $T_{PULSE}$      | Minimum Pulse Width for EXT_OSC Signal     |   |       | 5     |      | $\mu\text{s}$ |
| Duty Cycle       | Duty Cycle for EXT_OSC Signal              |   |       | 50    |      | %             |
| INL              | Integral Nonlinearity Error                |   |       | 1.3   |      | LSB           |
| DNL              | Differential Nonlinearity Error            |   |       | 0.5   |      | LSB           |
| $F_{OSC}$        | Internal Refresh Oscillator Frequency      | OSC_Select = 0  |       | 21    |      | kHz           |

## Pin Descriptions

| PIN NUMBER | PIN NAME                       | PIN TYPE               | PIN FUNCTION   |
|------------|--------------------------------|------------------------|--|
| 1          | $\overline{\text{EN}}\text{A}$ | Logic Input            | Chip select, low enables data input to logic                       |
| 2          | SDI                            | Logic Input            | Serial data input  |
| 3          | SCLK                           | Logic Input            | Serial data clock  |
| 4          | SDO                            | Logic Output           | Serial data output   |
| 5          | EXT_OSC                        | Logic Input/Output     | External oscillator input or internal oscillator output            |
| 6, 10      | VS+                            | Analog Power           | Positive supply voltage for analog circuits                        |
|            | NC                             |                        | Not connected  |
| 7          | VSD                            | Digital Power          | Positive power supply for digital circuits (3.3V - 5V)             |
| 8          | REFH                           | Analog Reference Input | High reference voltage   |
| 9          | REFL                           | Analog Reference Input | Low reference voltage  |
| 11         | GND                            | Ground                 | Ground   |
| 12         | CAP                            | Analog Bypass Pin      | Decoupling capacitor for internal reference generator, 0.1 $\mu$ F |
| 13         | OUTJ                           | Analog Output          | Channel J programmable output voltage                              |
| 14         | OUTI                           | Analog Output          | Channel I programmable output voltage                              |
| 15         | OUTH                           | Analog Output          | Channel H programmable output voltage                              |
| 17         | OUTG                           | Analog Output          | Channel G programmable output voltage                              |
| 18         | OUTF                           | Analog Output          | Channel F programmable output voltage                              |
| 19         | OUTE                           | Analog Output          | Channel E programmable output voltage                              |
| 20         | OUTD                           | Analog Output          | Channel D programmable output voltage                              |
| 22         | OUTC                           | Analog Output          | Channel C programmable output voltage                              |
| 23         | OUTB                           | Analog Output          | Channel B programmable output voltage                              |
| 24         | OUTA                           | Analog Output          | Channel A programmable output voltage                              |
|            | OUTL                           | Analog Output          | Channel L programmable output voltage                              |
|            | OUTK                           | Analog Output          | Channel K programmable output voltage                              |
| 16, 21     | GND                            | Power                  | Ground   |

### Typical Performance Curves

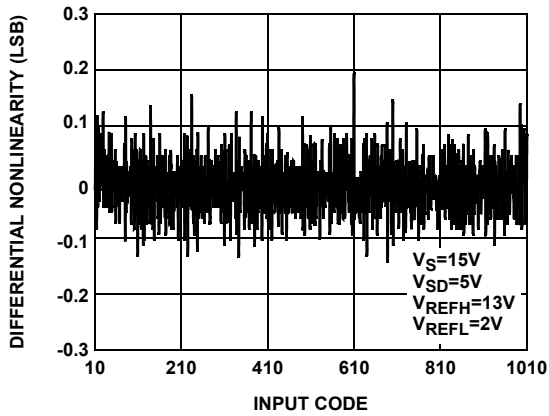


FIGURE 1. DIFFERENTIAL NONLINEARITY vs CODE

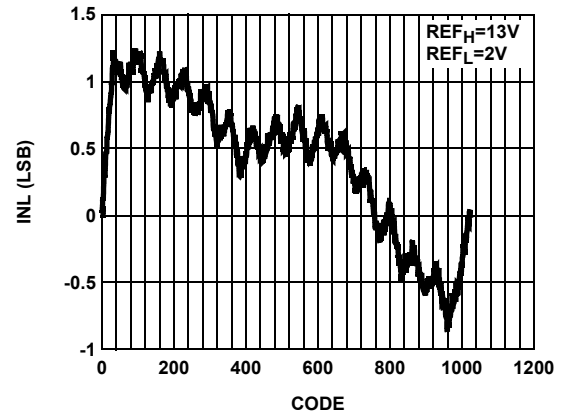


FIGURE 2. INTEGRAL NONLINEARITY ERROR

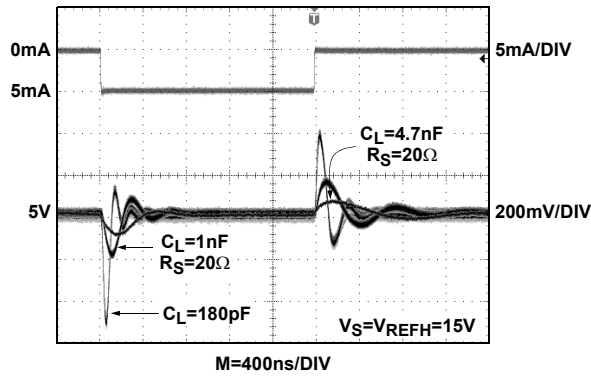


FIGURE 3. TRANSIENT LOAD REGULATION (SOURCING)

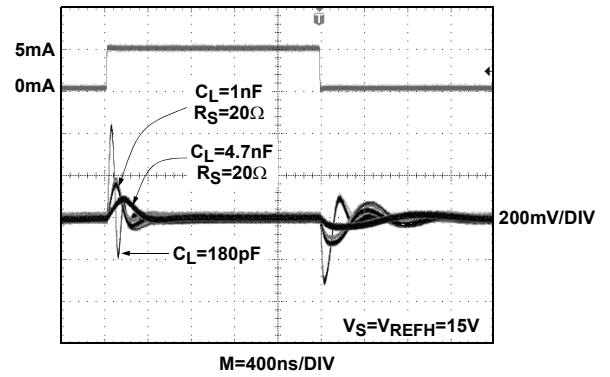


FIGURE 4. TRANSIENT LOAD REGULATION (SINKING)

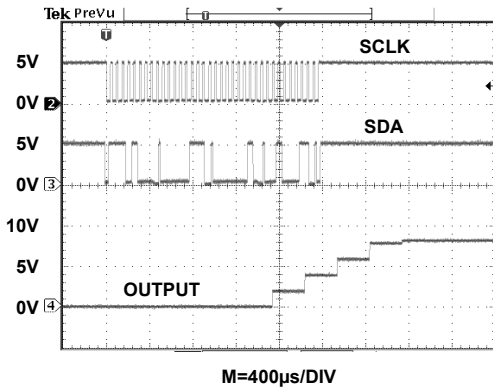


FIGURE 5. LARGE SIGNAL RESPONSE (RISING FROM 0V TO 8V)

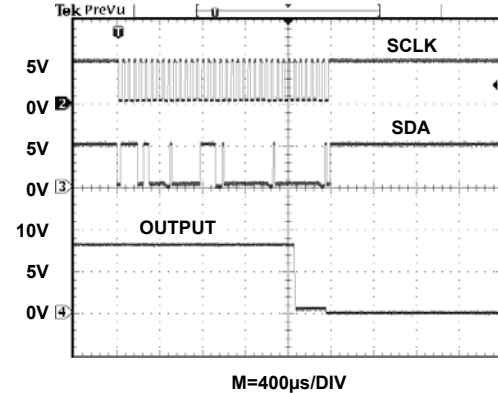


FIGURE 6. LARGE SIGNAL RESPONSE (FALLING FROM 8V TO 0V)

**Typical Performance Curves** (Continued)

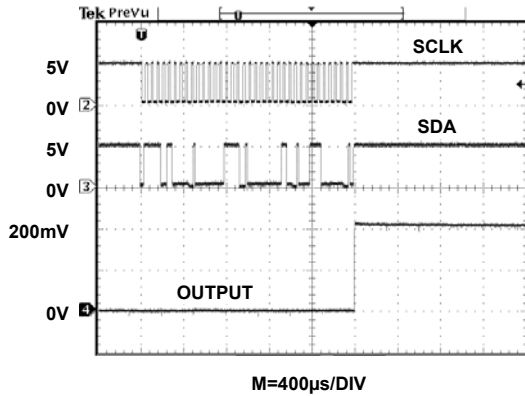


FIGURE 7. SMALL SIGNAL RESPONSE (RISING FROM 0V TO 200mV)

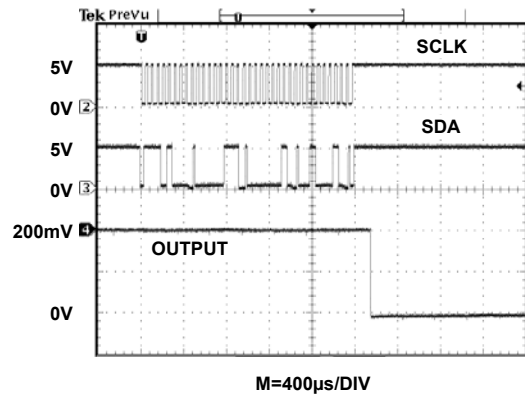


FIGURE 8. SMALL SIGNAL RESPONSE (FALLING FROM 200mV TO 0V)

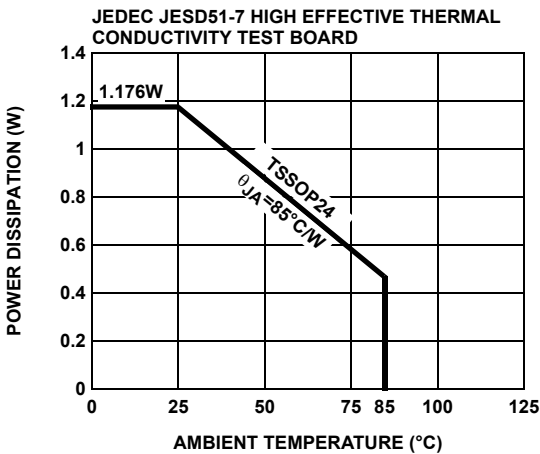


FIGURE 9. POWER DISSIPATION vs AMBIENT TEMPERATURE

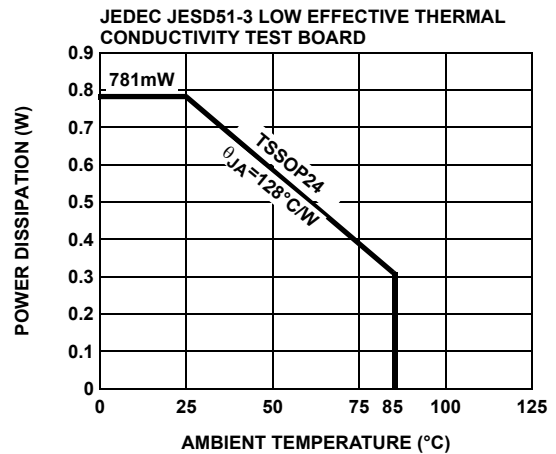


FIGURE 10. POWER DISSIPATION vs AMBIENT TEMPERATURE

**General Description**

The EL5225 provides a versatile method of providing the reference voltages that are used in setting the transfer characteristics of LCD display panels. The V/T (Voltage/Transmission) curve of the LCD panel requires that a correction is applied to make it linear; however, if the panel is to be used in more than one application, the final curve may differ for different applications. By using the EL5225, the V/T curve can be changed to optimize its characteristics according to the required application of the display product. Each of the eight reference voltage outputs can be set with a 10-bit resolution. These outputs can be driven to within 50mV of the power rails of the EL5225. As all of the output buffers are identical, it is also possible to use the EL5225 for applications other than LCDs where multiple voltage references are required that can be set to 10 bit accuracy.

**Digital Interface**

The EL5225 uses a simple 3-wire SPI compliant digital interface to program the outputs. The EL5225 can support the clock rate up to 5MHz.

**Serial Interface**

The EL5225 is programmed through a three-wire serial interface. The start and stop conditions are defined by the  $\overline{\text{EN}}\text{A}$  signal. While the  $\overline{\text{EN}}\text{A}$  is low, the data on the SDI (serial data input) pin is shifted into the 16-bit shift register on the positive edge of the SCLK (serial clock) signal. The MSB (bit 15) is loaded first and the LSB (bit 0) is loaded last (see Table 1). After the full 16-bit data has been loaded, the  $\overline{\text{EN}}\text{A}$  is pulled high and the addressed output channel is updated. The SCLK is disabled internally when the  $\overline{\text{EN}}\text{A}$  is high. The SCLK must be low before the  $\overline{\text{EN}}\text{A}$  is pulled low.

To facilitate the system designs that use multiple EL5225 chips, a buffered serial output of the shift register (SDO pin) is available. Data appears on the SDO pin at the 16th falling SCLK edge after being applied to the SDI pin.

To control the multiple EL5225 chips from a single three-wire serial port, just connect the  $\overline{\text{ENA}}$  pins and the SCLK pins together, connect the SDO pin to the SDI pin on the next chip. While the  $\overline{\text{ENA}}$  is held low, the 16m-bit data is loaded to the SDI input of the first chip. The first 16-bit data will go to the last chip and the last 16-bit data will go to the first chip. While the  $\overline{\text{ENA}}$  is held high, all addressed outputs will be updated simultaneously.

The Serial Timing Diagram and parameters table show the timing requirements for three-wire signals.

The serial data has a minimum length of 16 bits, the MSB (most significant bit) is the first bit in the signal. The bits are allocated to the following functions (also refer to the Control Bits Logic Table)

- Bit 15 is always set to a zero
- Bit 14 controls the source of the clock, see the next section for details
- Bits 13 through 10 select the channel to be written to, these are binary coded with channel A = 0, and channel H = 7
- The 10-bit data is on bits 9 through 0. Some examples of data words are shown in the table of Serial Programming Examples

TABLE 1. CONTROL BITS LOGIC TABLE

| BIT | NAME       | DESCRIPTION                |
|-----|------------|----------------------------|
| B15 | Test       | Always 0                   |
| B14 | Oscillator | 0 = Internal, 1 = External |
| B13 | A3         | Channel Address            |
| B12 | A2         | Channel Address            |
| B11 | A1         | Channel Address            |
| B10 | A0         | Channel Address            |
| B9  | D9         | Data                       |
| B8  | D8         | Data                       |
| B7  | D7         | Data                       |
| B6  | D6         | Data                       |
| B5  | D5         | Data                       |
| B4  | D4         | Data                       |
| B3  | D3         | Data                       |
| B2  | D2         | Data                       |
| B1  | D1         | Data                       |
| B0  | D0         | Data                       |

### Serial Timing Diagram

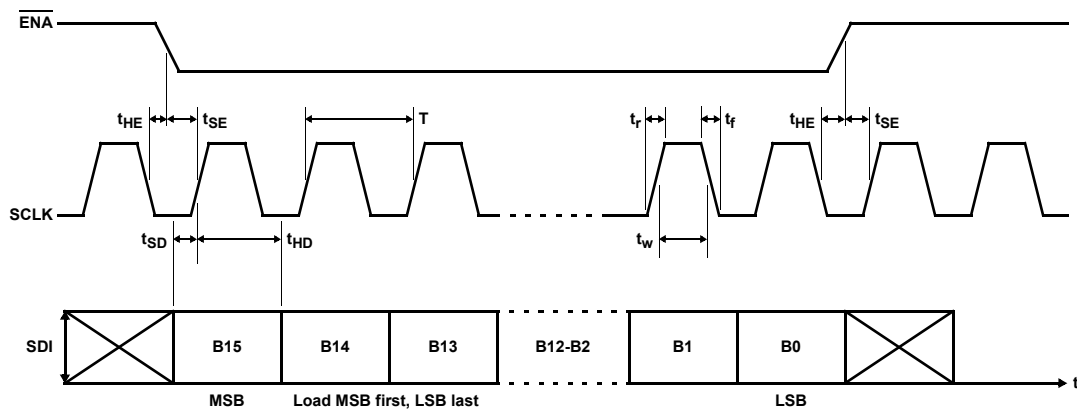


TABLE 2. SERIAL TIMING PARAMETERS

| PARAMETER                      | RECOMMENDED OPERATING RANGE | DESCRIPTION                        |
|--------------------------------|-----------------------------|------------------------------------|
| T                              | ≥200ns                      | Clock Period                       |
| t <sub>r</sub> /t <sub>f</sub> | 0.05 * T                    | Clock Rise/Fall Time               |
| t <sub>HE</sub>                | ≥10ns                       | $\overline{\text{ENA}}$ Hold Time  |
| t <sub>SE</sub>                | ≥10ns                       | $\overline{\text{ENA}}$ Setup Time |
| t <sub>HD</sub>                | ≥10ns                       | Data Hold Time                     |
| t <sub>SD</sub>                | ≥10ns                       | Data Setup Time                    |
| t <sub>W</sub>                 | 0.50 * T                    | Clock Pulse Width                  |

TABLE 3. SERIAL PROGRAMMING EXAMPLES

| CONTROL |    | CHANNEL ADDRESS |    |    |    | DATA |    |    |    |    |    |    |    |    |    | CONDITION |  |
|---------|----|-----------------|----|----|----|------|----|----|----|----|----|----|----|----|----|-----------|--|
| C1      | C0 | A3              | A2 | A1 | A0 | D9   | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |           |  |
| 0       | 0  | 0               | 0  | 0  | 0  | 0    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0         | Internal Oscillator, Channel A, Value = 0    |
| 0       | 0  | 0               | 0  | 0  | 0  | 1    | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1  | 1         | Internal Oscillator, Channel A, Value = 1023 |
| 0       | 0  | 0               | 0  | 0  | 0  | 1    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0         | Internal Oscillator, Channel A, Value = 512  |
| 0       | 0  | 0               | 0  | 1  | 1  | 1    | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 0  | 1  | t         | Internal Oscillator, Channel C, Value = 513  |
| 0       | 0  | 0               | 1  | 1  | 1  | 0    | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1         | Internal Oscillator, Channel H, Value = 31   |
| 0       | 1  | 0               | 1  | 1  | 1  | 0    | 0  | 0  | 0  | 0  | 1  | 1  | 1  | 1  | 1  | 1         | External Oscillator, Channel H, Value = 31   |

### Analog Section

#### TRANSFER FUNCTION

The transfer function is:

$$V_{\text{OUT(IDEAL)}} = V_{\text{REFL}} + \frac{\text{data}}{1024} \times (V_{\text{REFH}} - V_{\text{REFL}})$$

where data is the decimal value of the 10-bit data binary input code.

The output voltages from the EL5225 will be derived from the reference voltages present at the V<sub>REFL</sub> and V<sub>REFH</sub> pins. The impedance between those two pins is about 32kΩ.

Care should be taken that the system design holds these two reference voltages within the limits of the power rails of the EL5225.  $GND < V_{\text{REFH}} \leq V_S$  and  $GND \leq V_{\text{REFL}} \leq V_{\text{REFH}}$ .

In some LCD applications that require more than 10 channels, the system can be designed such that one EL5225 will provide the Gamma correction voltages that are more positive than the V<sub>COM</sub> potential. The second EL5225 can provide the Gamma correction voltage more negative than the V<sub>COM</sub> potential. The Application Drawing shows a system connected in this way.

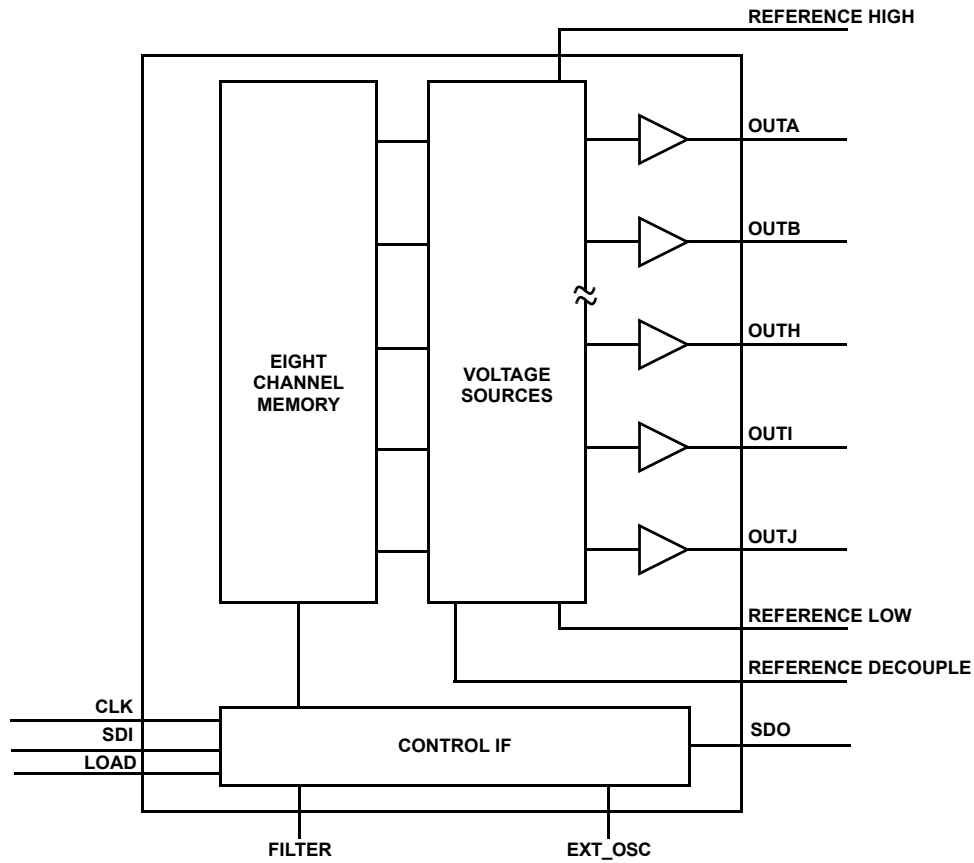
#### CLOCK OSCILLATOR

The EL5225 requires an internal clock or external clock to refresh its outputs. The outputs are refreshed at the falling OSC clock edges. The output refreshed switches open at the rising edges of the OSC clock. The driving load shouldn't be changed at the rising edges of the OSC clock. Otherwise, it will generate a voltage error at the outputs. This clock may be input or output via the clock pin labeled OSC. The internal clock is provided by an internal oscillator running at approximately 21kHz and can be output to the OSC pin. In a 2 chip system, if the driving loads are stable, one chip may be programmed to use the internal oscillator; then the OSC pin will output the clock from the internal oscillator. The second chip may have the OSC pin connected to this clock source.

For transient load application, the external clock Mode should be used to ensure all functions are synchronized together. The positive edge of the external clock to the OSC pin should be timed to avoid the transient load effect. The Application Drawing shows the LCD H rate signal used, here the positive clock edge is timed to avoid the transient load of the column driver circuits.

After power on, the chip will start with the internal oscillator mode. At this time, the OSC pin will be in a high impedance condition to prevent contention. By setting B14 to high, the chip is on external clock mode. Setting B14 to low, the chip is on internal clock mode.

**Block Diagram**



**CHANNEL OUTPUTS**

Each of the channel outputs has a rail-to-rail buffer. This enables all channels to have the capability to drive to within 50mV of the power rails, (see Electrical Characteristics for details).

When driving large capacitive loads, a series resistor should be placed in series with the output. (Usually between 5Ω and 50Ω).

Each of the channels is updated on a continuous cycle, the time for the new data to appear at a specific output will depend on the exact timing relationship of the incoming data to this cycle.

The best-case scenario is when the data has just been captured and then passed on to the output stage immediately; this can be as short as 48μs. In the worst-case scenario, this will be 480μs when the data has just missed the cycle.

When a large change in output voltage is required, the change will occur in 2V steps, thus the requisite number of timing cycles will be added to the overall update time. This means that a large change of 16V can take between 3.8ms

and 4.2ms depending on the absolute timing relative to the update cycle.

**Output Stage and the Use of External Oscillator**

Simplified output sample and hold amp stage for one channel.

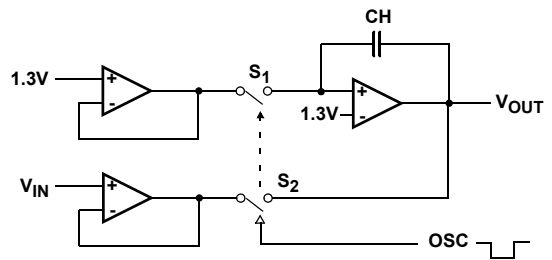


FIGURE 11.

The output voltage is generated from the DAC, which is  $V_{IN}$  at the above circuit. The refreshed switches are controlled by the internal or external oscillator signal. When the OSC clock signal is low, the switch  $S_1$  and  $S_2$  are closed. The output  $V_{OUT} = V_{IN}$  and at the same time the sample and hold cap CH is being charged. When the OSC clock signal is high, the refreshed switch  $S_1$  and  $S_2$  are opened and the output voltage is maintained by CH. This refreshed process



will repeat every 10-clock cycles for each channel. The time takes to update the output depends on the timing at the  $V_{IN}$  and the state of the switches. It can take 1 to 10 clock cycles to update each output.

For the sample and hold capacitor CH to maintain the correct output voltage, the driving load shouldn't be changed at the rising edge of the OSC signal. Since at the rising edge of the OSC clock, the refreshed switches are being opened, if the load changes at that time, it will generate an error output voltage. For a fixed load condition, the internal oscillator can be used.

For the transient load condition, the external OSC mode should be used to avoid the conflict between the rising edge of the OSC signal and the changing load. So a timing delay circuit will be needed to delay the OSC signal and avoid the rising edge of the OSC signal and changing the load at the same time.

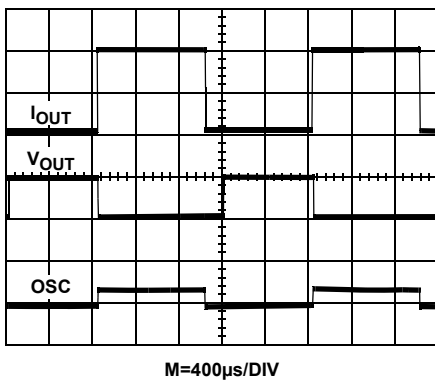


FIGURE 12. TRANSIENT LOAD RESPONSE

Channel 3 - sinking and sourcing 5mA current

Channel 2 - EXT\_OSC signal

Channel 1 -  $V_{OUT}$

Here, the OSC signal is synchronized to the load signal. The rising edge of the OSC signal is then delayed by some amount of time and gives enough time for CH to be charged to a new voltage before the switches are opened.

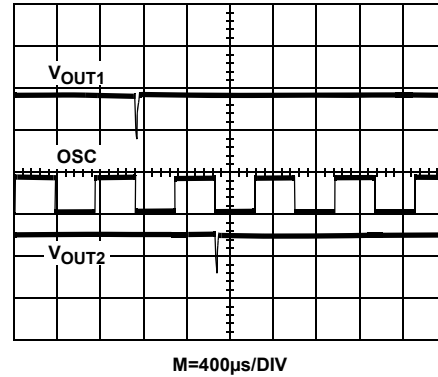


FIGURE 13. CHANNEL-TO-CANNEL REFRESH

Ch1 - Output1

Ch3 - Output2

Ch2 - EXT\_OSC

At the falling edge of the OSC, output 1 is refreshing and one clock cycle later, output2 is being refreshed. The spike you see here is the response of the output amplifier when the refreshed switches are closed. When driving a big capacitor load, there will be ringing at the spikes because the phase margin of the amplifier is decreased.

The speed of the external OSC signal shouldn't be greater than 70kHz because for the worst condition, it will take at least 4µs to charge the sample and hold Capacitor CH. The pulse width has to be at least 4µs long. From our lab test, the duty cycle of the OSC signal must be greater than 30%.

**POWER DISSIPATION**

With the 30mA maximum continues output drive capability for each channel, it is possible to exceed the 125°C absolute maximum junction temperature. Therefore, it is important to calculate the maximum junction temperature for the application to determine if load conditions need to be modified for the part to remain in the safe operation.

The maximum power dissipation allowed in a package is determined according to:

$$P_{DMAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}}$$

where:

- $T_{JMAX}$  = Maximum junction temperature
- $T_{AMAX}$  = Maximum ambient temperature
- $\theta_{JA}$  = Thermal resistance of the package
- $P_{DMAX}$  = Maximum power dissipation in the package

The maximum power dissipation actually produced by the IC is the total quiescent supply current times the total power supply voltage and plus the power in the IC due to the loads.

$$P_{D\text{MAX}} = V_S \times I_S + \Sigma[(V_S - V_{\text{OUT}i}) \times I_{\text{LOAD}i}]$$

when sourcing, and:

$$P_{D\text{MAX}} = V_S \times I_S + \Sigma(V_{\text{OUT}i} \times I_{\text{LOAD}i})$$

when sinking.

Where:

- $i = 1$  to total 10
- $V_S$  = Supply voltage
- $I_S$  = Quiescent current
- $V_{\text{OUT}i}$  = Output voltage of the  $i$  channel
- $I_{\text{LOAD}i}$  = Load current of the  $i$  channel

By setting the two  $P_{D\text{MAX}}$  equations equal to each other, we can solve for the  $R_{\text{LOAD}i}$  to avoid the device overheat. The package power dissipation curves provide a convenient way to see if the device will overheat.

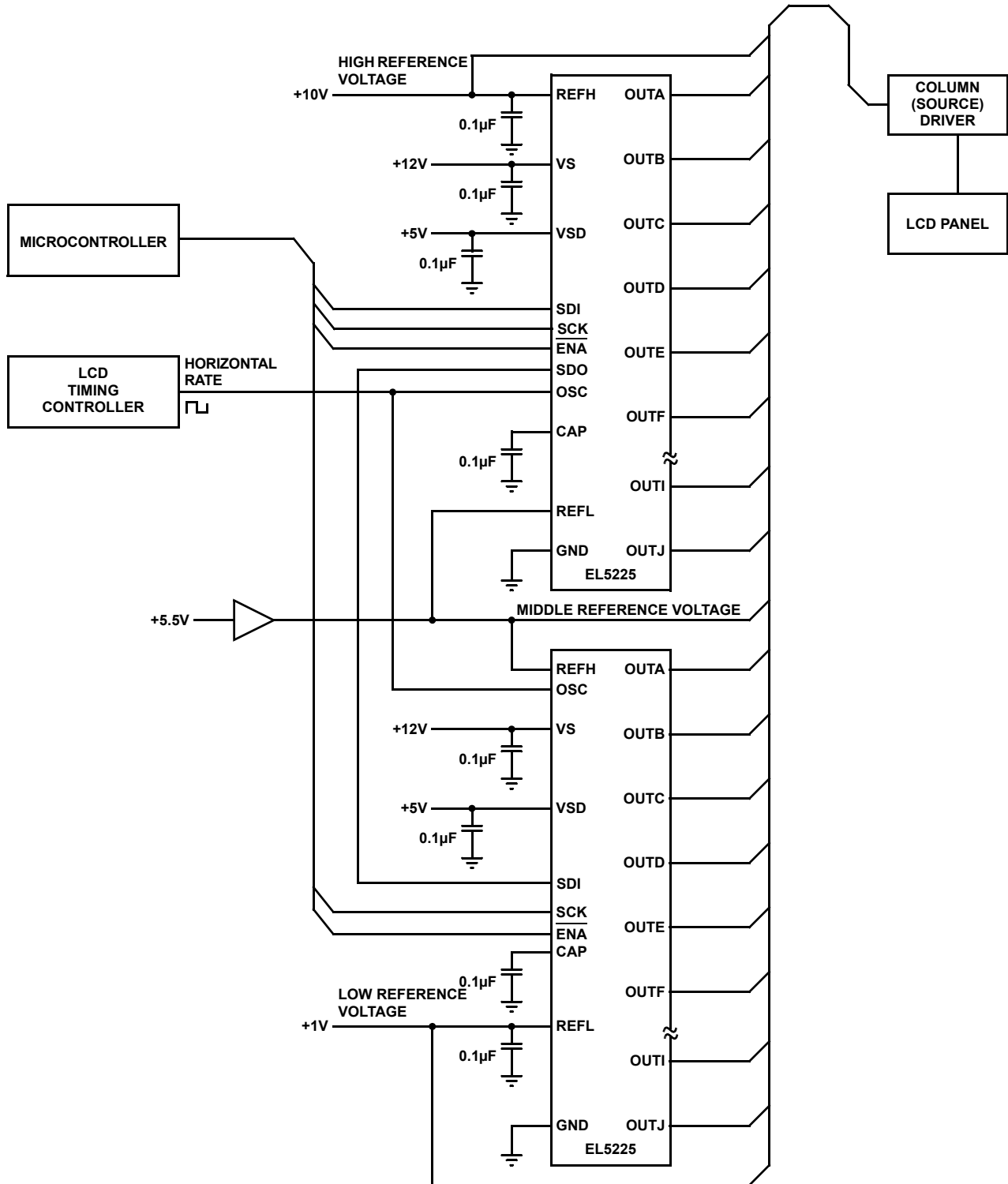
## POWER SUPPLY BYPASSING AND PRINTED CIRCUIT BOARD LAYOUT

Good printed circuit board layout is necessary for optimum performance. A low impedance and clean analog ground plane should be used for the EL5225. The traces from the two ground pins to the ground plane must be very short. Lead length should be as short as possible and all power supply pins must be well bypassed. A 0.1 $\mu$ F ceramic capacitor must be placed very close to the  $V_S$ ,  $V_{\text{REFH}}$ ,  $V_{\text{REFL}}$ , and CAP pins. A 4.7 $\mu$ F local bypass tantalum capacitor should be placed to the  $V_S$ ,  $V_{\text{REFH}}$ , and  $V_{\text{REFL}}$  pins.

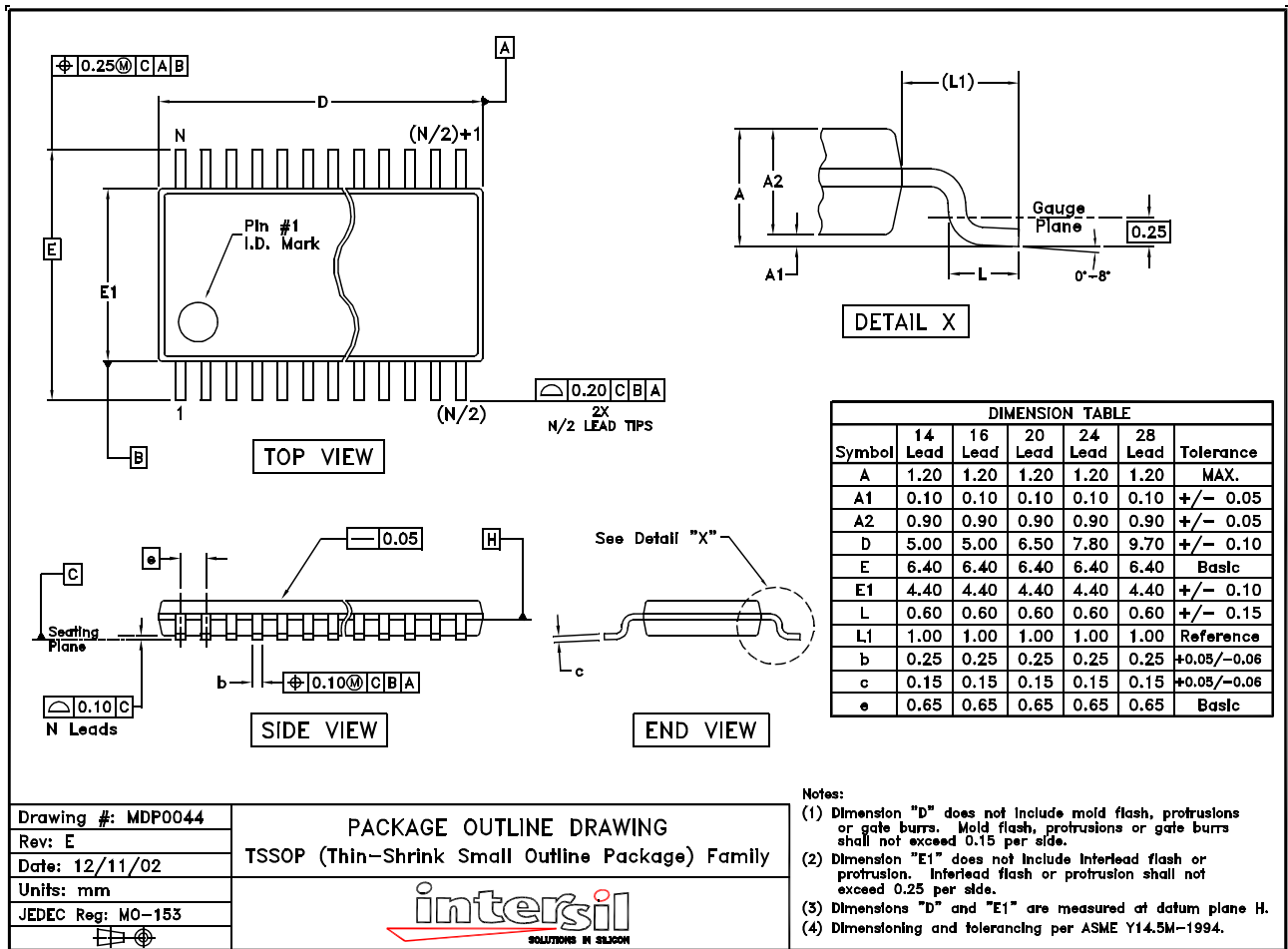
## APPLICATION USING THE EL5225

In the first application drawing, the schematic shows the interconnect of a pair of EL5225 chips connected to give 10 gamma corrected voltages above the  $V_{\text{COM}}$  voltage, and 10 gamma corrected voltages below the  $V_{\text{COM}}$  voltage.

**Application Drawing**



# TSSOP Package Outline Drawing



NOTE: The package drawing shown here may not be the latest version. To check the latest revision, please refer to the Intersil website at <http://www.intersil.com/design/packages/index.asp>

© Copyright Intersil Americas LLC 2002-2004. All Rights Reserved.  
 All trademarks and registered trademarks are the property of their respective owners.

For additional products, see [www.intersil.com/en/products.html](http://www.intersil.com/en/products.html)

Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted in the quality certifications found at [www.intersil.com/en/support/qualandreliability.html](http://www.intersil.com/en/support/qualandreliability.html)

Intersil products are sold by description only. Intersil may modify the circuit design and/or specifications of products at any time without notice, provided that such modification does not, in Intersil's sole judgment, affect the form, fit or function of the product. Accordingly, the reader is cautioned to verify that datasheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see [www.intersil.com](http://www.intersil.com)