Ph. 480-503-4295 | NOPP@FocusLCDs.com

TFT | OLED | CHARACTER | GRAPHIC | UWVD | SEGMENT | CUSTOM

TFT Display Module

Part Number

E50RA-I-MW490-C

Overview:

- 5.0" IPS TFT (67.56mm x 122.35mm)
- 480x854 pixels
- 2 Lane MIPI Interface
- Operating Temperature: -20C to 70C
- All View
- Transmissive, IPS
- Controller: ILI9806E
- Capacitive Touch Panel
- 490 NITS
- RoHS Compliant

Description

This is a color active matrix TFT (Thin Film Transistor) LCD (Liquid Crystal Display) that uses amorphous silicon TFT as a switching device. This model is composed of a transmissive type TFT LCD Panel, driver circuit, capacitive touch panel and a backlight unit. The resolution of the 5.0" TFT LCD contains 480(RGB)x854 pixels and can display up to 16.7M colors.

TFT Features

Low Input Voltage: 3.3V
Display Colors: 16.7M
TFT Interface: 2 Lane MIPI
CTP Interface: I2C

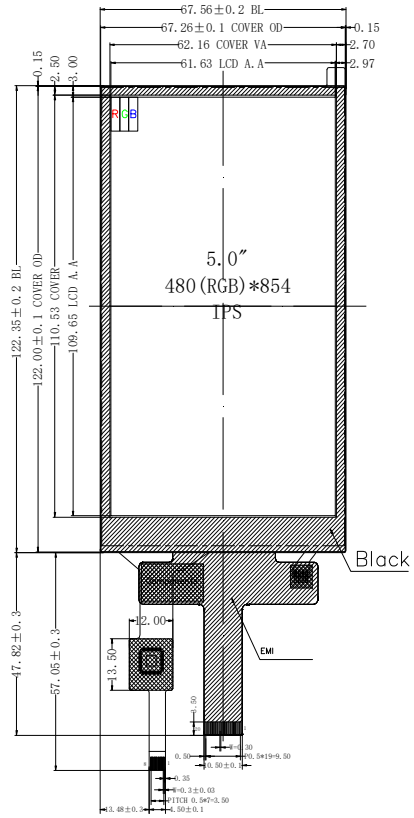
General Information Items	Specification	Unit	Note
	Main Panel		
TFT Display Area (AA)	61.63(H) x 109.65(V) (5.0 inch)	mm	-
Driver Element	TFT active matrix	-	-
Display Colors	16.7M	colors	-
Number of pixels	480(RGB)x854	dots	-
TFT Pixel arrangement	RGB vertical stripe	-	-
Pixel Pitch	0.1284(H)x0.1284(V)	mm	-
Viewing angle	All	o'clock	-
Display mode	Transmissive, Normally Black	-	-
TFT Controller	ILI9806E	-	-
Operating temperature	-20C to 70C	℃	-
Storage temperature	-30C to 80C	℃	-

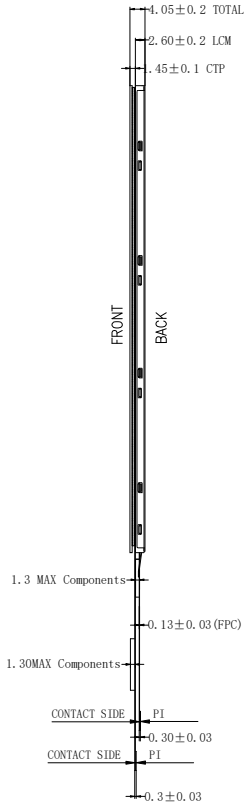
Mechanical Information

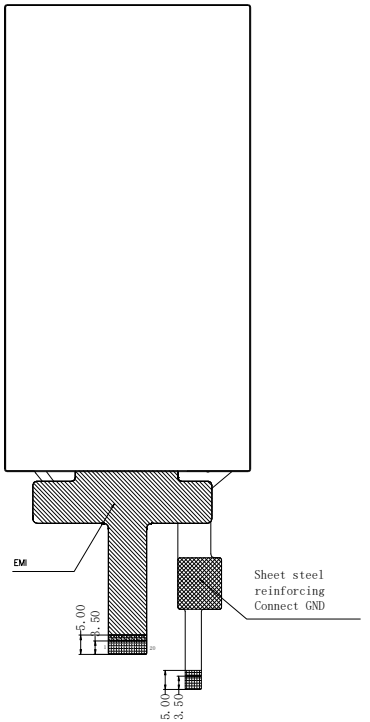
Item		Min	Typ.	Max	Unit	Note
Module Size	Horizontal (H)		67.56		mm	-
	Vertical (V)		122.35		mm	-
	Depth (D)		4.05		mm	-
	Weight		--		g	

1. Outline Dimensions

Rev.	Description	Date
1.0	First	







Number	Pin Name
1	NC
2	LEDK
3	NC
4	LEDA
5	NC
6	VCI
7	IOVCC
8	TE
9	RESET
10	GND
11	MIPI_D1P
12	MIPI_D1N
13	GND
14	MIPI_CLP
15	MIPI_CLN
16	GND
17	MIPI_D0P
18	MIPI_D0N
19	GND
20	GND

CTP FPC Logic

Pin	Logic
1	GND
2	NC
3	VDD
4	SCL
5	SDA
6	INT
7	RST
8	GND

NOTES:

1. DISPLAY TYPE: 5.0" TFT LCD, 16.7M Colors
2. DISPLAY MODE: IPS, NORMALLY BLACK
3. LCM DRIVER IC: ILI9806E
4. SUPPLY VOLTAGE: 3.3V
5. OPERATING TEMPERATURE: -20°C TO +70°C
6. STORAGE TEMPERATURE: -30°C TO +80°C
7. VIEWING DIRECTION: ALL
8. BACKLIGHT: WHITE LED, VF = 19.2V IF = 40mA
9. ROHS COMPLIANT.

Model Name: E50RA-I-MW490-C		
General Tol: ±0.2		
Approvals	Date	
DWN:		
CHK:		
APP:		

FOCUS LCDs
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Drawing No.:		Scale:	
Size:		Unit: mm	Page: 1/1

2. Input Terminal Pin Assignment

Recommended TFT Connector: Part # FH19C-20S-0.5SH(10)

NO.	Symbol	Description	I/O
1	NC	Not connected	
2	LEDK	Cathode pin of backlight	P
3	NC	Not connected	
4	LEDA	Anode pin of backlight	P
5	NC	Not connected	
6	VCI	Supply Voltage (3.3V)	P
7	IOVCC	I/O power supply voltage	P
8	TE	-Tearing effect output. Leave the pin to open when not in use.	O
9	RESET	- The external reset input. Initializes the chip with a low input. Be sure to execute a power-on reset after supplying power.	I
10	GND	Ground	P
11	MIPI_D1P	MIPI DSI differential data pair (DSI-Dn+/-)	I/O
12	MIPI_D1N	If not used, they should be connected to DGND	I/O
13	GND	Ground	P
14	MIPI_CLP	MIPI DSI differential clock pair (DSI-CLK+/-)	I
15	MIPI_CLN	If not used, they should be connected to DGND	I
16	GND	Ground	P
17	MIPI_D0P	MIPI DSI differential data pair (DSI-Dn+/-)	I/O
18	MIPI_D0N	If not used, they should be connected to DGND	I/O
19	GND	Ground	P
20	GND	Ground	P

CTP Pin Assignment

Recommended CTP Connector: Part # FH12-8S-0.5SH(55)

NO.	Symbol	Description	I/O
1	GND	Ground	P
2	NC	Not connected	
3	VDD	Supply Voltage	P
4	SCL	I2C clock input	I
5	SDA	I2C data input and output	I/O
6	INT	External interrupt to the host	I
7	RST	External Reset, Low is active	I
8	GND	Ground	P

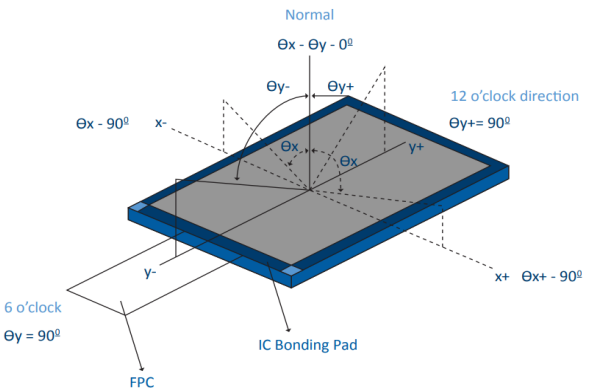
3. LCD Optical Characteristics

3.1 Optical Specifications

Item		Symbol	Condition	Min	Typ.	Max	Unit	Note
Contrast Ratio		CR	θ=0 Normal viewing angle	640	800	--		(2)
Response Time	Rising	TR		--	16	21	ms	
	Falling	TF		--	19	24	ms	
Color Filter Chromaticity	White	W_X		0.250	0.290	0.330		(5)(6)
		W_Y		0.282	0.322	0.362		
	Red	R_X		0.602	0.642	0.682		
		R_Y		0.306	0.346	0.386		
	Green	G_X		0.280	0.320	0.360		
		G_Y		0.576	0.616	0.656		
	Blue	B_X		0.102	0.142	0.182		
		B_Y		0.039	0.079	0.119		
Viewing Angle	Hor.	ΘL	CR≥10	--	80	--	degree	(1)(6)
		ΘR		--	80	--		
	Ver.	ΘT		--	80	--		
		ΘB		--	80	--		
Option View Direction				ALL				(1)

Optical Specification Reference Notes:

(1) Definition of Viewing Angle: The viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3,9 o'clock direction and the vertical or 6,12 o'clock direction with respect to the optical axis which is normal to the LCD surface.

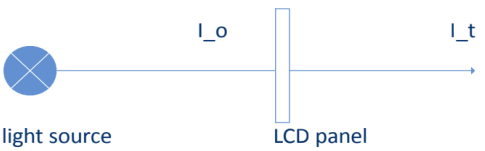


(2) Definition of Contrast Ratio (Cr): measured at the center point of panel. The contrast ratio (Cr) measured on a module, is the ratio between the luminance (Lw) in a full white area (R=G=B=1) and the luminance (Ld) in a dark area (R=G=B=0).

$$Cr = \frac{Lw}{Ld}$$

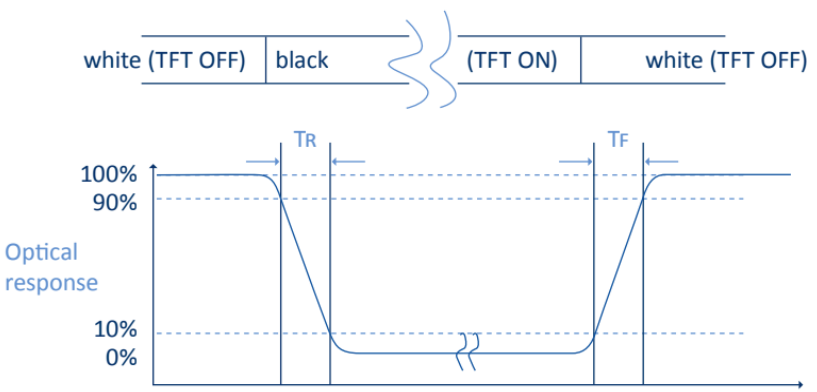
(3) Definition of transmittance (T%): The transmittance of the panel including the polarizers is measured with electrical driving. The equation for transmittance Tr is:

$$Tr = \frac{It}{Io} x\ 100\%$$



Io = the brightness of the light source.
It = the brightness after panel transmission

(4) Definition of Response Time (Tr, Tf): The rise time 'Tr' is defined as the time for luminance to change from 90%to 10% as a result of a change of the electrical condition. The fall time 'Tf' is defined as the time for luminance to change from 10% to 90% as a result of a change of the electrical condition.



(5) Definition of Color Gamut:
Measuring machine CFT-01. NTSC's Primaries: R(x,y,Y),G(x,y,Y), B(x,y,Y). FPM520 of Westar Display Technologies, INC., which utilized SR-3 for Chromaticity and BM-5A for other optical characteristics.The color chromaticity shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

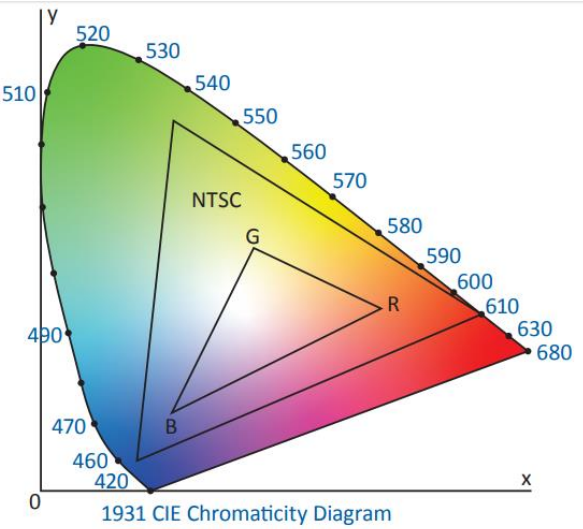
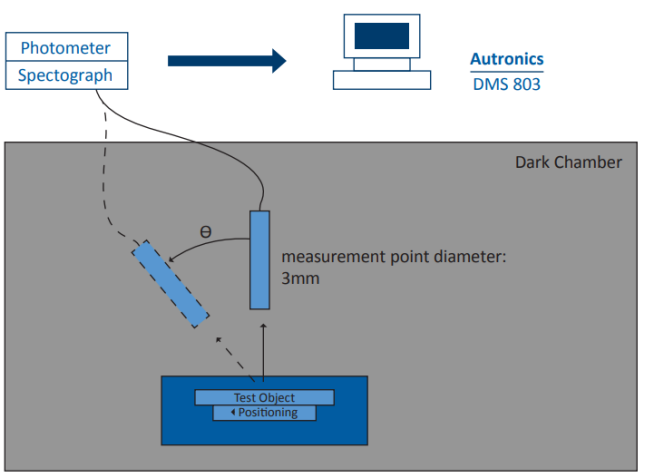


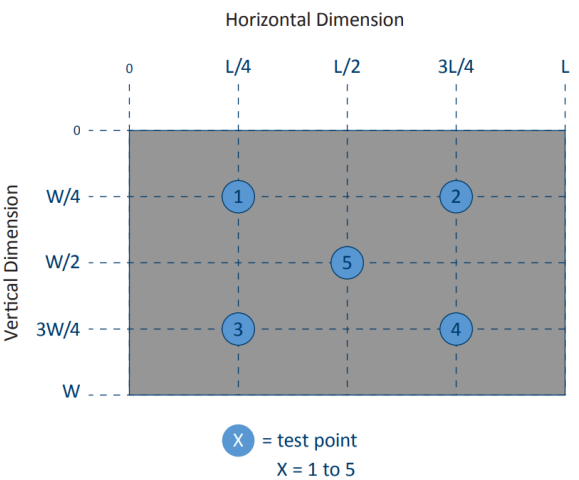
Fig. 1931 CIE chromacity diagram

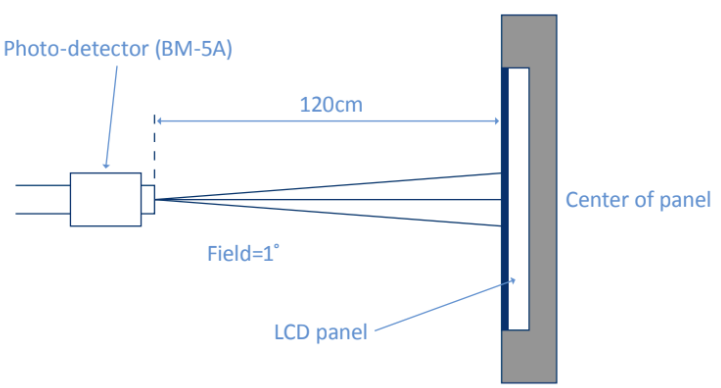
Color gamut: $S = \frac{\text{Area of RGB triangle}}{\text{Area of NTSC triangle}} \times 100\%$

(6) Definition of Optical Measurement Setup:

The LCD module should be stabilized at a given temperature for 20 minutes to avoid abrupt temperature change during measuring. In order to stabilize the luminance, the measurement should be executed after lighting backlight for 20 minutes.







4. TFT Electrical Characteristics

4.1 Absolute Maximum Rating (Ta=25 ˚C, VSS=0V)

Characteristics	Symbol	Min	Max	Unit
Digital Supply Voltage	VCI	-0.3	4.6	V
Digital Interface Supply Voltage	IOVCC	-0.3	4.6	V
Operating Temperature	TOP	-20	+70	℃
Storage Temperature	TST	-30	+80	℃

NOTE: If the absolute maximum rating of the above parameters is exceeded, even momentarily, the quality of the product may be degraded. Absolute maximum ratings specify the values which the product may be physically damaged if exceeded. Be sure to use the product within the range of the absolute maximum ratings.

4.2 DC Electrical Characteristics

Characteristics	Symbol	Min	Typ.	Max	Unit	Note
Analog power supply voltage	VCI	2.5	3.3	3.6	V	
Digital Interface Supply Voltage	IOVCC	1.65	1.8	3.6	V	
Normal Mode Current Consumption	IDD	--	30	--	mA	

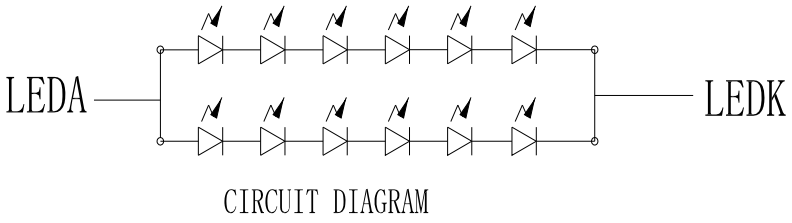
4.3 LED Backlight Characteristics

The backlight system is edge lighting type with 30 chips LED

Item	Symbol	Min	Typ.	Max	Unit	Note
Forward Current	I_F	30	40	--	mA	
Forward Voltage	V_F	--	19.2	--	V	
LCM Luminance	LV	490	--	--	cd/m2	Note 3
LED lifetime	Hr	50000	--	--	hour	Note1 & 2
Uniformity	Avg	80	--	--	%	Note 3

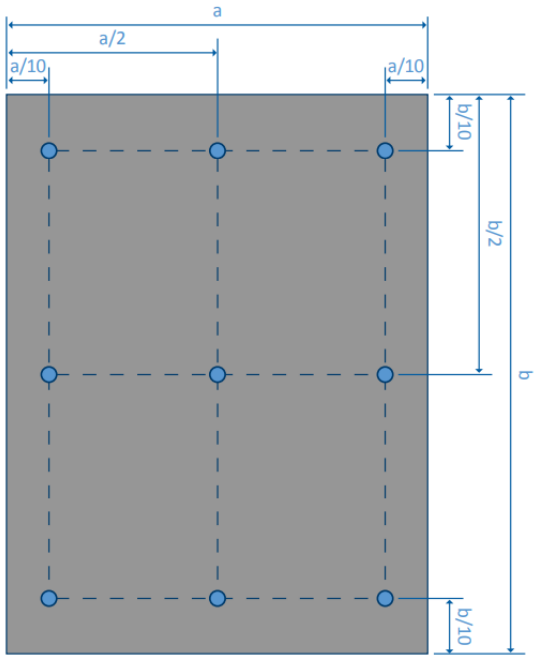
Note 1: LED lifetime (Hr) can be defined as the time in which it continues to operate under the condition: Ta=25±3 ℃, typical IL value indicated in the above table until the brightness becomes less than 50%.

Note 2: The "LED lifetime" is defined as the module brightness decrease to 50% original brightness at Ta=25℃ and IL = 40mA. The LED lifetime could be decreased if operating IL is larger than 40 mA. The constant current driving method is suggested.



CIRCUIT DIAGRAM

Note 3: Luminance Uniformity of these 9 points is defined as below:

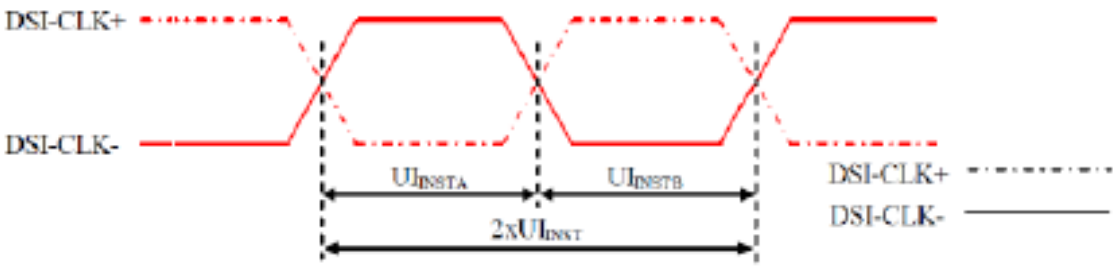


$$\text{Luminance} = \frac{\text{(Total Luminance of 9 points)}}{9}$$

$$\text{Uniformity} = \frac{\text{minimum luminance in 9 points(1-9)}}{\text{maximum luminance in 9 points(1-9)}}$$

5 MIPI Interface Characteristics

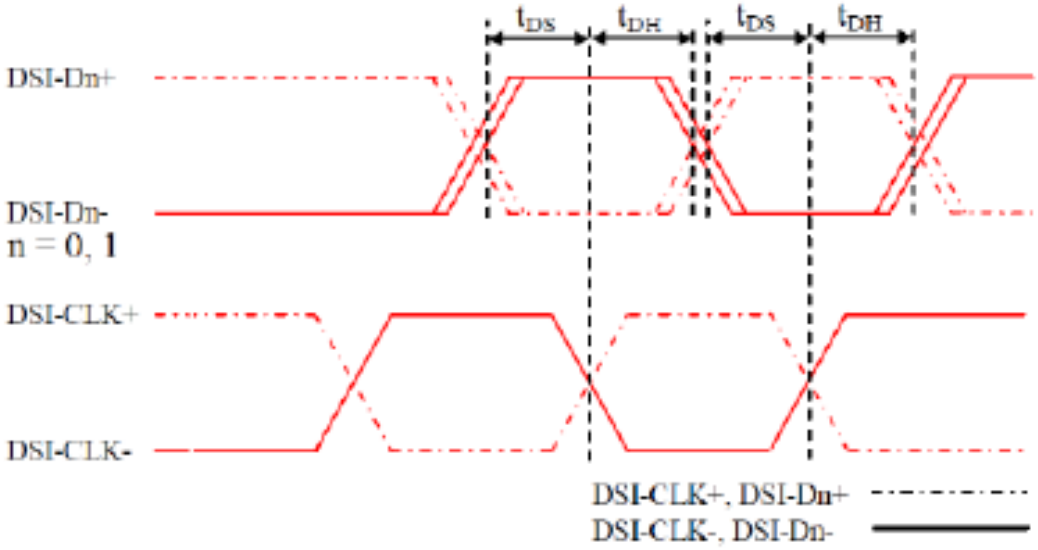
5.1 High Speed Mode – Clock Channel Timing



Signal	Symbol	Parameter	Min	Max	Unit
DSI-CLK +/-	2xUIINST	Double UI Instantaneous	4	25	ns
DSI-CLK +/-	UIINSTA UIINSTB	UI Instantaneous Half	2	12.5	ns

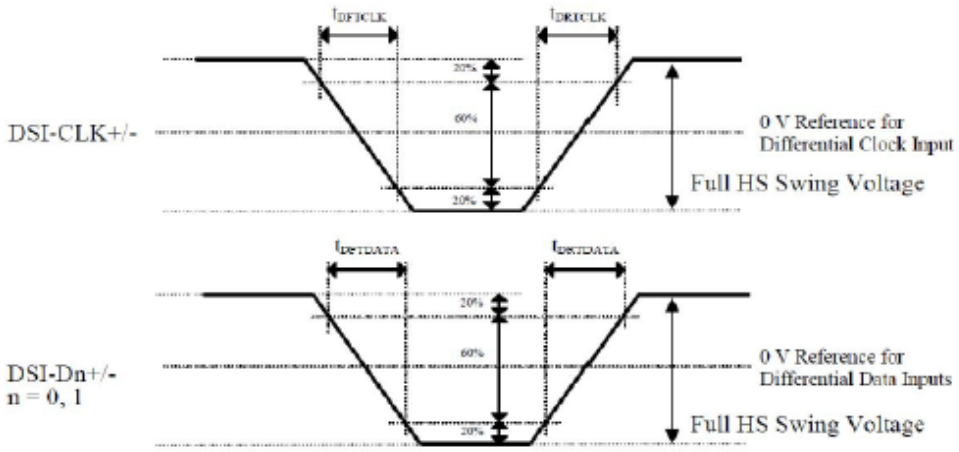
Note: UI = UIINSTA = UIINSTB

5.2 High Speed Mode – Data Clock Channel Timing



Signal	Symbol	Parameter	Min	Max
DSI-Dn+/- , n=0 and 1	tDS	Data To Clock Setup Time	4	25
	tDH	Clock to Data Hold Time	2	12.5

5.3 High Speed Mode – Rise and Fall Timings



Parameter	Symbol	Condition	Specification	
			Min	Typ
Differential Rise Time For Clock	tDRTCLK	DSI-CLK +/-	-	-
Differential Rise Time For Data	tDRTDATA	DSI-Dn+/- , n=0 and 1	-	-
Differential Fall Time For Clock	tDFTCLK	DSI-CLK +/-	-	-
Differential Fall Time For Data	tDFTDATA	DSI-Dn+/- , n=0 and 1	-	-

5.4 Low Speed Mode – Bus Turn Around

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the MPU to the Display Module (ILI9806E) sequence below.

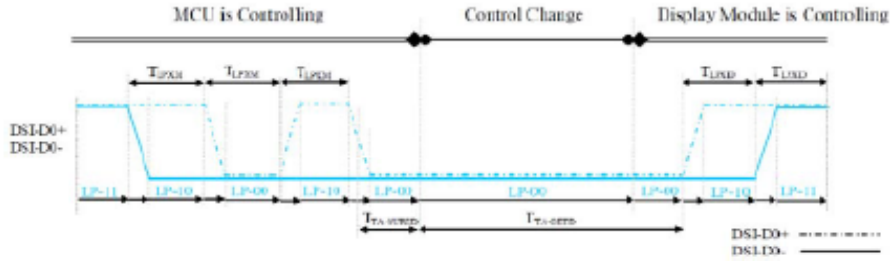


Figure 117 BTA from the MPU to the Display Module

Lower Power Mode and its State Periods are illustrated for reference purposes on the Bus Turnaround (BTA) from the Display Module (ILI9806E) to the MPU sequence below.

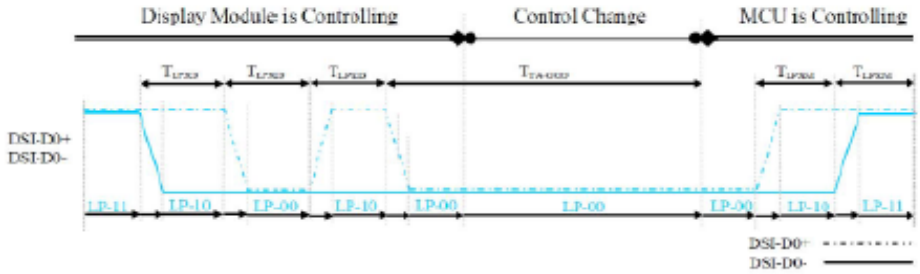


Figure 118 BTA from the Display Module to the MPU

Signal	Symbol	Parameter	Min	Max	Unit
DSI-D0+/-	T_{LPXM}	Length of LP-00,LP-01,LP-10 or LP-11 MPU	50	75	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00,LP-01,LP-10 or LP-11 MPU	50	75	ns
DSI-D0+/-	$T_{TA-SURED}$	Time out before display module starts driving	T_{LPXD}	$2XT_{LPXD}$	ns

Signal	Symbol	Parameter	Min	Max	Unit
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by Display Module (ILI9806E)	4	25	ns
DSI-D0+/-	T_{TA-OOD}	Time to Drive LP-00 after turnaround request - MPU	2	12.5	ns

5.5 Data Lanes from Low Power Mode to High Speed Mode

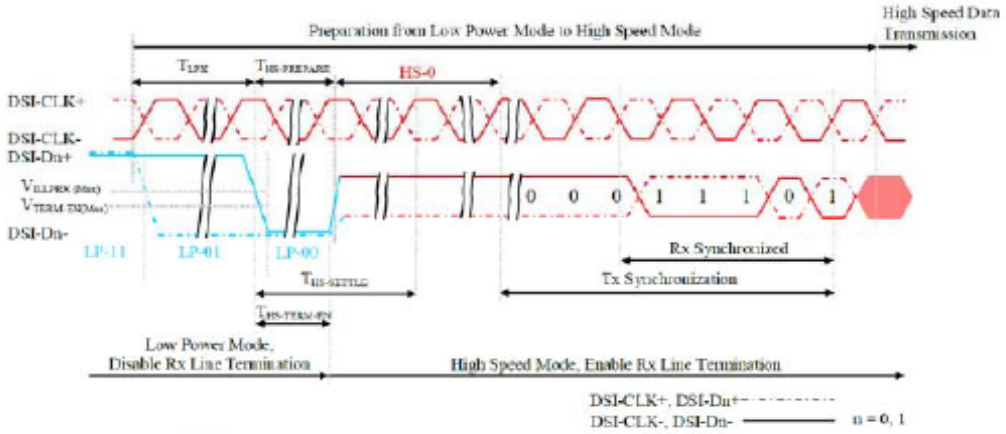


Figure 119 Data Lanes – Low Power Mode to High Speed Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/- , n=0 and 1	T_{LPX}	Length of low power state period	50	-	ns
DSI-Dn+/- , n=0 and 1	$T_{HS\text{-}Prepare}$	Time to drive LP-00 to prepare for hs transmission	40+4XUI	85+6xUI	ns
DSI-Dn+/- , n=0 and 1	$T_{HS\text{-}TERM\text{-}EN}$	Time to enable data lane receiver line termination measured from when Dn crosses VILMAX	-	35+4xUI	ns

5.6 Data Lanes from High Speed Mode to Low Power Mode

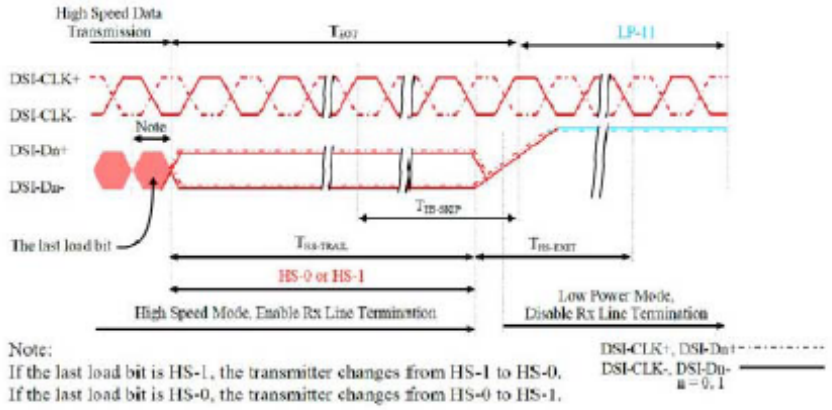


Figure 120 Data Lanes – High Speed Mode to Low Power Mode Timings

Signal	Symbol	Description	Min	Max	Unit
DSI-Dn+/- , n=0 and 1	THS-SKIP	Time-Out at display module (ILI9806E) to ignore transition period of EoT	40	55+4xUI	ns
DSI-Dn+/- , n=0 and 1	THS-EXIT	Time to driver LP-11 after HS burst	100	-	ns

5.7 DSI Clock Burst – High Speed Mode to/from Low Power Mode

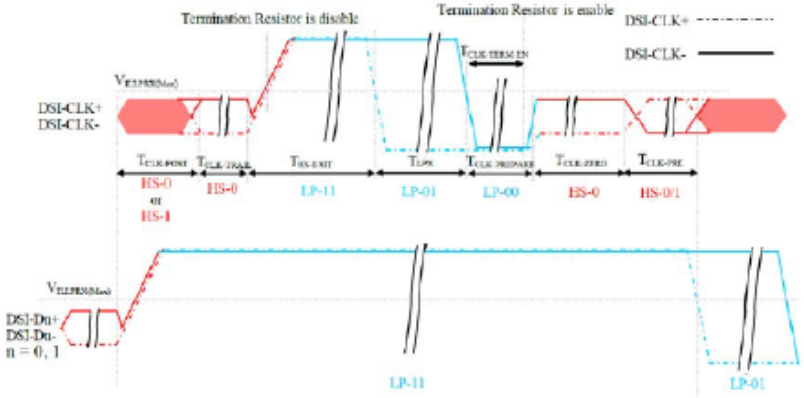


Figure 121 Clock Lanes – High Speed Mode to/from Low Power Mode Timings

Signal	Symbol	Parameter	Min
DSI-CLK +/-	TCLK-POST	Time that the mpu shall continue sending HS clock after the last associated Data Lanes has transitioned to LP mode	60+52UI
DSI-CLK +/-	TCLK-TRAIL	Time To drive HA differential state after last payload clock bit of a HS transmission burst	60
DSI-CLK +/-	THS-EXIT	Time to drive LP-11 after HS burst	100
DSI-CLK +/-	TCLK-PREPARE	Time to drive LP-00 to prepare for HS transmission	38
DSI-CLK +/-	TCLK-TERM-EN	Time-out at Clock Lane to enable HS termination	-
DSI-CLK +/-	TCLK-PREPARE	Minimum lead HS-0 drive period before starting clock	300
DSI-CLK +/-	TCLK-PRE	Time that the HS clock shall be driven prior to any associated data lane begin the transition from LP to HS mode.	8xUI

5.8 Reset input timing

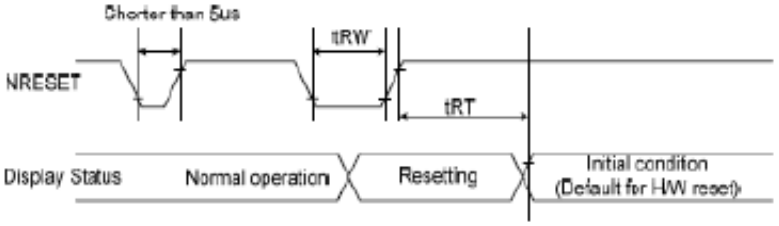


Figure 102 Reset Timing

Table 41 Reset Timing

Signal	Symbol	Parameter	Min	Max	Unit
RESX	tRW	Reset pulse duration	10		us
	tRT	Reset cancel		5(note 1,5)	ms
				120 (note 1,6,7)	ms

Note:

1. The reset cancel includes also required time for loading ID bytes, VCOM setting and other settings from OTP to registers. This loading is done every time when there is H/W reset cancel time (tRT) within 5 ms after a rising edge of RESX.
2. Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the Table 43.

Table 42 Reset Descript

RESX Pulse	Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset starts

3. During the Resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out mode. The display remains the blank state in Sleep In mode.) and then return to Default condition for Hardware Reset.
4. Spike Rejection also applies during a valid reset pulse as shown below:

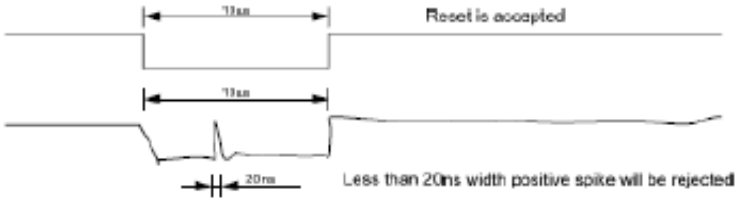


Figure 103 Positive Noise Pulse during Reset Low

5. When Reset applied during Sleep In Mode.
6. When Reset applied during Sleep Out Mode.
7. It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec.

6. CTP Specifications

6.1 Electrical Characteristics

6.1.1 Absolute Maximum Rating

ITEM	SYMBOL	MIN	MAX	UNIT	NOTE
POWER SUPPLY VOLTAGE	VDD	2.66	3.47	V	-
OPERATING TEMPERATURE	TOP	-20	70	C	-
STORAGE TEMPERATURE	TST	-30	-80	C	-

6.1.2 DC Electrical Characteristics (Ta=25℃)

(Ambient temperature:25℃, AVDD=2.8V, VDDIO=1.8V or VDDIO=AVDD)

ITEM	MIN	TYP	MAX	UNIT	NOTE
NORMAL MODE OPERATING CURRENT	-	8	14.5	mA	-
GREEN MODE OPERATING CURRENT	-	3.3	-	mA	-
SLEEP MODE OPERATING CURRENT	70	-	120	uA	-
DOZE MODE OPERATING CURRENT	-	0.78	-	mA	-
DIGITAL INPUT LOW VOLTAGE/VIL	-0.03	-	0.25*VDDIO	v	-
DIGITAL INPUT HIGH VOLTAGE/VIH	0.75*VDDIO	-	VDDIO+0.3	v	-
DIGITAL OUTPUT LOW VOLTAGE / VOL	-	-	0.15*VDDIO	v	-
DIGITAL OUTPUT HIGH VOLTAGE / VOH	0.85*VDDIO	-	-	v	-

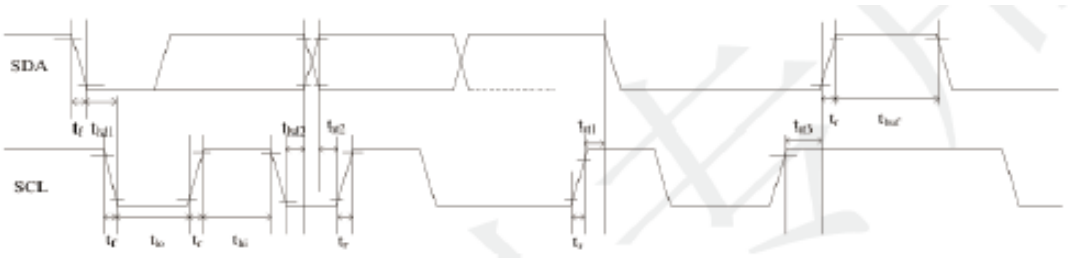
6.1.3 AC Characteristics

(Ambient temperature:25℃, AVDD=2.8V, VDDIO=1.8V)

Parameter	Min	Typ	Max	Unit
OSC Oscillation Frequency	59	60	61	Mhz
I/O output rise time, low to high	-	14	-	ns
I/O Output fall time, high to low	-	14	-	ns

6.2 I2C Timing

GT911 provides a standard I2C interface for SCL and SDA to communicate with the host. GT911 always serves as slave device in the system with all communication being initialized by the host. It is strongly recommended that transmission rate be kept at or below 400Kbps. The I2C timing is shown below:



Test Condition 1: 1.8v host interface voltage, 400 Kbps transmission rate, 2k pull-up resistor

Parameter	Symbol	Min	Max	Unit
SCL low Period	tIO	1.3	-	us
SCL high period	tHI	0.6	-	us
SCL setup time for start condition	tST1	0.6	-	us
SCL setup time for stop condition	tST3	0.6	-	us
SCL hold time for start condition	thd1	0.6	-	us
SDA setup time	tst2	0.1	-	us
SDA hold time	tnd2	0	-	us

Test Condition 2: 3.3v host interface voltage, 400 Kbps transmission rate, 2k pull-up resistor

Parameter	Symbol	Min	Max	Unit
SCL low Period	tIO	1.3	-	us
SCL high period	tHI	0.6	-	us
SCL setup time for start condition	tST1	0.6	-	us
SCL setup time for stop condition	tST3	0.6	-	us
SCL hold time for start condition	thd1	0.6	-	us
SDA setup time	tst2	0.1	-	us
SDA hold time	tnd2	0	-	us

7. Cautions and Handling Precautions

7.1 Handling and Operating the Module

1. When the module is assembled, it should be attached to the system firmly. Do not warp or twist the module during assembly work.
2. Protect the module from physical shock or any force. In addition to damage, this may cause improper operation or damage to the module and back-light unit.
3. Note that polarizer is very fragile and could be easily damaged. Do not press or scratch the surface.
4. Do not allow drops of water or chemicals to remain on the display surface. If you have the droplets for a long time, staining and discoloration may occur.
5. If the surface of the polarizer is dirty, clean it using some absorbent cotton or soft cloth.
6. The desirable cleaners are water, IPA (Isopropyl Alcohol) or Hexane. Do not use ketene type materials (ex. Acetone), Ethyl alcohol, Toluene, Ethyl acid or Methyl chloride. It might permanent damage to the polarizer due to chemical reaction.
7. If the liquid crystal material leaks from the panel, it should be kept away from the eyes or mouth. In case of contact with hands, legs, or clothes, it must be washed away thoroughly with soap.
8. Protect the module from static; it may cause damage to the CMOS ICs.
9. Use fingerstalls with soft gloves in order to keep display clean during the incoming inspection and assembly process.
10. Do not disassemble the module.
11. Protection film for polarizer on the module shall be slowly peeled off just before use so that the electrostatic charge can be minimized.
12. Pins of I/F connector shall not be touched directly with bare hands.
13. Do not connect, disconnect the module in the “Power ON” condition.
14. Power supply should always be turned on/off by the item Power On Sequence & Power Off Sequence.

7.2 Storage and Transportation.

1. Do not leave the panel in high temperature, and high humidity for a long time. It is highly recommended to store the module with temperature from 0 to 35 ℃ and relative humidity of less than 70%
2. Do not store the TFT-LCD module in direct sunlight.
3. The module shall be stored in a dark place. When storing the modules for a long time, be sure to adopt effective measures for protecting the modules from strong ultraviolet radiation, sunlight, or fluorescent light.
4. It is recommended that the modules should be stored under a condition where no condensation is allowed. Formation of dewdrops may cause an abnormal operation or a failure of the module. In particular, the greatest possible care should be taken to prevent any module from being operated where condensation has occurred inside.
5. This panel has its circuitry FPC on the bottom side and should be handled carefully in order not to be stressed.